COMPUTER ARCHITECTURE AND ORGANISATION SYLLABUS

Module 1: Overview of Organization and Architecture

- Functional Components of a Computer: Registers and Register Files
- Interconnection of Components
- Overview of IAS Computer Function
- Organization of the von Neumann Machine
- Harvard Architecture
- CISC & RISC Architectures

Module 2: Data Representation and Computer Arithmetic

- Algorithms for Fixed Point Arithmetic Operations: Booth's and Modified Booth's Multiplication, Restoring and Non-Restoring Division
- Algorithms for Floating Point Arithmetic Operations
- Representation of Nonnumeric Data (Character Codes)

Module 3: Instruction Sets and Control Unit

- Computer Instructions: Instruction Sets, Instruction Set Architecture, Instruction Formats, Instruction Set Categories
- Addressing Modes
- Phases of the Instruction Cycle
- ALU
- Data Path and Control Unit: Hardwired and Microprogrammed Control Unit
- Performance Metrics: Execution Time Calculation, MIPS, MFLOPS

Module 4: Memory System Organization and Architecture

- Memory Systems Hierarchy: Characteristics, Byte Storage Methods, Conceptual View of Memory Cell
- Design of Scalable Memory Using RAMs and ROMs
- Construction of Larger Size Memories, Memory Interleaving
- Memory Interface Address Map
- Cache Memory: Principles, Management Techniques, Types of Caches, Cache Misses, Mean Memory Access Time Evaluation

Module 5: Interfacing and Communication

- I/O Fundamentals: Handshaking, Buffering, I/O Modules
- I/O Techniques: Programmed I/O, Interrupt-Driven I/O, Direct Memory Access, Direct Cache Access
- Interrupt Structures: Vectored and Prioritized, Interrupt Overhead
- Arbitration
- Buses: Synchronous and Asynchronous

Module 6: Subsystems

- External Storage Systems: Solid State Drives
- Organization and Structure of Disk Drives: Electronic, Magnetic, and Optical Technologies
- Reliability of Memory Systems: Error Detection and Correction Systems
- RAID Levels
- I/O Performance and Error Handling

Module 7: High-Performance Processors

- Classification of Models: Flynn's Taxonomy of Parallel Machine Models (SISD, SIMD, MISD, MIMD)
- Pipelining: Two-Stage and Multistage Pipelining, Performance Issues, Hazards, Methods to Prevent and Resolve Hazards
- Branch Handling Approaches
- Superscalar Architecture: Limitations of Scalar Pipelines, Superscalar vs. Superpipeline Architecture, Superscalar Techniques, Performance Evaluation
- Performance Evaluation of Parallel Processors: Amdahl's Law, Speed-Up, and Efficiency