DIGITAL SYSTEMS DESIGN SYLLABUS

Module 1: Digital Logic

- Boolean Algebra: Basic Definitions, Axiomatic Definition of Boolean Algebra, Basic Theorems and Properties, Boolean Functions, Canonical and Standard Forms, Simplification of Boolean Functions
- Gate-Level Minimization: The Map Method (K-map up to 4 variables), Product of Sums and Sum of Products Simplification, NAND and NOR Implementation
- Logic Families: Digital Logic Gates, TTL and CMOS Logic Families

Module 2: Verilog HDL

- Lexical Conventions
- Ports and Modules
- Operators
- Dataflow Modelling
- Gate Level Modelling
- Behavioural Modeling
- Test Bench

Module 3: Design of Combinational Logic Circuits

- Design Procedure: Half Adder, Full Adder, Half Subtractor, Full Subtractor, Decoders, Encoders, Multiplexers, De-multiplexers, Parity Generator and Checker
- Applications: Decoder, Multiplexer, and De-multiplexer
- Modeling: Combinational Logic Circuits using Verilog HDL

Module 4: Design of Data Path Circuits

- N-bit Parallel Adder/Subtractor
- Carry Look Ahead Adder

- Unsigned Array Multiplier
- Booth Multiplier
- 4-Bit Magnitude Comparator
- Modeling: Data Path Circuits using Verilog HDL

Module 5: Design of Sequential Logic Circuits

- Latches and Flip-Flops: SR, D, JK, T
- Buffer Registers
- Shift Registers: SISO, SIPO, PISO, PIPO
- Design of Synchronous Sequential Circuits: State Table and State Diagrams
- Design of Counters: Modulo-n, Johnson, Ring, Up/Down, Asynchronous Counter
- Modeling: Sequential Logic Circuits using Verilog HDL

Module 6: Design of FSM

- Finite State Machine (FSM): Mealy FSM and Moore FSM
- Design Example: Sequence Detection
- Modeling: FSM using Verilog HDL

Module 7: Programmable Logic Devices

- Types of Programmable Logic Devices: PLA, PAL, CPLD, FPGA
- Generic Architecture