CS220 Quiz#2

General instructions: Please write brief explanation for your answers. If you submit multiple times, your last submission will be used for grading. Please provide an email address below where your responses can be sent.

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Q1. Consider a single-channel DIMM card with a 32-bit channel. The channel has two ranks. The DIMM card uses x4 chips and each chip has 16 banks. If each bank has 8192 rows and 2048 columns, what is the total capacity of the DIMM card in bits? (1 point)

Total capacity = 4 bits per column x 2048 columns per row x 8192 rows per bank x 16 banks per chip x 8 chips per rank x two ranks per channel x one channel per DIMM card = 16Gb

Q2. Suppose the following five access requests have come to a particular bank of a DRAM module, where each request is listed as (row number, column number): (19, 43), (13, 43), (17, 11), (19, 32), (17, 32). Write down the sequence in which the requests must be sent to the bank such that it takes the minimum amount of time to complete all the requests. Initially, the bank is in the precharged state. (1 point)

Requests going to the same row should be served first before switching row. Therefore, one possible sequence is (19, 43), (19, 32), (13, 43), (17, 11), (17, 32).

Q3. An SRAM module with 16M rows and eight-bit width is implemented using eight ranks of 1K x 2048-bit SRAM chips. To get eight-bit output, the chips in one of the ranks are selected. Calculate the number of address bits used to generate the row address, column address, and chip select. (1 point)

There are 8 chips in a rank. Number of bits for row address = 10. Number of bits for column address = 11. Number of bits to generate chip select = 3 (to select one of the eight ranks).

Q4. A finite state machine (FSM) having 900 states is implemented using a state sequencer, a microcode ROM, and 35 dispatch ROMs. The FSM also has 13 next states that do not come from the dispatch ROMs and nor is it equal to (current state + 1). The FSM takes a ten-bit input. Compute the minimum width (in bits) of the microinstructions and the total size (in bits) of each dispatch ROM. (1+1 points)

The width of a microinstruction is same as the width of the microcode ROM. The width of the microcode ROM is same as the number of selection bits in the state selection multiplexer. There are 49 inputs to this multiplexer (35 from dispatch ROMs, 13 constants, and one from state sequencer). So, the width of a microinstruction is six bits. The dispatch ROM stores the next states of the branches. So, the width of one dispatch ROM entry is ten bits (log of 900). The number of dispatch ROM rows is 2^n if there are n input bits. So, the total size of each dispatch ROM is 10x1024 bits i.e., 10240 bits.

Q5. Write down the binary representation of the decimal fraction 25.4375 in normalized scientific notation. You can write x to the power of y as (x^y). (1 point)

25.4375 = 11001.0111 = 1.10010111 x (2^4)