CS220A Quiz#1

Please write brief explanation for your answers. Do not submit the quiz more than once. Please provide an email address below where your responses can be sent.

Email address *

mainakc@cse.iitk.ac.in

Your name *

Mainak Chaudhuri

Your roll number *

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Q1. Suppose you would like to design a PLA that can implement an arbitrary 13-input Boolean function where each input is a single-bit variable. The OR plane of the PLA has just one horizontal line because at a time it can implement only one function. (a) What is the number of input lines in the PLA (i.e., horizontal lines in the AND plane)? (b) What is the number of vertical lines in the AND plane? If this PLA is used to realize a function whose output is one irrespective of the input values, (c) how many intersections would have dots in the AND plane and (d) how many intersections would have dots in the OR plane? (0.5+0.5+0.5+0.5 points) Note: you need not worry about the exact mechanism through which the PLA would be programmed torealize a desired 13-input function. Also, do not worry about minimizing the Boolean function's SoP representation.

(a) Number of horizontal lines is 26 (each input bit and its inversion).
(b) Number of vertical lines is equal to the number of minterms. Using 13 Boolean variables, one can construct 8192 different minterms. So, the number of vertical lines is 8192.
(c) One way to implement 1 is to have all minterms. So, for each vertical line, 13 intersections would have dots. So, the total number of dots in AND plane is 106496.
(d) We will OR all minterms. So, there will be 8192 dots in the OR plane.

Q2. Consider implementing the following four three-input functions using a ROM: (i) A + B + C, (ii) max(A, B, C), (iii) quotient of (A*B)/C, and (iv) remainder of (A*B)/C, where the inputs are A, B, C. If each input is 10-bit wide and is interpreted as a non-negative number, calculate the number of rows and number of columns in the ROM. Assume that when the divisor of a division operation is zero, both the quotient and remainder are stored as zero. (0.5+0.5 points)

(a) Total number of inputs is 30. So, the number of rows is 2^{30}.
(b) To compute the number of columns, we need to find out the maximum number of bits needed to store each of the functions. Since each input can range from 0 to 1023, A+B+C would need 12 bits; max(A, B, C) would need 10 bits; quotient of (A*B)/C is maximized when A=B=1023 and C=1 needing 20 bits; remainder of (A*B)/C would need 10 bits. So, the total number of columns is 52.

Q3. Suppose the inputs to a one-bit full adder are sent from three flip-flops A, B, C. The sum and carry outputs are sent to two flip-flops D and E, respectively. All five flip-flops receive the same clock signal. Assume zero clock skew. It takes 400 picoseconds to compute the sum bit and 700 picoseconds to compute thecarry output. The propagation delay through each of A, B, C is 80 picoseconds, while that through each of D and E is 130 picoseconds. The setup timeof each of A, B, C is 170 picoseconds, while the setup time of each of D and E is 230 picoseconds. The hold time of all flip-flops is 30 picoseconds. What is the minimum clock cycle time required for correct storage of sum and carry outputs? (1 point)

Minimum clock cycle time = propagation delay through input flip-flops + max. delay through combinational logic + setup time of output flip-flops = max(80, 80, 80) + max(400, 700) + max(230, 230) picoseconds = 1010 picoseconds.

Q4. A register file having 32 registers each of width 64 bits has 7 read ports and 3 write ports. Each port uses its own decoder and no decoder is shared across ports. What is the number of input bits and output bits to each decoder? (0.5+0.5 points) What is the total number of wordlines and bitlines in the register file? (0.5+0.5 points)

The decoder decodes a register number. So, the number of input bits to the decoder is 5 and the number of output bits is 32. Number of wordlines = number of registers*number of ports = 320. Number of bitlines = width of registers*number of ports = 640.