CS220 Quiz#2

General instructions: Please write brief explanation for your answers. If you submit multiple times, your last submission will be used for grading. Please provide an email address below where your responses can be sent.

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Q1. Consider a single-channel DIMM card with a 32-bit channel. The channel has two ranks. The DIMM card uses x4 chips and each chip has 16 banks. If each bank has 8192 rows and 2048 columns, what is the total capacity of the DIMM card in bits? (1 point)

Size of each:
Column=2^2 bits (from x4)
Row=No of columns*Size of each column=2^11*2^2=2^13
Bank=No of rows*Size of each row=2^13*2^13=2^26
Chip=No of banks per chip*Size of each bank=2^4*2^26=2^30
Rank=No of chips per rank*Size of each chip=2^3*2^30=2^33 (No of chips per rank is 2^3=8 as it is a 32 bit channel and x4 chips are used. So, number of chips per rank have to be 32/4=8 to get 32 bits per burst)
Size of DIMM Card=Size of each rank*No. of ranks=2^33*2^1=2^34 bits

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Q2. Suppose the following five access requests have come to a particular bank of a DRAM module, where each request is listed as (row number, column number): (19, 43), (13, 43), (17, 11), (19, 32), (17, 32). Write down the sequence in which the requests must be sent to the bank such that it takes the minimum amount of time to complete all the requests. Initially, the bank is in the precharged state. (1 point)

(13,43), (17, 11), (17, 32), (19,32), (19,43)
This is an optimal sequence in which the requests must be sent to the bank because in this method, the requests are grouped based on the row numbers which will save time due to row hit in requests 3 and 5 which occurs when the requested row is already open. In the first case, row miss will occur as initially no row will be open, while in the rest cases, row conflict will occur due to closing of one row and opening of the other.

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Q3. An SRAM module with 16M rows and eight-bit width is implemented using eight ranks of 1K x 2048-bit SRAM chips. To get eight-bit output, the chips in one of the ranks are selected. Calculate the number of address bits used to generate the row address, column address, and chip select. (1 point)

The number of address bits used to generate:
The row address: 10 bits (1k=2^10)
The column address: 11 bits (2k=2^11)
Chip select: 3 bits (8=2^3; No of ranks is eight.)

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Q4. A finite state machine (FSM) having 900 states is implemented using a state sequencer, a microcode ROM, and 35 dispatch ROMs. The FSM also has 13 next states that do not come from the dispatch ROMs and nor is it equal to (current state + 1). The FSM takes a ten-bit input. Compute the minimum width (in bits) of the microinstructions and the total size (in bits) of each dispatch ROM. (1+1 points)

No of dispatch ROMs=35 gives No of states having branching=35
No of states having unconditional flow towards a lesser numbered state=13
So, No of states having incremental states=900-35-13=842

The minimum width (in bits) of the microinstructions is: ceil(log(1+35+13) base 2)=6
and the total size (in bits) of each dispatch ROM is: 10

1+0

Q5. Write down the binary representation of the decimal fraction 25.4375 in normalized scientific notation. You can write x to the power of y as (x^y). (1 point)

25.4375 = 2^4+2^3+2^0+2^(-2)+2^(-3)+2^(-4) = 11001.0111 in binary notation
This can be expressed in normalized scientific notation as 1.10010111*2^(100).

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