CS220A Quiz#1

Please write brief explanation for your answers. Do not submit the quiz more than once. Please provide an email address below where your responses can be sent.

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Q1. Suppose you would like to design a PLA that can implement an arbitrary 13-input Boolean function where each input is a single-bit variable. The OR plane of the PLA has just one horizontal line because at a time it can implement only one function. (a) What is the number of input lines in the PLA (i.e., horizontal lines in the AND plane)? (b) What is the number of vertical lines in the AND plane? If this PLA is used to realize a function whose output is one irrespective of the input values, (c) how many intersections would have dots in the AND plane and (d) how many intersections would have dots in the OR plane? (0.5+0.5+0.5+0.5 points) Note: you need not worry about the exact mechanism through which the PLA would be programmed torealize a desired 13-input function. Also, do not worry about minimizing the Boolean function's SoP representation.

a) 26 horizontal lines will be required, 2 for each single-bit variable and its negation.
b) 2^13 vertical lines will be required as for each variable x, we can use either x or not of x. Since there are 13 variables, total number of vertical lines required will be 2^13.
c) A total 13*(2^13) intersections will have dots in the AND plane, one for each input variable in each vertical line.
d) A total 2^13 intersections will have dots in the OR plane, one for each of the vertical lines in the AND plane.

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Q2. Consider implementing the following four three-input functions using a ROM: (i) A + B + C, (ii) max(A, B, C), (iii) quotient of (A*B)/C, and (iv) remainder of (A*B)/C, where the inputs are A, B, C. If each input is 10-bit wide and is interpreted as a non-negative number, calculate the number of rows and number of columns in the ROM. Assume that when the divisor of a division operation is zero, both the quotient and remainder are stored as zero. (0.5+0.5 points)

Number of columns: Number of functions*bit-width of each function=4*10=40
Number of rows: 2^(No of inputs*bit-width of each input)=2^30.

0.5+0

Q3. Suppose the inputs to a one-bit full adder are sent from three flip-flops A, B, C. The sum and carry outputs are sent to two flip-flops D and E, respectively. All five flip-flops receive the same clock signal. Assume zero clock skew. It takes 400 picoseconds to compute the sum bit and 700 picoseconds to compute thecarry output. The propagation delay through each of A, B, C is 80 picoseconds, while that through each of D and E is 130 picoseconds. The setup timeof each of A, B, C is 170 picoseconds, while the setup time of each of D and E is 230 picoseconds. The hold time of all flip-flops is 30 picoseconds. What is the minimum clock cycle time required for correct storage of sum and carry outputs? (1 point)

0

1180 picoseconds

Q4. A register file having 32 registers each of width 64 bits has 7 read ports and 3 write ports. Each port uses its own decoder and no decoder is shared across ports. What is the number of input bits and output bits to each decoder? (0.5+0.5 points) What is the total number of wordlines and bitlines in the register file? (0.5+0.5 points)

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Number of input bits= 5 as 2^5=32 and we need to find the address of a specific register among the 32 registers. Output bits to each decoder will be 32, one for each of the registers.
Total number of wordlines= No of ports*No of registers=10*32=320 and bitlines in the register file=No of ports*Size of each register=10*64=640