Design and Optimization of an Energy-Efficient High-Performance Serial Data Scrambler

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***Abstract*—Modern digital communication systems demand high data rates and energy efficiency while ensuring robust signal integrity and precise timing synchronization. Extended sequences of identical bits disrupt clock recovery and degrade signal quality in high-speed applications like USB, SATA, and Ethernet. This paper presents an innovative, energy-efficient serial scrambler designed to address these challenges with minimal trade-offs. The proposed architecture integrates a 2:1 multiplexer and pass transistor logic (PTL)-based clock gating to enhance throughput and reduce power consumption. The design was developed and simulated using Cadence Virtuoso in 45nm CMOS technology. Compared to the traditional scrambler's power consumption and 60-transistor footprint, the optimized design achieves a doubled data rate of 2 bits per clock cycle, reduces power with a 21 % reduction from a MUX-only design, and maintains a compact area. These advancements ensure superior efficiency, making the scrambler ideal for high-speed protocols. Comprehensive simulations validate its performance, demonstrating a balanced trade-off between speed, power, and area. This pioneering solution paves the way for scalable, low-power designs in next-generation communication systems, with potential for further optimization using advanced techniques.**

***Index Terms*—Area optimization, Clock gating, Clock inefficiency, Energy efficiency, Linear feedback shift register (LFSR), Multiplexer, Pass transistor logic (PTL), Power consumption, Serial scrambler, Throughput**

I. Introduction

In traditional serial scrambler design, the core architecture typically consists of linear feedback shift registers (LFSR), XOR gates, and D flip-flops [1]. The fundamental purpose of this type of scrambler is to remove long sequences of identical bits (e.g., multiple consecutive 1s or 0s) [2]. The traditional serial scrambler consists of a series of D flip-flops connected in a shift register configuration. Selected outputs are XORed with one or more bits of the LFSR and given to the first D flip-flop as a feedback. The data is again shifted in the flip-flops and this process continues. This scrambling process ensures that the output data has a more randomized and balanced distribution of ones and zeros, which improves signal characteristics such as spectral density and reduces electromagnetic interference (EMI) [3].

Among the different types of scramblers, serial scramblers stand out for their simplicity, energy efficiency, and reduced hardware requirements [4]. They work by processing data bit by bit, using LFSR and XOR gates [1]. This sequential method results in lower switching activity, which translates into reduced power consumption and smaller silicon area [5].

Despite the simplicity of the serial scrambler, traditional designs face critical limitations that make them increasingly unsuitable for modern digital communication systems. One of the main challenges is their low throughput, as a traditional serial scrambler processes one bit per clock cycle [6]. This makes the serial scrambler highly inefficient, particularly for applications such as USB 3.0, PCI Express, or high-speed Ethernet, where multiple bits must be processed per clock cycle [7]. Traditional serial scramblers also lack power optimization features, causing the clock to toggle the flip-flops even when data processing is minimal. This switching activity during high-speed operation may lead to EMI and higher noise, affecting signal integrity [8]. Parallel scramblers address these issues but incur higher area and power overhead [9]. Therefore, unoptimized serial scramblers risk becoming obsolete, necessitating new design approaches that enhance speed and power efficiency without significantly increasing circuit complexity or area.

This paper proposes an energy-efficient serial scrambler architecture that integrates a 2:1 multiplexer to double the data rate to 2 bits per clock cycle and employs pass transistor logic (PTL)-based clock gating to reduce power consumption by 21% compared to a MUX-only design. Designed and simulated in 45nm CMOS using Cadence Virtuoso, the proposed design maintains a compact area while achieving superior performance, making it suitable for high-speed protocols like USB and Ethernet. The methodology, results, and comparisons with traditional and intermediate designs are detailed, highlighting the trade-offs and future optimization potential.

Industry designs are transitioning from traditional serial scramblers to parallel scramblers. While parallel scramblers offer higher throughput and increased speed, they often come at the cost of increased circuit complexity, silicon area, and power consumption [10]. Some industry implementations also include hybrid scramblers, which switch between serial and parallel modes based on data rate or application requirements [11]. For application-specific integrated circuit (ASIC) and system-on-chip (SoC) applications, parameterized RTL scrambler cores have been developed, allowing designers to easily integrate optimized scrambler blocks tailored for specific pro-

tocols such as USB, SATA, or Ethernet [12]. These modern solutions aim to build an architecture that is simple and robust; therefore, the proposed architecture optimizes the system for modern digital communication applications [13].

The rest of this paper is structured as follows: Section II covers related work and existing architecture for traditional serial and parallel scramblers. Section III details the design of the traditional serial scrambler architecture. Section IV presents the proposed serial scrambler, highlighting its working principles along with its low power advantages. Section V presents simulation results. Section VI presents the comparison tables, followed by conclusions in Section VII.

II. Literature Review

Recent research on scramblers has focused on improving data integrity and signal synchronization in high-speed communication systems. Implementing multiplexers and gated clocks in the architecture of a serial scrambler can achieve optimal modern digital communication. The following studies are presented in chronological order with citations in sequential order to highlight the evolution of scrambler designs.

An early study on low-power clock and data recovery describes a clock and data recovery (CDR) circuit implemented in 45nm CMOS, achieving a power efficiency of 2.7pJ/bit [1]. Another work focuses on integrating error detection capabilities in LFSR using XOR-based parity checks with minimal hardware overhead, improving reliability in serial scramblers [2].

A novel low-power synchronous preamble data line chip design demonstrates up to 30 percent power reduction compared to traditional designs by implementing optimized flip-flops and gated clocks [3]. A power-efficient finite state machine (FSM)-based universal asynchronous receiver-transmitter (UART) achieves a 25 percent reduction in power and improved throughput for serial communication [4].

Further advancements include the use of leakage control transistor (LECTOR) techniques to reduce leakage and dynamic power in sequential circuits, critical for low-power scrambler designs [5]. Another study clarifies power reduction and area optimization in serial communication using adaptive voltage level scaling (AVLS) and true single-phase clocking (TSPC) D flip-flops [6].

A design employing hybrid AVLS and LECTOR techniques in a phase frequency detector for low-power PLLs reduces switching activity in flip-flops using pass transistor logic (PTL) [7]. A real-time Wi-Fi energy detection testbed for low-power signal detection enhances energy efficiency in communication systems [8].

An AVLS-based 32/33 prescaler for frequency dividers achieves a compact design with reduced power consumption [9]. A low-power 16/17 dual-modulus prescaler using TSPC and AVLS techniques in 45nm CMOS is presented [10]. Another study addresses both power optimization and security concerns by combining clock gating with secure communication techniques, improving bit error rates and power efficiency [11].

An evaluation of various gating techniques identifies the most effective approach for low-power prescaler designs, informing the proposed architecture [12]. A recent study shows improved bit error rates and power efficiency, relevant to secure communication systems using scramblers [13].

The latest advancements enhance throughput by predicting LFSR states, reducing latency in communication systems, validated through simulations [14]. Studies explore FinFET-based 4-bit hybrid carry select adders and low-power CMOS-based 28T full adders, offering insights into transistor sizing and low-power sequential circuit design for modern scramblers [15], [16].

Collectively, these advancements underscore the ongoing need to balance design complexity with performance metrics in scrambler circuit development, especially as communication standards evolve towards higher data rates and lower power budgets.

III. Methodology and Implementation

The primary challenge in modern high-speed digital communication systems is mitigating issues caused by long sequences of identical bits, which can disrupt clock recovery and degrade signal integrity. To address this, traditional serial scramblers employ a linear feedback shift register (LFSR) architecture comprising D flip-flops and XOR gates [1]. This design, typically processing one bit per clock cycle, uses a series of D flip-flops in a shift register configuration, with selected outputs XORed and fed back to the input, ensuring a randomized data output to enhance signal characteristics [2]. The baseline traditional scrambler implemented in this study, consisting of four D flip-flops and one XOR gate, was designed and simulated using Cadence Virtuoso with the GPDK 45nm technology node to serve as a reference model for further enhancements.

Despite their simplicity and low hardware requirements, traditional serial scramblers suffer from significant power consumption limitations that hinder their suitability for modern high-data-rate applications such as USB 3.0 or high-speed Ethernet. The continuous clock toggling in traditional designs results in excessive switching activity in D flip-flops, leading to high dynamic power dissipation, particularly at high frequencies [3]. This inefficiency is compounded by the lack of power optimization mechanisms, which increases overall energy consumption and electromagnetic interference (EMI) [1]. These power-related shortcomings necessitate innovative design approaches, such as multiplexer-based architectures and clock gating, to enhance energy efficiency while maintaining compact and reliable operation.

To overcome the throughput limitation, a 2:1 multiplexer (MUX) was integrated into the traditional scrambler design, enabling the processing of two bits per clock cycle. This modification doubles the data rate by selecting between two input streams based on a control signal, effectively enhancing the scrambling speed [4]. The MUX-based design retains the core LFSR structure with four D flip-flops but incorporates three XOR gates to handle additional logic operations, as

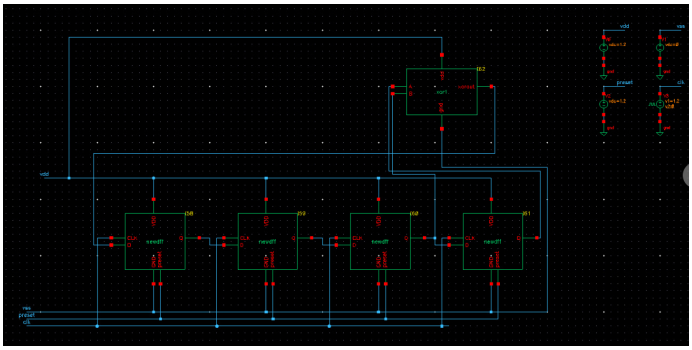

Fig. 1. Traditional serial scrambler schematic with 4 D flip-flops and 1 XOR gate, designed in Cadence Virtuoso.

shown in the schematic. The power consumption of this enhanced design is governed by the equation:

$$P = \alpha C_L V_{DD}^2 f + I_{\text{leakage}} V_{DD} \tag{1}$$

where α is the switching activity factor, C_L is the load capacitance, V_{DD} is the supply voltage, f is the operating frequency, and I_{leakage} accounts for static power. While this design significantly improves efficiency, it increases power consumption to 5.92 µW and transistor count to 104 compared to the traditional scrambler's 3.09 µW and 60 transistors [5].

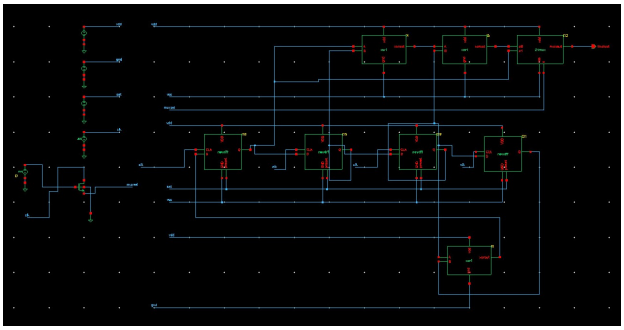

Fig. 2. Modified serial scrambler schematic with a 2:1 multiplexer and three XOR gates, designed in Cadence Virtuoso.

To address the increased power consumption of the MUX-based design, a clock gating mechanism was introduced using an AND gate to control the MUX select line [6]. This approach reduces unnecessary switching by enabling the clock signal only when data processing is required, lowering the dynamic power component. The power reduction due to clock gating can be expressed as:

$$P_{\text{gated}} = P_{\text{ungated}} \cdot (1 - d) \tag{2}$$

where d represents the duty cycle of the gated clock. This modification reduced power consumption to 5.52 µW while maintaining the doubled data rate, though it slightly increased the transistor count to 110 [7].

Further optimization was achieved by replacing the AND gate-based clock gating with pass transistor logic (PTL). The PTL-based approach uses a transmission gate, comprising complementary NMOS and PMOS transistors, to selectively propagate the clock signal based on an enable input [8]. This design minimizes switching activity more effectively, reducing power consumption to 4.70 µW while keeping the transistor count at 105. The PTL-based gated clock enhances power efficiency by ensuring the clock signal is transmitted only when the enable signal is active, as illustrated in the schematic.

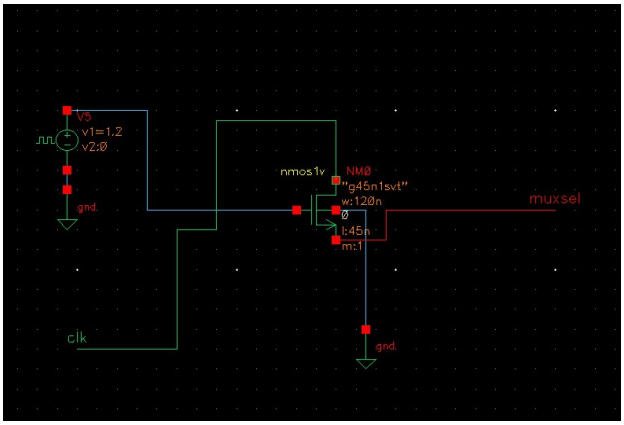

Fig. 3. Optimized serial scrambler schematic with a 2:1 multiplexer and PTL-based clock gating, designed in Cadence Virtuoso.

The iterative enhancements demonstrate a clear progression in balancing throughput, power, and area. The MUX-based design addresses the throughput limitation of traditional scramblers, while the PTL-based clock gating optimizes power efficiency, making the proposed architecture suitable for high-speed, low-power digital communication systems [9]. Post-layout simulations in Cadence Virtuoso validate these improvements, highlighting the PTL-based design as the optimal solution for modern applications.

IV. Results and Discussion

The results from the scrambler design project highlight notable improvements in performance and efficiency. The conventional serial scrambler, which processes a single bit per clock cycle, demonstrated a power usage of 3.09 µW and required 60 transistors. Despite its low power consumption and minimal area, its limited speed made it unsuitable for high-frequency digital applications. To address this, a 2:1 MUX was integrated at the output, enabling the scrambling of two bits per clock cycle. This modification significantly improved processing speed but resulted in a rise in power consumption to 5.92 µW and an increase in the transistor count to 104, presenting a tradeoff between speed enhancement and power efficiency.

The sequence obtained is as shown in figure (3) where the topmost graph represents the serial scrambler output.

The graphs below represent the power distribution of the sequence and the clock signal pulse. To counteract the higher power requirements introduced by the MUX, a clock gating mechanism based on an AND gate was incorporated. This technique minimized unnecessary transitions, reducing the

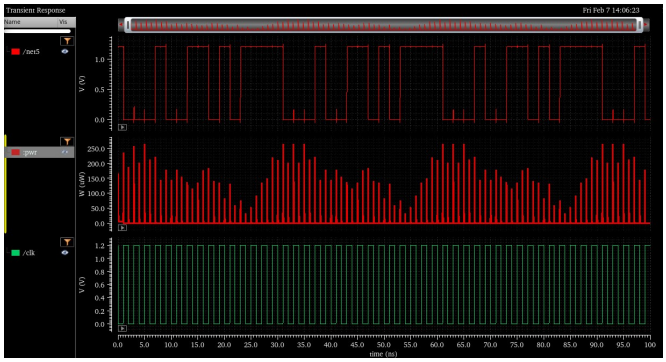

Fig. 4. The output sequence of a traditional serial scrambler along with the power analysis of the sequence.

overall power consumption to 5.52 µW while sustaining the improved data rate. However, this modification also slightly expanded the circuit's area to 110 transistors. Although the reduction in power was beneficial, it was not enough to fully compensate for the increase in energy usage compared to the baseline scrambler. This emphasized the need for a more optimized approach to balancing power efficiency with speed improvements.

Figure (4) represents the output of the modified scrambler with the use of 2:1 MUX and the gated clock. The topmost graph represents the graph of the serial scrambler which is similar to the first graph in figure (3). The graph below represents the power distribution of the sequence. The third graph represents the MUX select input and the final graph represents the clock signal pulse.

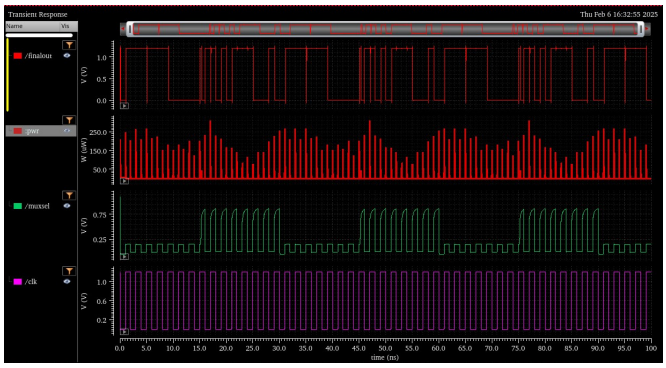

Fig. 5. The modified serial scrambler output graphs.

Overall, the design iterations resulted in a 100 percent increase in data processing speed while simultaneously leading to an 83 percent rise in circuit area and a 91 percent increase in power consumption. The final optimized design effectively reduced power consumption by 21 percent and minimized the area by 5 percent, achieving a more efficient balance between speed, energy usage, and circuit complexity. This illustrates the importance of strategic modifications in digital VLSI systems to enhance performance without excessive power tradeoffs.

The findings of this study reinforce the critical role of clock gating techniques in power-sensitive applications, especially in high-speed communication systems. By leveraging PTL-based gating, the proposed scrambler managed to sustain high data rates with improved power efficiency. Future work could explore additional optimization techniques, such as dynamic voltage scaling or alternative low-power design methodologies, to further refine the tradeoff between speed, power, and area in digital circuit design.

TABLE I
COMPARISON TABLE OF ALL THE PROPOSED MODELS FOR 2 BITS/CLOCK

Type of scrambler	Power consumption (µW)	Area (transistor count)
Traditional serial scrambler[2]	6.18	120
Serial scrambler with 2:1 MUX[4]	5.92	104
Serial scrambler with 2:1 MUX with gated clock (AND gate)[6]	5.52	110
The proposed serial scrambler with 2:1 MUX with gated clock (PTL)	4.70	105

V. Conclusion and Future Scope

The proposed serial scrambler design achieves a doubled data rate of 2 bits per clock cycle by integrating a 2:1 multiplexer, addressing the throughput limitations of traditional scramblers. Initial power consumption increased to 5.92 µW from 3.09 µW, but clock gating techniques, particularly PTL-based gating, reduced it to 4.70 µW, a 21% improvement over the MUX-only design. The transistor count rose from 60 to 105, a modest increase for the performance gains. Simulated in 45nm CMOS using Cadence Virtuoso, the design balances speed, power, and area, making it ideal for high-speed protocols like USB and Ethernet. Future work can explore dynamic voltage scaling, FinFET-based designs, or adaptive clock gating to further reduce power and enhance scalability. Approximate computing and reconfigurable logic could also improve efficiency and flexibility for applications like 5G and cryptographic systems. These advancements position the scrambler for next-generation communication systems, with potential for further optimization in power-aware circuit design.

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