4. ELECTRICAL SPECIFICATIONS

4.1 TMS7000/TMS7020/TMS7040/TMS70120/TMS7001/TMS7041

4.1.1 Description Of The TMS7000/TMS7020/TMS7040/TMS70120/TMS7001/TMS7041

The TMS70X0 devices (TMS7000, TMS7020, TMS7040, and TMS70120) are single chip 8-bit microcomputers containing a CPU, timer, I/O, RAM, and various amounts of on-chip ROM. The TMS7020 contains the CPU, RAM, timer, and I/O on-chip, and also provides 2K bytes of on-chip ROM. The TMS7040 offers the same features as the TMS7020 and has an increased on-chip ROM size of 4K bytes. The TMS70120 offers the same features as the general family and efficiently handles large programs with 12K bytes of on-chip ROM. The TMS7000 family member contains the same features of the TMS7020 except it contains no on-chip ROM.

The TMS70X1 devices (TMS7001 and TMS7041) contain a flexible on-chip serial port in addition the CPU, timer, I/O, and on-chip RAM and ROM. The TMS7041 contains 4K bytes of on-chip ROM, while the TMS7001 has no on-chip ROM.

Each member in the TMS70X0 and TMS70X1 families have 128 bytes of on-chip RAM, and all have the capability through memory expansion modes, to access up to 64K bytes of address space. For additional information on the TMS7000 family architecture, refer to Section 2.

Table 4-1 depicts the TMS70X0 and TMS70X1 family features.

TABLE 4-1 – TMS70X0 AND TMX70X1 FAMILY FEATURES

FEATURES		FAMILY MEMBERS					
		7000	7020	7040	70120	7001	7041
ON-CHIP ROM (BYTES)		NONE	2K	4K	12K	NONE	4K
ON-CHIP RAM (BYTES)		128	128	128	128	128	128
INTERRUPT LEVELS		4	4	4	4	6	6
TIMERS	13-BIT	1	1	1	1	2	2
	10-BIT	0	0	0	0	1	1
I/O LINES:							
BI-DIRECTIONAL		16	16	16	16	22	22
INPUT ONLY		8	8	8	8	2	2
OUTPUT ONLY		8	8	8	8	8	8
ADDITIONAL I/O		–	–	–	–	SERIAL PORT	SERIAL PORT
PROCESS TECHNOLOGY		NMOS	NMOS	NMOS	NMOS	NMOS	NMOS

Unless otherwise indicated the following specifications for the TMS7000 apply to the TMS7020, TMS7040, TMS70120, TMS7001, and TMS7041.

4.1.2 Key Features

- Microprogrammable instruction set
- Strip Chip Architecture Topology (SCAT) for rapid family expansion
- Register-to-register architecture
- Family members with 2K, 4K, and 12K bytes of on-chip ROM and ROMless versions
- On-chip 8-bit timer/event counter with 5-bit prescale:
  - Internal interrupt with automatic reload
  - Capture latch
  - Second 8-bit timer/event counter with 5-bit prescale and cascade capability (TMS7001 and TMS7041 only)
- Flexible on-chip serial port (TMS7001 and TMS7041 only)
  - Fully software programmable
  - Internal or external baud rate generator
  - Separate baud rate timer usable as a third timer
  - Asynchronous, isosynchronous, or serial modes
  - Two multiprocessor communication formats
- 128-byte RAM register file
- Full-feature data/program stack
- 32 TTL-compatible I/O pins:
  - 16 bi-directional pins (22 bi-directional pins on TMS7001 and TMS7041)
  - 8 output pins
  - 8 high-impedance input pins (2 input pins on TMS7001 and TMS7041)
- Memory-mapped ports for easy addressing
- 256-byte peripheral file
- Memory expansion capability:
  - 64K byte address space
- 8-bit instruction word
- Eight powerful addressing formats including:
  - Register-to-register arithmetic
  - Indirect addressing on any register pair
  - Indexed and indirect branches and calls
- Two's complement arithmetic
- Single-instruction binary coded decimal (BCD) add and subtract
- Two external maskable interrupts
- Flexible interrupt handling:
  - Priority servicing of simultaneous interrupts
  - Software execution of hardware interrupts
  - Precise timing of interrupts with the capture latch
  - Software monitoring of interrupt status
- Accurate pulse width measurement and modulation
- N-channel silicon gate MOS, 5-volt power supply
- 40-pin, 600-mil, dual-in-line package
- 100-mil or 70-mil pin-to-pin spacing packages

4.1.3 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage, V_{CC} (See Note 1) . . . . . −0.3 V to 7 V
All input voltages . . . . . −0.3 V to 20 V
All output voltages . . . . . −0.3 V to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise noted, all voltages are with respect to V_{SS}.

4.1.4 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	CLOCKIN	2.6		$V_{CC}+0.5$	V
	MC	14			V
	All others	2		$V_{CC}+0.5$	V
Low-level input voltage, V_{IL}	CLOCKIN			0.6	V
	All others			0.8	V
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				10	mA
Operating free-air temperature, T_A		0		70	°C

4.1.5 Electrical Characteristics Over Full Range of Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
I_I	Input current, Port A INPUT-only pins	$V_I = V_{SS}$ to V_{CC}		±2	±10	μA
I_I	Input current, I/O pins	$V_I = 0.4$ V to V_{CC}		±10	±100	μA
C_I	Input capacitance			2		pF
V_{OH}	High-level output voltage	$I_O = -400$ μA	2.4	2.8		V
V_{OL}	Low-level output voltage	$I_O = 3.2$ mA		0.2	0.4	V
$t_{r(O)}$	Output rise time‡			9	50	ns
$t_{f(O)}$	Output fall time‡			10	60	ns
I_{CC}	Supply current	All outputs open		80	150	mA
$P_{D(av)}$	Average power dissipation			400	825	mW

† All typical values are at $V_{CC} = 5$ V, $T_A = 25$°C.
‡ Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points (see Figure 4-2). Outputs have 100-pF loads to V_{SS}.

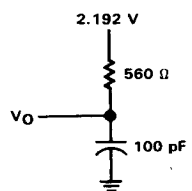


FIGURE 4-1 — OUTPUT LOADING CIRCUIT FOR TEST

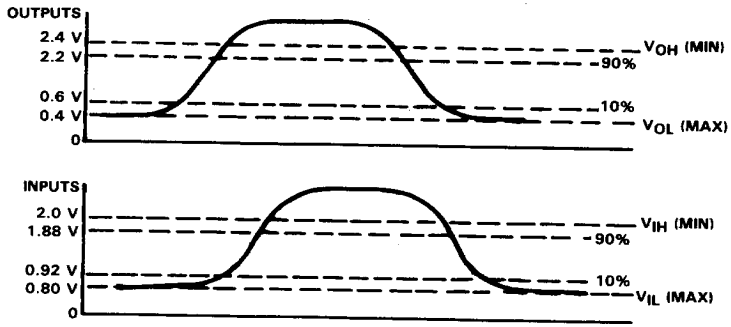


FIGURE 4-2 — MEASUREMENT POINTS FOR SWITCHING CHARACTERISTICS

4.1.6 Recommended CRYSTAL/CLOCKIN Operating Conditions Over Full Operating Range

	PARAMETER	MIN	TYP	MAX	UNIT
f_{osc}	CRYSTAL/CLOCKIN frequency (divide-by-4 option)	2.0		10.1	MHz
f_{osc}	CRYSTAL frequency (divide-by-2 option) (see Note 1)	1.0		5.05	MHz
$t_{c(P)}$	CRYSTAL/CLOCKIN cycle time (divide-by-4 option)	99		500	ns
$t_{c(P)}$	CRYSTAL cycle time (divide-by-2 option)	198		1000	ns
$t_{c(S)}$	Internal state cycle time	396		2000	ns
$t_{w(PH)}$	CLOCKIN pulse width high	45			ns
$t_{w(PL)}$	CLOCKIN pulse width low	45			ns
t_r	CLOCKIN rise time‡			30	ns
t_f	CLOCKIN fall time‡			30	ns
$t_{d(PH-CL)}$	CLOCKIN rise to CLOCKOUT rise delay		125	200	ns

‡ Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points (see Figure 4-2). Outputs have 100-pF loads to V_{SS}.

NOTE 1: Divide-by-4 option recommended with external clock drive.

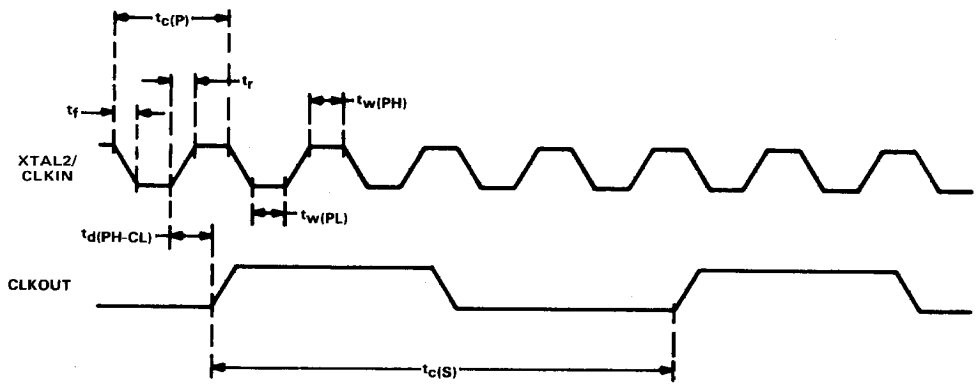
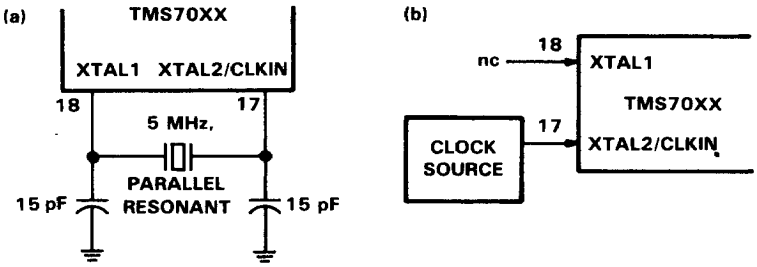


FIGURE 4-3 — CLOCK TIMING



NOTES: The divide-by-2 input can be used with XTAL only. Divide-by-4 can be used with XTAL or CLKIN inputs. Alternative use of ceramic resonators is illustrated in Section 4.1.8.

FIGURE 4-4 — RECOMMENDED CLOCK CONNECTIONS

4.1.7 Memory Interface Timing At 10 MHz Over Full Operating Free-Air Temperature Range

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(C)}$	CLOCKOUT cycle time (see Note)	400		2000	ns
$t_{w(CH)}$	CLOCKOUT high pulse width	130	170	200	ns
$t_{w(CL)}$	CLOCKOUT low pulse width	150	190	240	ns
$t_{d(CH-JL)}$	CLOCKOUT rising to ALATCH falling edge	260	300	340	ns
$t_{d(CH-EL)}$	CLOCKOUT rising to $\overline{ENA}$ falling	-10	15	50	ns
$t_{w(JH)}$	ALATCH high pulse width	150	190	230	ns
$t_{d(AH-JL)}$	High address valid before ALATCH fall	50	170	220	ns
$t_{d(AL-JL)}$	Low address valid before ALATCH fall	50	150	220	ns
$t_{h(JL-AL)}$	Low address hold after ALATCH fall	30	45	80	ns
$t_{d(RW-JL)}$	RD/$\overline{WR}$ valid before LATCH fall	50	140	200	ns
$t_{h(EH-RW)}$	RD/$\overline{WR}$ hold after $\overline{ENA}$ rise	40	100		ns
$t_{h(EH-AH)}$	High address hold after $\overline{ENA}$ rise	30	40		ns
$t_{h(EH-Q)}$	Data out hold after $\overline{ENA}$ rise	65	80		ns
$t_{d(Q-EH)}$	Data out valid before $\overline{ENA}$ rise	230	290		ns
$t_{d(AF-EL)}$	$\overline{ENA}$ fall after low address HI-Z	0	30	120	ns
$t_{d(EH-AF)}$	$\overline{ENA}$ rising to next address drive	60	85		ns
$t_{d(EL-D)}$	Data in after $\overline{ENA}$ falling	155	190		ns
$t_{h(EH-D)}$	Data in hold after $\overline{ENA}$ rise	0			ns
$t_{d(A-D)}$	Access time, data in from valid address	400	470		ns
$t_{d(A-EH)}$	$\overline{ENA}$ high after address valid	580		730	ns

NOTE: $t_c(C)$ is defined to be $4/f_{osc}$ (or $2/f_{osc}$ if the divide-by-2 option is selected) and may be referred to as a machine state or simply a state.

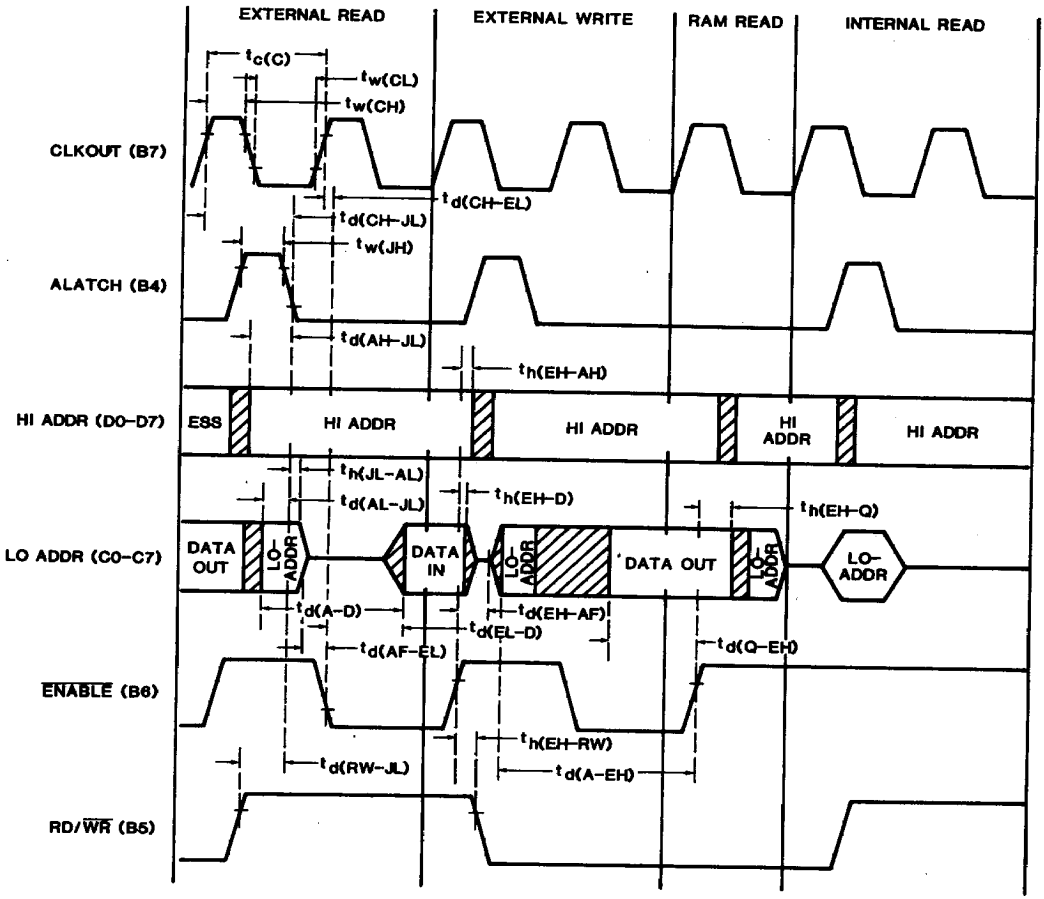


FIGURE 4-5 — READ AND WRITE CYCLE TIMING

4.1.8 Application of Ceramic Resonator

The resonant circuit shown in Figure 4-6 provides an economical alternative to quartz crystals where frequency tolerance is not a major concern. Frequency tolerance over temperature is about 1%.

Ceramic resonator suppliers.

MURATA CORPORATION OF AMERICA
1148 Franklin Rd. SE.
Marrietta, GA. 30067
404/952-9777
Telex: 0542329 Murata ATL

For 5 MHz operation
Resonator ceralock CSA5.00MT
Resistor 1 MΩ 10%
Capacitors (both) 30 pF

NGK SPARK PLUGS (USA) INC.
20608 Madrona Ave.
Torrance, CA 90503
213/328-6882
Telex: 664290

For 5 MHz operation
Resonator R5.0M
Resistor 1 MΩ 10%
Capacitors 68 pF ± 10%

KYOCERA INTERNATIONAL
8611 Balboa Ave.
San Diego, CA 92123
714/279-8310
Telex: 697929

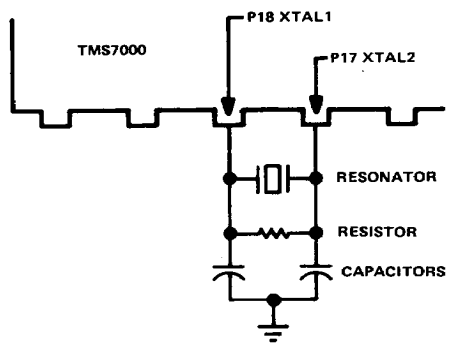
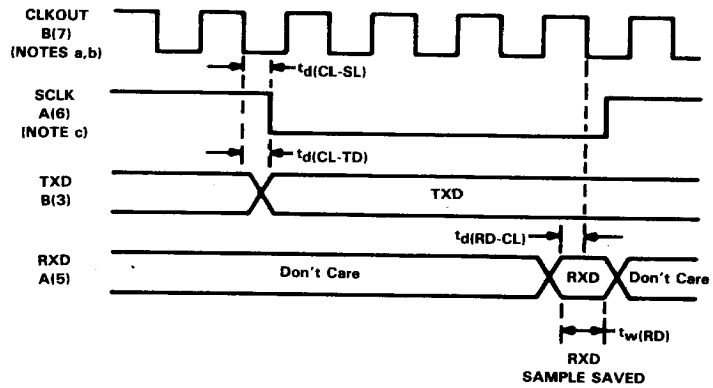


FIGURE 4-6 — CERAMIC RESONATOR CIRCUIT

4.1.9 Serial Port Timing (TMS7001, TMS7041, And SE70P161 Only)

4.1.9.1 Internal Serial Clock

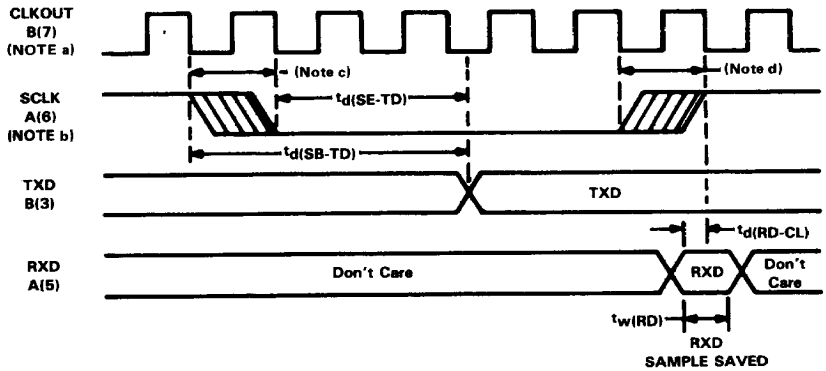


NOTES:

a) The CLKOUT signal is not available in Single-Chip mode.
b) CLKOUT = $t_{c(C)} = \emptyset$
c) Example shows SCLK = $\emptyset/8$.

PARAMETER		TYP	UNIT
$t_{d(CL-SL)}$	CLKOUT low to SCLK low	1/4 $t_{c(C)}$	ns
$t_{d(CL-TD)}$	CLKOUT low to new TXD data	1/4 $t_{c(C)}$	
$t_{d(RD-CL)}$	RXD data valid before CLKOUT low	1/4 $t_{c(C)}$	
$t_{w(RD)}$	RXD data valid time	1/2 $t_{c(C)}$	

4.1.9.2 *External Serial Clock*

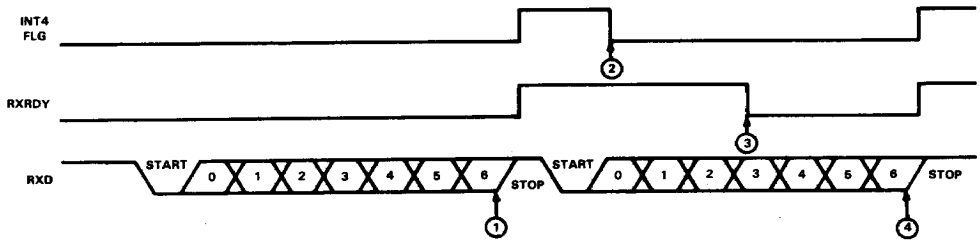


NOTES:

a) The CLKOUT signal is not available in Single-Chip mode.
CLKOUT = $t_{c(C)} = \emptyset$
b) Example shows SCLK = $\emptyset/10$.
c) SCLK sampled; if 1 then 0, fall transition found.
d) SCLK sampled; if 0 then 1, rise transition found.

	PARAMETER	TYP	UNIT
$t_{d(RD-CL)}$	RXD data valid before CLKOUT low	1/4 $t_{c(C)}$	ns
$t_{w(RD)}$	RXD data valid time	1/2 $t_{c(C)}$	
$t_{d(SB-TD)}$	Start of SCLK sample to new TXD data	3¼ $t_{c(C)}$	
$t_{d(SE-TD)}$	End of SCLK sample to new TXD data	2¼ $t_{c(C)}$	

4.1.9.3 Rx Signals In Communication Modes



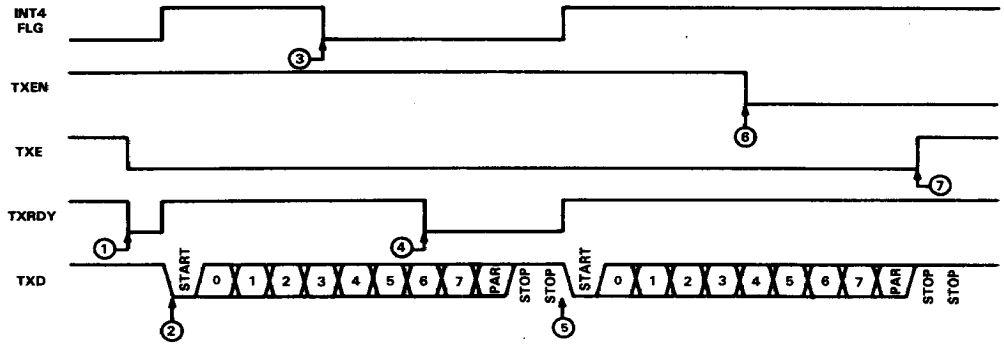
NOTES:

a) Format shown is start bit + seven data bits + stop bits.
b) SCLK is continuous, external or internal.
c) User means user software executed by CPU.
d) If RXEN = 0, RXSHF still receives data from RXD. However, the data is not transferred to RXBUF and RXRDY and INT4 FLG are not set.

SEQUENCE OF EVENTS

1) RXSHF data is transferred to RXBUF. Error status bits are set if an error is detected.
2) } User writes to INT4 CLR to clear INT4 FLG. If not, CPU clears.
3) } INT4 FLG on entry to Level 4 interrupt routine.
4) User reads RXBUF.

4.1.9.4 Tx Signals In Communication Modes



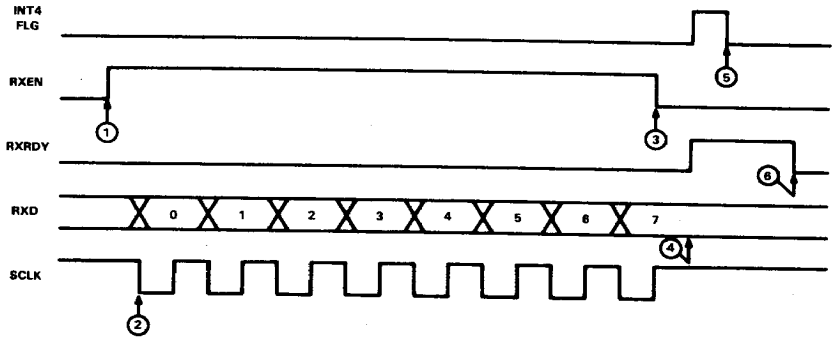
NOTES:

a) Format shown is start plus eight data parity bits plus two stop bits.
b) SCLK is continuous whether internal or external.
c) User means user software executed by CPU.

SEQUENCE OF EVENTS

1) } User writes to TXBUF.
4) }
2) } TXBUF and WU data is transferred to TXSHF and WUT and
5) } INT4 FLG and TXRDY are set.
6) User resets TXEN; current frame will finish and transmission will stop whether TXBUF is full or empty.
7) TXE is set if TXBUF and TXSFT are empty.
3) User writes to INT4 CLR to clear INT4 FLG or CPU clears INT4 FLG on entry to level 4 interrupt routine.

4.1.9.5 Rx Signals in Serial I/O Modes



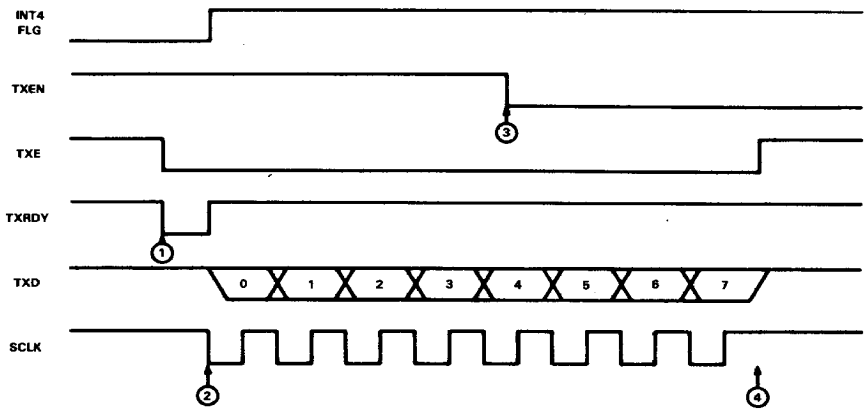
NOTES:

a) RXEN has no effect on INT4 FLG or RXRDY in serial I/O mode.
b) RXD is sampled on SCLK rise; external shift registers should be clocked on SCLK fall.
c) The SCLK source should be internal as it is gated by internal circuitry.

SEQUENCE OF EVENTS

1) User starts receiving by setting RXEN.
2) Gated SCLK starts and data is received.
3) RXEN is automatically cleared in last data bit.
4) RXSHF data is transferred to RXBUF and RXRDY and INT4 are set.
5) User writes to INT4 CLR to clear INT4 FLG; if not CPU clears INT4 FLG on entry to level 4 interrupt routine.
6) User reads RXBUF.

4.1.9.6 Tx Signals in Serial I/O Modes



NOTES:

a) Format shown is eight data bits.
b) The SCLK source should be internal as it is gated by internal circuitry.

SEQUENCE OF EVENTS

1) User writes to TXBUF.
2) TXBUF data is transferred to TXSFT; INT4 FLG and TXRDY are set and SCLK starts.
3) User resets TXEN, current frame will finish and transmission will halt whether TXBUF is full or empty.
4) Frame ends and SCLK stops because TXEN = 0.

4.1.10 Pin Descriptions

4.1.10.1 Pin Description of The TMS7000/TMS7020/TMS7040/TMS70120

Figure 4-7 defines the pin assignments and describes the function of each pin for the Single-Chip (SC), Peripheral Expansion (PE), Full Expansion (FE), and Microprocessor Modes for the TMS70X0 family (TMS7000, TMS7020, TMS7040, TMS70120).

SIGNATURE	PIN	I/O	DESCRIPTION
A0 (LSB)	6	IN	I/O Port A: Input lines
A1	7	IN	(Specific I/O configuration for;
A2	8	IN	Single Chip Mode — see Section 2.3.1,
A3	9	IN	Peripheral Expansion Mode — see
A4	10	IN	Section 2.3.2, Full Expansion
A5	16	IN	Mode — see Section 2.3.3, Micro-
A6	15	IN	processor Mode — see Section 2.3.4)
A7 (MSB)	11	IN	
B0 (LSB)	3	OUT	I/O Port B: Output lines
B1	4	OUT	(Specific I/O configuration for;
B2	5	OUT	Single Chip Mode — see Section 2.3.1,
B3	37	OUT	Peripheral Expansion Mode — see
B4/ALATCH	38	OUT	Section 2.3.2, Full Expansion
B5/R/$\overline{W}$	1	OUT	Mode — see Section 2.3.3,
B6/$\overline{ENABLE}$	39	OUT	Microprocessor Mode — see Section
B7/CLOCKOUT	2	OUT	2.3.4)
C0 (LSB)	28	I/O	I/O Port C: General purpose bidirectional
C1	29	I/O	lines (Specific I/O configuration for; Single
C2	30	I/O	Chip Mode — see Section 2.3.1, Peripheral
C3	31	I/O	Expansion Mode — see Section 2.3.2,Full
C4	32	I/O	Expansion Mode — see Section 2.3.3,
C5	33	I/O	
C6	34	I/O	Microprocessor Mode — see Section 2.3.4)
C7 (MSB)	35	I/O	
D0 (LSB)	27	I/O	I/O Port D: General purpose
D1	26	I/O	bidirectional lines (Specific
D2	24	I/O	I/O Configurations for; Single
D3	23	I/O	Chip Mode — see Section 2.3.1,
D4	22	I/O	Peripheral Expansion Mode — see
D5	21	I/O	Section 2.3.2, Full Expansion Mode —
D6	20	I/O	see Section 2.3.3, Microprocessor
D7 (MSB)	19	I/O	Mode — see Section 2.3.4)
$\overline{INT1}$	13	IN	Maskable Interrupt
$\overline{INT3}$	12	IN	Maskable Interrupt
$\overline{RESET}$	14	IN	$\overline{RESET}$
MC	36	IN	Mode Control
XTAL2/CLKIN	17	IN	Crystal input for control of internal OSC.; input pin for external OSC. or LRC networks
XTAL1	18	IN	Crystal input for control of internal OSC.; leave open for external OSC.
V_{CC}	25	IN	Supply voltage (+5V)
V_{SS}	40	IN	Ground reference

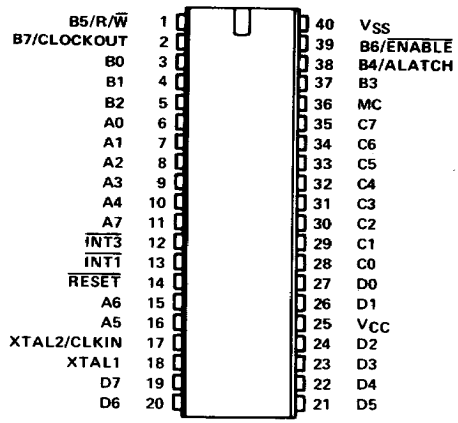


FIGURE 4-7 — SC, FE, PE, AND MICROPROCESSOR MODE PIN ASSIGNMENTS

4.1.10.2 Pin Description Of The TMS7001/TMS7041

Figure 4-8 defines the pin assignments and describes the function of each pin for the Single-Chip (SC), Peripheral Expansion (PE), Full Expansion (FE), and Microprocessor Modes for the TMS70X1 family (TMS7001 and TMS7041)

SIGNATURE	PIN	I/O	DESCRIPTION
A0 (LSB)	6	I/O	I/O Port A: General Purpose Bidirectional lines
A1	7	I/O	(Specific I/O configuration for:
A2	8	I/O	Single Chip Mode — see Section 2.3.1,
A3	9	I/O	Peripheral Expansion Mode — see
A4	10	I/O	Section 2.3.2, Full Expansion
A5/RXD	16	IN	Mode — see Section 2.3.3, Micro-
A6/SCLK	15	I/O	processor Mode — see Section 2.3.4)
A7	11	IN	
B0 (LSB)	3	OUT	I/O Port B: General purpose Output lines
B1	4	OUT	(Specific I/O configuration for:
B2	5	OUT	Single Chip Mode — see Section 2.3.1,
B3/TXD	37	OUT	Peripheral Expansion Mode — see
B4/ALATCH	38	OUT	Section 2.3.2, Full Expansion
B5/R/$\overline{W}$	1	OUT	Mode — see Section 2.3.3,
B6/$\overline{ENABLE}$	39	OUT	Microprocessor Mode — see Section
B7/CLOCKOUT	2	OUT	2.3.4)
C0 (LSB)	28	I/O	I/O Port C: General purpose bidirectional
C1	29	I/O	lines (Specific I/O configuration for: Single
C2	30	I/O	Chip Mode — see Section 2.3.1, Peripheral
C3	31	I/O	Expansion Mode — see Section 2.3.2, Full
C4	32	I/O	Expansion Mode — see Section 2.3.3,
C5	33	I/O	
C6	34	I/O	Microprocessor Mode — see Section 2.3.4).
C7 (MSB)	35	I/O	
D0 (LSB)	27	I/O	I/O Port D: General purpose
D1	26	I/O	bidirectional lines (Specific
D2	24	I/O	I/O Configuration for: Single
D3	23	I/O	Chip Mode — see Section 2.3.1,
D4	22	I/O	Peripheral Expansion Mode — see
D5	21	I/O	Section 2.3.2, Full Expansion Mode —
D6	20	I/O	see Section 2.3.3, Microprocessor
D7 (MSB)	19	I/O	Mode — see Section 2.3.4).
$\overline{INT1}$	13	IN	Maskable Interrupt
$\overline{INT3}$	12	IN	Maskable Interrupt
$\overline{RESET}$	14	IN	$\overline{RESET}$
MC	36	IN	Mode Control
XTAL2/CLKIN	17	IN	Crystal input for control of internal OSC.; input pin for external OSC. or LRC networks
XTAL1	18	IN	Crystal input for control of internal OSC.; leave open for external OSC.
V_{CC}	25	IN	Supply voltage (+5 V)
V_{SS}	40	IN	Ground reference

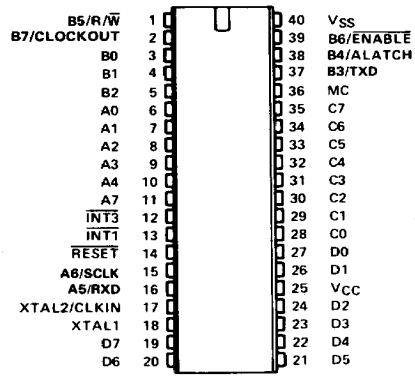


FIGURE 4-8 — SC, FE, PE, AND MICROPROCESSOR MODE PIN ASSIGNMENTS

4.2 TMS70C00/TMS70C20/TMS70C40

4.2.1 DESCRIPTION OF THE TMS70C00/TMS70C20/TMS70C40

The TMS70C00, TMS70C20, and TMS70C40 devices extend the TMS7000 family line into low power CMOS applications. They are single chip 8-bit microcomputers containing CPU, timers, I/O, and on-chip RAM and ROM. Table 4-2 presents the basic features of the present TMS70CXX family members.

The TMS70CXX family (TMS70C00, TMS70C20, and TMS70C40 devices) are fully software and pin compatible with their TMS70XX NMOS counterparts. They differ in the areas of interrupt operation, power down modes, input/output levels, operating voltage, and frequency range.

The TMS70CXX family maintains the four hardware interrupt levels of the TMS70XX family ($\overline{\text{RESET}}$, $\overline{\text{INT1}}$, $\overline{\text{INT2}}$, and $\overline{\text{INT3}}$). The TMS70CXX family implements $\overline{\text{INT1}}$ as only a latched interrupt, not a latched and level interrupt as on the TMS70XX NMOS devices. The TMS70CXX family implements $\overline{\text{RESET}}$, $\overline{\text{INT2}}$, and $\overline{\text{INT3}}$ in exactly the same manner as in the TMS70XX family (i.e., $\overline{\text{INT3}}$ is both latch and level sensitive). Refer to Section 2.5 for additional information on interrupt operation.

The TMS70CXX family supports two low power modes, the WAKE-UP mode and the HALT modes. Both of these modes are entered via execution of the IDLE instruction. The selection of the power down mode is determined by bit 5 of the timer 1 control register (T1CTRL) and then executing the IDLE instruction. The device is released from both power down modes through activation of $\overline{\text{RESET}}$ or acknowledgement of an enabled interrupt. Note that interrupts must be enabled in the status register and the I/O control register (IOCNT0) before the power down mode is entered for $\overline{\text{INT1}}$, $\overline{\text{INT2}}$ (timer), or $\overline{\text{INT3}}$ to be acknowledged. It is important that both power down modes provide RAM data retention.

Unless otherwise indicated, the following specifications for the TMS70C00 apply to the TMS70C20 and TMS70C40 as well.

TABLE 4-2 — TMS70CX0 FAMILY FEATURES

FEATURES	FAMILY MEMBER		
	70C00	70C20	70C40
ON-CHIP ROM (BYTES)	NONE	2K	4K
ON-CHIP RAM (BYTES)	128	128	128
INTERRUPT LEVELS	4	4	4
GENERAL PURPOSE INTERNAL REGISTERS	128	128	128
TIMERS	13-BIT	13-BIT	13-BIT
I/O LINES:			
BI-DIRECTIONAL	16	16	16
INPUT ONLY	8	8	8
OUTPUT ONLY	8	8	8
ADDITIONAL I/O	–	–	–
PROCESS TECHNOLOGY	CMOS	CMOS	CMOS

4.2.2 Key Features

- Microprogrammable instruction set
- Strip Chip Architecture Topology (SCAT) for rapid family expansion
- Register-to-register architecture
- Family members with 2K and 4K bytes of on-chip ROM and a ROMless version
- On-chip 8-bit timer/event counter with:
  - Programmable 5-bit prescale
  - Internal interrupt with automatic reloading
  - Capture latch
- 128-byte RAM register file
- Full-feature data/program stack
- 32 CMOS-compatible I/O pins:
  - 16 bi-directional pins
  - 8 output pins
  - 8 high-impedance input pins
- Memory-mapped ports for easy addressing
- Wide voltage operating range, frequence range
  - 3 V - 1 MHz typical
  - 5 V - 3.3 MHz typical
- Two software selectable low-power modes
- 256-byte peripheral file
- Memory expansion capability:
  - 64K byte address space
- 8-bit instruction word
- Eight powerful addressing formats including:
  - Register-to-register arithmetic
  - Indirect addressing on any register pair
  - Indexed and indirect branches and calls
- Two's complement arithmetic
- Single-instruction binary coded decimal (BCD) add and subtract
- Two external maskable interrupts
- Flexible interrupt handling:
  - Priority servicing of simultaneous interrupts
  - Software execution of hardware interrupts
  - Precise timing of interrupts with the capture latch
  - Software monitoring of interrupt status
- Accurate pulse width measurement and modulation
- Complementary silicon gate MOS
- 40-pin, 600-mil, dual-in-line package
- 100-mil or 70-mil pin-to-pin spacing packages

4.2.3 Absolute Maximum Rating Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage, V_{DD} (See Note 1) . . . . . −0.3 V to 7 V
All input voltages . . . . . −0.3 V to V_{DD} + 0.3 V
All output voltages . . . . . −0.3 V to V_{DD} + 0.3 V
Input current . . . . . + 10 mA
Continuous power dissipation . . . . . 0.5 W
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −55°C to 150°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditons for extended periods may affect device reliability.

NOTE 1: Unless otherwise noted, all voltages are with respect to V_{SS}.

4.2.4 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{DD}		3		5.5	V
High-level input voltage, V_{IH}	V_{DD} = 5 V	V_{DD} − 1			V
	V_{DD} = 4 V	V_{DD} − 0.7			V
	V_{DD} = 3 V	V_{DD} − 0.5			V
Low-level input voltage, V_{IL}	V_{DD} = 5 V			1	V
	V_{DD} = 4 V			0.7	V
	V_{DD} = 3 V			0.5	V
Operating temperature range, T_A†		0		70	°C

† Plans are underway to extend the operating temperature range from −40°C to 85°C.

4.2.5 Electrical Characteristics Over Full Range Of Operating Conditions

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −1 mA,	V_{DD} = 5 V	V_{DD} − 2.5	V_{DD} − 0.5		V
		I_{OH} = −0.4 mA,	V_{DD} = 5 V	V_{DD} − 0.5	V_{DD} − 0.2		
V_{OL}	Low-level output voltage	I_{OL} = 1.7 mA,	V_{DD} = 5 V		0.3	0.4	V
I_I	Input leakage current	V_I = V_{DD},	V_{DD} = 5V			5	μA
I_{OH}	Source current	V_{OH} = V_{DD} − 0.5 V,	V_{DD} = 5V	−0.3	−1.2		mA
		V_{OH} = V_{DD} − 0.5 V,	V_{DD} = 4 V	−0.2	−0.8		
		V_{OH} = V_{DD} − 0.5 V,	V_{DD} = 3 V	−0.1	−0.5		
		V_{OH} = 2.5 V,	V_{DD} = 5 V	−1	−4.5		
I_{OL}	Sink current	V_{OL} = 0.4 V,	V_{DD} = 5 V	1.7	2.4		mA
		V_{OL} = 0.4 V,	V_{DD} = 4 V	1.2	1.8		
		V_{OL} = 0.4 V,	V_{DD} = 3 V	0.7	1		
I_{DD}	Supply current	Operating, f_{osc} = 3 MHz,	V_{DD} = 5 V		5.5	8	mA
		Wake-up mode, f_{osc} = 3 MHz,	V_{DD} = 5 V		500	800	μA
		Halt mode, f_{osc} = 3 MHz	V_{DD} = 5 V		250	550	μA
		Halt mode, XTAL/CLKIN = GND, all input = V_{DD} or GND,	V_{DD} = 5 V		2	10	μA

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

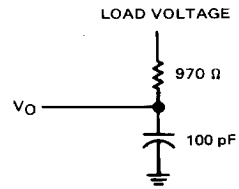


FIGURE 4-9 — OUTPUT LOADING CIRCUIT FOR TEST

4.2.6 AC Characteristics For Input/Output Ports

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
$t_{r(IO)}$	I/O port output rise time‡	C_L = 15 pF, V_{DD} = 5 V		50		ns
		C_L = 50 pF, V_{DD} = 5 V	70	110	150	
$t_{f(IO)}$	I/O port output full time‡	C_L = 15 pF, V_{DD} = 5 V		20		ns
		C_L = 50 pF, V_{DD} = 5 V	25	50	70	
$t_{t(IO)}$	I/O port input rise/fall time‡	V_{DD} = 5 V			70	ns

† All typical values are at V_{DD} = 5 V, T_A = 25°C.

‡ Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points (see Figure 4-11).

4.2.7 Recommended CRYSTAL/CLOCKIN Operating Conditions Over Full Operating Range

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{osc}	CRYSTAL frequency (see note 1)	V_{DD} = 5 V	0.5		3.6	MHz
		V_{DD} = 4 V	0.5		2.7	MHz
		V_{DD} = 3 V	0.5		1.3	MHz
$t_{c(P)}$	CRYSTAL cycle time	V_{DD} = 5 V	277		2000	ns
		V_{DD} = 4 V	370		2000	ns
		V_{DD} = 3 V	769		2000	ns
$t_{c(S)}$	Internal state cycle time	V_{DD} = 5 V	554		4000	ns
		V_{DD} = 4 V	740		4000	ns
		V_{DD} = 3 V	1538		4000	ns
t_r	CRYSTAL rise time†				30	ns
t_f	CRYSTAL fall time†				30	ns
d_{osc}	CRYSTAL duty cycle		45	50	55	%
$t_{d(PL-CL)}$	CRYSTAL fall to CLOCKOUT rise delay			100	200	ns

† Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points.

NOTE 1: TMS70CXX family members currently use only the divide-by-two option as the INPUT CLOCK option.

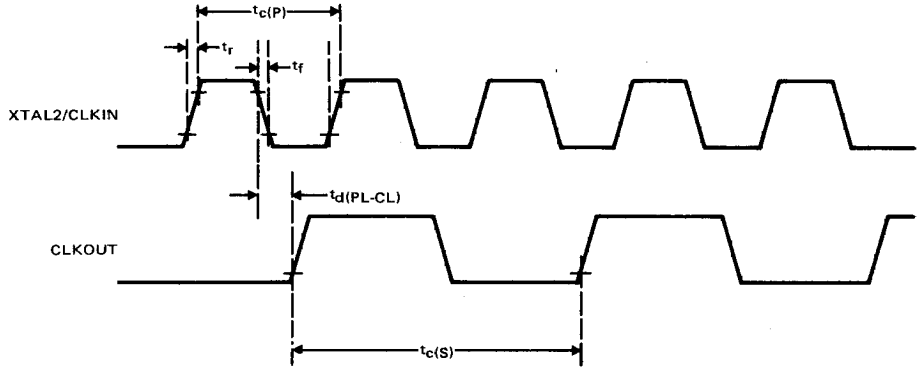


FIGURE 4-10 — CLOCK TIMING

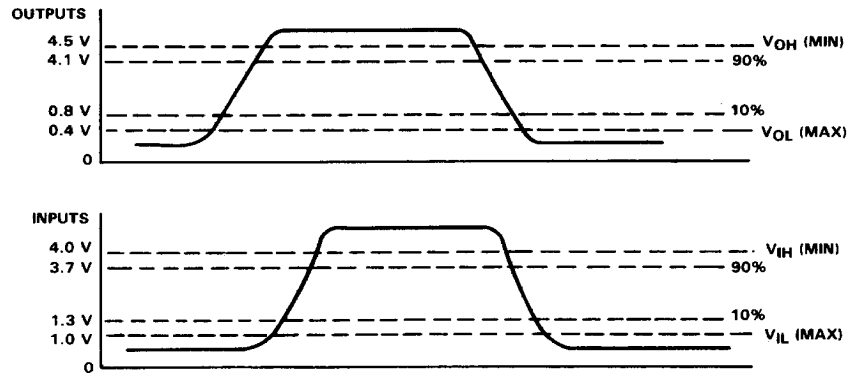


FIGURE 4-11 — MEASUREMENT POINTS FOR SWITCHING CHARACTERISTICS (V_{DD} = 5 V)

4.2.8 Memory Inteface Timing At V_{DD} = 5 V, f_{osc} = 3 MHz Over The Full Operating Free-Air Temperature Range

PARAMETER		MIN	TYP	MAX	UNIT
$t_{c(C)}$	CLOCKOUT cycle time (see note)		665		ns
$t_{w(CH)}$	CLOCKOUT high pulse duration	260	340	470	ns
$t_{w(CL)}$	CLOCKOUT low pulse duration	190	270	360	ns
$t_{d(CH-JL)}$	CLOCKOUT rising to ALATCH falling edge	400	580		ns
$t_{d(CH-EL)}$	CLOCKOUT rising to $\overline{\text{ENABLE}}$ falling	30	60		ns
$t_{w(JH)}$	ALATCH high pulse duration	260	370		ns
$t_{d(AH-JL)}$	High address valid before ALATCH fall	230	330		ns
$t_{d(AL-JL)}$	Low address valid before ALATCH fall	220	320		ns
$t_{d(JL-AL)}$	Low address hold after ALATCH fall	110	160		ns
$t_{d(RW-JL)}$	RD/$\overline{\text{WR}}$ valid before ALATCH fall	220	320		ns
$t_{h(EH-RW)}$	RD/$\overline{\text{WR}}$ hold after $\overline{\text{ENABLE}}$ rise		170		ns
$t_{h(EH-AH)}$	High address hold after $\overline{\text{ENABLE}}$ rise		165		ns
$t_{h(EH-Q)}$	Data out hold after $\overline{\text{ENABLE}}$ rise	130	190		ns
$t_{d(Q-EH)}$	Data out valid before $\overline{\text{ENABLE}}$ rise	330	480		ns
$t_{d(AF-EL)}$	$\overline{\text{ENABLE}}$ fall after low address HI-Z	0	0	20	ns
$t_{d(EH-AF)}$	$\overline{\text{ENABLE}}$ rising to next address drive		130		ns
$t_{d(EL-D)}$	Data in after $\overline{\text{ENABLE}}$ falling			290	ns
$t_{h(EH-D)}$	Data in hold after $\overline{\text{ENABLE}}$ rise	0			ns
$t_{d(A-D)}$	Access time, data in from valid address			770	ns
$t_{d(A-EH)}$	$\overline{\text{ENA}}$ high after address valid	800	1150		ns

NOTE: TMS70CXX family members use a cycle time, $t_{c(C)}$, that is equal to $2/f_{osc}$ and is referred to as a machine state or simply a state.

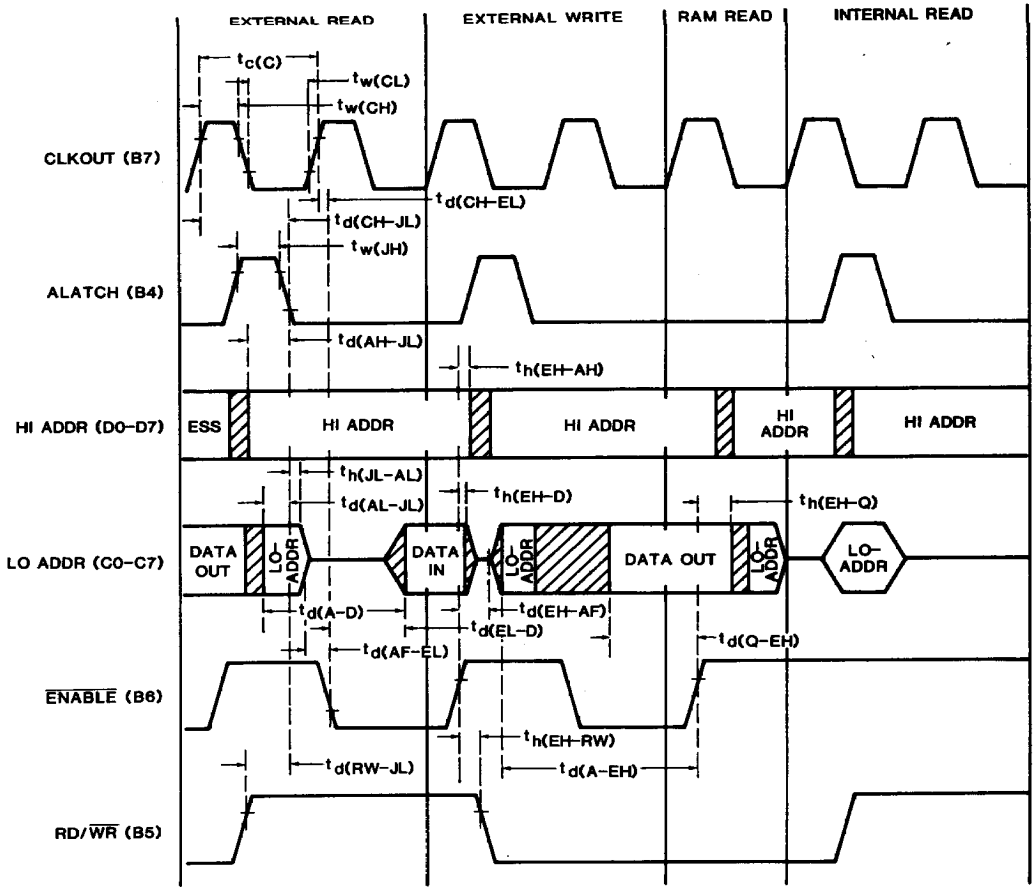
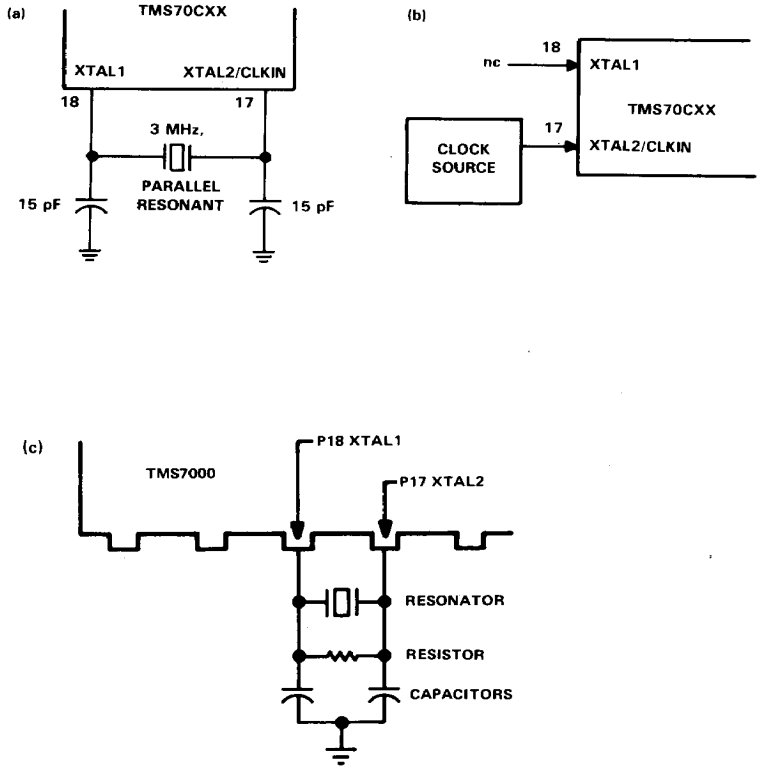


FIGURE 4-12 — READ AND WRITE CYCLE TIMING



NOTE: The TMS70CXX family currently uses only the divide-by-two option as the input clock options. Sources of ceramic resonators are given in Section 4.1.8.

FIGURE 4-13 — RECOMMENDED CLOCK CONNECTIONS

4.2.9 Pin Description Of The TMS70C00/TMS70C20/TMS70C40

Figure 4-14 defines the pin assignments and describes the function of each pin for the Single-Chip (SC), Peripheral Expansion (PE), Full Expansion (FE), and Microprocessor modes for the TMS70CX0 family (TMS70C00, TMS70C20, TMS70C40).

SIGNATURE	PIN	I/O	DESCRIPTION
A0 (LSB)	6	IN	I/O Port A: Input lines
A1	7	IN	(Specific I/O configuration for;
A2	8	IN	Single Chip Mode – see Section 2.3.1,
A3	9	IN	Peripheral Expansion Mode – see
A4	10	IN	Section 2.3.2, Full Expansion
A5	16	IN	Mode – see Section 2.3.3, Micro-
A6	15	IN	processor Mode – see Section 2.3.4)
A7 (MSB)	11	IN	
B0 (LSB)	3	OUT	I/O Port B: Output lines
B1	4	OUT	(Specific I/O configuration for;
B2	5	OUT	Single Chip Mode – see Section 2.3.1,
B3	37	OUT	Peripheral Expansion Mode – see
B4/ALATCH	38	OUT	Section 2.3.2, Full Expansion
B5/R/$\overline{W}$	1	OUT	Mode – see Section 2.3.3,
B6/$\overline{ENABLE}$	39	OUT	Microprocessor Mode – see Section
B7/CLOCKOUT	2	OUT	2.3.4)
C0 (LSB)	28	I/O	I/O Port C: General purpose bidirectional
C1	29	I/O	lines (Specific I/O configuration for; Single
C2	30	I/O	Chip Mode – see Section 2.3.1, Peripheral
C3	31	I/O	Expansion Mode – see Section 2.3.2,Full
C4	32	I/O	Expansion Mode – see Section 2.3.3,
C5	33	I/O	
C6	34	I/O	Microprocessor Mode – see Section 2.3.4)
C7 (MSB)	35	I/O	
D0 (LSB)	27	I/O	I/O Port D: General purpose
D1	26	I/O	bidirectional lines (Specific
D2	24	I/O	I/O Configurations for; Single
D3	23	I/O	Chip Mode – see Section 2.3.1,
D4	22	I/O	Peripheral Expansion Mode – see
D5	21	I/O	Section 2.3.2, Full Expansion Mode –
D6	20	I/O	see Section 2.3.3, Microprocessor
D7 (MSB)	19	I/O	Mode – see Section 2.3.4)
$\overline{INT1}$	13	IN	Maskable Interrupt
$\overline{INT3}$	12	IN	Maskable Interrupt
$\overline{RESET}$	14	IN	$\overline{RESET}$
MC	36	IN	Mode Control
XTAL2/CLKIN	17	IN	Crystal input for control of internal OSC.; input pin for external OSC. or LRC networks
XTAL1	18	IN	Crystal input for control of internal OSC.; leave open for external OSC.
V_{CC}	25	IN	Supply voltage (+5V)
V_{SS}	40	IN	Ground reference

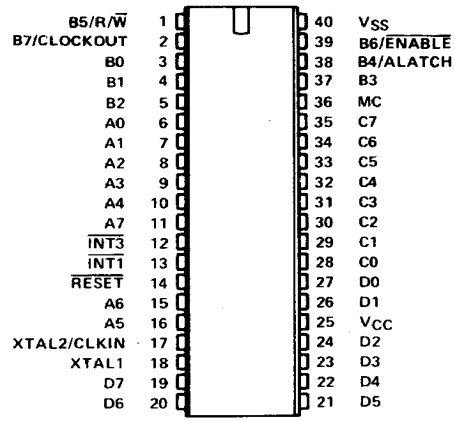


FIGURE 4-14 – SC, FE, PE, AND MICROPROCESSOR MODE PIN ASSIGNMENTS

4.3 SE70P161

4.3.1 Description Of The SE70P161 Prototyping Component

The SE70P161 prototyping component is another member of the TMS7000 family of single-chip 8-bit microcomputers. The SE70P161 is pin compatible with the TMS7020, TMS7040, TMS70120, TMS7041, and has the same instruction set described in Section 3 of this data manual.

The SE70P161 can also be used to emulate CMOS members of the TMS7000 family, with the following limitations. Because the SE70P161 is an NMOS device, its logic levels are not CMOS compatible. Also, this device does not support the low-power modes of the CMOS devices such as HALT or wake-up. Finally, INT1 on the SE70P161 is both latched and level triggered as in the NMOS devices, not just latched, as in the CMOS devices. Further details of these differences are provided in the sections which discuss the function.

The SE70P161 serves as a prototyping component for the TMS7000 devices and provides the ability to verify in real-time software written for all TMS7000 family members mentioned in the preceding paragraphs. This device uses standard TMS2764 or TMS27128 EPROMs. The EPROMs are located in a socket on top of a 40-pin dual-in-line package.

The SE70P161 is packaged so that an EPROM device can be plugged into the top of the package (piggy back). This two chip unit acts as an emulator of the TMS7020 (2K bytes of internal ROM space), the TMS7040/7041 (4K bytes of internal ROM space) and the TMS70120 (12K bytes of internal ROM space). The SE70P161 can also be used as an emulator of any future members derived from the TMS7040/7041 with up to 16K bytes of internal ROM space.

4.3.2 Prototyping

NOTE

System emulators and development tools are only to be used in a prototype environment. Texas Instruments does not warrant their use in customer's applications.

4.3.2.1 TMS7041 Prototyping

The SE70P161 uses either 2764 or 27128 EPROMs with 250 nanoseconds access time or better. The SE70P161 is identical to the TMS7041 except the supply current is a maximum of 150 mA higher because of the EPROM.

4.3.2.2 TMS7020/7040/70120 Prototyping

The SE70P161 system emulator can be used as a TMS7020/TMS7040/TMS70120 prototype. In this mode, internal peripheral port 16 must be cleared by adding MOVP% >00, P16 to the initialization routine.

In any expansion mode, peripheral ports 13 through 23 are used internally and are not accessible to external peripherals in this memory space. In addition, in the full expansion mode, memory locations C000 through FFFF are reserved for an EPROM and are not externally available.

4.3.3 Programming And Installing EPROMS

All EPROM access times are not more than 250 nanoseconds. Pin 1 is identified by a nearby L-shaped gold trace; socket 1 for the EPROM is located in in the same corner. Table 4-3 shows the use of the EPROMS.

TABLE 4-3 — EPROM USE

EPROM TYPE	70XX ROM SPACE	70XX + START ADDRESS	27XX START ADDRESS
27128	16K Bytes	>C006	>0006
2764	8K Bytes	>E006	>0006
2764	4K Bytes	>F006	>1006
2764	2K Bytes	>F806	>1806

†NOTE: Texas Instruments reserves the first 6 bytes of ROM. Addresses in this range may not be defined by the user program.

The SE70P161 is fabricated in two versions. Both versions have fixed internal ROM space of 16K bytes (C000-FFFF), one with a divide-by-two clock generator and the other with a divide-by-four. Note that on the SE70P161, none of the 16K EPROM address space can be mapped as external addresses except in microprocessor mode.

4.3.4 Absolute Maximum Ratings Over Operating Free-Air Temperature Range (Unless Otherwise Noted)†

Supply voltage, VCC (See Note 1) . . . . . −0.3 V to 7 V
All input voltage . . . . . −0.3 V to 20 V
All output voltages . . . . . − 0.3 V to 7 V
Continuous power dissipation . . . . . 1 W
Operating free-air temperature range . . . . . 0°C to 55°C
Storage temperature range . . . . . 0°C to 100°C

† Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Unless otherwise noted, all voltages are with respect to V_{SS}.

4.3.5 Recommended Operating Conditions

PARAMETER		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	V
High-level input voltage, V_{IH}	CLOCKIN	2.6		$V_{CC}+0.5$	V
	All others	2		$V_{CC}+0.5$	
Low-level input voltage, V_{IL}	CLOCKIN			0.6	V
	All others			0.8	
High-level output current, I_{OH}				−400	μA
Low-level output current, I_{OL}				10	mA
Operating free-air temperature, T_A		0		55	°C

4.3.6 Electrical Characteristics Over Full Range Of Recommended Operating Conditions

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = −0.4 mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2 mA			0.4	V
I_I	Input current	$V_I = V_{SS}$ to V_{CC}		10		μA
I_{CC}	Average supply current‡	All outputs open		80	150	mA

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ Average supply current without piggyback EPROM device installed.

4.3.7 Recommended CRYSTAL/CLOCKIN Operating Conditions Over Full Operating Range

PARAMETER		MIN	TYP	MAX	UNIT
f_{osc}	CRYSTAL/CLOCKIN frequency (divide-by-4 option)	2.0		10.1	MHz
f_{osc}	CRYSTAL frequency (divide-by-2 option) (see Note 1)	1.0		5.05	MHz
$t_{c(P)}$	CRYSTAL/CLOCKIN cycle time (divide-by-4 option)	99		500	ns
$t_{c(P)}$	CRYSTAL cycle time (divide-by-2 option)	198		1000	ns
$t_{c(S)}$	Internal state cycle time	396		2000	ns
$t_{w(PH)}$	CLOCKIN pulse width high	45			ns
$t_{w(PL)}$	CLOCKIN pulse width low	45			ns
t_r	CLOCKIN rise time‡			30	ns
t_f	CLOCKIN fall time‡			30	ns
$t_{d(PH-CL)}$	CLOCKIN rise to CLOCKOUT rise delay		125	200	ns

‡ Rise and fall times are measured between the maximum low level and the minimum high level using the 10% and 90% points (see Figure 4-3). Outputs have 100-pF loads to V_{SS}.
NOTE 1: Divide-by-4 option recommended with external clock drive.

4.3.8 Memory Interface Timing At 10 MHz Over Full Operating Free-Air Temperature Range

	PARAMETER	MIN	NOM	MAX	UNIT
$t_{c(C)}$	CLOCKOUT cycle time (see Note)	400		2000	ns
$t_{w(CH)}$	CLOCKOUT high pulse width	130	170	200	ns
$t_{w(CL)}$	CLOCKOUT low pulse width	150	190	240	ns
$t_{d(CH-JL)}$	CLOCKOUT rising to ALATCH falling edge	260	300	340	ns
$t_{d(CH-EL)}$	CLOCKOUT rising to $\overline{\text{ENABLE}}$ falling	−10	15	50	ns
$t_{w(JH)}$	ALATCH high pulse width	150	190	230	ns
$t_{d(AH-JL)}$	High address valid before ALATCH fall	50	170	220	ns
$t_{d(AL-JL)}$	Low address valid before ALATCH fall	50	150	220	ns
$t_{h(JL-AL)}$	Low address hold after ALATCH fall	30	45	80	ns
$t_{d(RW-JL)}$	RD/$\overline{\text{WR}}$ valid before ALATCH fall	50	140	200	ns
$t_{h(EH-RW)}$	RD/$\overline{\text{WR}}$ hold after $\overline{\text{ENABLE}}$ rise	40	100		ns
$t_{h(EH-AH)}$	High address hold after $\overline{\text{ENABLE}}$ rise	30	40		ns
$t_{h(EH-Q)}$	Data out hold after $\overline{\text{ENABLE}}$ rise	65	80		ns
$t_{d(Q-EH)}$	Data out valid before $\overline{\text{ENABLE}}$ rise	230	290		ns
$t_{d(AF-EL)}$	$\overline{\text{ENABLE}}$ fall after low address HI-Z	0	30	120	ns
$t_{d(EH-AF)}$	$\overline{\text{ENABLE}}$ rising to next address drive	60	85		ns
$t_{d(EL-D)}$	Data in after $\overline{\text{ENABLE}}$ falling	155	190		ns
$t_{h(EH-D)}$	Data in hold after $\overline{\text{ENABLE}}$ rise	0			ns
$t_{d(A-D)}$	Access time, data in from valid address	400	470		ns
$t_{d(A-EH)}$	$\overline{\text{ENA}}$ high after address valid	580		730	ns

NOTE: $t_{c(C)}$ is defined to be 4/fosc (or 2/fosc if the divide-by-2 option is selected) and may be referred to as a machine state or simply a state.

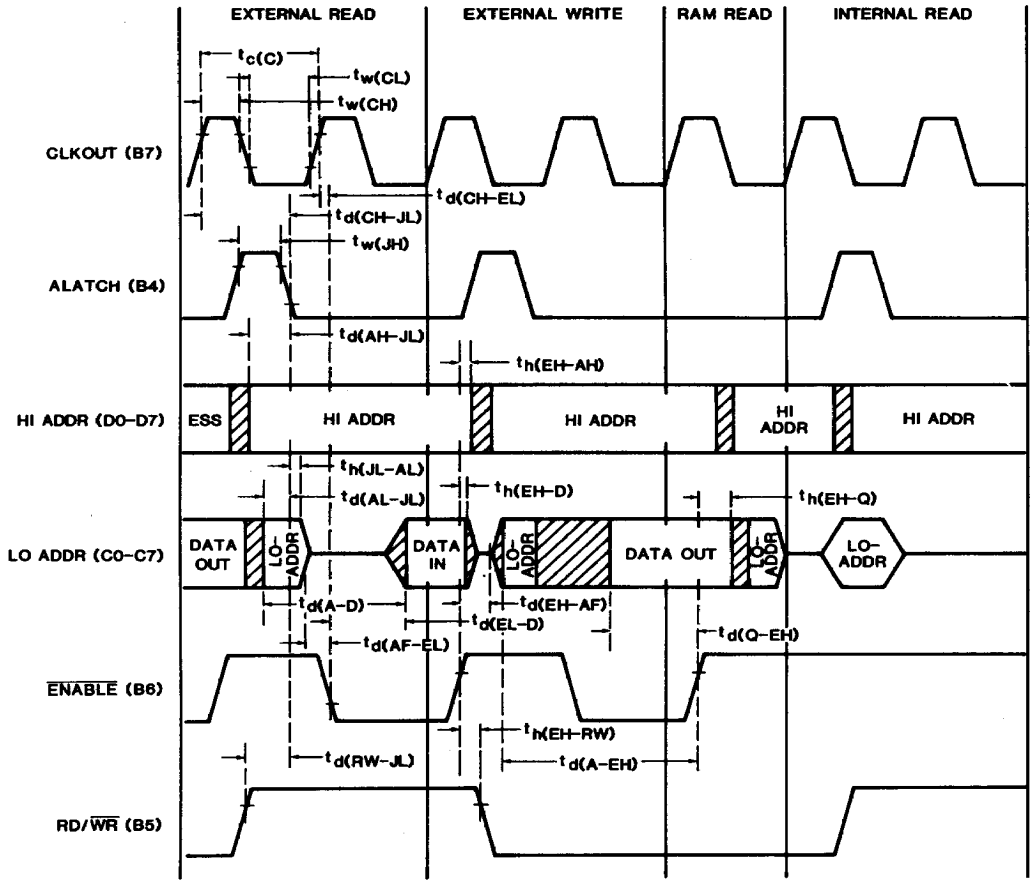
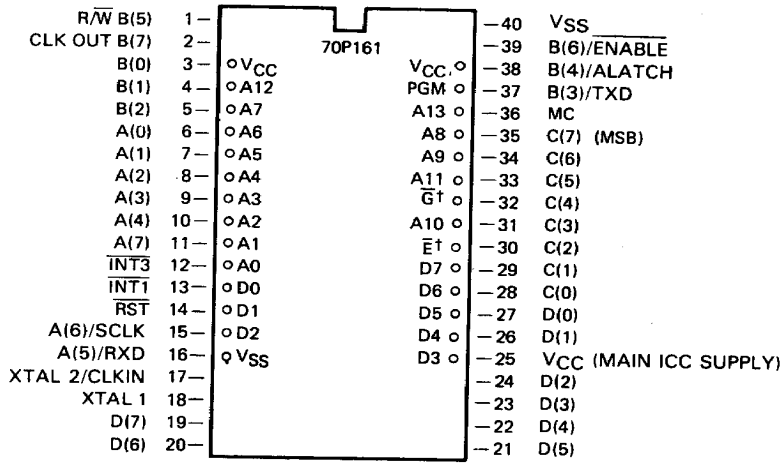


FIGURE 4-15 – READ AND WRITE CYCLE TIMING

4.3.9 Pin Description Of The SE70P161



† PIN LOW, EPROM ALWAYS ENABLED