PHY PCIE

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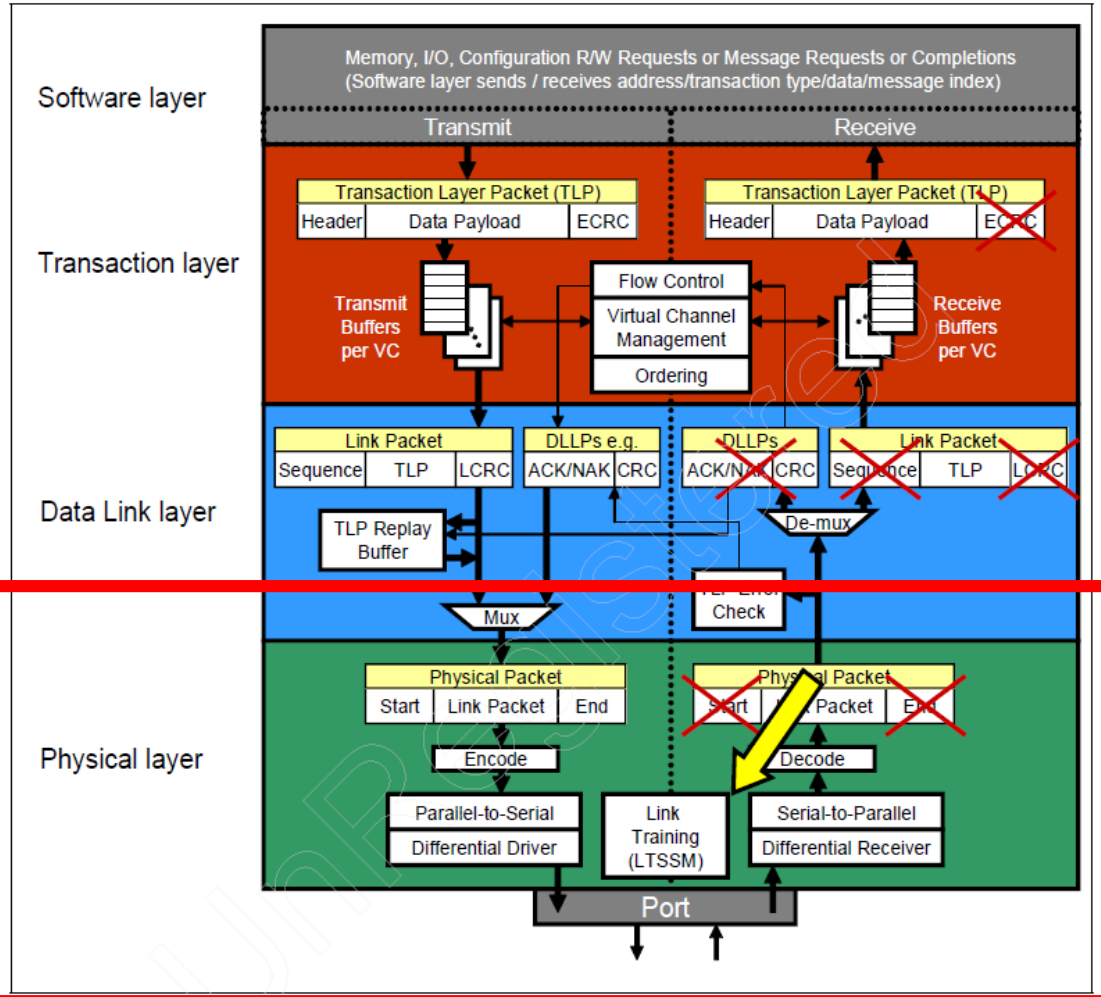
IE-0523 Circuitos Digitales II

Diagrama de capas PCIE

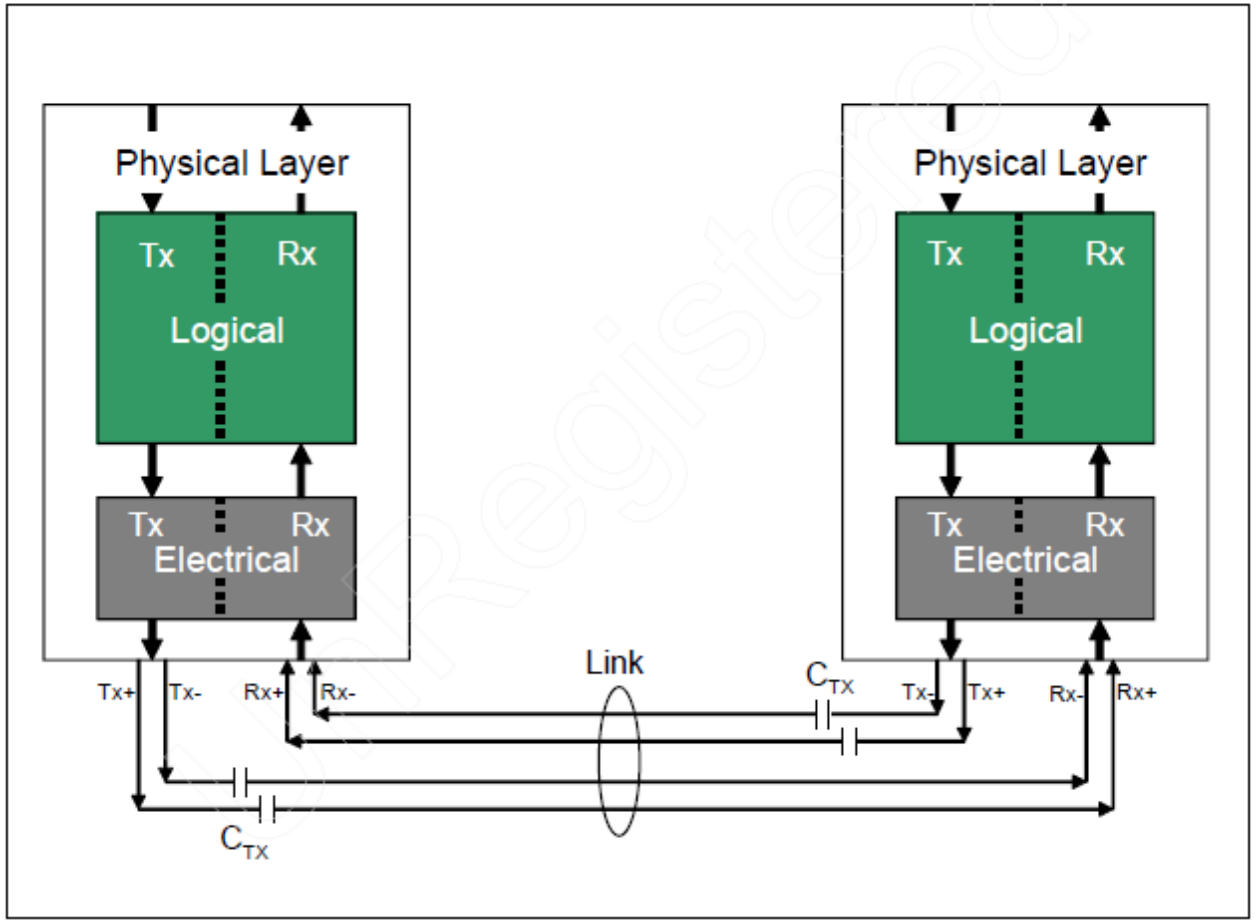
Figure 14-1: Link Training and Status State Machine Location



* PCI Express® System Architecture; Budruk, Anderson y Shanley; MindShare, Inc.; 2008

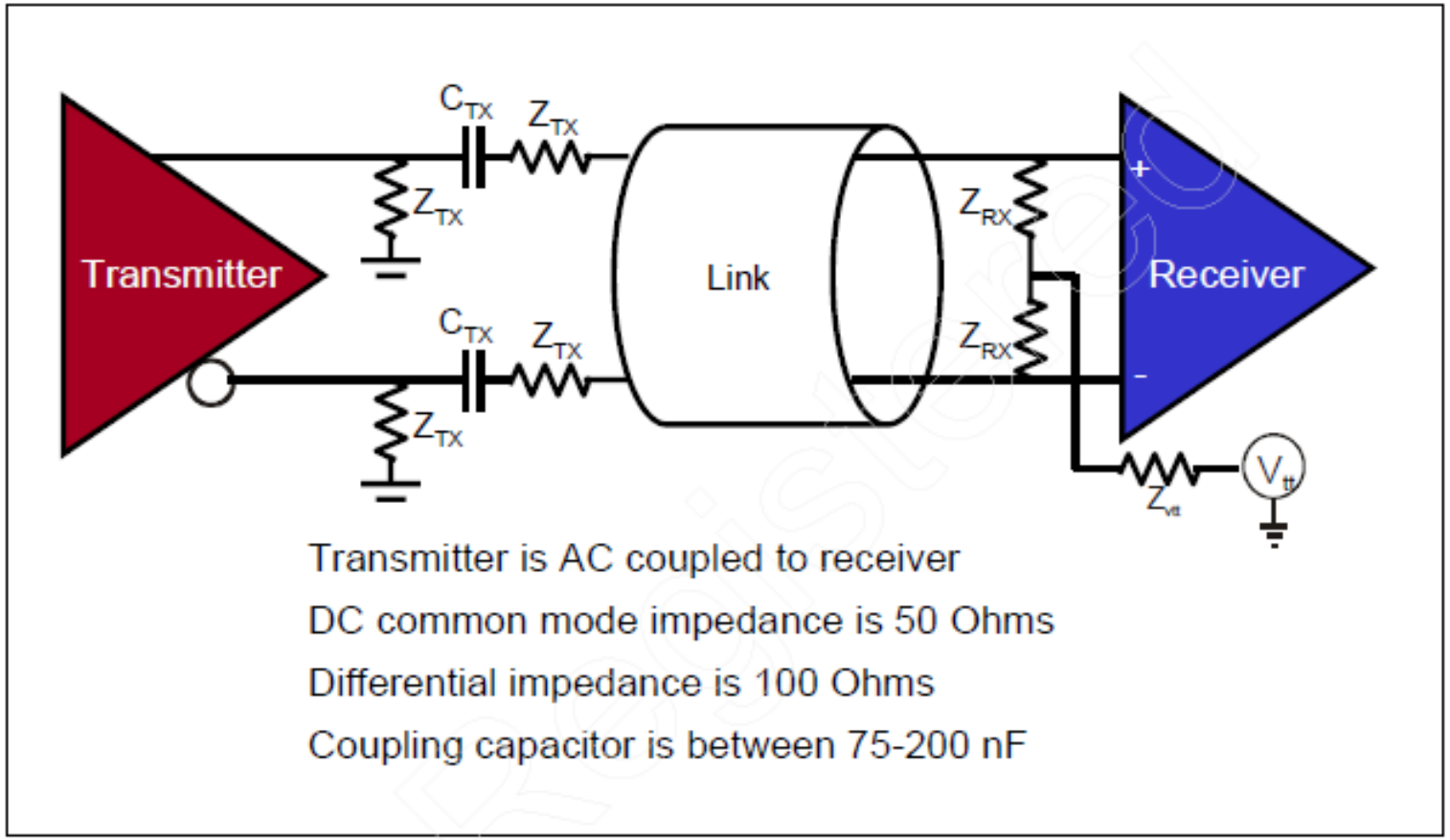
Enlace de dos capas físicas

Figure 11-2: Logical and Electrical Sub-Blocks of the Physical Layer



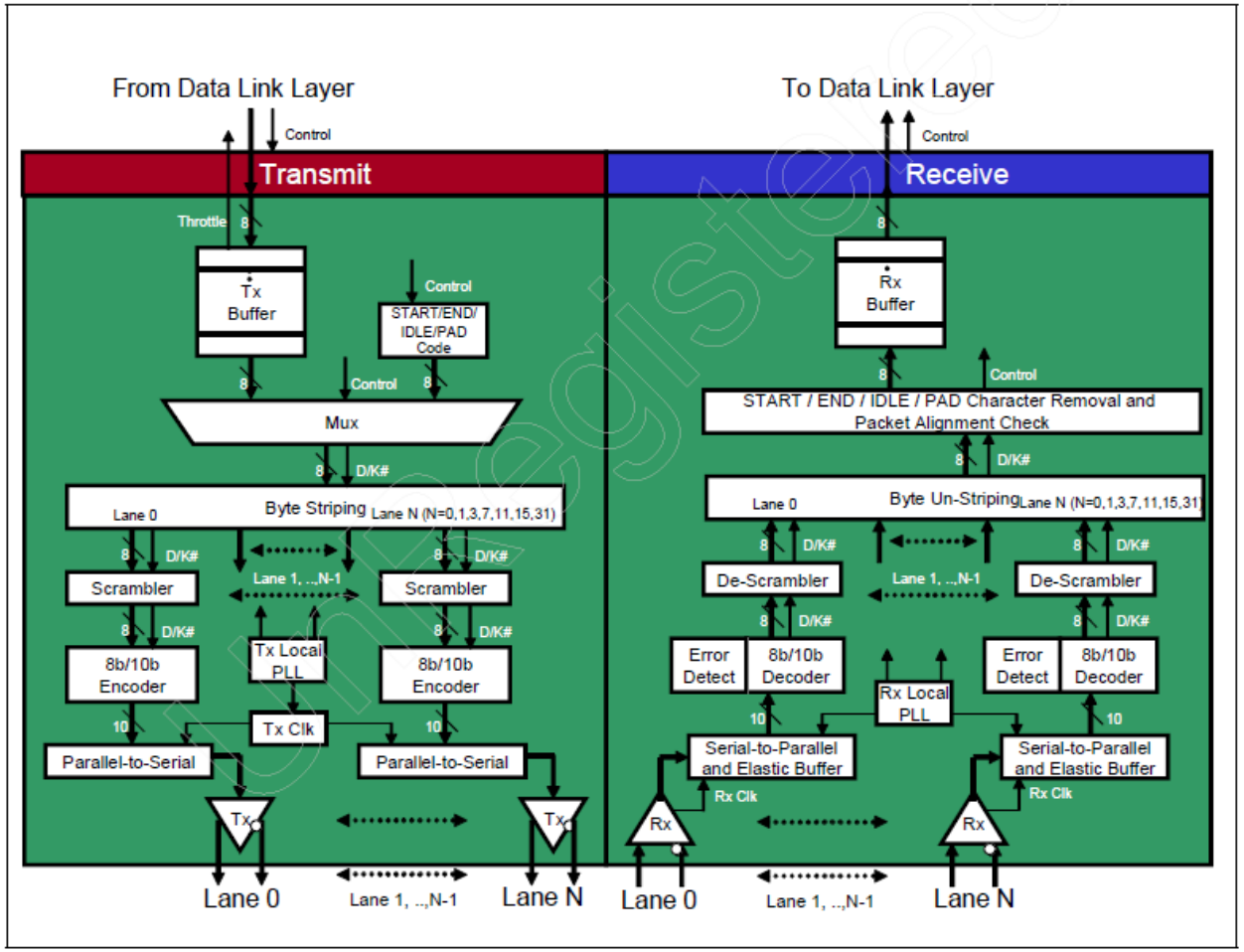
Capa física eléctrica

Figure 2-30: Electrical Physical Layer Showing Differential Transmitter and Receiver



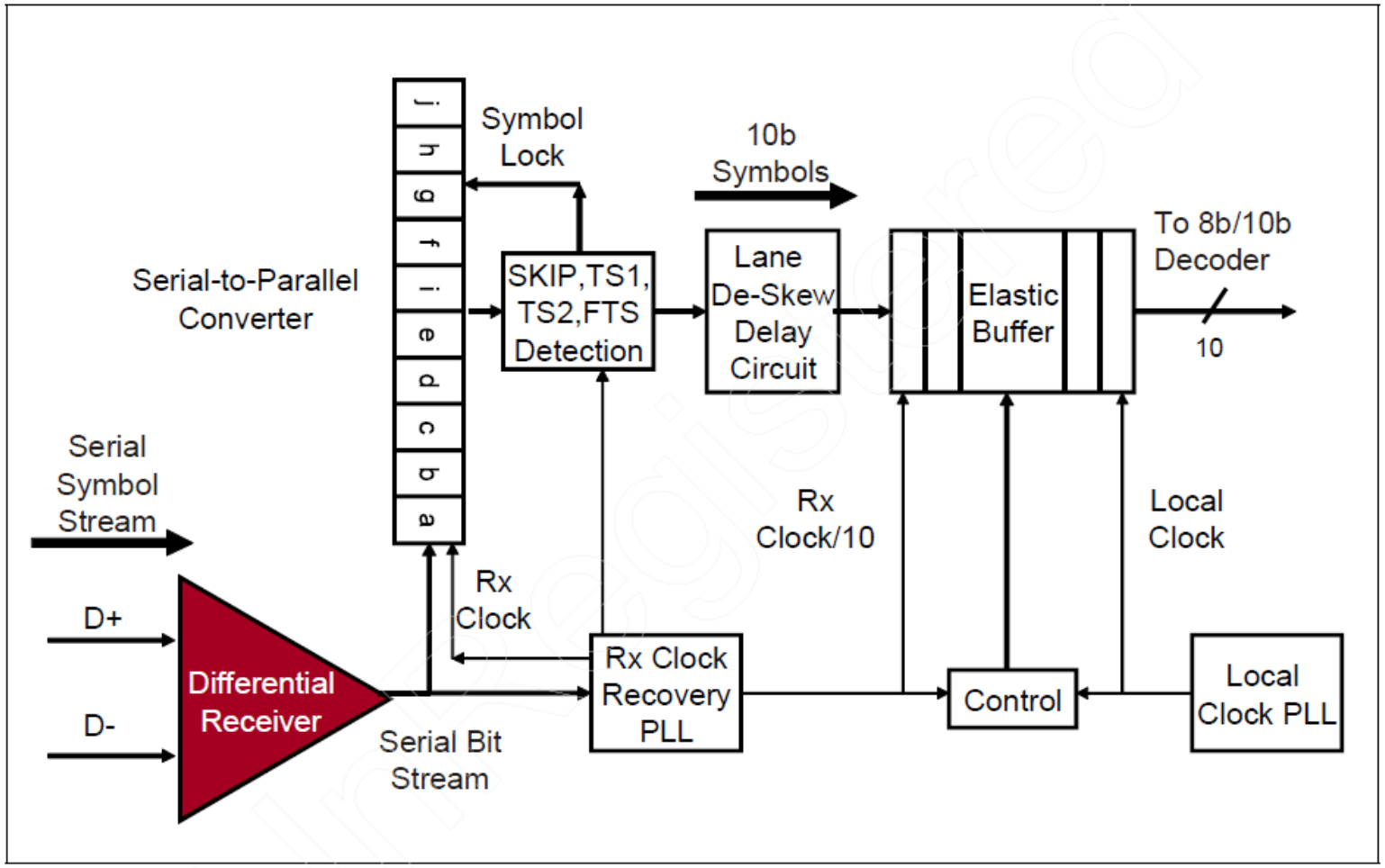
Detalles de la capa física en TX y RX

Figure 11-3: Physical Layer Details



Lógica RX

Figure 11-21: Receiver Logic's Front End Per Lane

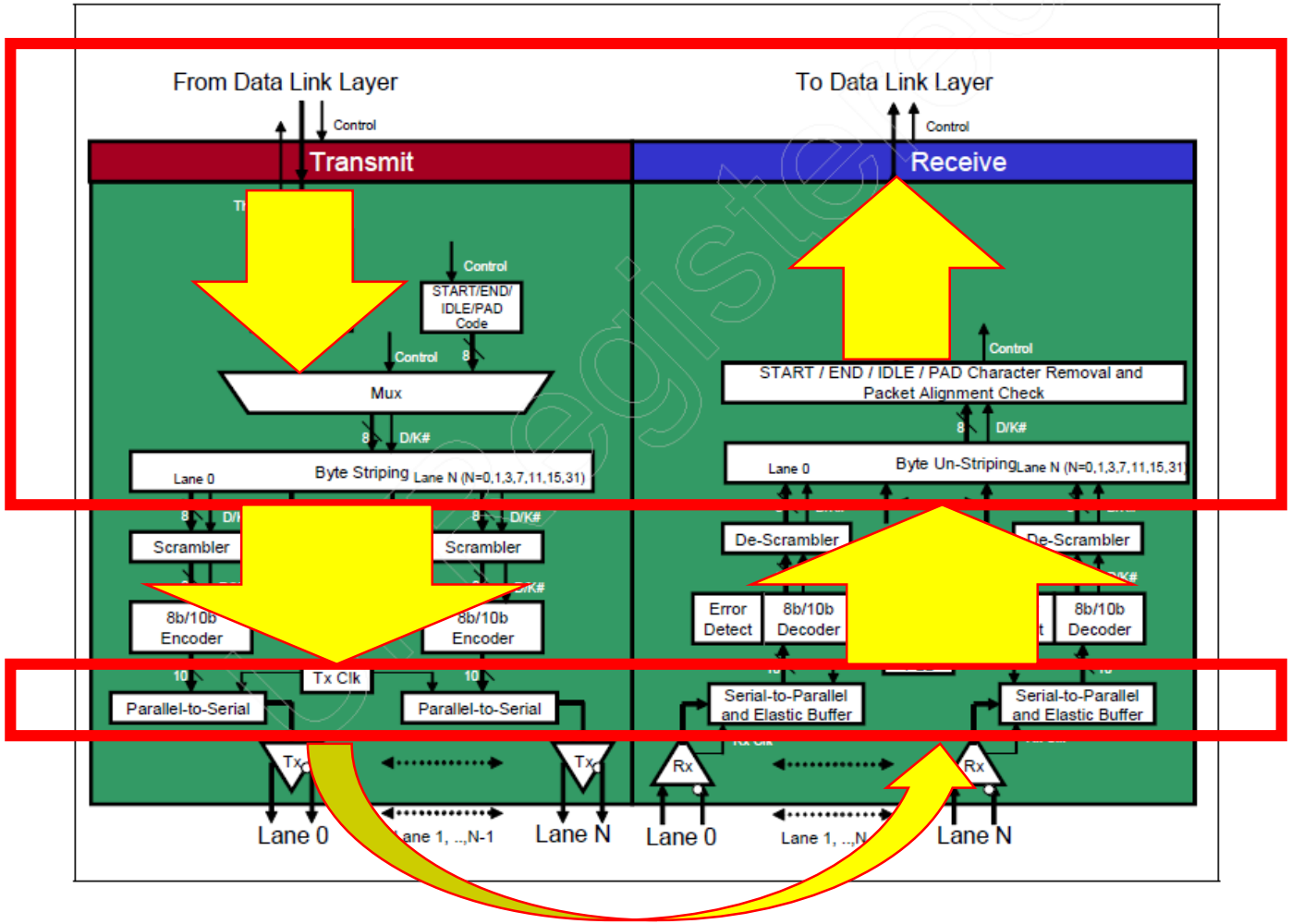


Microarquitectura del proyecto #1

Lógica de control y multiplexores para la transmisión (TX) y recepción (RX) de datos en el PHY.

Detalles del PHY para el proyecto #1

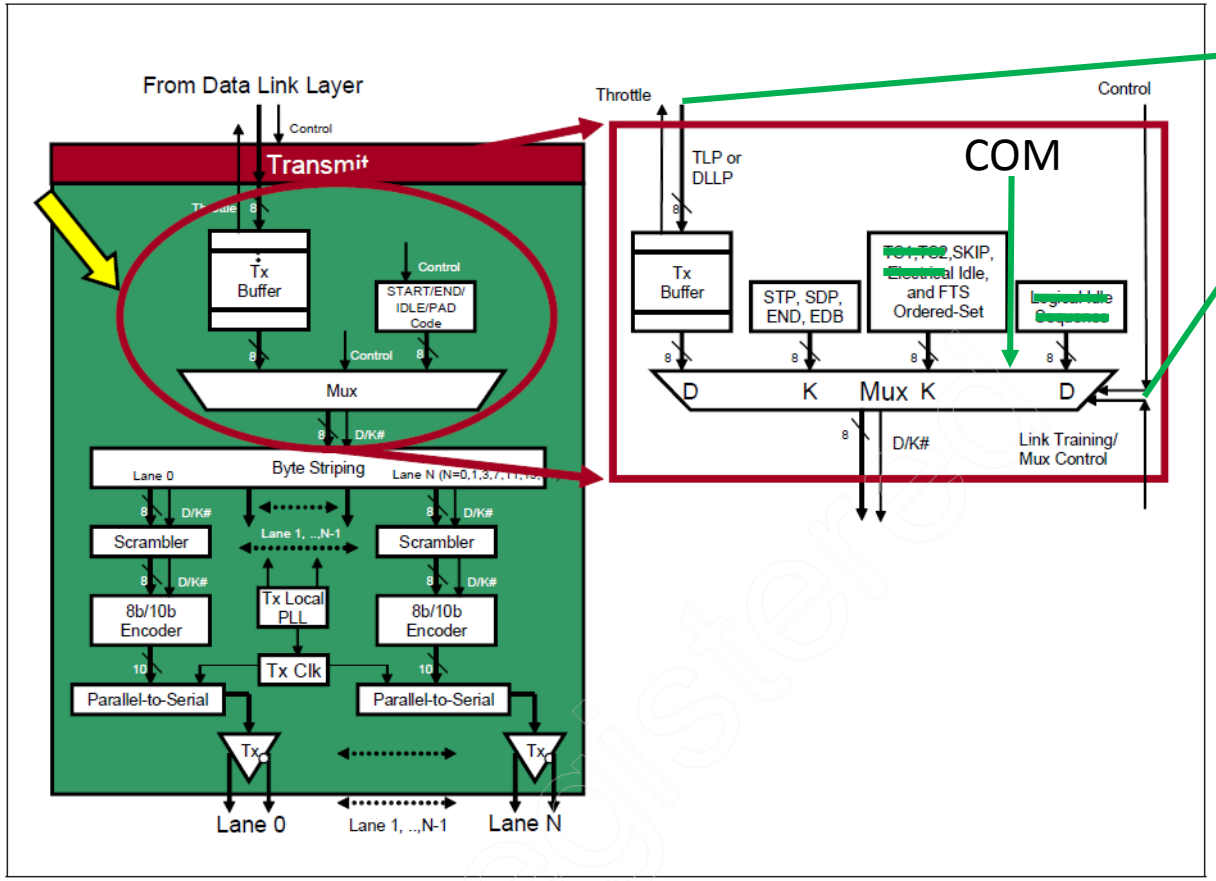
Figure 11-3: Physical Layer Details



Multiplexor de control

- Las entradas del mux se deben manejar desde una secuencia en el probador.

Figure 11-5: Transmit Logic Multiplexer



Manejados desde el testbench/ probador

Símbolos de control

Table 11-5: Control Character Encoding and Definition

Character Name	8b Name	10b (CRD-)	10b (CRD+)	Description
COM	K28.5 (BCh)	001111 1010	110000 0101	First character in any Ordered-Set. Detected by receiver and used to achieve symbol lock during TS1/TS2 Ordered-Set reception at receiver
PAD	K23.7 (F7h)	111010 1000	000101 0111	Packet Padding character
SKP	K28.0 (1Ch)	001111 0100	110000 1011	Used in SKIP Ordered-Set. This Ordered-Set is used for Clock Tolerance Compensation
STP	K27.7 (FBh)	110110 1000	001001 0111	Start of TLP character
SDP	K28.2 (5Ch)	001111 0101	110000 1010	Start of DLLP character
END	K29.7 (FDh)	101110 1000	010001 0111	End of Good Packet character
EDB	K30.7 (FEh)	011110 1000	100001 0111	Character used to mark the end of a 'nullified' TLP.

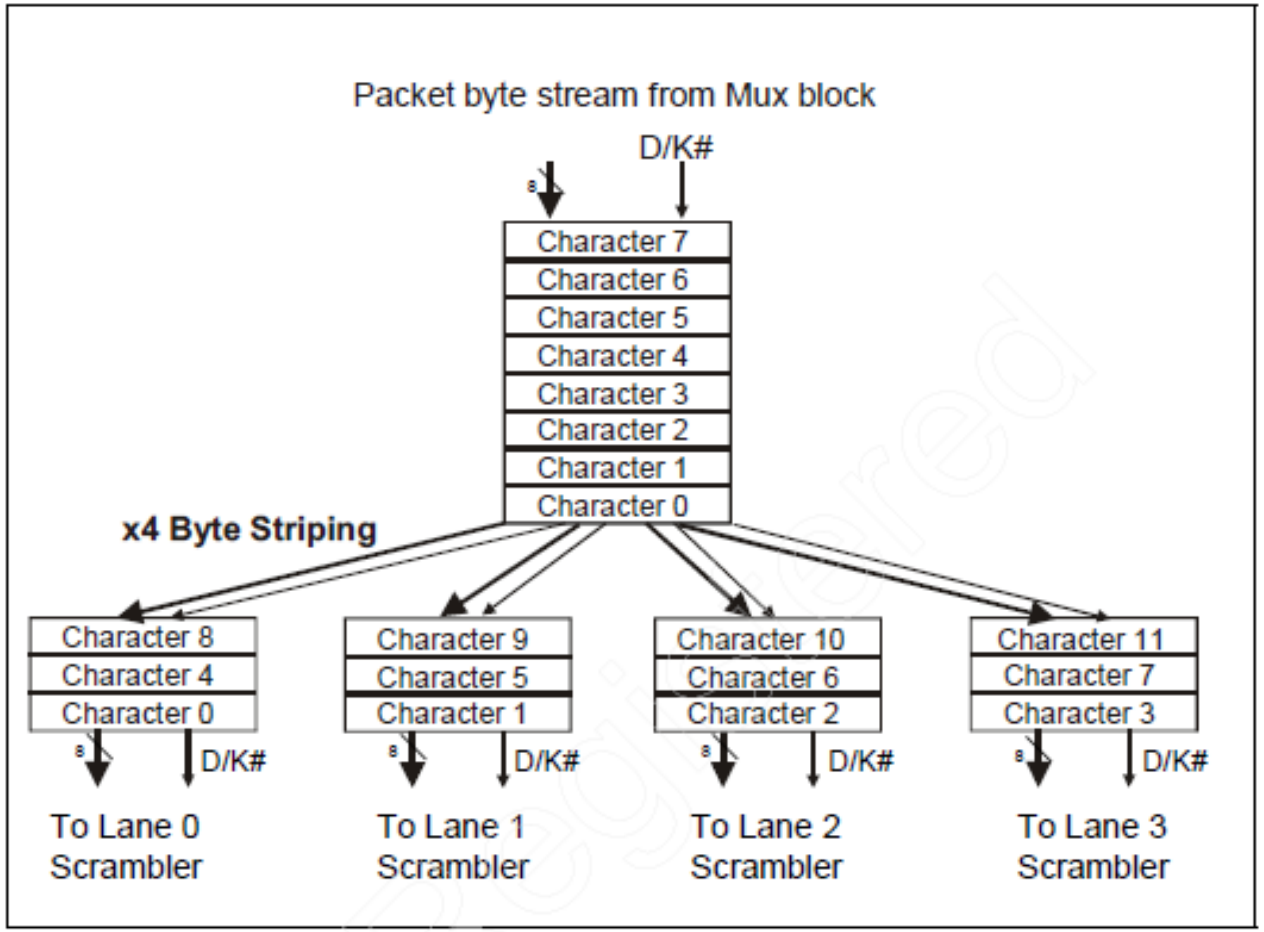
Símbolos de control

Table 11-5: Control Character Encoding and Definition

Character Name	8b Name	10b (CRD-)	10b (CRD+)	Description
FTS	K28.1 (3Ch)	001111 1001	110000 0110	Used in FTS Ordered-Set. This Ordered-Set used to exit from L0s low power state to L0
IDL	K28.3 (7Ch)	001111 0011	110000 1100	Used in Electrical Idle Ordered-Set. This Ordered-Set used to place Link in Electrical Idle state

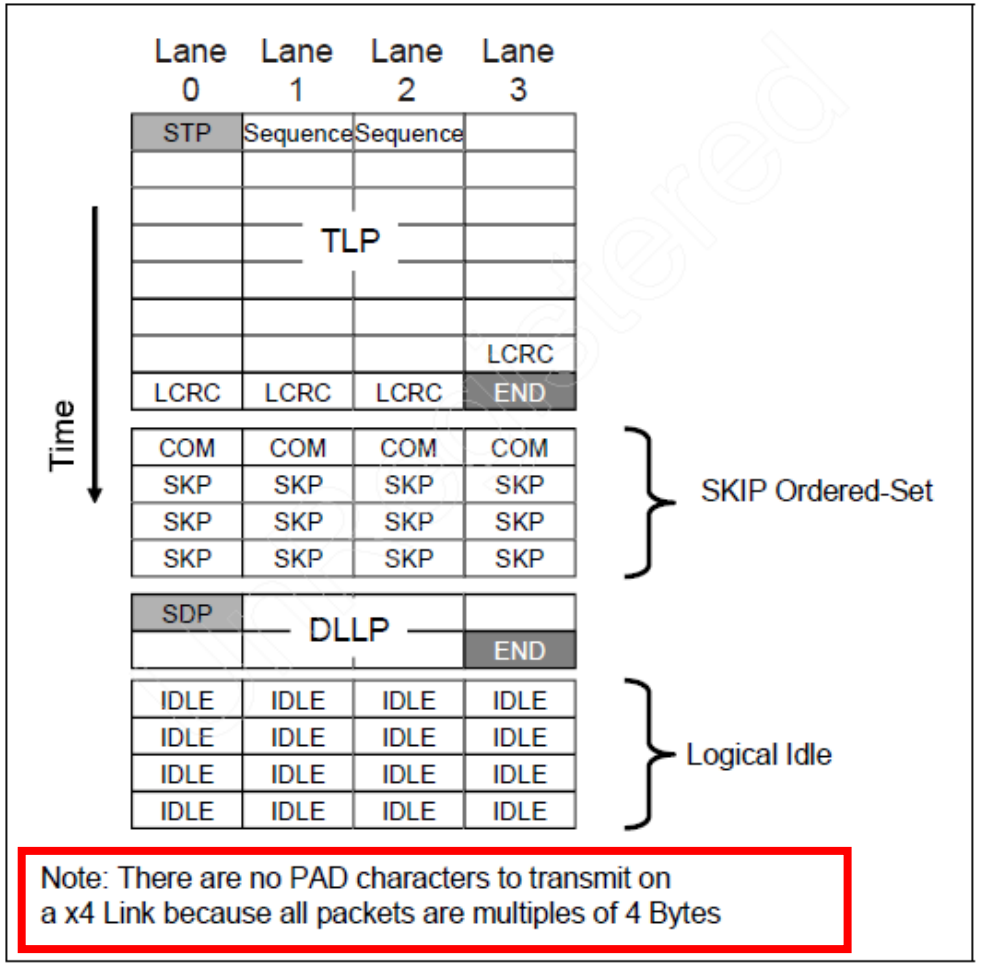
De-mux de datos hacia 4 lanes

Figure 11-8: x4 Byte Striping



De-mux de datos hacia 4 lanes

Figure 11-11: x4 Packet Format



Ejemplo de secuencia de prueba para 4 lanes

data	COM	COM	COM	COM
data	STP	DATA	DATA	END
data	COM	COM	COM	COM
data	SKP	SKP	SKP	SKP
data	SKP	SKP	SKP	SKP
data	SKP	SKP	SKP	SKP
data	STP	DATA	DATA	DATA
data	DATA	DATA	DATA	DATA
data	DATA	DATA	DATA	END
data	SDP	DATA	DATA	END
data	IDLE	IDLE	IDLE	IDLE
data	IDLE	IDLE	IDLE	IDLE

Figure 11-8: x4 Byte Striping