Debjit Pal

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Research Interests

Edge Intelligence (EI) as Service, Trustworthy EI, Blockchain-based Collaborative EI, Machine Learning for Electronic Design Automation (EDA) and System-on-Chip (SoC) Verification, Compiler-based Optimizations for High-Performance Computing.

Education

Post-Doctoral Associate, School of Electrical and Computer Engineering
Cornell University, New York, USA — September 2019 – Present
Supervisor: Prof. Zhiru Zhang

Post-Doctoral Associate (courtesy appointment), Electrical and Computer Engineering Dept.
University of Florida at Gainesville, Florida, USA — May 2021 – Present
Supervisor: Prof. Sandip Ray

Ph.D. in Electrical and Computer Engineering
University of Illinois at Urbana-Champaign, Illinois, USA — August 2012 – July 2019
Advisor: Prof. Shobha Vasudevan
Thesis title: Scalable Functional Validation of Next Generation SoCs

Master of Science (M.S. by Research) in Computer Science and Engineering
Indian Institute of Technology Kharagpur, West Bengal, India — January 2009 – July 2012
Advisor: Prof. Pallab Dasgupta and Prof. Siddhartha Mukhopadhyay
Thesis title: Automated Mixed-Signal Verification using Monitors and Simulation Relations

B.E. in Electronics and Tele-Communication Engineering
Jadavpur University, Kolkata, West Bengal, India — July 2004 – June 2008
Advisor: Prof. Hiranmay Saha
Thesis title: Development of Very Low Phase Noise RF VCO

Honors, Awards, and Fellowships

- Winner of the IEEE CEDA SVDTC Student Research Award 2016
- Best paper nomination in Design Automation Conference (DAC) 2018 (1 out of 691 submissions)
- Best paper nomination in International Conference on Computer Aided Design (ICCAD) 2015 (1 out of 382 submissions)
- Best paper nomination in Asia and South Pacific Design Automation Conference (ASP-DAC) 2019 (1 out of 304 submissions)
- Selected as one of the 7 semi-finalists in TTTC's E.J. McCluskey Best Doctoral Thesis competition 2020
- Selected as one of the 15 semi-finalists in ACM/Microsoft Student Research Competition (SRC) 2018
- Selected to present dissertation research in ACM SIGDA/IEEE CEDA Ph.D. Forum 2018
- Received UIUC Graduate College of Engineering Fall 2018 travel grant
- Received ACM/Microsoft travel grant for Student Research Competition (SRC) at ICCAD 2018
- Received ACM SIGDA travel grant for Ph.D. Forum at DAC 2018
- Received fellowship in International Conference on VLSI Design 2012
- Bronze Medal for Second Highest Aggregate of Marks among all the courses of Bachelor of Engineering Examination 2008 conducted by Jadavpur University (among 1200 students)

Industrial Collaborations

- Intel Strategic CAD Lab (Intel Strategic Research Alliance)
  - The goal of this ongoing collaboration is to develop formally verified special-purpose hardware accelerators and application-specific SoCs from algorithmic specifications.

- IBM Austin
  - The goal of this collaboration was to develop scalable post-silicon validation technology for system-level functional validation of SoCs.

TOOLS, BENCHMARKS DEVELOPED

- **GoldMine: An automatic assertion generator for hardware**
  Availability: `http://goldmine.csl.illinois.edu/`
  Impact: GoldMine is the first publicly available tool that applied machine learning for assertion generation for hardware designs. It has been licensed by several leading EDA companies including Qualcomm, IBM, Broadcom, and Intel. GoldMine also forms the basis of a commercial product since 2013. It has won/nominated for multiple research awards and has also been used by universities for their Verilog design course projects. GoldMine can be used outside of assertion generation to (i) generate design insights via static analysis such as bounded cone-of-influence analysis, use-def analysis, and control-data flow graph analysis, (ii) identify coverage holes in the test suite, and (iii) debug a failing assertion or test.
- **GLAIVE: Graph-learning assisted instruction vulnerability estimator**
  Availability: `https://github.com/cornell-zhang/GLAIVE`
  Impact: GLAIVE is the first graph-based deep learning-assisted scalable model for soft-error-induced program vulnerability estimation. GLAIVE leverages a synergy between static analysis and data-driven statistical reasoning to automatically learn signatures of instruction-level vulnerabilities and their propagation to program outputs. GLAIVE enables quick and accurate estimation of program vulnerability and allows the transfer of program vulnerability knowledge to unseen programs without retraining.
- **HeteroCL**: A Multi-Paradigm Programming Infrastructure for Software-Defined Heterogeneous Computing with End-to-End Verification
  Availability: `https://github.com/cornell-zhang/heterocl`
  Impact: HeteroCL is a Python-based domain-specific language (DSL) infrastructure and compilation flow to map an input algorithm into special-purpose accelerators through high-level synthesis (HLS). HeteroCL provides a clean functional and imperative programming abstraction that decouples algorithmic specifications and hardware optimizations to allow a programmer to explore various design trade-offs systematically and productively. While imperative programming and decoupling algorithmic specifications and optimizations in the HeteroCL benefit compilation and synthesis process, they also create new hurdles for programmers to debug and validate the correctness of the optimized design. To address this challenge, in collaboration with Intel (Intel ISRA), we have developed a Polyhedral compilation-based verification framework to analyze, reason, and prove the correctness of a variety of HLS-centric program optimizations implemented in HeteroCL. Our verification framework enables correct-by-construction special-purpose accelerators by (i) automatically proving the legality of user-specified hardware optimizations and (ii) checking equivalence between the original and transformed code after the compiler implements specified optimizations.
- **PolyBench DSL**: Polyhedral Benchmark Suite in DSL
  Availability: `https://github.com/cornell-zhang/poly-heterocl` (Private repo)
  Impact: PolyBench DSL is a re-implementation of PolyBench C benchmark suite in HeteroCL DSL. We have developed PolyBench DSL in collaboration with Intel (Intel ISRA) as the testbed for the verification framework of HeteroCL. In each of the benchmarks, we have used the programming abstraction of HeteroCL to decouple the algorithm and the optimizations to allow programmers to explore various hardware implementation trade-offs quickly. The salient features of PolyBench DSL are that (i) it is extensible i.e., the user can incorporate new hardware optimizations and can verify the legality of the new optimizations and the generated code, (ii) it contains both a complete regression test suite for run-time verification and a complete code-generation suite, and (iii) a single script with multiple command-line options to run regression and code generation for all of the benchmarks.

TALKS

- **Software Engineering Seminar 2021, CS Department, University of Illinois at Urbana-Champaign**
  Talk: Graph Learning-Assisted Instruction Vulnerability Estimation
  Virtual seminar
- **VLSI Test Symposium (VTS) 2020**
  Talk: Scalable Functional Validation of Next Generation SoCs
  Virtual presentation
- **Computer Systems Laboratory Student Seminar 2019, Cornell University**
  Talk: Post-Silicon validation of next generation SoCs: Challenges, solutions
  Ithaca NY

- **Feedback Friday Seminar Fall 2017, Coordinated Science Laboratory UIUC**
  Talk: Zoom Out and See Better: Scalable Message Tracing for Post-Silicon SoC Debug
  Urbana IL

PUBLICATIONS

- **Journals**

J1. Venkata Adithya Nimmagadda, Maneesh Merugu, **Debjit Pal**, and Sandip Ray, "ADePT: Assured Defense against 3PIP Trojans through Formal Methods and Assertion Mining" in preparation for IEEE Transaction on Information Forensics and Security (TIFS) 2021.

J2. **Debjit Pal** and Shobha Vasudevan, "Feature engineering for Scalable Application-Level Post-Silicon Debug", in preparation for IEEE Transaction on CAD (TCAD).

J3. **Debjit Pal**, Spencer Offenberger, and Shobha Vasudevan, "Assertion Ranking using RTL Source Code Analysis", accepted for publication in IEEE Transaction on Computer-Aided Design (TCAD) 2019.

J4. **Debjit Pal**, Sai Ma, and Shobha Vasudevan, "Emphasizing Functional Relevance Over State Restoration in Post-silicon Signal Tracing", accpted for publication in IEEE Transaction on Computer-Aided Design (TCAD) 2018.

J5. Antara Ain, **Debjit Pal**, P.Dasgupta, S.Mukhopadhyay et.al,"Chassis: A Platform for Verifying PMU Integration using Auto-generated Behavioral Models", ACM Transactions on Design Automation of Electronic Systems (TODAES) 2011.

- **Conferences**

C1. Tashfia Alam Rity, Raj Kshitij, **Debjit Pal**, and Sandip Ray, "Correct-by-Construction Synthesis of Application-Specific SoC Designs from Algorithmic Specifications" in preparation.

C2. **Debjit Pal***, Louis-Noël Pouchet*, and Zhiru Zhang, "Functional Verification of Domain -Specific Accelerators using Polyhedral Analysis" in preparation. (* indicates equal contribution.)

C3. **Debjit Pal** and Shobha Vasudevan, "Graph-learning-based Automated Debugging of Hardware Designs" in preparation.

C4. Jiajia Jiao*, **Debjit Pal***, Chenhui Deng, and Zhiru Zhang, "GLAIVE: Graph Learning Assisted Instruction Vulnerability Estimation", in the Design, Automation and Test in Europe (DATE) Conference 2021. (* indicates equal contribution.)

C5. Ecenur Ustun, Chenhui Deng, **Debjit Pal**, Zhijing Li, and Zhiru Zhang, "Accurate Operation Delay Prediction for High-Level Synthesis with Graph Neural Networks", in IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2020.

C6. Samuel Hertz, **Debjit Pal**, Spencer Offenberger, and Shobha Vasudevan, "A Figure of Merit for Assertions in Verification", in Asia and South Pacific Design Automation Conference (ASP-DAC) 2019.

C7. **Debjit Pal**, Abhishek Sharma, Sandip Ray, Flavio M. de Paula, and Shobha Vasudevan, "Application Level Hardware Tracing for Scaling Post-Silicon Debug", in Design Automation Conference (DAC) 2018.

C8. **Debjit Pal** and Shobha Vasudevan, "Symptomatic Bug Localization for Functional Debug of Hardware Designs", in International Conference on VLSI Design (VLSID) 2016.

C9. Sai Ma, **Debjit Pal**, Rui Jiang, Sandip Ray, and Shobha Vasudevan, "Can't See the Forest for the Trees: State Restoration's Limitations in Post-Silicon Trace Signal Selection", in IEEE/ACM International Conference on Computer-Aided Design (ICCAD) 2015.

C10. Parth Sagdeo, Nicholas Ewalt, **Debjit Pal**, and Shobha Vasudevan, "Using automatically generated invariants for regression testing and bug localization", in IEEE/ACM International Conference on Automated Software Engineering (ASE) 2013.

C11. **Debjit Pal**, P. Dasgupta, and S.Mukhopadhyay, "A Library for Passive Online Verification of Analog and Mixed-Signal Circuits", in IEEE International Conference on VLSI Design (VLSID) 2012.

- **Workshops**

W1. **Debjit Pal**, Vibhor Dodeja, Anjana S. Kumar, and Shobha Vasudevan, "GOLDMINE: A tool for enhancing verification productivity", in the Workshop on Open-Source EDA Technology (WOSET) 2020.

- **Technical reports**

T1. **Debjit Pal** and Shobha Vasudevan, "Zoom Out and See Better: Scalable Message Tracing for Post-Silicon SoC Debug", Technical Report UILU-ENG-17-2203, University of Illinois at Urbana-Champaign 2017.

Posters and Demos

- **Workshop on Open-Source EDA Technology (WOSET) 2020**
  Demo: Enhancing verification productivity with GoldMine
  Virtual presentation
- **Student Research Competition at ICCAD 2018**
  Poster: Scaling Post-Silicon Hardware Tracing: Large Heterogeneous SoCs and Beyond
  San Diego CA
- **Design Automation Conference 2018**
  Poster: Application Level Hardware Tracing for Scaling Post-Silicon Debug
  San Francisco CA
- **ACM SIGDA Ph.D. Forum 2018**
  Poster: Scaling Post-Silicon Observability: Bridging Gap between Micro Designs and Mega SoCs
  San Francisco CA

Teaching Activities

- **Teaching assistant**
  Course: Logic Synthesis (ECE 462) Fall 2013 and 2015
  Responsibility: Setting up homeworks and lab-based problem assignments, mid-term and final exam, and grading.
- **Teaching assistant**
  Course: Computer Organization and Design (ECE 411) Spring 2015
  Responsibility: Setting up homeworks, mid-term, and final exam grading.
- **Teaching assistant**
  Course: Digital System Laboratory (ECE 385) Spring 2016
  Responsibility: Grading lab assignments and helping students in understanding and debugging lab assignments.
- **Teaching assistant**
  Course: Computer Systems and Programming (ECE 220) Summer 2016
  Responsibility: Grading lab assignments and helping students in understanding and debugging lab assignments.

Students Mentored

- Tashfia Alam (University of Florida at Gainesville, 2021-current)
  - Mentoring for the project on "Correct-by-Construction Synthesis of Application-Specific SoC Designs"
- Kshitij Raj (University of Florida at Gainesville, 2021-current)
  - Mentoring for the project on "Correct-by-Construction Synthesis of Application-Specific SoC Designs"
- Nusrat Farzana Dipu (University of Florida at Gainesville, 2021-current)
  - Mentoring for the project on "Automated ranking of security assertions"
- Avinash Ayalasomayajula (University of Florida at Gainesville, 2021-current)
  - Mentoring for the project on "Automated ranking of security assertions"
- Adithya Venkata Nimmagadda (University of Florida at Gainesville, 2020-2021)
  - Mentored for Master's Thesis on "Formal Method Assisted 3PIP Trojan Detection"
- Maneesh Merugu (University of Florida at Gainesville, 2020-2021)
  - Mentored for the project on "Formal Method Assisted 3PIP Trojan Detection"
- Vibhor Dodeja (University of Illinois at Urbana-Champaign, 2019-2020)
  - Mentored for the project on "Learning-assisted Automated Functional Debugging of Hardware Designs"
- Anjana Suresh Kumar (University of Illinois at Urbana-Champaign, 2019-2020)
  - Mentored for the project on "Learning-based Deadlock Detection in Hardware Designs"
- Mentored several student groups to design an advanced LC-3B academic processor for ECE 411. One such group won the in-class final design competition and beat the reference design.

Professional Activities

- Technical Program Committee (TPC) Member
  - DAC 2021

- VLSI 2021
- DAC 2020
- VLSI 2020

- Reviewer
  - DAC (2014, 2015, 2016, 2017, 2018, 2019)
  - DATE (2017, 2018, 2019, 2021)
  - ICCAD (2017, 2018)
  - FMCAD (2016)
  - IWLS (2020)
  - IEEE TVLSI (2017, 2018, 2019)
  - IEEE TCAD (2016, 2020)
  - ACM TODAES (2019)
  - IEEE TC (2019)
  - FPGA (2021)
  - ASPLOS-LATTE Workshop (2021)

References Available upon request.