**ELEC6234 – Embedded Processor Synthesis**

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Electronics with Computer Systems

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**ABSTRACT:** *Summarise your work in less than 100 words stating briefly what was achieved.*

1. **1. Introduction**

*State the objectives of the assignment. Summarise briefly your preparation work, your experimental work,, and results achieved. Specifically, state which parts of the assignment were delivered according to the requirements and summarise any extensions to the basic specification you have carried out with references to the sections. ( approx. 0.5 page).*

1. **2. Overall architecture of the design**

*Describe your processor architecture , showing the Control Path and Data Path. You can show snippets of your source code. There is no need to show the full source code for all your modules in the report as the full source code must be submitted separately.* ***Do not copy any code or diagrams from the lectures.*** *Give your Modelsim testbenches and Modelsim results.* ***DO NOT make statements such as: “Figure 2 shows the simulation results of the module functioning correctly”.*** *Instead, explain the results shown in the figures to demonstrate that you understand how the tested modules work. You can show RTL level diagrams from Quartus if you wish. (max 2.5 pages).*

Figure : The application software

8800 //1000100000000000 BEQ %1 %0 0 # Wait while SW[8] == 0

1000 //0001000000000000 ACCI %2 %0 0 # Read SW[7:0] into %2

C800 //1100100000000000 BNE %1 %0 0 # Wait while SW[8] != 0

8800 //1000100000000000 BEQ %1 %0 0 # Wait while SW[8] == 0

1900 //0001100100000000 ACCI %3 %1 0 # Read SW[7:0] into %3

C800 //1100100000000000 BNE %1 %0 0 # Wait while SW[8] != 0

010C //0000000100001100 ACCI %0 %1 12 # Load b2 into ACC

42C0 //0100001011000000 MACI %0 %2 b11000000 # Add a21\*x1 to ACC

6360 //0110001101100000 MACI %4 %3 b01100000 # Add a22\*y1 to ACC to give y2. Save to %3

0105 //0000000100000101 ACCI %0 %1 5 # Set ACC to 5

4260 //0100001001100000 MACI %0 %2 b01100000 # Add a11\*x1 to ACC

4340 //0100001101000000 MACI %0 %3 b01000000 # Add a12\*y1 to ACC to give x2. Save to %4

8800 //1000100000000000 BEQ %1 %0 0 # Wait for SW[8] to become 1

2100 //0010000100000000 ACCI %4 %1 0 # Write y2 to ACC for dislpay

C800 //1100100000000000 BNE %1 %0 0 # Wait for SW[8] to go to 0

80F1 //1000000011110001 BEQ %0 %0 -15 # Unconditional jump to program beginning

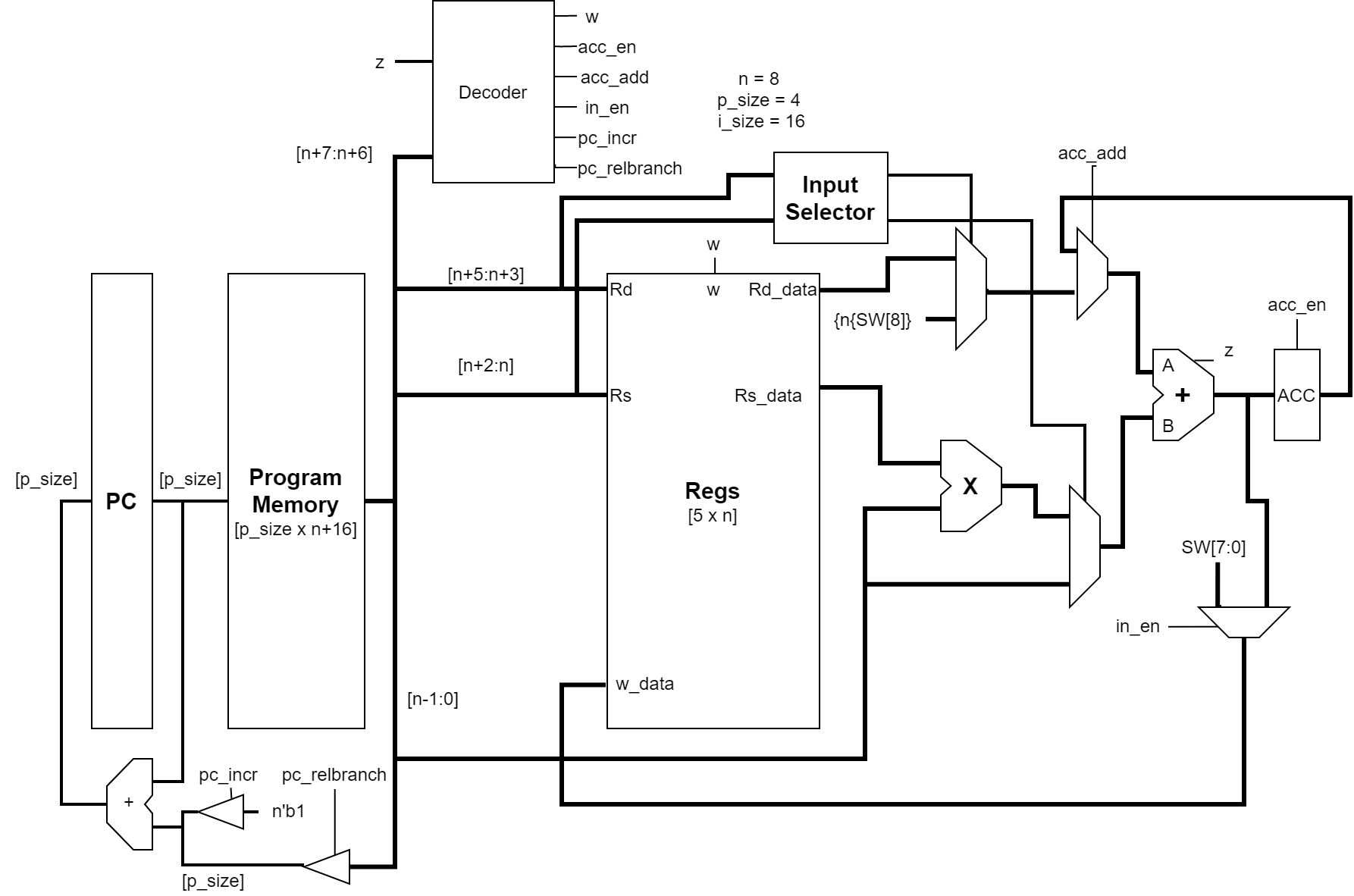
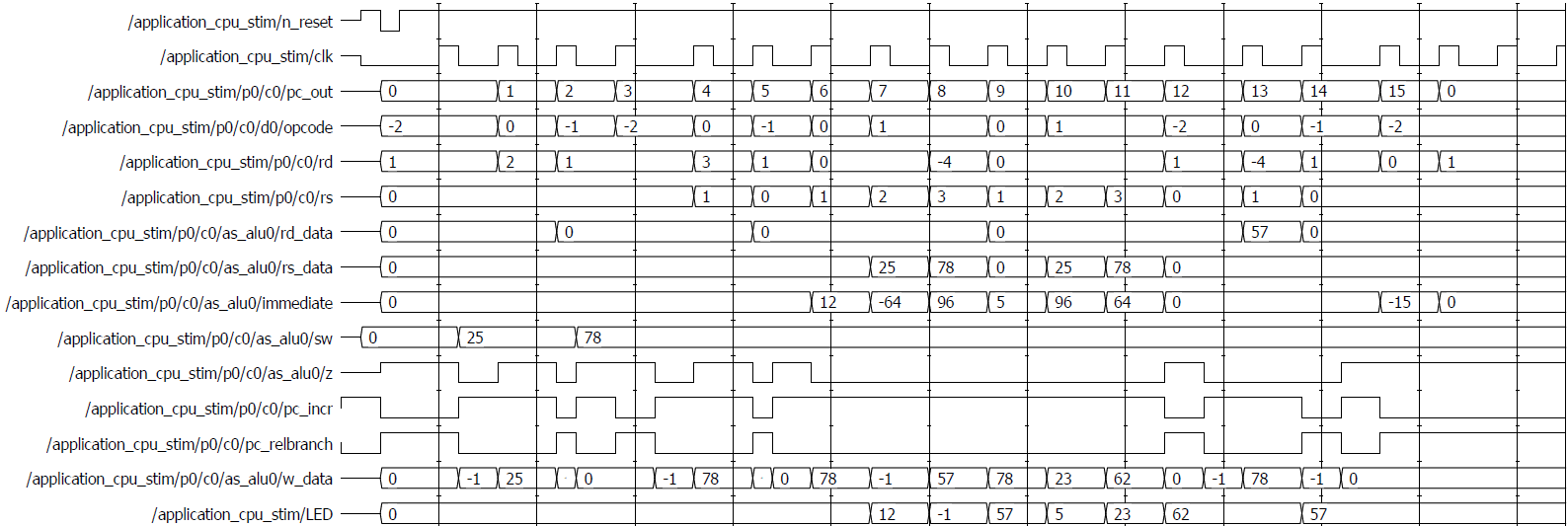


Figure : The system block diagram for the final design



%2 = 25

%3 = 78

%5 = ACC = 57

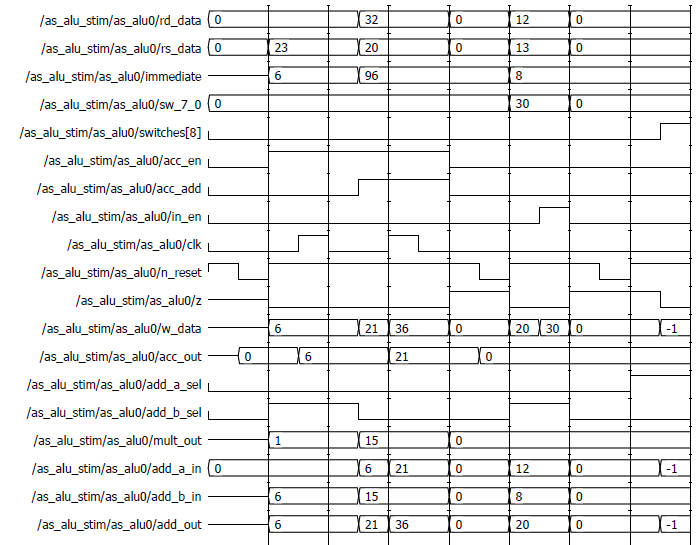


ACC = 62 = x2

ACC = %5 = 57 = y2

1. **3. Details of hardware blocks (use appropriate subsection titles for your hardware modules)**

Figure : A plot of the as\_alu module testbench



Test load immediate into ACC.

ACC goes to immediate (6) after clock.

Test MACC operation.

ACC goes to rs\*immediate + ACC

ACC =20\*0.75

+6 = 21

Test ADDI and switch[7:0] writeback.

in\_en = 0:

W\_data = rs + imm

= 20

in\_en = 0:

W\_data = sw[7:0]

= 30

Test SW[8] value detection using z (zero) flag.

Zeros on all inputs and a\_in\_sel = 1 sets

add\_out = {n{sw[8]}.

z flag detects change in sw[8] value.



1. **5. FPGA implementation**

*Explain how you tested your design after programming the FPGA. In case you had to edit your original code and resynthesize – explain what you did. ( approx. 1-2 pages)*

1. **6. Conclusion**

*State which objectives listed in your Introducton have been achieved. Calculate the cost figure of your design for synthesis on a Cyclone V. Give your general conclusion, comment on what you learnt. Comment on ways to improve the design or extend it further. ( approx.0.25 – 0.5 of a page)*

1. **7. References**

*Quote the sources of your information. Especially make reference to any sources you used in the development of your code.*