ELEC3208 Design Exercise CW FM Radar

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Contents

1 System Block Diagram

Figure 1 shows the system block diagram that was implemented for this project. It has been split into subsections each serving a particular function. The 8-Bit digital output of the system is sent to the microcontroller at the bottom right of the diagram.

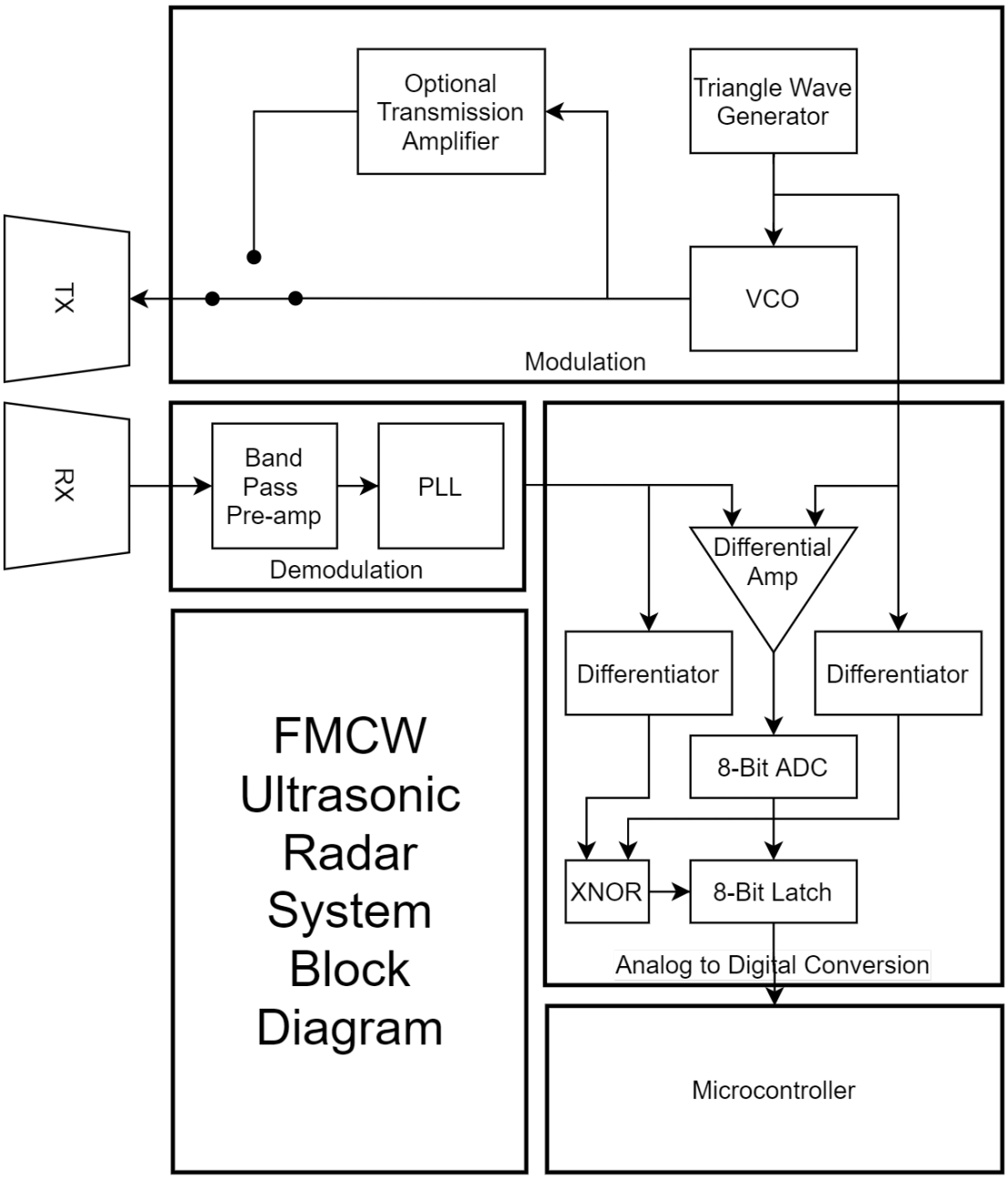

Figure 1: A figure showing the system block diagram from which the system described in this report was designed

1.1 Operational Principles

A periodic signal, in this case a triangle wave, is modulated onto an ultrasonic carrier to produce an FM-modulated signal that is emitted by an ultrasonic transducer. This signal propagates through the air at the speed of sound (344 m/s at sea level under normal conditions) and reflects off of any solid objects in its path. This reflection is converted back to an electrical signal by a second transducer.

A PLL with a center frequency equal to that of the FM modulator is used to demodulate the signal. The output of the loop filter will vary with the frequency of the incoming signal, accurately following the triangle wave generated in the Modulation stage. The reconstructed triangle wave is then compared with the wave generated at that instant. The potential difference between the signals is directly proportional to the time it took for the reconstructed signal to travel to and from the object off of which it reflected. The distance from the transducers to the reflecting surface can be calculated from this potential difference.

Below is a description of the function of each subsection and an outline of the function of each block from the practical system in Figure 1.

1.2 Modulation

The triangle wave is generated in the Triangle Wave Generator. It is used as the input to the VCO with a center frequency set at 40KHz. The bandwidth of the FM signal is specified in the tuning sensitivity (K_{VCO}) of the VCO. As the parameters of the transducers are not known, an optional transmission amplifier has been included. On a PCB, a jumper could be used to bypass the transmission amplifier if the VCO proved suitably powerful. The PCB area for the transmission amplifier would only be populated if required.

1.3 Demodulation

The output of the receiving transducer is fed into a band pass amplifier with a bandwidth equal to that of the signal generated by the VCO. A PLL with a 40 KHz center frequency is used to recover the triangle wave.

1.4 Analogue to Digital Conversion

The the potential difference between the two signals is measured using a differential amplifier and the result is converted to a digital value using an 8-Bit ADC. The gain of the differential amplifier is such that the maximum possible potential difference measured produces the maximum value on the ADC output.

The potential difference between the triangle waves is constant when they are both ramping in the same direction. However, when one changes direction the potential difference will fall to zero and rise again, producing erroneous data on the ADC output. To account for this, a latch is placed

between the ADC output and the microcontroller. This latch is transparent when both signals are ramping in the same direction and holds its value when the signals are ramping in opposite directions. The erroneous data is not transmitted to the microcontroller. The directions of the triangle wave are determined by differentiators with high gains producing TTL '1' when ramping up and TTL '0' when ramping down. An XOR/XNOR gate is used to produce a $\overline{LatchEnable}$ / $LatchEnable$ control signal.

2 Specification

2.1 System-Wide Specification

The system should run on $\pm$ 5 V as the robot will likely have a central PSU that provides this configuration. As stated in the specification, the maximum measurable distance d_{max} should be 5 m. The distance measurement is converted into an 8-Bit word so the minimum measurable distance d_{min} should be given by Equation (1)

$$\begin{aligned} d_{min} &= \frac{5\ m}{2^8 - 1} \\ &= \frac{5\ m}{255} \\ &= 2.0\ cm \end{aligned} \tag{1}$$

To get accurate results, the triangle waves measured by the differential amplifiers must have a phase difference of no more than π radians at the maximum measurable value of 5 m. To reduce the time spent in the latched state (where the two signals are moving in opposite directions) the phase difference at maximum range will be reduced to $\frac{2}{3}\pi$. With the speed of sound at sea level under normal conditions V_s equal to 344 m/s, the total propagation delay t_p imposed on the reflected signal given by Equation (2). This is $\frac{1}{3}$ of the total triangle wave period T. This gives T as 87.3 ms and a frequency F of 11.5 Hz.

$$\begin{aligned} t_p &= 2\frac{d_p}{V_s} \\ &= 2\frac{5\ m}{344\ m/s} \\ &= 29.1\ ms \end{aligned} \tag{2}$$

A maximum frequency variation Δf of 4 kHz, resulting in a bandwidth of 8 kHz, was chosen as a compromise between simpler filter/amplifier design requiring high bandwidth, and the use of more cost-effective VCO and PLL elements requiring lower bandwidth.

2.2 Modulation Section Specification

2.2.1 Triangle Wave Generator

- **Frequency** - 11.5 Hz $\pm$ 1 Hz to match the system spec in Section 2.1. The theoretical maximum of this value is 17.2 Hz, beyond this value the two triangle waves will be more than π radians out of phase when measuring 5 m and the digital output would be in the lathed state 50% of the time.
- **Amplitude** - 1 V $\pm$ 0.05 V as a compromise between low power operation and low K_{VCO}.
- **Offset** - 0 V $\pm$ 0.1 V to ensure center frequency at 40 kHz. The tolerance of the offset and amplitude values are to limit variations in the bandwidth of the FM signal.

2.2.2 VCO

- **Center Frequency** 40 kHz $\pm$ 200 Hz. Low tolerance offset error on PLL output is minimised
- K_{VCO} - KVCO of 4 kHz/V $\pm$ 500 Hz as calculated in Equation (3).

$$\begin{aligned} K_{VCO} &= \frac{f_{max} - f_{min}}{V_{max} - V_{min}} \\ &= \frac{44kHz - 36kHz}{1V - -1V} = 4kHz/V \end{aligned} \tag{3}$$

2.2.3 Transmission Amplifier

A MOSFET should be used to amplify the square wave produced by the VCO. An engineer should be able to set the fabricated PCB into two configurations:

1. **VCO $\rightarrow$ Transducer** - The output of the VCO is fed into the positive terminal of the transducer. The negative terminal of the transducer is set to ground.
2. **VCO $\rightarrow$ MOSFET Gate** - The output of the VCO is fed into the Gate of an N-channel MOSFET. The positive terminal of the transducer is connected to 5V or an external voltage supply. The negative terminal of the transducer is connected to the drain of the MOSFET.

The MOSFET should have the following parameters:

- **Voltage Rating** - 20 V, higher voltages could prove dangerous for engineers working with the hardware.
- **Current Rating** - 1A, electroacoustic transducers are capacitive devices so current requirements are relatively low.

2.3 Demodulator Specification

2.3.1 Pre-amp

As nothing is known about the transducers to be used on the system, few of the amplifier parameters can be specified. However, the following criteria can be specified:

- **Gain Selection** - The gain of the amplifier should easy to set using commonly available passive components
- **Gain Range** - The gain should be selectable between a factor of 2 and a factor of 2000.
- **Bandwidth Stability** - Setting the gain between 2 and 200 should not reduce the gain in the range of 3500 kHz to 45 kHz by more than 3 dB.

2.3.2 PLL

- **Centre Frequency** - 40 kHz $\pm$ 200 Hz to match that of the VCO.
- **Triangle Wave Output Offset** - 0V $\pm$ 0.1V to minimise systematic error at the differential amplifier.
- **Amplitude** 1 V $\pm$ 0.1 V to match that of the triangle wave generator. If necessary, this should be achieved with an additional amplifier.

2.4 Analogue to Digital Conversion

2.4.1 Differential Amplifier

Parameters for the differential amplifier rely on the parameters of the ADC so they shall be described as such.

- **Differential Gain** - A potential difference of 0.33 V, corresponding to the maximum phase difference between the triangle waves of $\frac{2}{3}\pi$ radians should result in the output of the ADC reaching the upper limit of the ADC input range $V_{ADC} \pm \frac{1}{2^8-1}V_{ADC}$. This is so the phase difference caused by the transmitted wave reflecting off an object 5 m away generates the maximum value on the ADC.
- **Rectified Output** - The polarity of the inputs will periodically switch as the triangle waves change direction. The output of the amplifier should include a full-wave rectifier with a lower limit below $\frac{1}{2^8-1}V_{ADC}$ so the minimum distance can still be measured.

2.4.2 Differentiator

- **Single Supply** - The output of the differentiators are used as the inputs to digital circuits so their output should not go below 0 V.
- **Gain** - The required gain can be calculated by first finding the minimum rate of change of the triangle wave and finding the minimum multiplier that results in an output meeting the TTL logic HIGH/LOW levels. The rate of change is calculated in Equation 4.

$$\begin{aligned} RateOfChange &= \frac{Peak-to-PeakVoltage}{\frac{1}{2} * MaximumPeriod} \\ &= \frac{1V - -1V}{\frac{1}{2} * 95.3ms} \\ &= 42.0V/s \end{aligned} \tag{4}$$

  Horowitz and Hill state in *The Art of Electronics* that the logic levels for TTL inputs are $V_{in} < 0.8V$ for guaranteed logic LOW and $V_{in} > 2V$ for logic HIGH. A gain of 0.5 will suffice.

3 Implementation

All simulations have been produced in LTSpice. Each simulated component is implemented as a hierarchical subcircuit and a testbench is produced to verify that the spec has been met.

3.1 Modulation

3.1.1 Triangle Wave Generator

The topology implemented for this subcircuit was found in *The Art of Electronics*[2]. It uses an integrator to generate a ramp from the output of a non-inverting schmitt trigger. This ramp is fed into the input of the schmitt trigger. When the ramp reaches a schmitt trigger threshold, the polarity of the schmitt trigger output reverses, forcing the integrator to ramp in the opposite direction. High precision, rail-to-rail opamps and E96 resistors ensure the amplitude and offset tolerances were met.

Figure 2 shows the schematic, and Figure 3 shows the testbench used to test it. The Spice error log shows the results of the measurement directives. The offset is 0.003V and the peak-to-peak voltage is 2.001 V. The steady-state frequency is measured as 11.3532 Hz. Each of these falls within the tolerances presented in Section 2.2.1. A cutting of the waveform produced can be found in Figure 4.

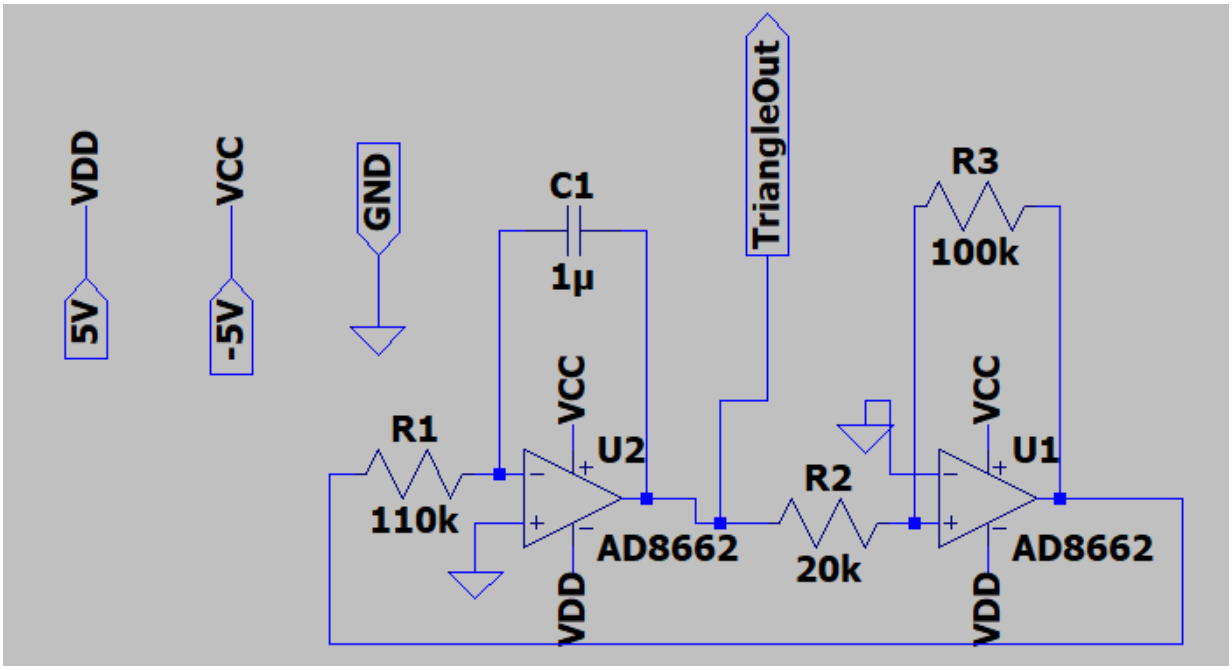

Figure 2: A screencap of the Triangle Wave Generator Subcircuit

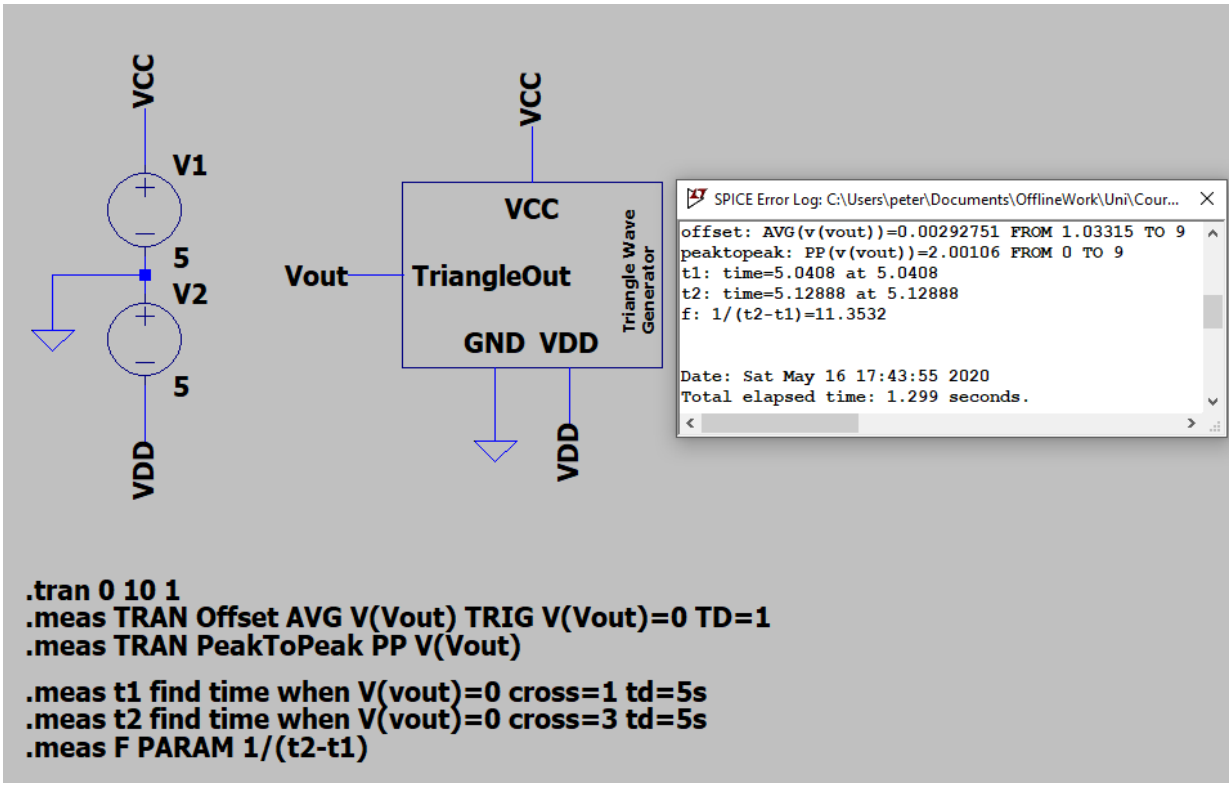

Figure 3: A screencap of the Triangle Wave Generator Subcircuit

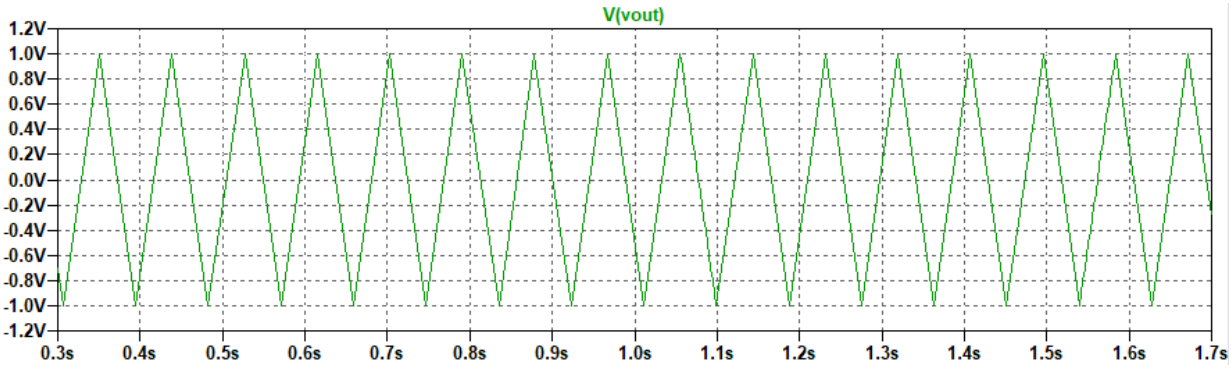

Figure 4: A screencap of the Triangle Wave Generator Subcircuit

3.1.2 VCO

The VCO subcircuit is based on the LTC6990 VCO IC. K_{VCO} and the centre frequency are set using E96 resistors. The LTSpice schematic was adapted from a circuit generatd automatically on an online design tool provided by Analog Devices[1]. The schematic is shown in Figure 5.

The testbench varies the control voltage VC and takes frequency measurements at the appropriate times. The testbench is shown in Figure 6. The waveform produced is shown in Figure 7.

The measurements showed that the centre‘ frequency (F_{Centre}) is 39842 Hz and the Bandwidth

[1] http://beta-tools.analog.com/timerblox/LTC6990

of the FM Modulated signal is 7905.5 Hz. This falls within the tolerances presented in Section 2.2.2.

This IC shifts the phase of the signal by π radians, the FM signal frequency increases when VC drops and vica versa. The differential amplifier will need to account for this.

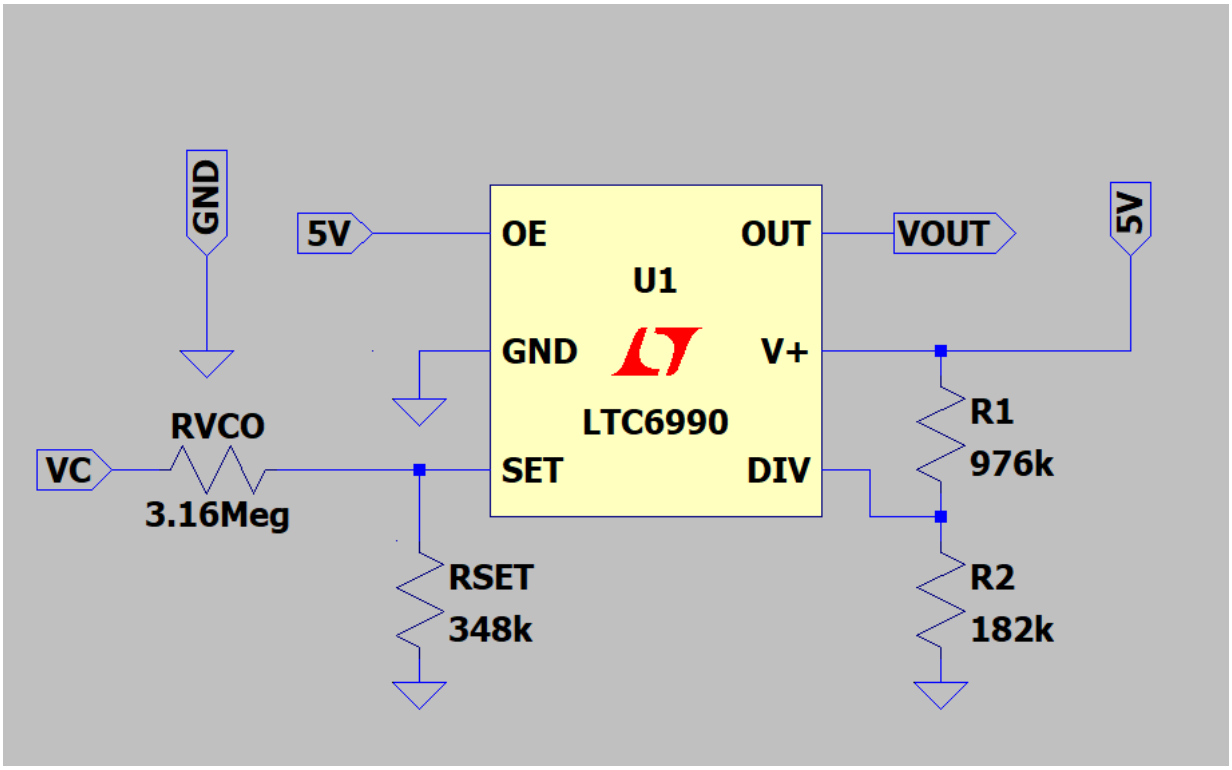

Figure 5: A screencap of the VCO Subcircuit

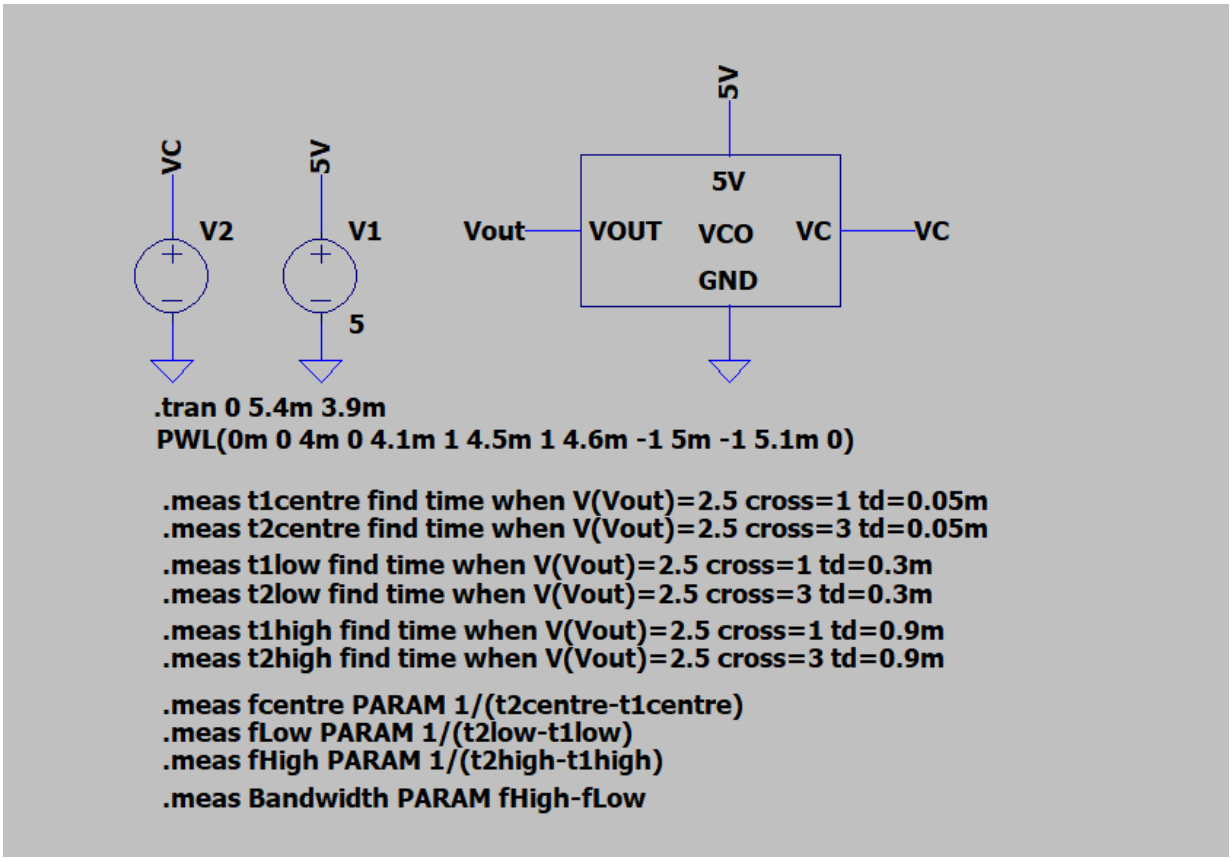

Figure 6: The testbench fort the VCO Subcircuit

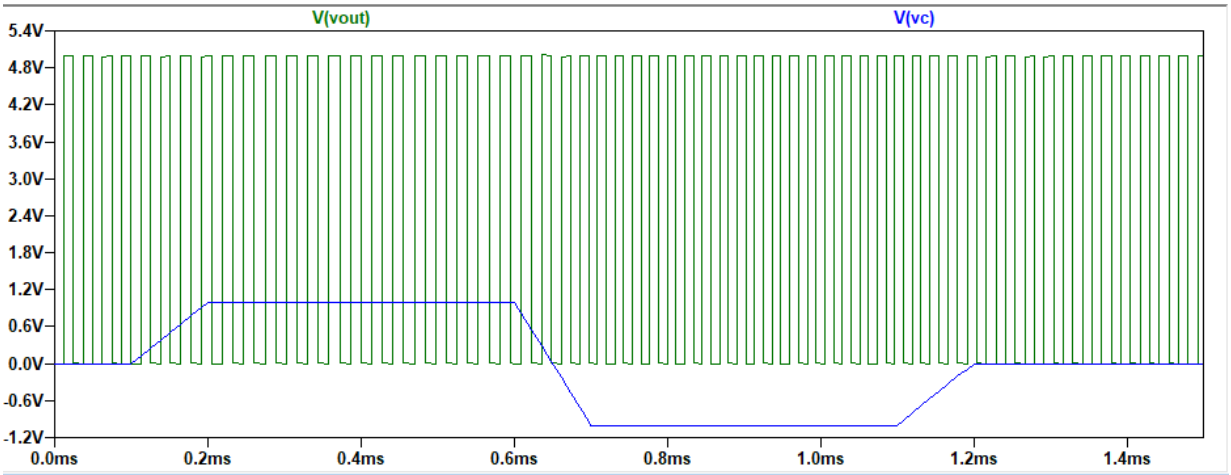

Figure 7: The Waveform produced by the VCO Testbench

3.1.3 Transmission Amplifier

Due to the low power requirements of the MOSFET, a SOT-23 package was chosen to conserve space and money. The Infineon IRLML6344[2] was used in the simulated version shown in Figure

[2] https://uk.rs-online.com/web/p/mosfets/9134070/

8 as it meets the power requirements discussed in Section 2.2.3 but any SOT-23 device could be used.

The testbench contains an Butterworth-Van Dyke equivalent circuit of a transducer with parameters taken from experimental data presented by Queirós, Girão, and Serra in their 2005 paper[3].

Figure 10 shows the mock VCO output superimposed over the current through the resistor R1. It shows the constant charge and discharge of the capacitor C1, demonstrating that the MOSFET is able to induce mechanical oscillation on this mock transducer.

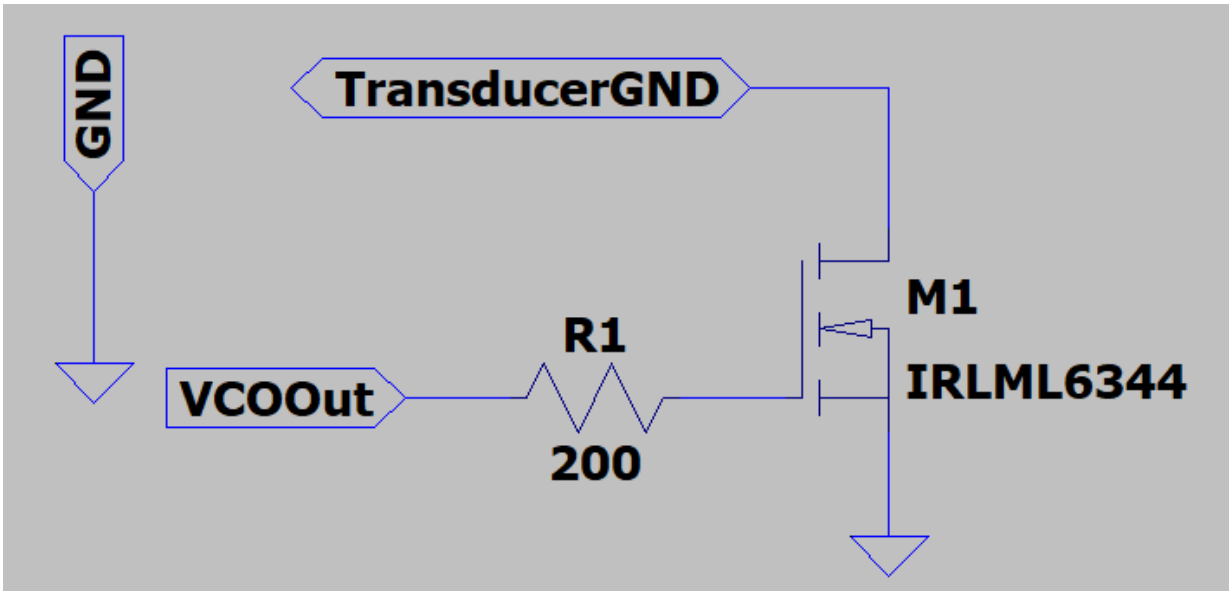

Figure 8: A screencap of the Transmission Amplifier Subcircuit

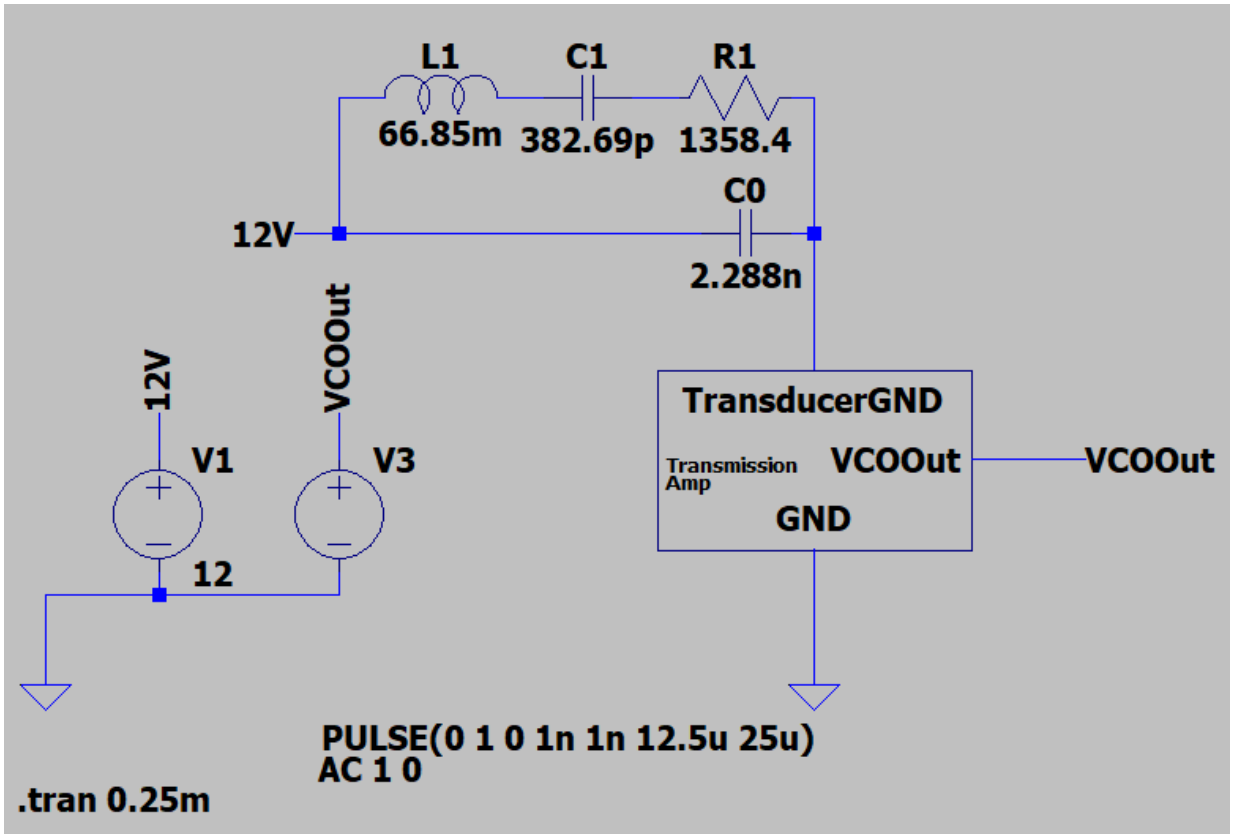

Figure 9: The testbench for the Transmission Amplifier Subcircuit

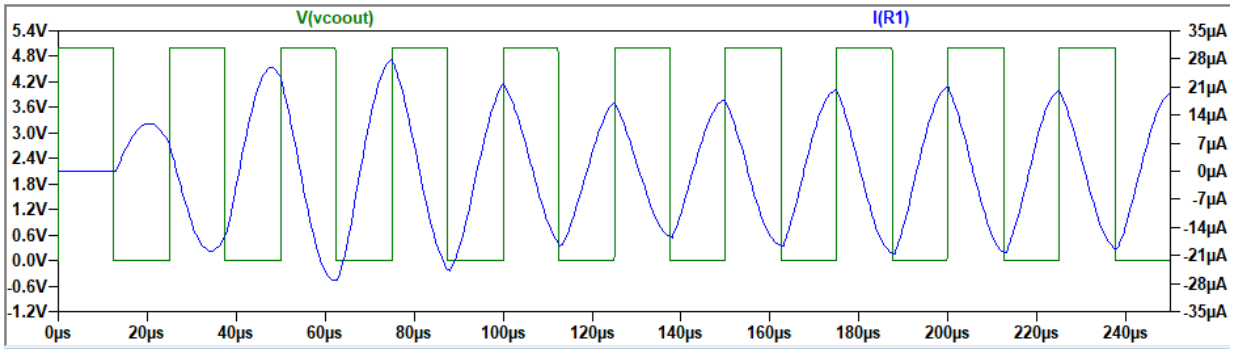

Figure 10: The Waveform produced by the Transmission Amplifier Testbench

3.2 Demodulation

3.2.1 Pre-Amp

The pre-amp was implemented using a non-inverting op-amp amplifier. This was to make setting the gain simple and to minimise costs. A high-speed op-amp was chosen to reproduce any of the square wave characteristics that were transmitted by the modulation stage.

Figure 11 shows the schematic for the preamp. The parameters for the resistances are set by the testbench.

Figure 12 shows the test bench. The gain is stepped across the range given in Section 2.3.1. Parameters passed to the pre-amp block for R1 and R2 are calculated as $R1 = Rbase = 1k\Omega$ and $R2 = Rbase \times gain$. The input amplitude is reduced by the same factor that the gain is increased to approximate the gain of the system increasing to compensate for greater attenuation. At each step the 3db point is calculated to give an approximation of the system bandwidth from 0 - 3db point. Figure 13 shows the output of the measure directive, showing that the bandwidth requirements given in Section 2.3.1 have been met.

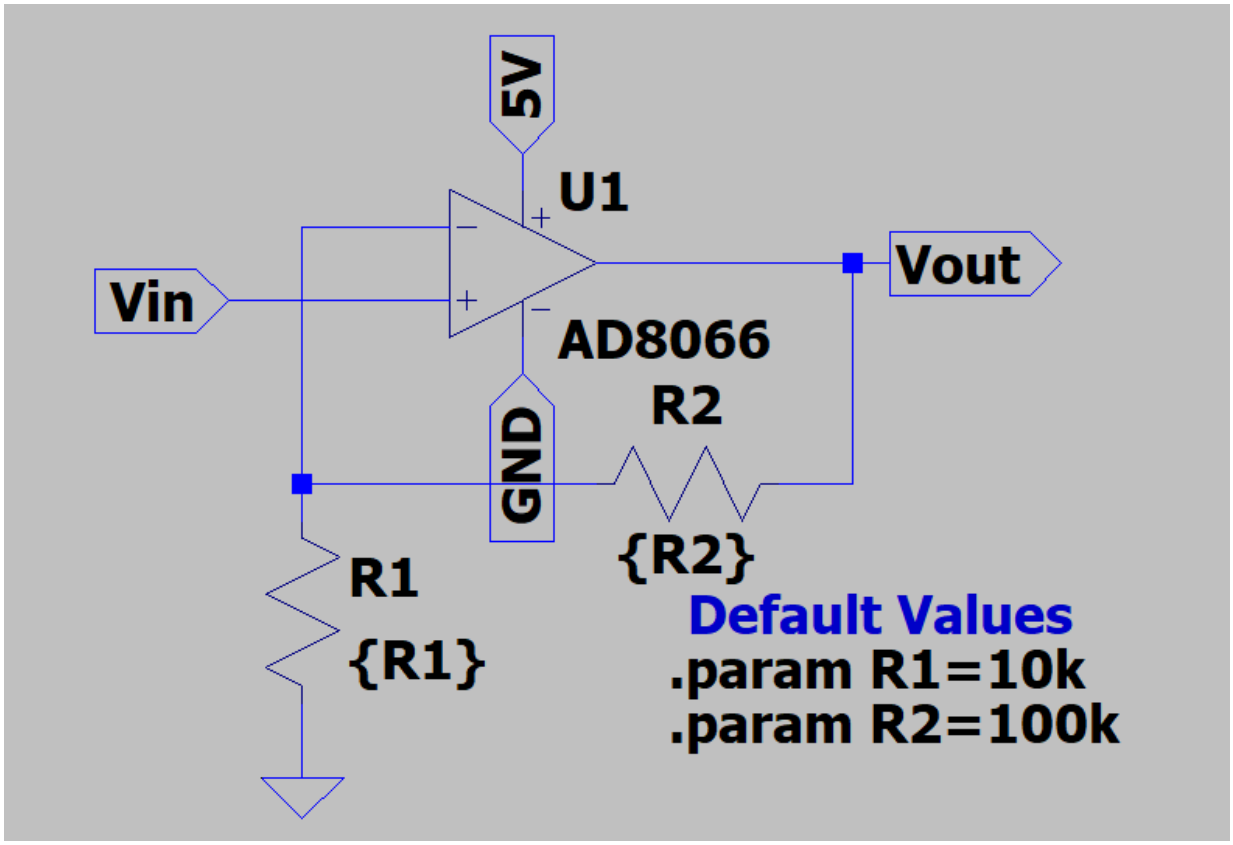

Figure 11: A screencap of the Pre-Amp Subcircuit

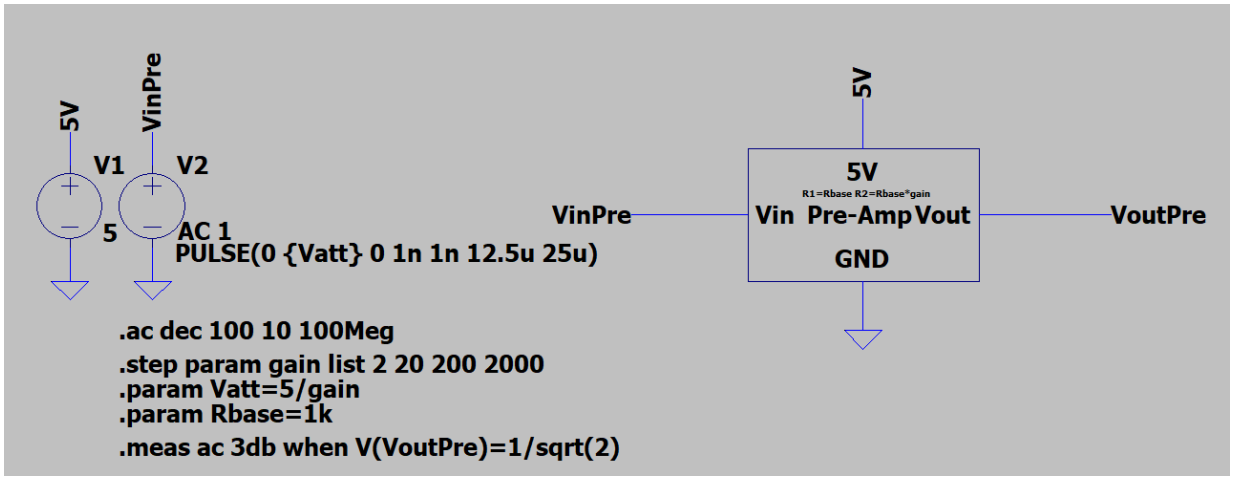

Figure 12: The testbench fort the Pre-Amp Subcircuit

```
Measurement: 3db
  step              v(voutpre)=1/sqrt(2)
     1              1.34464e+007
     2              7.34032e+006
     3              3.63284e+006
     4              934460
```

Figure 13: The Waveform produced by the Pre-Amp Testbench

3.2.2 PLL

The TI CD4046B has been chosen to implement the PLL as it is cheap and does not require many external components. The "CD4046B Phase-Locked Loop (Rev. A)" application note was used to design the circuit[3]. It was not simulated in LTSpice as TI does not provide a spice model.

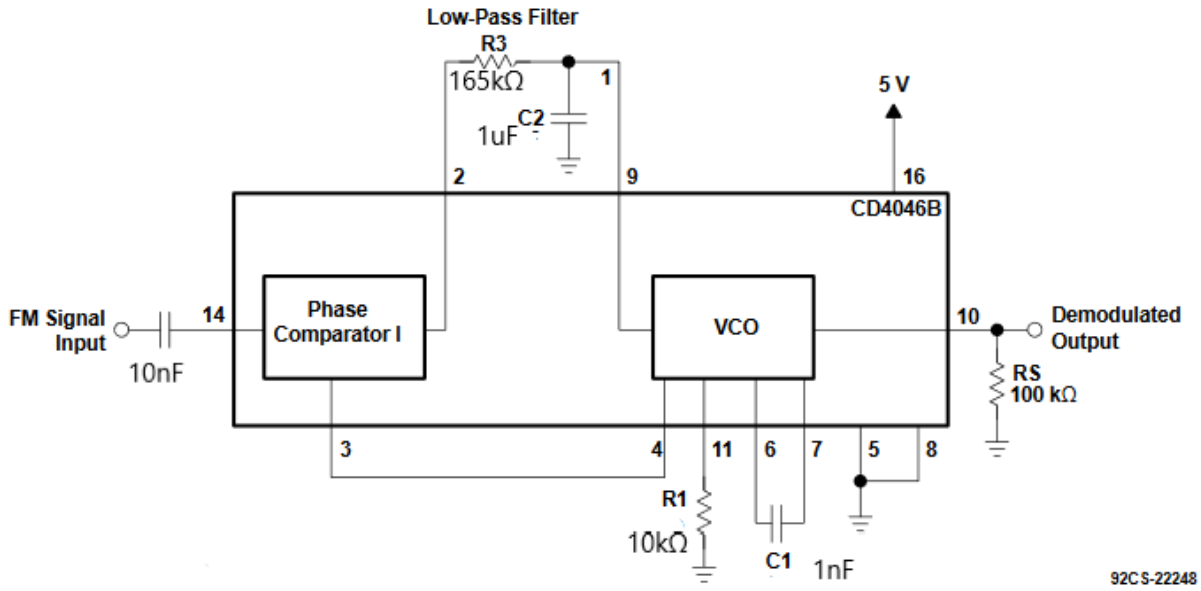

Figure 14: The PLL subcircuiit reproduced from the example circuit.

Figure 14 contains a schematic for the PLL subcircuit reproduced from Section 4.1 of the application note. The passive component values have been replaced with those calculated to meet the specification presented in Section 2.3.2. The values are derived by following the process described in Section 4.1 of the application note. The VCO center frequency is set using R1 and C1 as derived from Figure 9(a). The bandwidth, given by twice the capture frequency f_c in the application note, was set to 8 kHz by setting R_3 and C_2 using the Equation 5. The component values selected will enable the PLL to enter lock when the FM signal is received.

[3] https://www.ti.com/lit/an/scha002a/scha002a.pdf?&ts=1589738760062

$$
\begin{aligned}
2f_c &= \frac{1}{R_3 C_2}\sqrt{\frac{2\pi f_L}{R_3 C_2}} \\
R_3 C_2^{\frac{3}{2}} &= \frac{\sqrt{2\pi f_L}}{2f_c}
\end{aligned}
\tag{5}
$$

With $f_l = f_c = \frac{1}{2}BW = 4kHz$ and $C_2 = 1uF$:

$$
\begin{aligned}
R_3 C_2 &= 0.116s \\
R_3 &= 165k\Omega
\end{aligned}
$$

3.3 Analogue to Digital Conversion

3.3.1 Differentiators

The topology for the differentiator was taken from Figure 4.69 in *The Art of Electronics*[4]. The values for the passive components were copied but this gave a gain of $\frac{1}{1000}$ so C1 was increased to 1 uF to produce the required response. The minimum output value was set to 0 V by adding a diode to the output of the differentiator. Since the differentiator output is a digital signal, the forward voltage of the diode has no impact. To allow this diode to operate, a 1 MΩ resistor was added to the testbench output to simulate the low current drawn by a logic IC. The AD822 IC contains two opamps so both differentiators could be implemented using a single IC.

Figure 15 shows the schematic as described by Horowitz and Hill[4]. Figure 16 shows the test bench used to demonstrate the circuit. The input to the differentiator is driven by the triangle wave generator block as described in Section 3.1.1. Figure 17 shows the output of the differentiator.

The differentiator produces a square wave swinging between 0 and 4.2 V. The triangle wave is shown as well, demonstrating a clear digital signal is produced, with logic HIGH corresponding to the triangle wave ramping down, and logic LOW corresponding to the triangle wave ramping up. Inverting the inputs to an XOR/XNOR gate has no affect on the output signal so this inversion is not an issue.

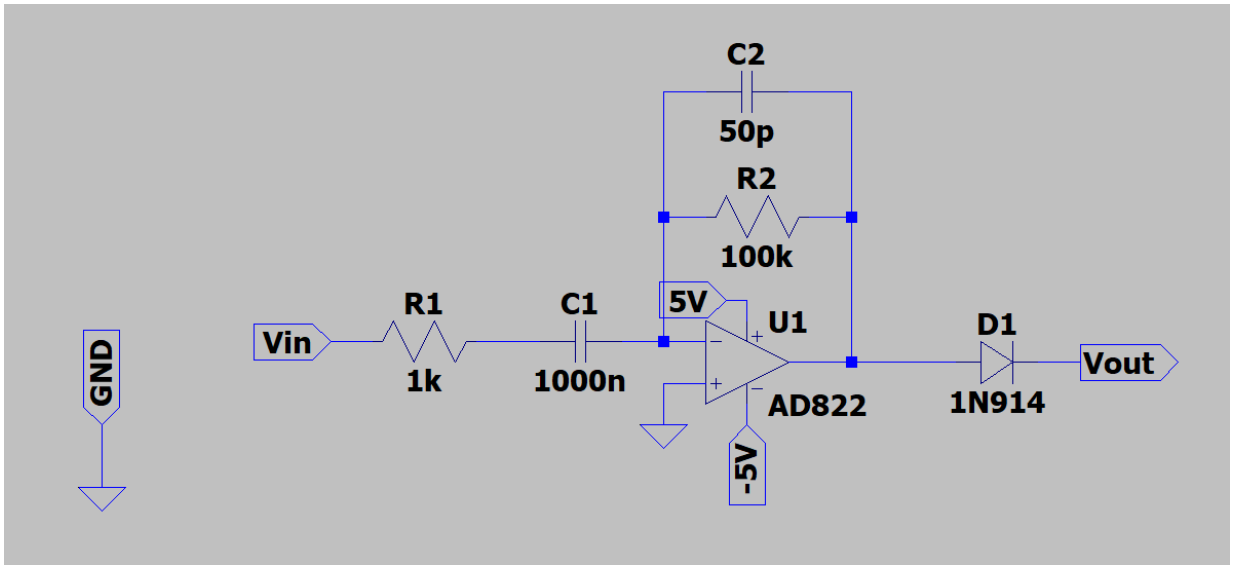

Figure 15: A screencap of the Pre-Amp Subcircuit

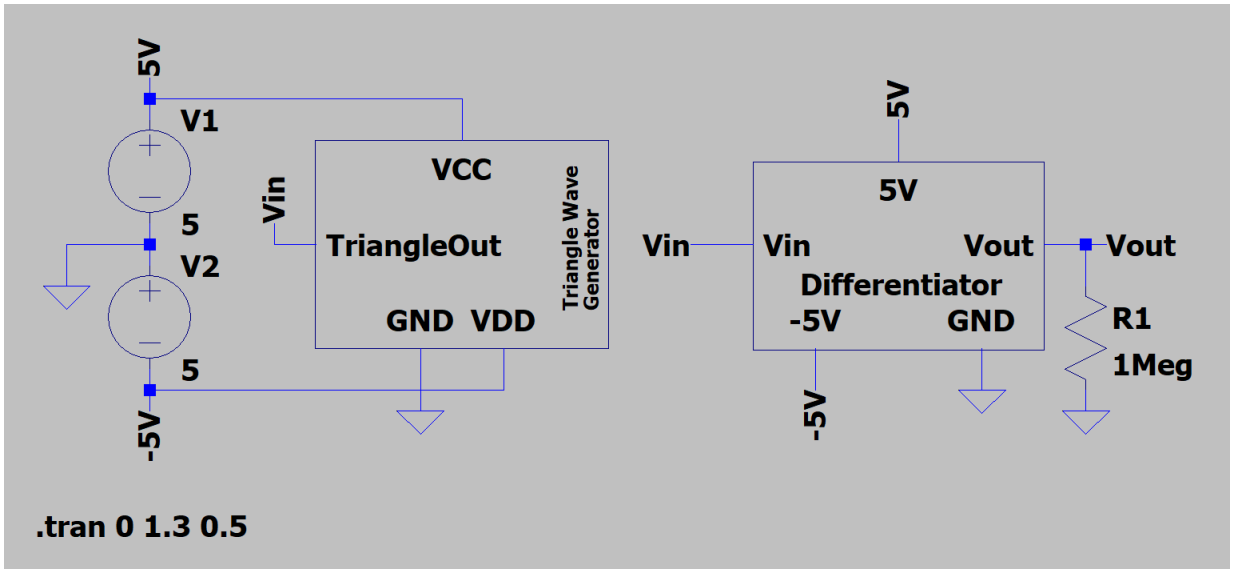

Figure 16: A screencap of the Pre-Amp Subcircuit

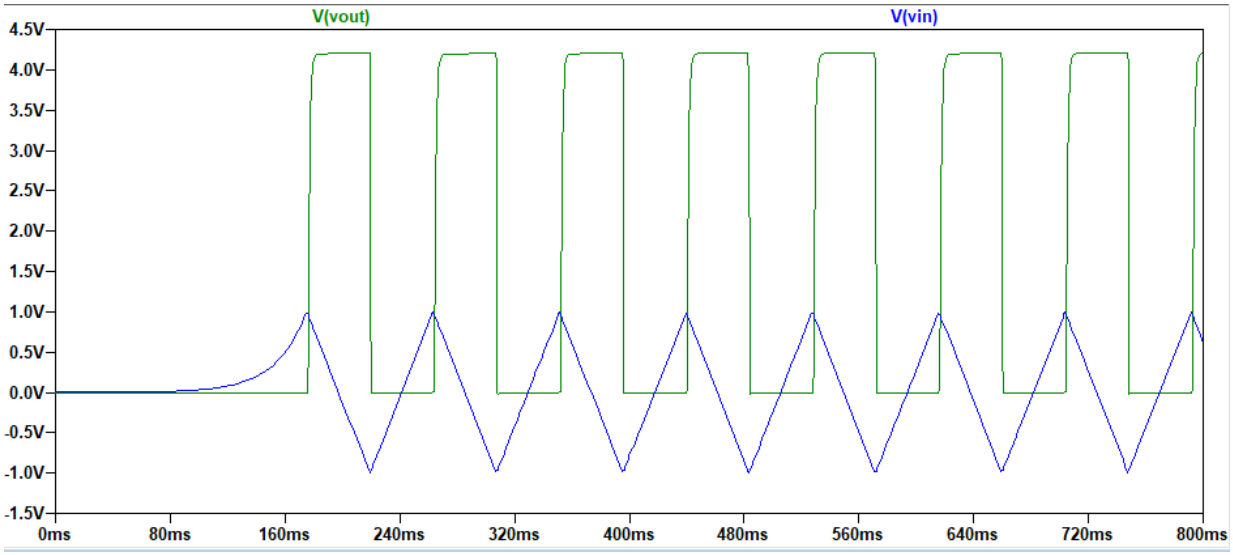

Figure 17: A screencap of the Pre-Amp Subcircuit

3.3.2 Differential Amplifier

The differential amplifier is split into three sections. The first is a unity-gain inverting amplifier to remove the inversion imposed by the VCO. The second is the LT6370 instrumentation amplifier for accurately converting the differential input to a single-ended output. The third is a full-wave rectifier so the output signal corresponds to the *magnitude* of the difference between the input signals, not the absolute difference. The schematic is shown in Figure 18

In the event that the PLL output amplitude does not match that of the Triangle Wave Generator, the gain of the inverting amplifier can be adjusted with R_1 and R_2 so both signals are precisely matched. The topology for the rectifier was reproduced from Figure 4.63 in Horowitz and Hill's *The Art of Electronics*[5]. The feedback circuits of the op-amps eliminate the voltage drop across the diodes in a passive full-wave rectifier.

Figure 19 shows the Differential Amplifier testbench. It generates two triangle waves of equal and opposite amplitude. The voltage source simulating the PLL output has an increasing delay imposed on it by the step command. The output of the testbench is shown in Figure 20. It can be seen that the maximum output voltage increases with as the delay increases.

A simulation involving more steps was used to produce the plot in Figure 21. The output voltage with 0 delay is 35.3 uV. The output voltage with the maximum delay of 14.5 ms is 3.31 V. Figure 21 shows a correlation coefficient of 0.999999959, meaning the differential amplifier easily meets the specification stated in Section 2.4.1.

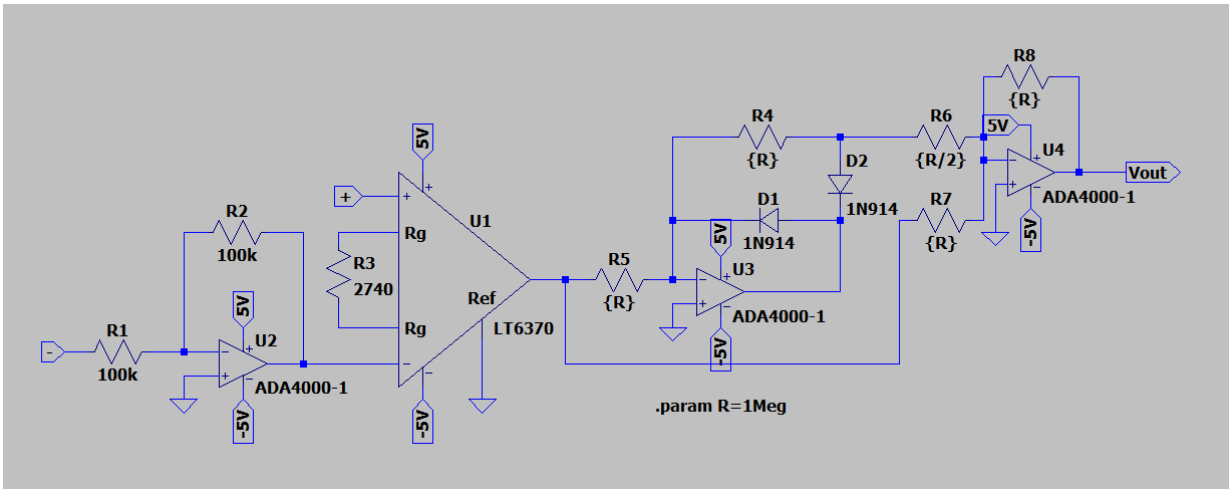

Figure 18: A screencap of the Differential Amplifier Subcircuit

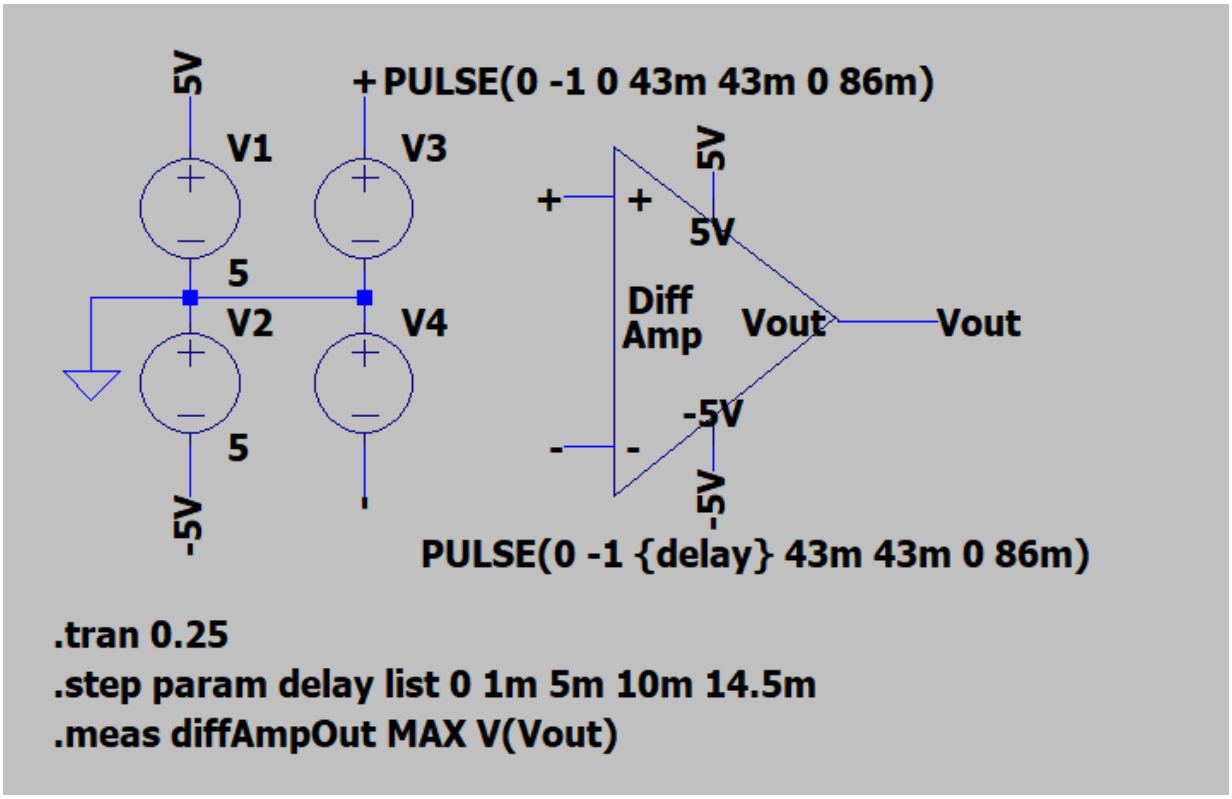

Figure 19: A screencap of the Differential Amplifier Testbench

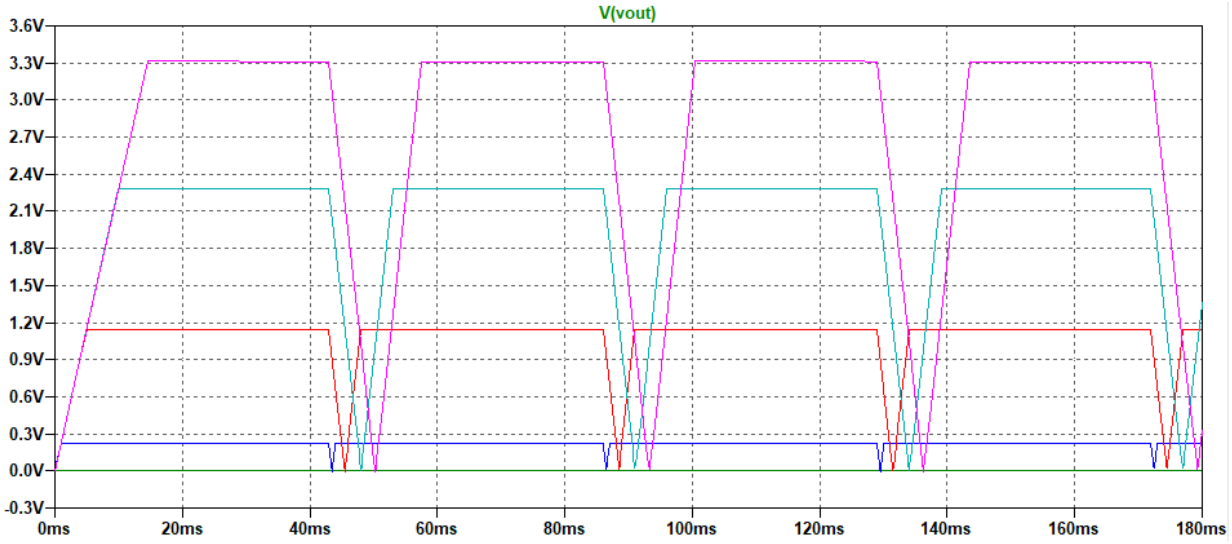

Figure 20: A screencap of the output produced by the Differential Amplifier Testbench

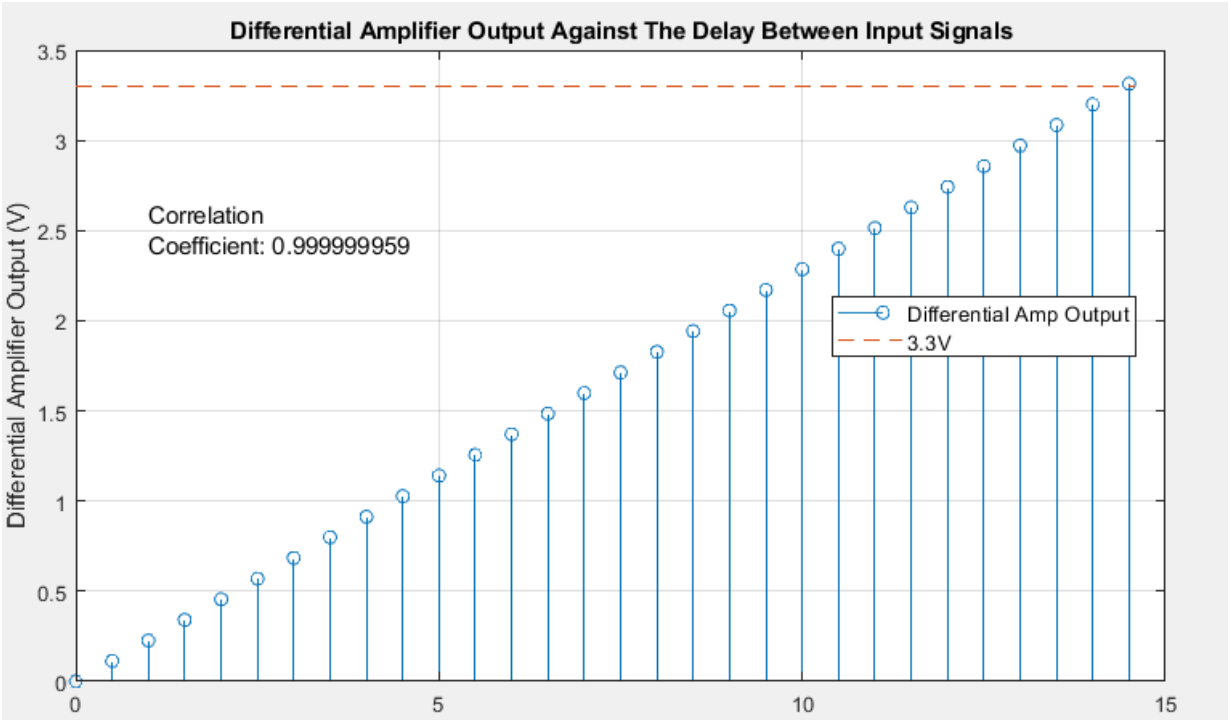

Figure 21: A plot showing the linearity of the Differential Amplifier

3.3.3 Digital Logic

The AD7819 should be used as the ADC. It provides a parallel interface with with chip select and read data controls. The datasheet can be found here[4].

The microcontroller should be interfaced as shown in Figure 4 of the datasheet with the parallel interface interrupted by the 8-bit latch. Vref should be tied to 3.3 volts through a voltage divider

[4] https://www.analog.com/media/en/technical-documentation/data-sheets/AD7819.pdf

between 5V and GND. To perform a conversion, the microcontroller should follow the timing diagram as described in Figure 15 of the datasheet.

The SN74HC573AN should be used as the 8-bit latch. The characteristics of this device far exceed the timing requirements of this circuit in terms of switching speed. The latch enable line is active HIGH so an XNOR gate should be used to generate the latch enable signal as specified in Section 2.1.

The XNOR gate should be implemented using the NC7SZ57P6X universal logic gate. The datasheet can be found here[5]. It is a cheap, space-friendly way to produce an XNOR gate. It should be wired up as shown in Figure 8 of the data sheet, with connections A and B connected to the differentiator outputs and Y connected to the latch enable pin of the 8-bit latch. As with the latch, the characteristics of this device exceed the timing requirements of this circuit.

[5] https://www.onsemi.com/pub/Collateral/NC7SZ58-D.PDF

4 Critical Analysis

It was assumed during the completion of this document that the requirement for a bespoke FMCW radar sensor meant that the robot being produced required high levels of performance and had a budget to match. If not, an off-the-shelf pulse-based device such as the HC-S04[6] would have been used. To this end, the system designed is suitable for a moderate to high-budget, high-performance system. Conversely, this system would not be appropriate for a low-budget, low-performance system such as a toy. The components used are high performance and rely on a dual-rail power supply of a kind that would be expensive to implement.

The component choices themselves work well for the designs in which they are used, but more thought could be put in to optimising for price. Only Spice models shipped with LTSpice were used in the simulations but there may be better, more cost-effective devices not found in the LTSpice device library. The number of different op-amps could also be reduced. Replacing each op-amp in the design with the ADA4000-1 used in the differential amplifier should be investigated as it performed well in the inverting amplifier and the full-wave rectifier.

The lack of knowledge regarding the robot and the ultrasound transducers resulted in some uncertainty with component values. The ability to set the gain of the Pre-Amp and the inverter in the differential amplifier resulted in reduced bandwidth of both circuits. The addition of jumpers to configure the use of the transmission amplifier also adds extra complexity to the system. However, it is felt that making the circuit configurable was the right choice for this project. Once the system has been built and tested using the real hardware the component values can be set in stone ready for a high volume production run. If this was a real project, a test circuit for the PLL could be produced and evaluated separately if development time allowed to ensure the implementation of the support circuitry was correct.

More research could have been made into PLLs with spice models but a compromise was made with the the chosen device. Its low price and simple support circuitry meant that the parameters of the PLL subcircuit would be easy to edit during PCB testing. Similarly, the timing requirements of the digital circuits were lenient enough that time was not spent finding spice models for each device so that simulation could be completed. In a future design, this digital logic could be replaced with a low-cost CPLD to save on PCB space and board revisions.

Over all, it is felt that the brief has been met but testing with physical hardware should be performed before a mass-production run of the circuit is advised.

[6] `https://cdn.sparkfun.com/datasheets/Sensors/Proximity/HCSR04.pdf`

References

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