
STM32
CubeMX

1. Description

1.1. Project

Project Name	oscilliscope
Board Name	custom
Generated with:	STM32CubeMX 6.3.0
Date	07/27/2021

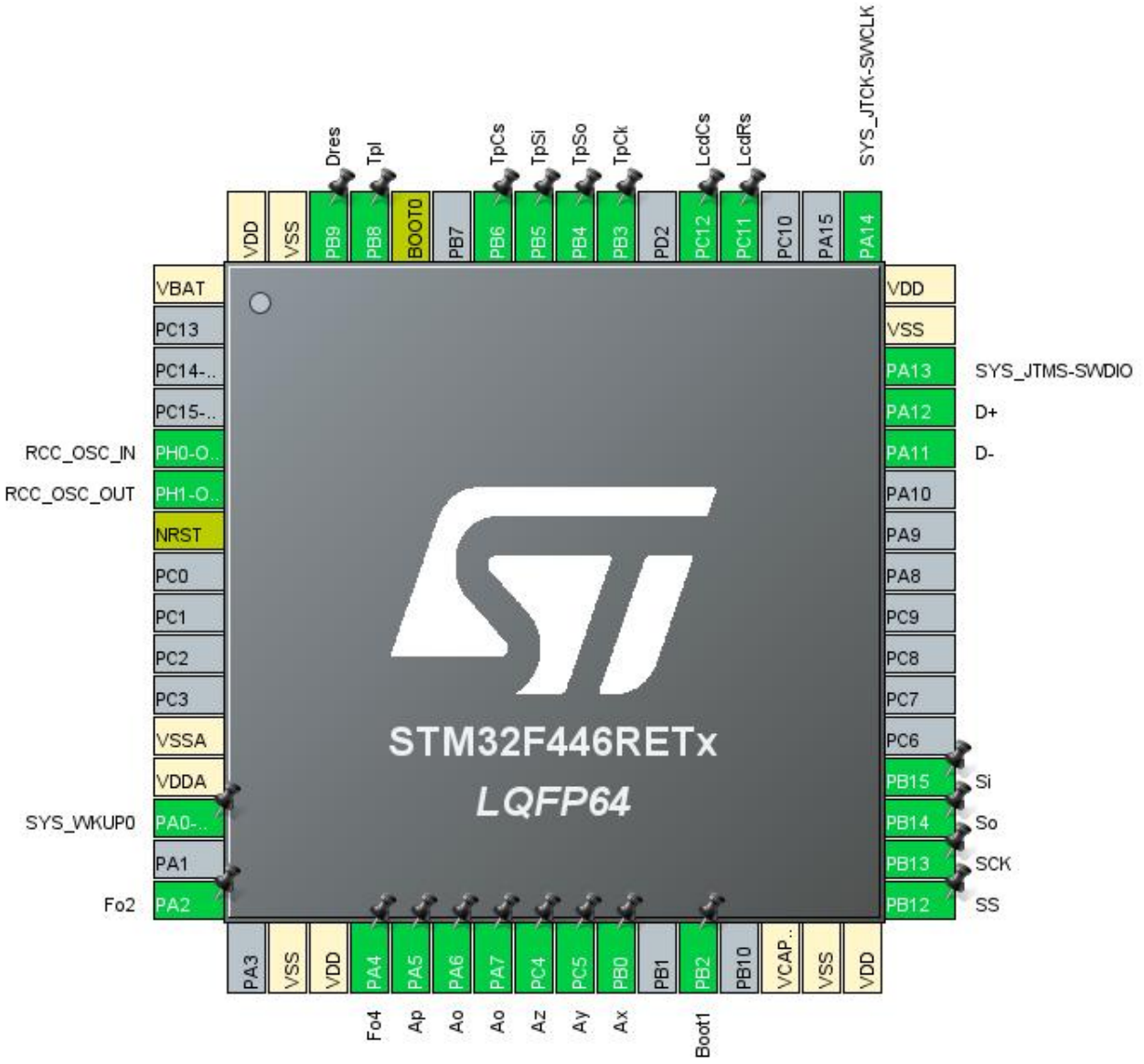
1.2. MCU

MCU Series	STM32F4
MCU Line	STM32F446
MCU name	STM32F446RETx
MCU Package	LQFP64
MCU Pin number	64

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration



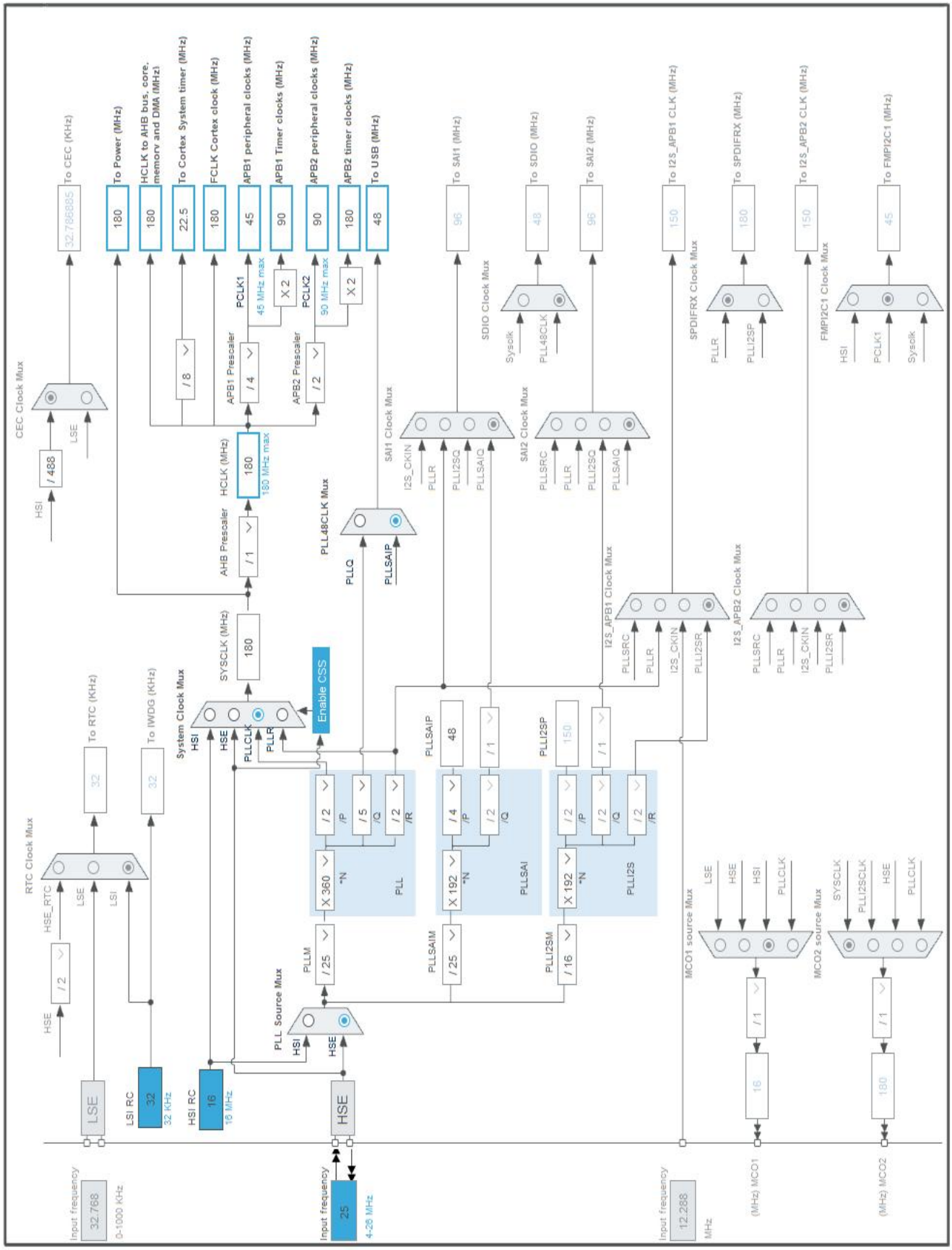
3. Pins Configuration

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VBAT	Power		
5	PH0-OSC_IN	I/O	RCC_OSC_IN	
6	PH1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
12	VSSA	Power		
13	VDDA	Power		
14	PA0-WKUP	I/O	SYS_WKUP0	
16	PA2 *	I/O	GPIO_Output	Fo2
18	VSS	Power		
19	VDD	Power		
20	PA4	I/O	DAC_OUT1	Fo4
21	PA5	I/O	DAC_OUT2	Ap
22	PA6	I/O	ADC1_IN6	Ao
23	PA7	I/O	ADC2_IN7	Ao
24	PC4 *	I/O	GPIO_Output	Az
25	PC5 *	I/O	GPIO_Output	Ay
26	PB0 *	I/O	GPIO_Output	Ax
28	PB2 *	I/O	GPIO_Input	Boot1
30	VCAP_1	Power		
31	VSS	Power		
32	VDD	Power		
33	PB12 *	I/O	GPIO_Output	SS
34	PB13	I/O	SPI2_SCK	SCK
35	PB14	I/O	SPI2_MISO	So
36	PB15	I/O	SPI2_MOSI	Si
44	PA11	I/O	USB_OTG_FS_DM	D-
45	PA12	I/O	USB_OTG_FS_DP	D+
46	PA13	I/O	SYS_JTMS-SWDIO	
47	VSS	Power		
48	VDD	Power		
49	PA14	I/O	SYS_JTCK-SWCLK	
52	PC11 *	I/O	GPIO_Output	LcdRs
53	PC12 *	I/O	GPIO_Output	LcdCs
55	PB3	I/O	SPI3_SCK	TpCk
56	PB4	I/O	SPI3_MISO	TpSo
57	PB5	I/O	SPI3_MOSI	TpSi

Pin Number LQFP64	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
58	PB6 *	I/O	GPIO_Output	TpCs
60	BOOT0	Boot		
61	PB8	I/O	GPIO_EXTI8	TpI
62	PB9 *	I/O	GPIO_Output	Dres
63	VSS	Power		
64	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	oscilliscope
Project Folder	C:\Users\paul_\STM32CubeIDE\workspace_1.6.1\oscilliscope
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F4 V1.26.1
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x800
Minimum Stack Size	0x600

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No
Enable Full Assert	No

5.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	MX_GPIO_Init	GPIO
2	MX_DMA_Init	DMA
3	SystemClock_Config	RCC
4	MX_ADC1_Init	ADC1
5	MX_ADC2_Init	ADC2
6	MX_DAC_Init	DAC
7	MX_SPI2_Init	SPI2
8	MX_SPI3_Init	SPI3
9	MX_TIM1_Init	TIM1
10	MX_TIM3_Init	TIM3
11	MX_TIM5_Init	TIM5

Rank	Function Name	Peripheral Instance Name
12	MX_USB_DEVICE_Init	USB_DEVICE
13	MX_TIM7_Init	TIM7

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F4
Line	STM32F446
MCU	STM32F446RETx
Datasheet	DS10693_Rev6

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

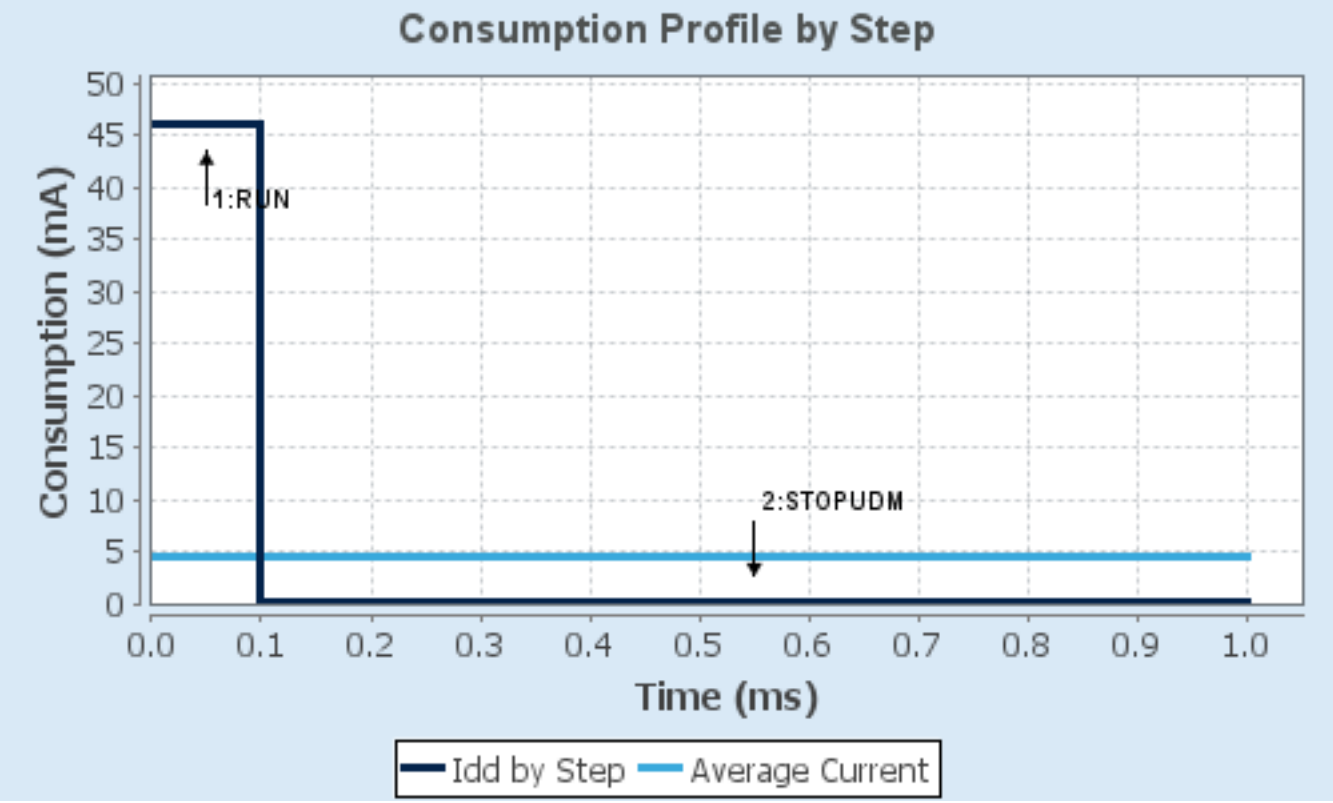
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	RAM/FLASH/REGON/ART/PREFETCH	n/a
CPU Frequency	180 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	46 mA	55 µA
Duration	0.1 ms	0.9 ms
DMIPS	225.0	0.0
Ta Max	98.02	104.99
Category	In DS Table	In DS Table

6.5. Results

Sequence Time	1 ms	Average Current	4.65 mA
Battery Life	1 month	Average DMIPS	225.0 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
50
45
40
35
30
25
20
15
10
5
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. Peripherals and Middlewares Configuration

7.1. ADC1

mode: IN6

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	**Timer 1 Capture Compare 1 event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 6
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ADC2

mode: IN7

7.2.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 4
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment

Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	**Timer 1 Capture Compare 1 event ***
External Trigger Conversion Edge	Trigger detection on the rising edge
Rank	1
Channel	Channel 7
Sampling Time	3 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.3. DAC

mode: OUT1 Configuration

mode: OUT2 Configuration

7.3.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	None

DAC Out2 Settings:

Output Buffer	**Disable ***
Trigger	None

7.4. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled

Data Cache	Enabled
Flash Latency(WS)	5 WS (6 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

Power Parameters:

Power Regulator Voltage Scale	Power Regulator Voltage Scale 1
Power Over Drive	Enabled

7.5. SPI2

Mode: Full-Duplex Master

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	8 Bits
First Bit	**LSB First ***

Clock Parameters:

Prescaler (for Baud Rate)	2
Baud Rate	**22.5 MBits/s ***
Clock Polarity (CPOL)	**High ***
Clock Phase (CPHA)	**2 Edge ***

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.6. SPI3

Mode: Full-Duplex Master

7.6.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**16 Bits ***
First Bit	**LSB First ***

Clock Parameters:

Prescaler (for Baud Rate)	**8 ***
Baud Rate	**5.625 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSS Signal Type	Software

7.7. SYS

Debug: Serial Wire
mode: System Wake-Up 0
Timebase Source: SysTick

7.8. TIM1

Clock Source : Internal Clock

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**89 ***
Counter Mode	**Down ***
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
Repetition Counter (RCR - 8 bits value)	0
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.9. TIM3

Clock Source : Internal Clock

7.9.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**11 ***

Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**7499 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	**Update Event ***

7.10. TIM5
mode: Clock Source
7.10.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**9 ***
Counter Mode	Up
Counter Period (AutoReload Register - 32 bits value)	**18000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.11. TIM7
mode: Activated
7.11.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**2 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.12. USB_OTG_FS

Mode: Device_Only

7.12.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Disabled
Signal start of frame	Disabled

7.13. USB_DEVICE

Class For FS IP: Mass Storage Class

7.13.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

MSC_MEDIA_PACKET (Media I/O buffer Size)	512

7.13.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	1155
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	STMicroelectronics

Device Descriptor FS:

PID (Product IDentifier)	22314
PRODUCT_STRING (Product Identifier)	STM32 Mass Storage
CONFIGURATION_STRING (Configuration Identifier)	MSC Config
INTERFACE_STRING (Interface Identifier)	MSC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA6	ADC1_IN6	Analog mode	No pull-up and no pull-down	n/a	Ao
ADC2	PA7	ADC2_IN7	Analog mode	No pull-up and no pull-down	n/a	Ao
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	Fo4
	PA5	DAC_OUT2	Analog mode	No pull-up and no pull-down	n/a	Ap
RCC	PH0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1-OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SPI2	PB13	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	SCK
	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	So
	PB15	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	Si
SPI3	PB3	SPI3_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	TpCk
	PB4	SPI3_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	TpSo
	PB5	SPI3_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	TpSi
SYS	PA0-WKUP	SYS_WKUP0	n/a	n/a	n/a	
	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
USB_OTG_FS	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	D-
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	D+
GPIO	PA2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Fo2
	PC4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Az
	PC5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Ay
	PB0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Ax
	PB2	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	Boot1
	PB12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	SS

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LcdRs
	PC12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	LcdCs
	PB6	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	TpCs
	PB8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	**Pull-up ***	n/a	TpI
	PB9	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	Dres

8.2. DMA configuration

DMA request	Stream	Direction	Priority
TIM7_UP	DMA1_Stream2	Peripheral To Memory	Low
ADC1	DMA2_Stream0	Peripheral To Memory	Low
DAC1	DMA1_Stream5	Memory To Peripheral	Low

TIM7_UP: DMA1_Stream2 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

ADC1: DMA2_Stream0 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

DAC1: DMA1_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	Half Word
Memory Data Width:	Half Word

8.3. NVIC configuration

8.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
DMA1 stream2 global interrupt	true	0	0
DMA1 stream5 global interrupt	true	0	0
EXTI line[9:5] interrupts	true	0	0
TIM3 global interrupt	true	0	0
SPI2 global interrupt	true	1	0
SPI3 global interrupt	true	1	0
TIM6 global interrupt and DAC1, DAC2 underrun error interrupts	true	0	0
DMA2 stream0 global interrupt	true	0	0
USB On The Go FS global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1, ADC2 and ADC3 interrupts	unused		
TIM1 break interrupt and TIM9 global interrupt	unused		
TIM1 update interrupt and TIM10 global interrupt	unused		
TIM1 trigger and commutation interrupts and TIM11 global interrupt	unused		
TIM1 capture compare interrupt	unused		
TIM5 global interrupt	unused		
TIM7 global interrupt	unused		
FPU global interrupt	unused		

8.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false

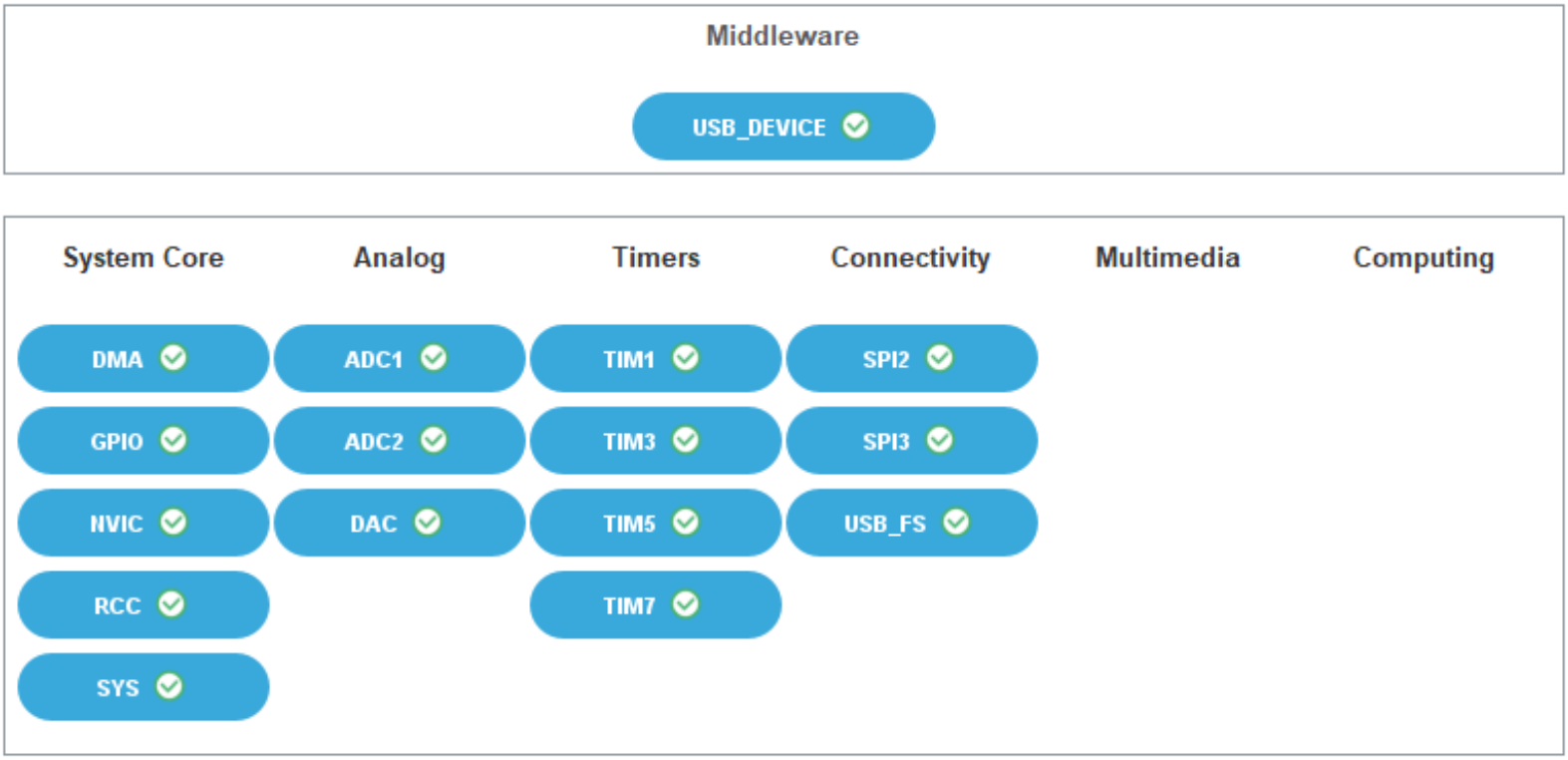
Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	true	false
Debug monitor	false	true	false
Pendable request for system service	false	true	false
System tick timer	false	true	true
DMA1 stream2 global interrupt	false	true	true
DMA1 stream5 global interrupt	false	true	true
EXTI line[9:5] interrupts	false	true	true
TIM3 global interrupt	false	true	true
SPI2 global interrupt	false	true	true
SPI3 global interrupt	false	true	true
TIM6 global interrupt and DAC1, DAC2 underrun error interrupts	false	false	false
DMA2 stream0 global interrupt	false	true	true
USB On The Go FS global interrupt	false	true	true

*** User modified value**

9. System Views

9.1. Category view

9.1.1. Current



10. Docs & Resources

Type	Link
Datasheet	http://www.st.com/resource/en/datasheet/DM00141306.pdf
Reference manual	http://www.st.com/resource/en/reference_manual/DM00135183.pdf
Programming manual	http://www.st.com/resource/en/programming_manual/DM00046982.pdf
Errata sheet	http://www.st.com/resource/en/errata_sheet/DM00155929.pdf
Application note	http://www.st.com/resource/en/application_note/CD00167594.pdf
Application note	http://www.st.com/resource/en/application_note/CD00211314.pdf
Application note	http://www.st.com/resource/en/application_note/CD00249778.pdf
Application note	http://www.st.com/resource/en/application_note/CD00259245.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264321.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264342.pdf
Application note	http://www.st.com/resource/en/application_note/CD00264379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00024853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040802.pdf
Application note	http://www.st.com/resource/en/application_note/DM00040808.pdf
Application note	http://www.st.com/resource/en/application_note/DM00042534.pdf
Application note	http://www.st.com/resource/en/application_note/DM00046011.pdf
Application note	http://www.st.com/resource/en/application_note/DM00072315.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073742.pdf
Application note	http://www.st.com/resource/en/application_note/DM00073853.pdf
Application note	http://www.st.com/resource/en/application_note/DM00080497.pdf
Application note	http://www.st.com/resource/en/application_note/DM00081379.pdf
Application note	http://www.st.com/resource/en/application_note/DM00115714.pdf
Application note	http://www.st.com/resource/en/application_note/DM00129215.pdf
Application note	http://www.st.com/resource/en/application_note/DM00154959.pdf
Application note	http://www.st.com/resource/en/application_note/DM00160482.pdf

Application note	http://www.st.com/resource/en/application_note/DM00161778.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00226326.pdf
Application note	http://www.st.com/resource/en/application_note/DM00227538.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00272912.pdf
Application note	http://www.st.com/resource/en/application_note/DM00281138.pdf
Application note	http://www.st.com/resource/en/application_note/DM00296349.pdf
Application note	http://www.st.com/resource/en/application_note/DM00315319.pdf
Application note	http://www.st.com/resource/en/application_note/DM00327191.pdf
Application note	http://www.st.com/resource/en/application_note/DM00354244.pdf
Application note	http://www.st.com/resource/en/application_note/DM00373474.pdf
Application note	http://www.st.com/resource/en/application_note/DM00380469.pdf
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Application note	http://www.st.com/resource/en/application_note/DM00725181.pdf