EE-271 PROJECT

VENDING MACHINE

Abstract

Vending machines are very well known for their purpose in providing good quality of food products in no amount of time. This kind of machines are results of the modern and fast life styles which we have developed

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1. **Abstract:-**

Vending machines are very well known for their purpose in providing good quality of food products in no amount of time. This kind of machines are results of the modern and fast life styles which we have developed. This report elaborates in detail how the vending machine has been designed using with features like multi products, automated billing system with change return and transaction cancelling options. This design is made using the Finite State Machine (FSM) modeling approach which leads to optimized hardware and hence increased performance. The design consists of seven states (Display Products, Select Products, Money Insertion, Product Dispatch, Return Change, Cancel Transaction, Thanks) which has been modeled using mealy machine. The design has been coded using Verilog-HDL in Quartus Prime Lite software and have been tested on FPGA DE10-Lite (Altera Max 10 DA) development board.

2. **Introduction:-**

Vending Machines are used to deliver food products like cold drinks, cookies, chocolates, chips etc. over few button presses. These kinds of machine are very user friendly and fast as compared to standard convention of purchasing and selling. These kinds of machines can now a days be found at various places like cinemas, railways, bus stops, clubs, casinos etc. The FPGA based design tends to be more flexible and are also re-programmable unlike micro-controller based design where in one have to change the architecture to upgrade the design. FPGA based design will be able to expand up to N number of products.

I. **Features**:-

- The machine consists of 5 products.
- User have to use $1, $5 or $10 to purchase the products.
- Cancel transaction at any point of time. Cancelling transaction after money input will return the money.
- Capability to decline transaction if no stock available.
- Vending Machine owner can refill the products by pressing refill button.
- Auto billing system with change return.
- Configurable display time. (Max supported is 5 seconds)
- Configurable watchdog timer. (Max supported is 5 minutes)
- Parameterized design
    - Product Price
    - Number of Products
    - Number of Money Buttons
- Incorporated a unique feature of no stock where if user select a product which it out of stock, the machine will display no stock.
- Also designed added feature of refill which machine owner can press to refill stock, at any point of time. Moreover, we have coded transaction cancel, which will return if user has input some money after cancel.

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II. **Specifications**:-

- FPGA DE10-Lite (Altera Max 10 DA) running on 50 Mhz clock cycle.
- 6-seven segments for display.
- 4x4 keypad for product, money, cancel transaction and product refill input.
- One reset button(FPGA button 0) to reset the vending machine.

III. **Working**:-

- **IDEAL state:** seven segments will show user the number of 5 products. In the interval of every designated time, products will loop one by one. It will show product number – product price – product quantity available.
- User will select a product using 4x4 keypad and the machine will jump to state ***"PRODUCT_PROC"***.
- **PRODUCT_PROC state:** Jump to ***"CNCEL"*** if ***"Cancel"*** button is pressed. If a product is selected then FSM displays product selected and its price. After the selection the display will show user how much amount is to be paid for the chosen product for few seconds and then jump to state ***"MONEY_PROC"***.
- User will enter money for the selected product using 4x4 keypad.
- **MONEY_PROC state:** Wait for user to enter money. Display price of selected product on the left and accumulation of money entered by user, on the right. At any time, user can press ***"Cancel***" button to cancel the transaction. FSM will proceed to ***"DISPATCH"*** if money amount entered is equal to or exceeds the price of product. A watchdog timer will trigger at the start of state which will reset on every money input. If the timer expires before user enters the expected price of selected product, FSM will move to ***"THANKS"***.
- **DISPATCH state:** Display ***"ENJOY"*** to let user know that the product is dispatched. If money entered is greater than expected price, FSM will jump to ***"MONEY_RETURN***". If there is no money to return, FSM will move to ***"THANKS"***. User cannot cancel transaction at this time.
- **MONEY_RETURN state:** FSM will reach this state only if vending machine has to return any amount of money to user. This state will Display the amount to return till timer expires
- **CANCEL state:** FSM will jump to CANCEL state if user presses ***"Cancel"*** at any point of time in the ongoing transaction. Display ***"CANCEL"*** till timer expires. If user has entered any money then the amount will be returned if the transaction is canceled.
- **THANKS state:** DISPLAY ***"THANKS"*** on successful completion of a transaction. If user enters a product that is out of stock, then FSM will display ***"NOSTOCK"***.
- **Quantity and Refill:** Vending Machine is equipped with configurable quantity for each product. On reset, the machine shows maximum quantity available. The quantity reduced on successful dispatch of each product. If user selects a product, which has no available stock, the FSM is capable of displaying ***"NOSTOCK"***. When refill button is pressed it will refill the all product quantity to configured values.
- **Display Timers:** The display timers of is used to hold the display for the current state. The timer is configurable and currently configured to 2 sec.
- **Watchdog Timer:** The watch dog timer is used to avoid the deadlock when user leaves the vending machine hanging after selecting the product. This timer is set to 10 sec.

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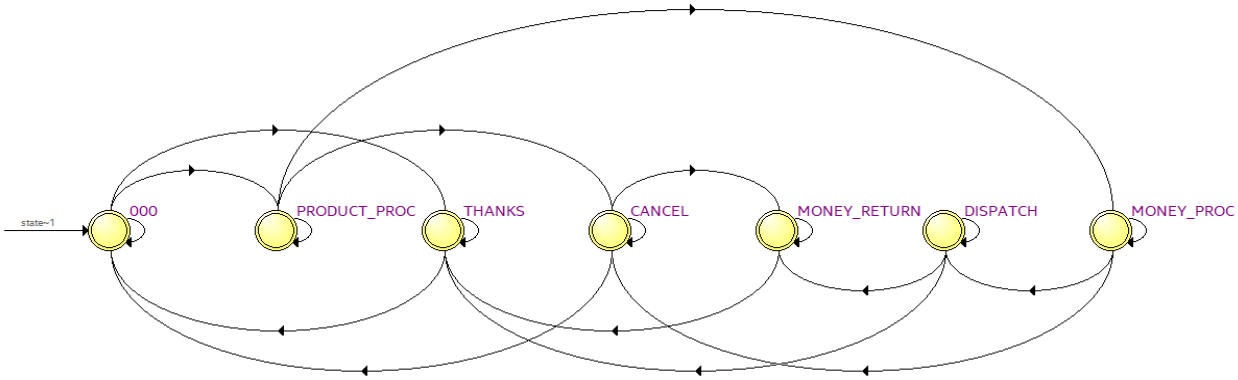

Figure 1. Vending Machine FSM

IV. Product Details:-

Product	Price($)
PRODUCT 1	2
PRODUCT 2	5
PRODUCT 3	7
PRODUCT 4	15
PRODUCT 5	18

V. 4x4 keypad configuration:-

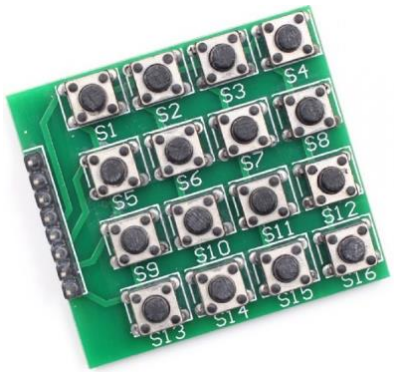

Figure 2. 4x4 Keypad

Product i/p	***Switch No.***	***Money i/p***	***Switch No.***
PRODUCT 1	13	$1	3
PRODUCT 2	9	$5	7
PRODUCT 3	5	$10	11
PRODUCT 4	1	***Function***	***Switch No.***
PRODUCT 5	2	Cancel	4
		Refill	8

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3. **Design:-**

Design consists of 4 modules and 1 header file for parameters.

- vending_machine_top.v (top module)
  - vending_machine.v (Vending Machine)
  - keypad.v (4x4 keypad)[1][2]
  - Pedge_det.v (Debounceer for 4x4 keypad)
  - binary2bcd.v (convert binary to binary coded decimal for seven segment)
  - define.vh (header file contains parameters related to seven segment display)

i. Top Module:-

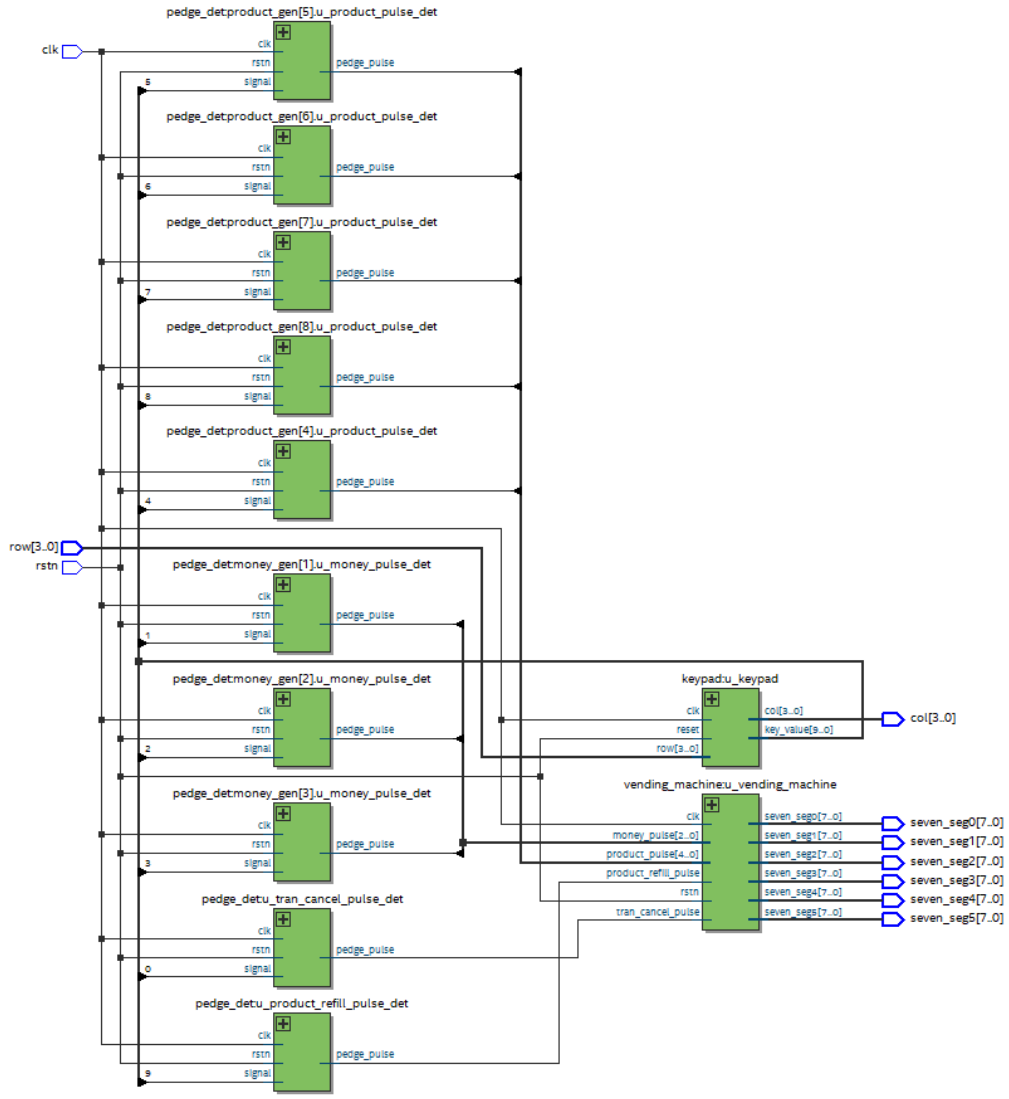

Figure 3. RTL schematic of top module

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ii. Sub Modules:-

A. vending Machine:-

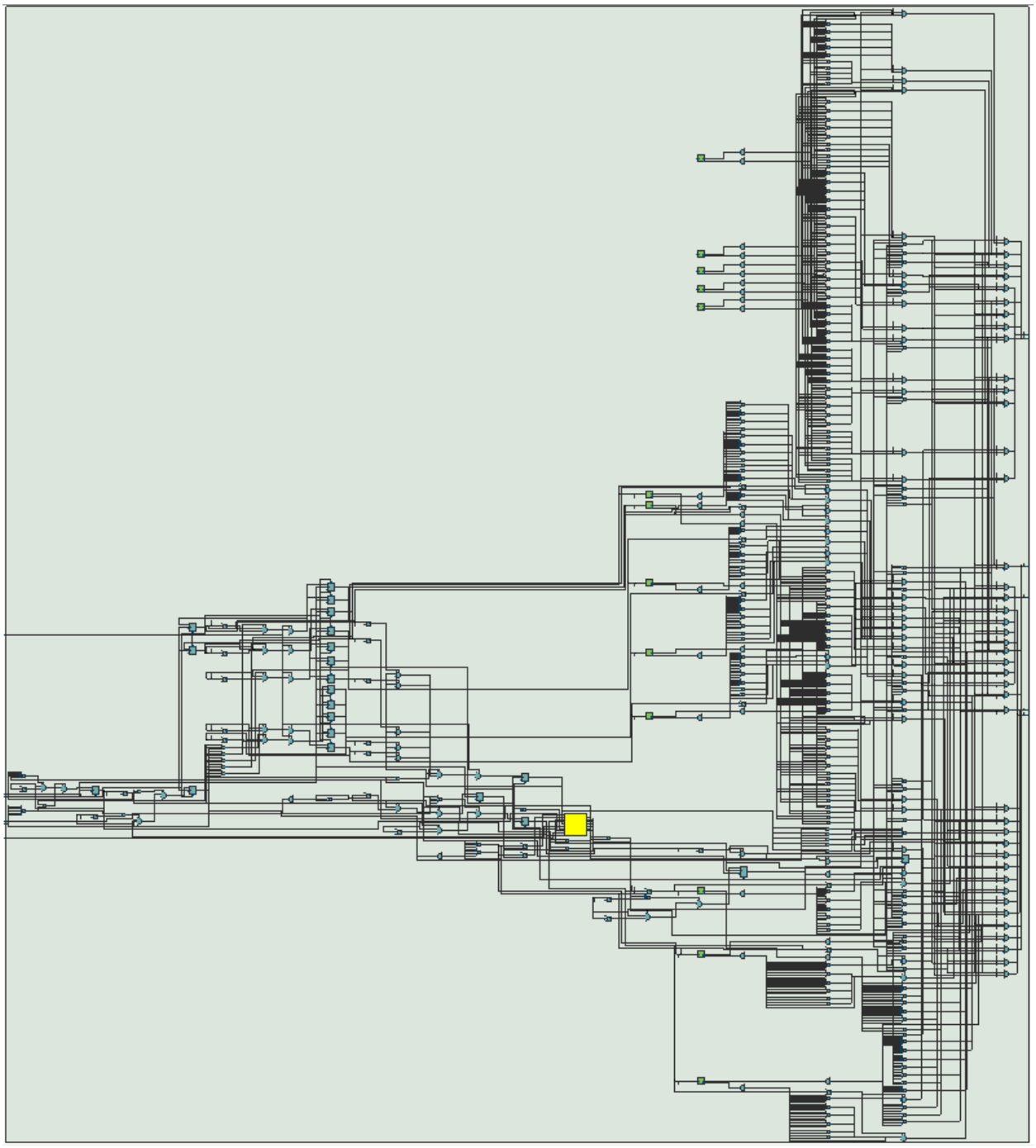

Figure 4. RTL Schematic of vending Machine

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B. keypad:-

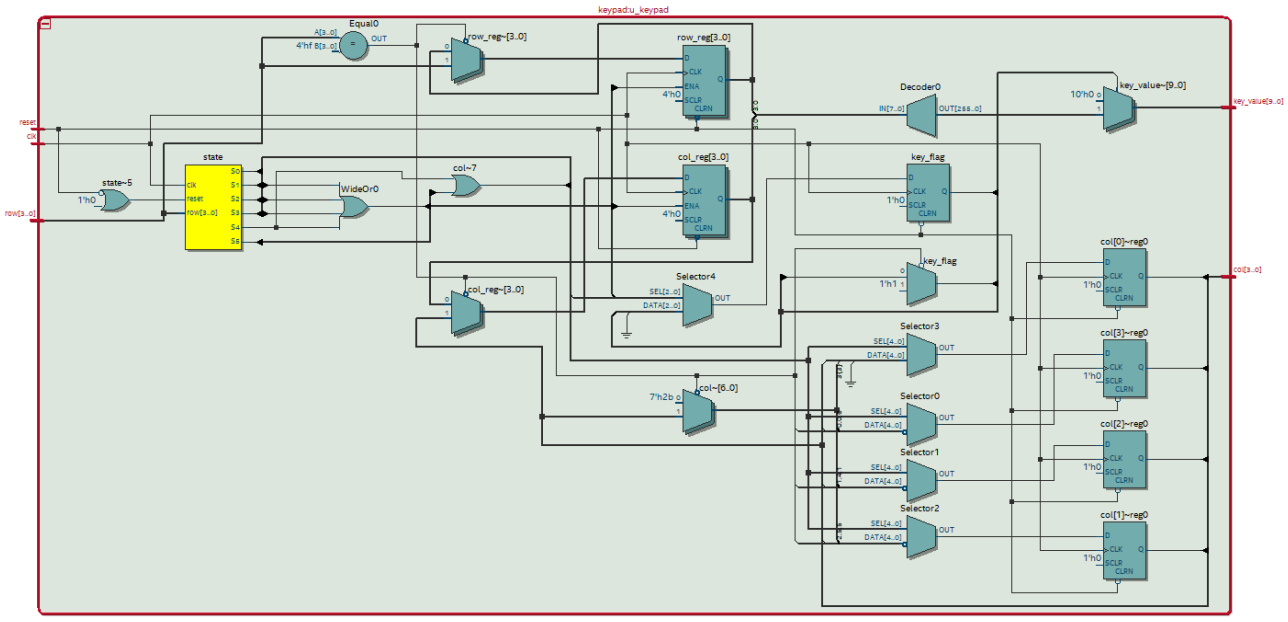

Figure 5. RTL Schematic of 4x4 keypad

C. pedge_det:-

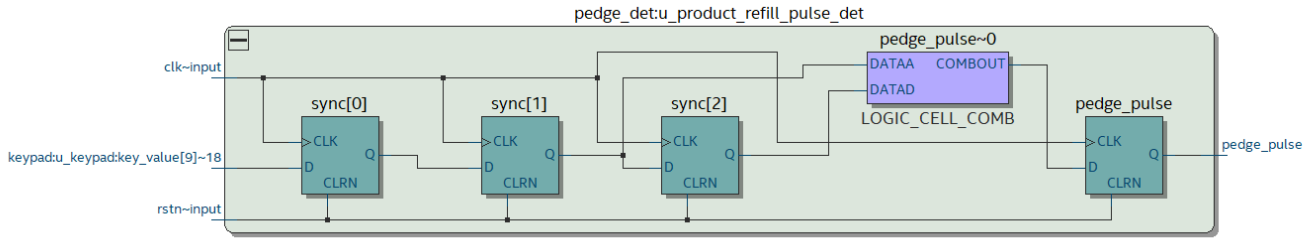

Figure 6. RTL Schematic of debouncer

D. binary2bcd:-

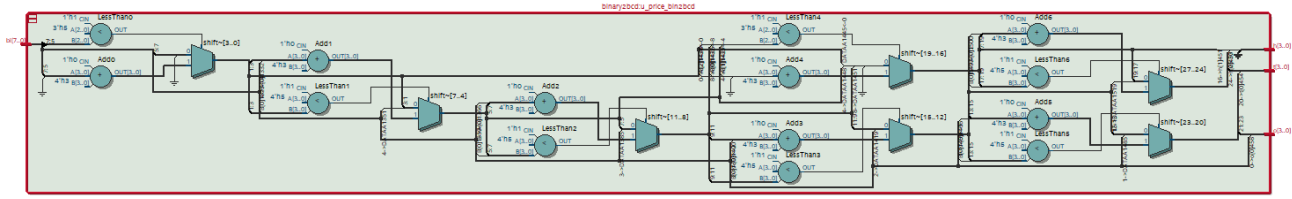

Figure 7. RTL Schematic of binary to BCD converter

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4. FPGA Synthesis Report:-

- The reports shown below are generated by Quartus Prime Lite 18.1 tool which summarized how much amount of the FPGA resources have been used to synthesis this vending machine design.

	Resource	Usage
1	Estimated Total logic elements	489
2		
3	Total combinational functions	461
4	Logic element usage by number of LUT inputs	
1	-- 4 input functions	299
2	-- 3 input functions	55
3	-- <=2 input functions	107
5		
6	Logic elements by mode	
1	-- normal mode	397
2	-- arithmetic mode	64
7		
8	Total registers	163
1	-- Dedicated logic registers	163
2	-- I/O registers	0
9		
10	I/O pins	58
11		
12	Embedded Multiplier 9-bit elements	0
13		
14	Maximum fan-out node	clk~input
15	Maximum fan-out	163
16	Total fan-out	2275
17	Average fan-out	3.07

Figure 8. Analysis and Resource Usage Report

	Compilation Hierarchy Node	Combinational ALUTs	Dedicated Logic Registers	Memory Bits	UFM Blocks
1	|vending_machine_top	461 (0)	163 (0)	0	0
1	|keypad:u_keypad|	40 (40)	19 (19)	0	0
2	|pedge_det:money_gen[1].u_money_pulse_det|	1 (1)	4 (4)	0	0
3	|pedge_det:money_gen[2].u_money_pulse_det|	1 (1)	4 (4)	0	0
4	|pedge_det:money_gen[3].u_money_pulse_det|	1 (1)	4 (4)	0	0
5	|pedge_det:product_gen[4].u_product_pulse_det|	1 (1)	4 (4)	0	0
6	|pedge_det:product_gen[5].u_product_pulse_det|	1 (1)	4 (4)	0	0
7	|pedge_det:product_gen[6].u_product_pulse_det|	1 (1)	4 (4)	0	0
8	|pedge_det:product_gen[7].u_product_pulse_det|	1 (1)	4 (4)	0	0
9	|pedge_det:product_gen[8].u_product_pulse_det|	1 (1)	4 (4)	0	0
10	|pedge_det:u_product_refill_pulse_det|	1 (1)	4 (4)	0	0
11	|pedge_det:u_tran_cancel_pulse_det|	1 (1)	4 (4)	0	0
12	|vending_machine:u_vending_machine|	411 (399)	104 (104)	0	0

Figure 9. Resource Utilization by Each Module

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	Type	Count
1	boundary_port	58
2	cycloneiii_ff	163
1	CLR	88
2	CLR SCLR	6
3	ENA CLR	34
4	ENA CLR SCLR	35
3	cycloneiii_lcell_comb	464
1	arith	64
1	2 data inputs	56
2	3 data inputs	8
2	normal	400
1	0 data inputs	1
2	1 data inputs	5
3	2 data inputs	48
4	3 data inputs	47
5	4 data inputs	299
4		
5	Max LUT depth	7.40
6	Average LUT depth	3.90

Figure 10. Post Synthesis Netlist Statistics

Flow Status	Successful - Sun Dec 08 13:08:24 2019
Quartus Prime Version	18.1.1 Build 646 04/11/2019 SJ Lite Edition
Revision Name	vending_machine_top
Top-level Entity Name	vending_machine_top
Family	MAX 10
Device	10M50DAF484C7G
Timing Models	Final
Total logic elements	482 / 49,760 (< 1 %)
Total registers	163
Total pins	58 / 360 (16 %)
Total virtual pins	0
Total memory bits	0 / 1,677,312 (0 %)
Embedded Multiplier 9-bit elements	0 / 288 (0 %)
Total PLLs	0 / 4 (0 %)
UFM blocks	0 / 1 (0 %)
ADC blocks	0 / 2 (0 %)

Figure 11. Resource Utilization Summary

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5. **Timing Report:-**

	Clock	Slack	End Point TNS
1	clk	12.101	0.000

Figure 12. Setup Timing Report

	Clock	Slack	End Point TNS
1	clk	0.342	0.000

Figure 13. Hold Timing Report

Clocks Summary

	Clock Name	Type	Period	Frequency	Rise	Fall
1	clk	Base	20.000	50.0 MHz	0.000	10.000

Figure 14. Clock Report

- Max Frequency at which this vending machine will work without any violation is 126.6 Mhz.

	Fmax	Restricted Fmax	Clock Name	Note
1	126.6 MHz	126.6 MHz	clk	

Figure 15. Fmax Report.

- As we can see from the above shown results there are no timing violations in the design.

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6. Testbench Simulation:-

- Following are the testbench simulation for vending machine module.

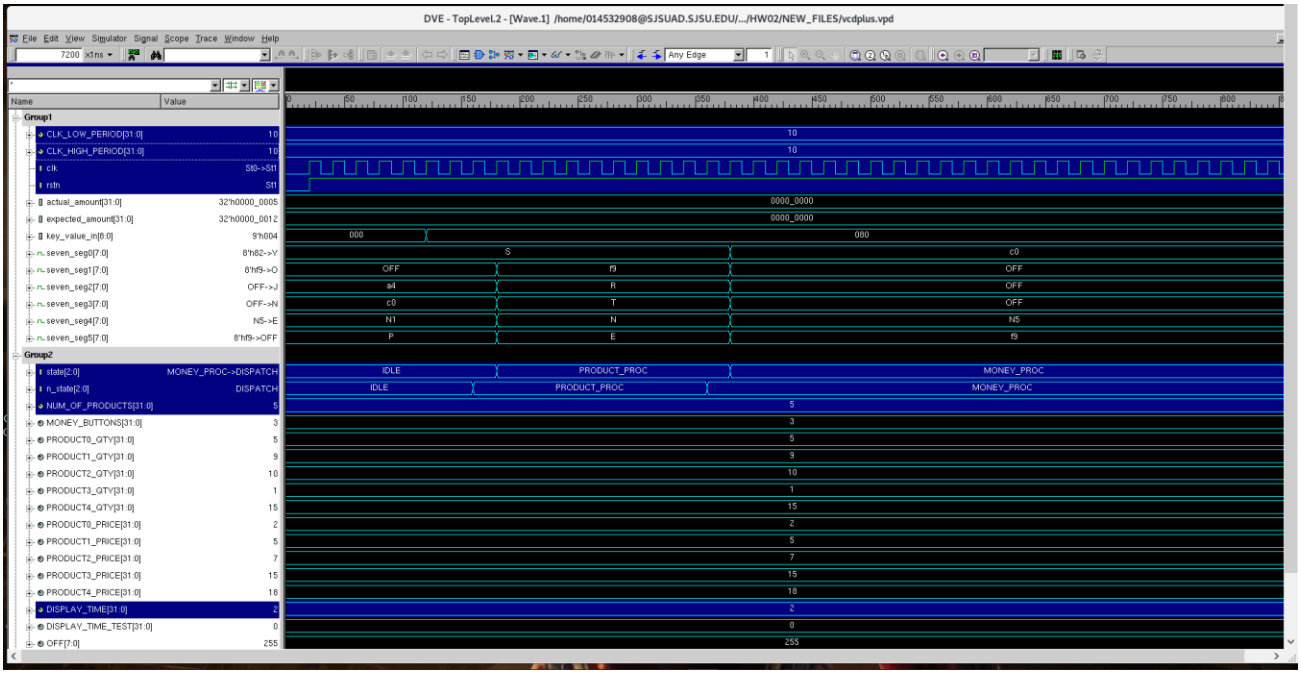

Figure 16. Simulation 1

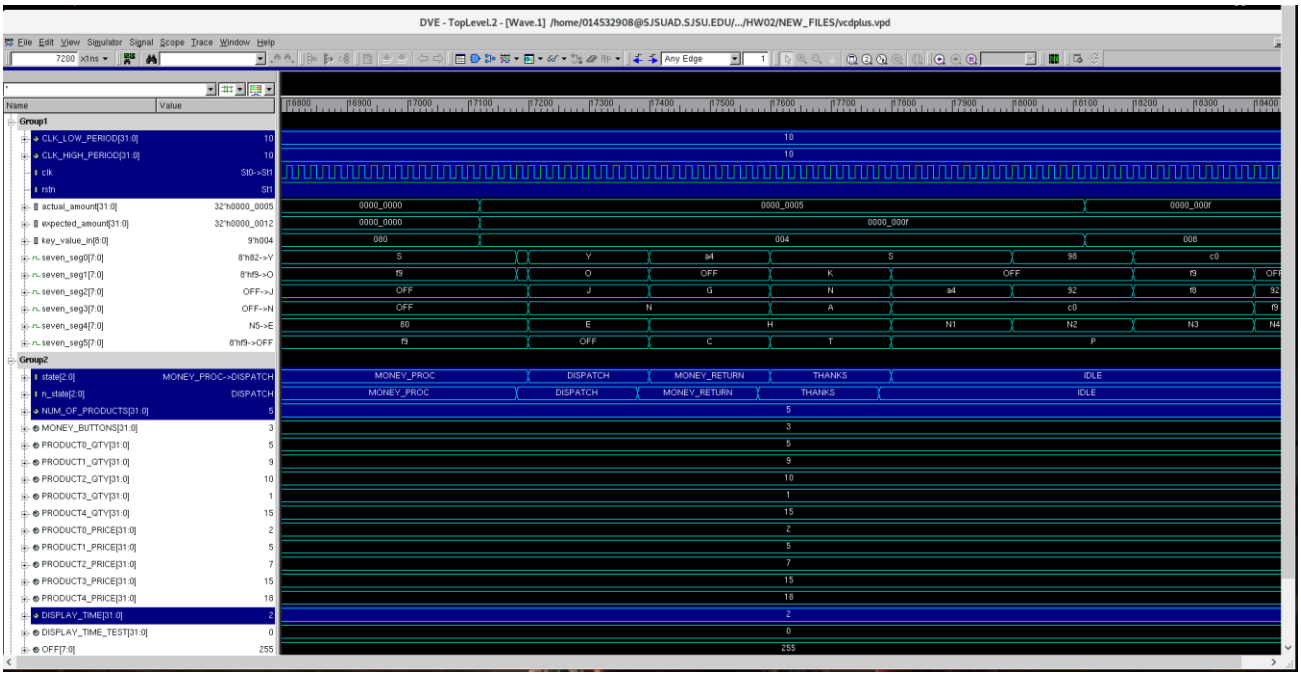

Figure 17. Simulation 2

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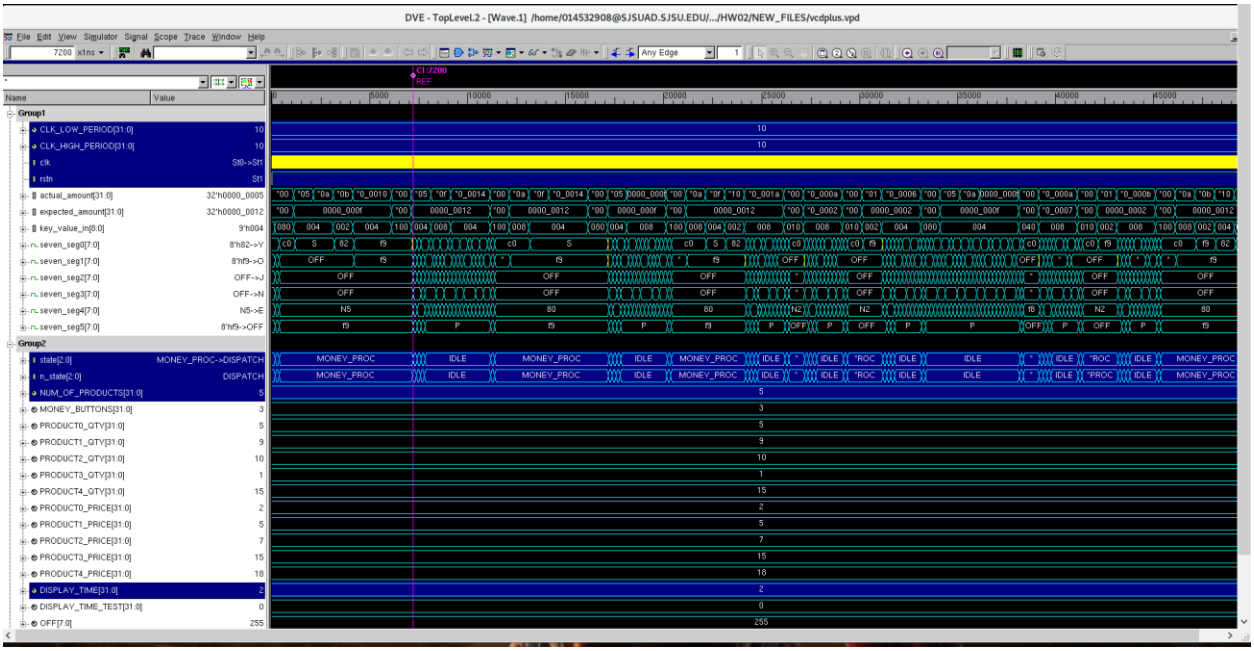

Figure 18. Simulation 3

- Above images are not clearly visible so these images are submitted with project in the Testbench Simulation Folder.

7. **Conclusion:-**

The FPGA based vending machine is been designed and implemented using Quartus Prime Lite 18.1. The designed has been tested on the FPGA board DE-10 Lite Max. This vending machine enhances the capability of the machine due to its modularity as well as scalability in terms of products due to its reprogrammable feature. The design is user friendly as well as its response time is fast. The future scope of this design is to add more functionality such as multi product selection and product refill for individual products as per the owners will.

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8. **Contribution:-**
    - **Architecture designed** of product from scratch.
    - Defined **micro product architecture** which includes **state machine, state defining** and designing of each and every module with precise number of i/o ports and functionality.
    - Designed product features like on-fly transaction cancel, product refill and watchdog timeout if product transaction timed out to avoid deadlock scenario, maintained product stock and check before approving transaction to use, return money if extra added
    - Designed architecture of verification bench to implement and test all features
    - Coded parameterized and auto generation random testbench
    - Designed script to run testbench automatically
    - Designed script for adding state and other variable name in waveform viewer
    - Designed eye catching and very informative display, which can display all the information needed for user, like product stock, price, money given until the time, total money expected, no stock, etc. In the IDLE state, the machine displays the product number, price and stock left in loop of every 2 seconds until user selects a product.
    - RTL coding and interfacing of 4x4 keypad.
    - Configuring 4x4 keypad for product i/p, money i/p and cancel and refill functionality. It is configured in such a way that user if by mistake user will press multiple inputs at a time it will only take the input which was recorded first in the order. It Is also configured in such a way that the buttons which are of no use will never ever affect the vending machine in any state.
    - Designed Binary to BCD converter to display decimal values on seven segment display.
    - Synthesis and implementation of vending machine on FPGA.
    - Timing analysis of the full vending machine using Quartus Prime Lite 18.1 timing analyzer for eg. post synthesis netlist was showing negative slack in setup timing and the clock report was showing the clock frequency as 1000Mhz. In order to fix that a SDC file was created where in clock was given constraint using the following command, ***"create_clock -period 20 {get_ports clk}"***. This means that clock period is set to 20ns (50Mhz).
    - Bug reporting and fixing for eg. user was able to select product when in money input state. Product refill functionality was not working. Few sevensegment display were not configured properly.

Name	Contribution (%)
Rahul Shah	33.33
Pal Nikola	33.33
Dharm Patel	33.33

9. **References:-**

[1] https://www.youtube.com/watch?v=bNOVg9vwFRM&app=desktop

[2] https://github.com/douglaskastle/3S500E/blob/master/verilog/4x4%20Keypad/keyscan.v

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10. **Annexure:-**

Provided report of ---- words shows the details of the micro architecture designed of each and every module. The report demonstrates the unique and eye-catching functionalities added in the vending machine with future scopes to expand the design according to will owners will. Also the product has been formally and fully verified using the testbench to ensure the proper working of the product. Following things are submitted as a part of the project.

1) Report
2) RTL Verilog files
3) QSF pin config file
4) SDC constraint file
5) Testbench verilog files
6) Testbench simulations
7) Vending_machine_full_project_quartus_18.1_lite
8) Vending_machine_full_project_verification
9) Video Link:-
    - https://drive.google.com/open?id=16xlO1H2qevtLNnnyk3OQsibRAtDHOypk

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