AHB-Lite to SPI Bridge using PYNQ – Z2

Project Specification/Limitation Guide

1. Data Transfer Characteristics

- → **Data Width:** 8-bit (byte-wise transmission)
- → **Transfer Direction:** Unidirectional
  - AHB Master → SPI Slave
  - MOSI supported, MISO not used (write-only SPI)
- → **SPI Mode:** Mode 0
  - CPOL = 0 (clock idle low)
  - CPHA = 0 (data sampled on rising edge)

2. Clocking and Timing

- → **AHB Clock (HCLK):** 100 MHz
- → **SPI Clock (SCLK):** 6.25 MHz
  - Derived internally using a **÷16 clock divider**
- → **SPI Bit Order:** MSB first
- → **Chip Select Behavior:**
  - CS asserted low for exactly **8 SPI clock cycles per byte**
  - CS deasserted high between bytes

3. Bus Interface

- → **Bus Standard:** AHB-Lite (Slave Interface)
- → **Addressing:** Word-aligned (32-bit)
- → **Transfer Type:** Single-byte writes routed via FIFO
- → **Wait-State Handling:**
  - HREADY deasserted when FIFO is full
  - Ensures safe back-pressure to AHB master

4. Memory-Mapped Interface

→ **MMIO Base Address:** `0x4000_0000`

→ **Register Map:**

Register	Offset	Purpose
TX FIFO	`0x00`	Write SPI data byte
DC	`0x08`	Data / Command control
FLAGS	`0x0C`	`{…, dc, fifo_full, fifo_empty}`
TX_CNT	`0x10`	Total number of transmitted bytes
FSM	`0x14`	SPI FSM debug state
RESET	`0x18`	SPI slave reset control

5. FIFO Buffer

→ **Type:** Single-clock FIFO

→ **Width:** 8 bits

→ **Depth:** 16 bytes

→ **Purpose:**

- Decouples AHB writes from SPI timing
- Enables smooth byte-streaming without stalling the bus

6. Control and Debug Features

→ **DC Signal:**

- Supports command/data distinction for display controllers

→ **RESET Signal:**

- Software-controlled SPI slave reset

→ **TX Counter:**

- Allows software-side verification of transmitted bytes

→ **FSM Debug Register:**

- Exposes internal SPI FSM state for validation

7. Validation and Testing

- → **Software Interface:**
  - Python MMIO access via Jupyter Notebook (PYNQ)
- → **Hardware Observation:**
  - DSO used to verify:
    - SPI Clock frequency
    - MOSI data patterns
    - CS timing
    - DC and RESET behavior
- → **Verified Conditions:**
  - Correct 8-bit shifting
  - Accurate clock division
  - Deterministic FSM operation

8. Design Scope and Limitations

- → Supports **only SPI write operations**
- → No MISO sampling (no read / full-duplex support)
- → No DMA or burst aggregation

9. Application Target

- → OLED displays
- → General-purpose SPI write-only peripherals
- → Embedded systems requiring simple, deterministic SPI control