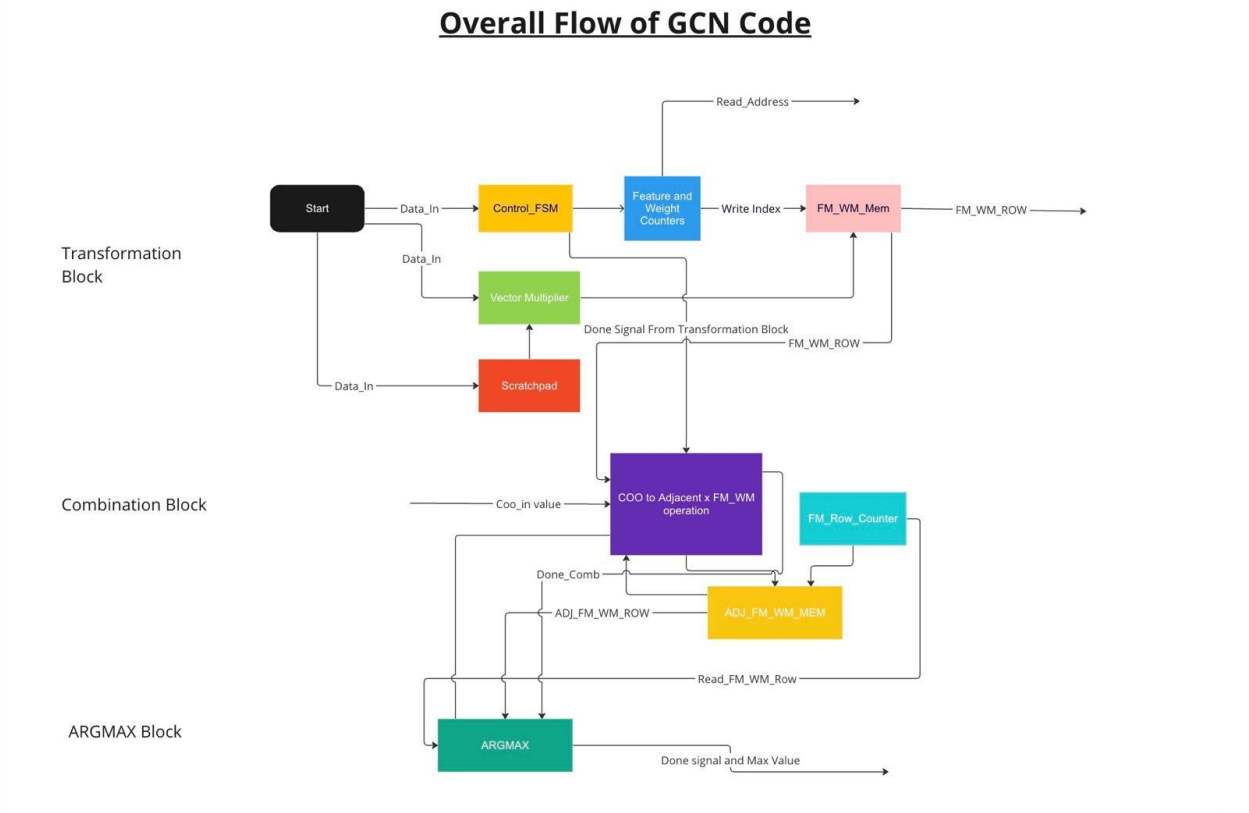
Architecture and High Level Block Diagram:



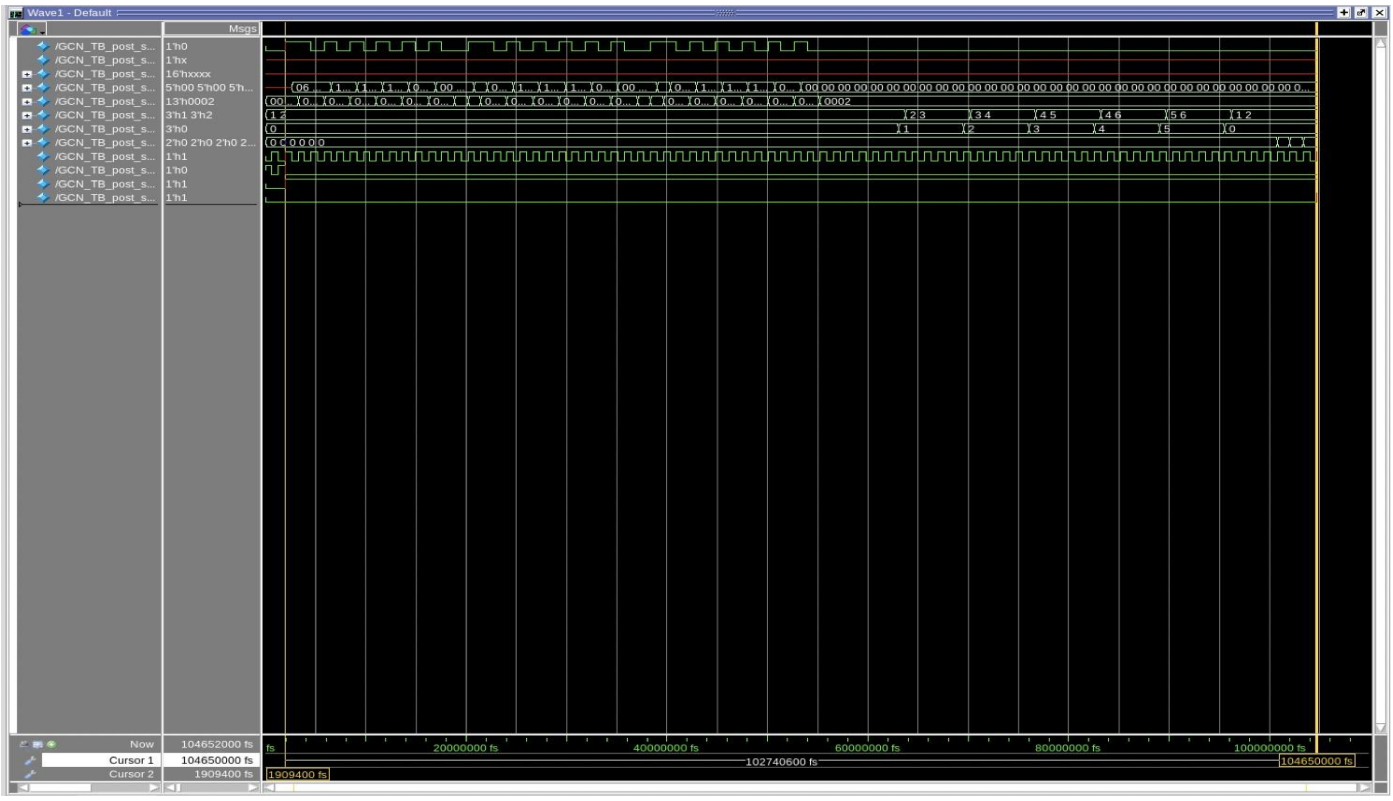
Design Decisions:

The Transformation Module performs matrix multiplication using combinational logic for memory reading and a vector multiplier for weight and feature multiplication. Its FSM initiates from Start, reads weights and features in cycles, multiplies them, and completes after 6 cycles.

The Combination Module indirectly computes FW matrix and Adj matrix multiplication by adding rows. Its FSM controls row addition from FW matrix memory to a zero-initialized combination memory block. It iterates through cycles based on edge numbers, managing memory write signals for row addition.

The Argmax Module ensures uniformity across blocks by using an FSM, Memory, and Comparator. It reads rows from the Combination Block's memory, identifies the index of the maximum value in a row, and progresses sequentially through states from Start to indicate the output/result.

Total latency:

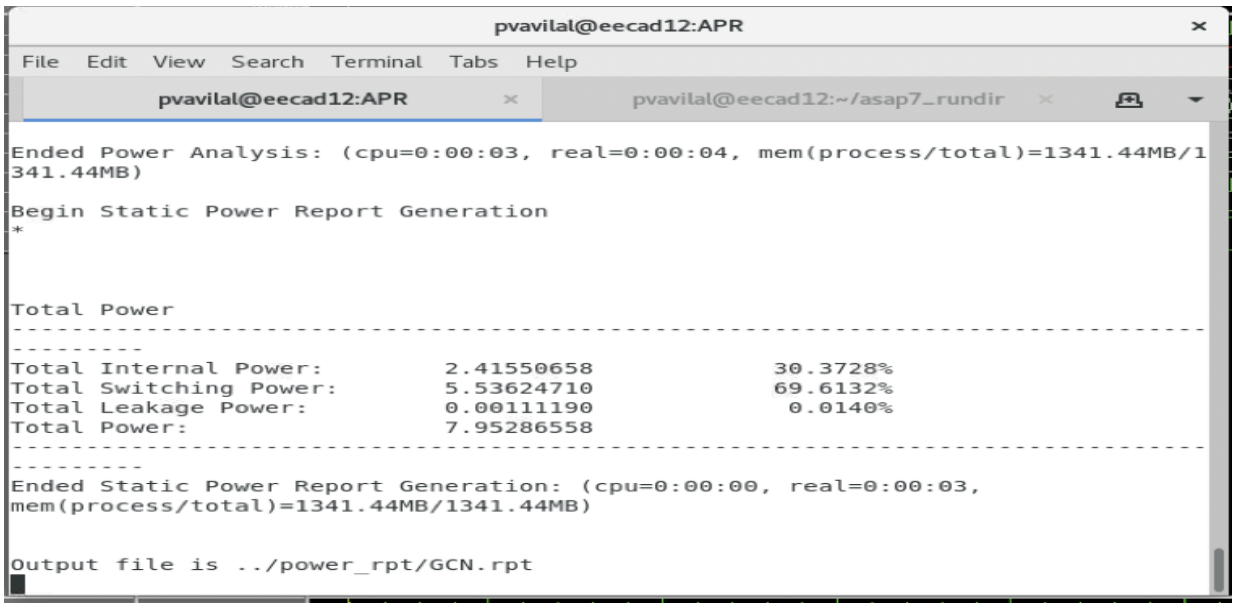


Latency: 104650000 fs - 1909400 fs

= 0.00010465 ms - 0.0000019094 ms

= 0.0001027406 ms

Power:



Area:

```
% Pure Gate Density #1 (Subtracting BLOCKAGES): 99.966%
% Pure Gate Density #2 (Subtracting BLOCKAGES and Physical Cells): 48.414%
% Pure Gate Density #3 (Subtracting MACROS): 99.966%
% Pure Gate Density #4 (Subtracting MACROS and Physical Cells): 48.414%
% Pure Gate Density #5 (Subtracting MACROS and BLOCKAGES): 99.966%
% Pure Gate Density #6 (Subtracting MACROS and BLOCKAGES for insts are not placed): 48.414%
% Core Density (Counting Std Cells and MACROs): 99.966%
% Core Density #2(Subtracting Physical Cells): 48.414%
% Chip Density (Counting Std Cells and MACROs and IOs): 91.039%
% Chip Density #2(Subtracting Physical Cells): 44.091%
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Total area of Standard cells: 44625.298 um^2
Total area of Standard cells(Subtracting Physical Cells): 21612.226 um^2
Total area of Macros: 0.000 um^2
Total area of Blockages: 0.000 um^2
Total area of Pad cells: 0.000 um^2
Total area of Core: 44640.461 um^2
Total area of Chip: 49017.540 um^2
Effective Utilization: 1.0000e+00
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Area = area of chip x Gate density
= 49.01754 mm^2 x 48.414
= 2372.88 mm^2

Innovus density: 0.48

Number of gates:
Gate area 0.6998 um^2
[0] GCN Gates=30881 Cells=10835 Area=21612.2 um^2