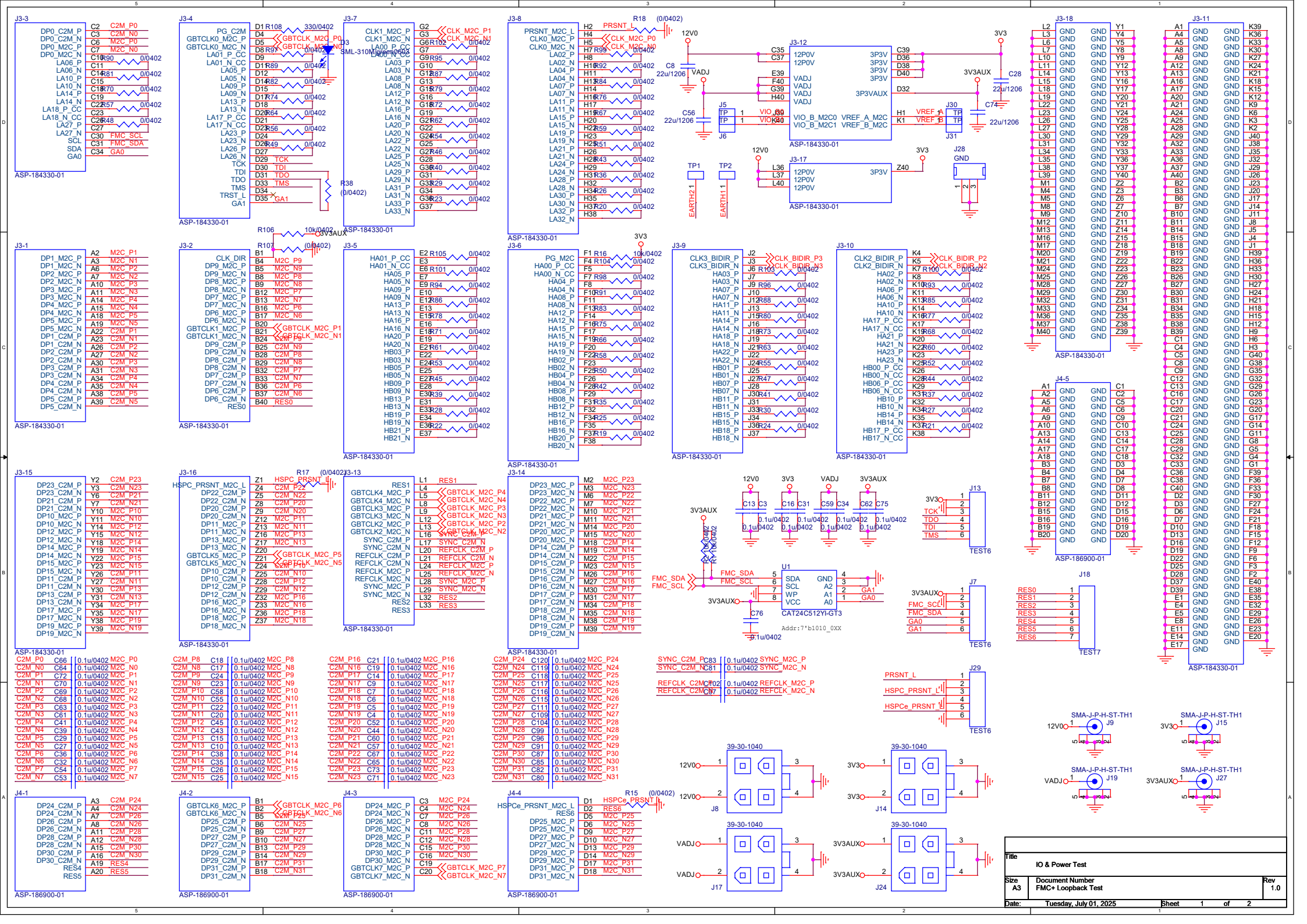
J3-3
ASP-184330-01
J3-4
ASP-184330-01
J3-7
ASP-184330-01
J3-8
ASP-184330-01
J3-12
ASP-184330-01
J3-18
ASP-184330-01
J3-11
ASP-184330-01
J3-1
ASP-184330-01
J3-2
ASP-184330-01
J3-5
ASP-184330-01
J3-6
ASP-184330-01
J3-9
ASP-184330-01
J3-10
ASP-184330-01
J4-5
ASP-186900-01
J3-15
ASP-184330-01
J3-16
ASP-184330-01
J3-13
ASP-184330-01
J3-14
ASP-184330-01
U1
CAT24C512YI-GT3
J7
TEST6
J13
TEST6
J18
TEST7
J29
TEST6
J4-1
ASP-186900-01
J4-2
ASP-186900-01
J4-3
ASP-186900-01
J4-4
ASP-186900-01
39-30-1040
J8
39-30-1040
J14
39-30-1040
J17
39-30-1040
J24
SMA-J-P-H-ST-TH1
J9
SMA-J-P-H-ST-TH1
J15
SMA-J-P-H-ST-TH1
J19
SMA-J-P-H-ST-TH1
J27
Title
IO & Power Test
Size
A3
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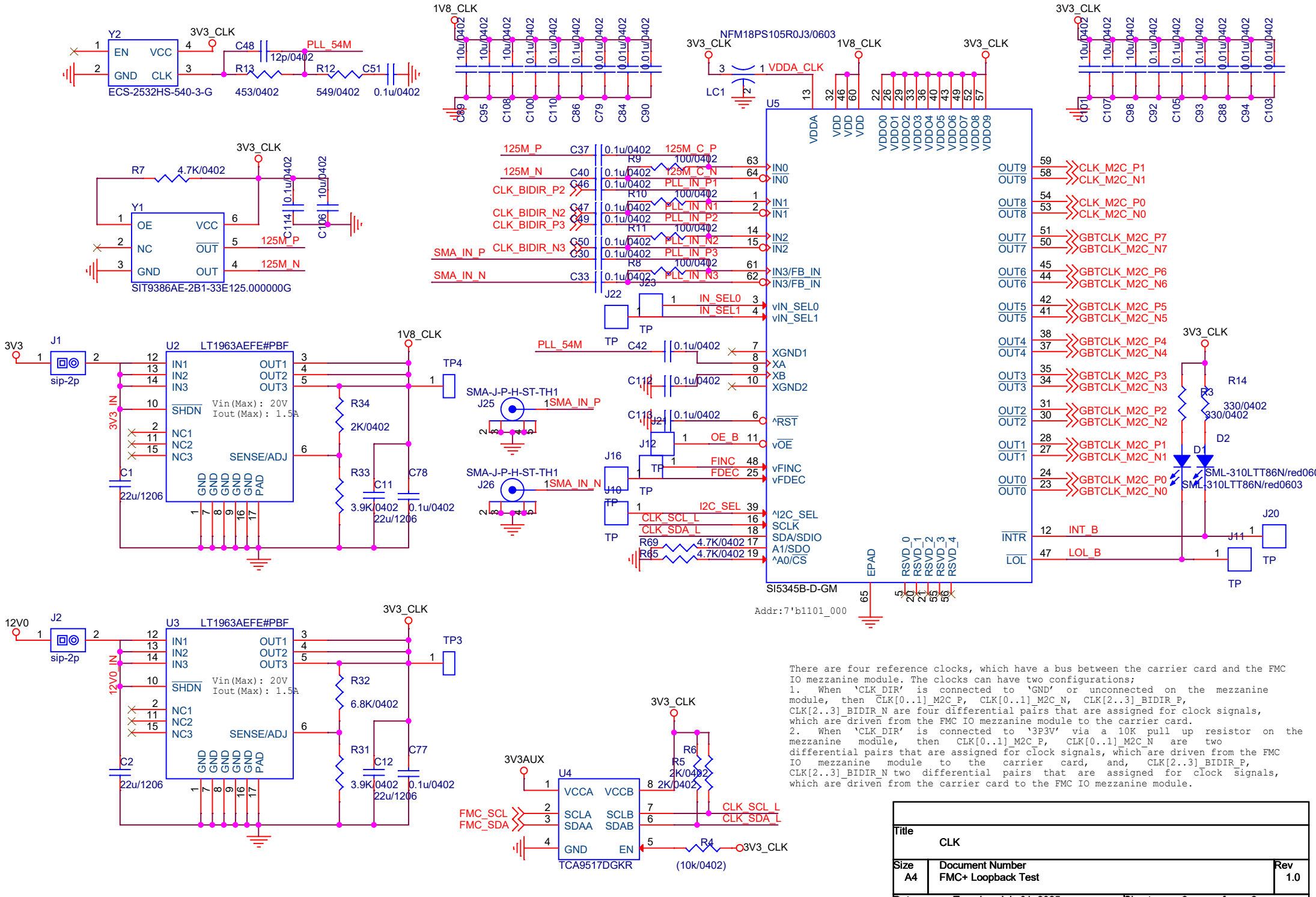
Y2
ECS-2532HS-540-3-G
3V3_CLK
C48
12p/0402
PLL_54M
R13
453/0402
R12
549/0402
C51
0.1u/0402
1V8_CLK
NFM18PS105R0J3/0603
LC1
VDDA_CLK
3V3_CLK
U5
SI5345B-D-GM
Addr:7'b1101_000
Y1
SIT9386AE-2B1-33E125.000000G
R7
4.7K/0402
125M_P
125M_N
125M_C_P
125M_C_N
PLL_IN_P1
PLL_IN_N1
PLL_IN_P2
PLL_IN_N2
PLL_IN_P3
PLL_IN_N3
CLK_BIDIR_P2
CLK_BIDIR_N2
CLK_BIDIR_P3
CLK_BIDIR_N3
SMA_IN_P
SMA_IN_N
IN_SEL0
IN_SEL1
PLL_54M
OE_B
FINC
FDEC
I2C_SEL
CLK_SCL_L
CLK_SDA_L
INT_B
LOL_B
J1
sip-2p
U2
LT1963AEFE#PBF
Vin(Max): 20V
Iout(Max): 1.5A
R34
2K/0402
R33
3.9K/0402
C11
22u/1206
C78
0.1u/0402
C1
TP4
SMA-J-P-H-ST-TH1
J25
J26
J12
J16
J10
J20
J11
R14
R3
330/0402
D1
D2
SML-310LTT86N/red0603
J2
U3
TP3
R32
6.8K/0402
R31
C12
C77
C2
U4
TCA9517DGKR
3V3AUX
FMC_SCL
FMC_SDA
R6
R5
2K/0402
R4
(10k/0402)
There are four reference clocks, which have a bus between the carrier card and the FMC IO mezzanine module. The clocks can have two configurations;
1. When 'CLK_DIR' is connected to 'GND' or unconnected on the mezzanine module, then CLK[0..1]_M2C_P, CLK[0..1]_M2C_N, CLK[2..3]_BIDIR_P, CLK[2..3]_BIDIR_N are four differential pairs that are assigned for clock signals, which are driven from the FMC IO mezzanine module to the carrier card.
2. When 'CLK_DIR' is connected to '3P3V' via a 10K pull up resistor on the mezzanine module, then CLK[0..1]_M2C_P, CLK[0..1]_M2C_N are two differential pairs that are assigned for clock signals, which are driven from the FMC IO mezzanine module to the carrier card, and, CLK[2..3]_BIDIR_P, CLK[2..3]_BIDIR_N two differential pairs that are assigned for clock signals, which are driven from the carrier card to the FMC IO mezzanine module.
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CLK
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A4
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