

FMC2

FPGA

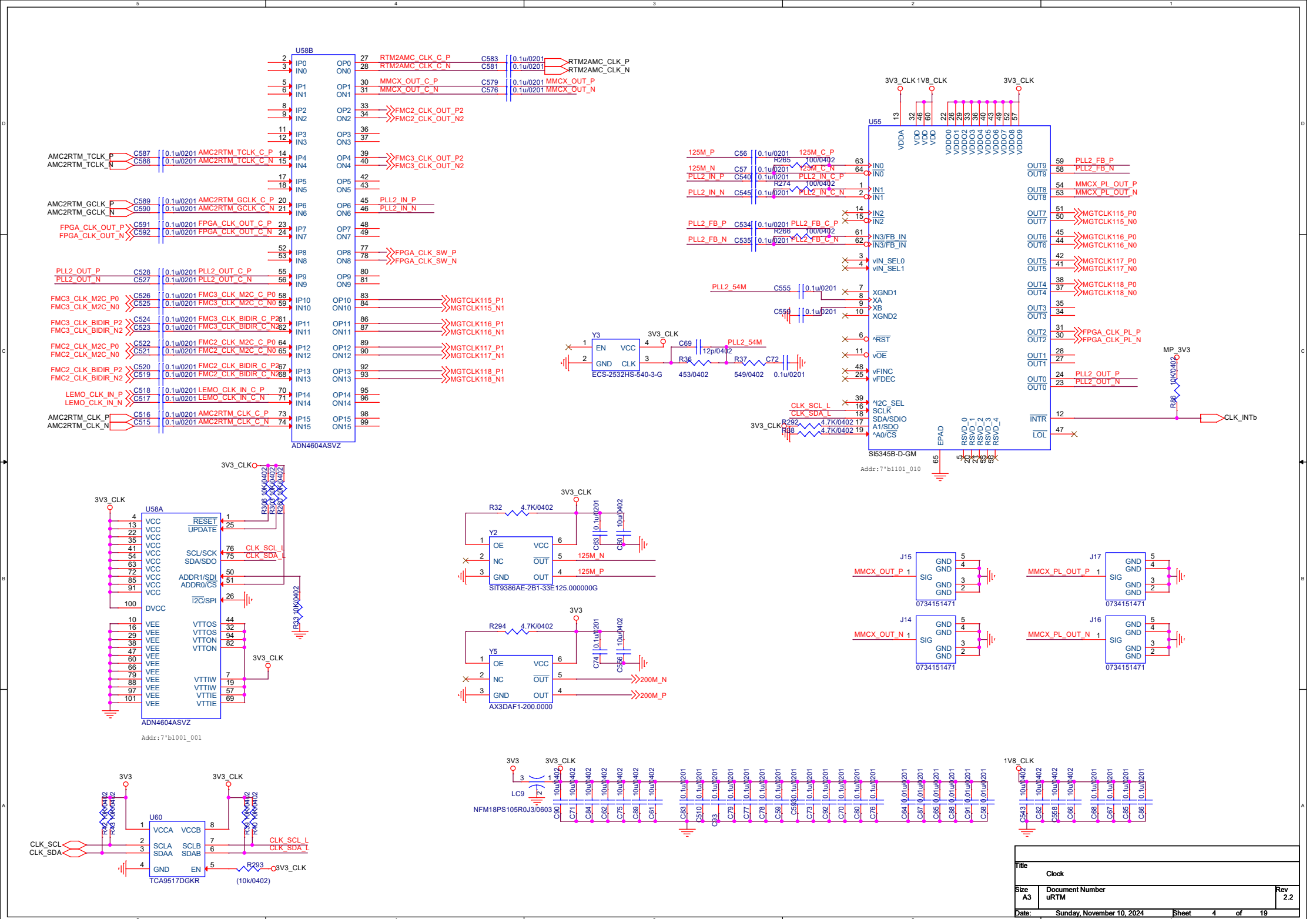
RTM

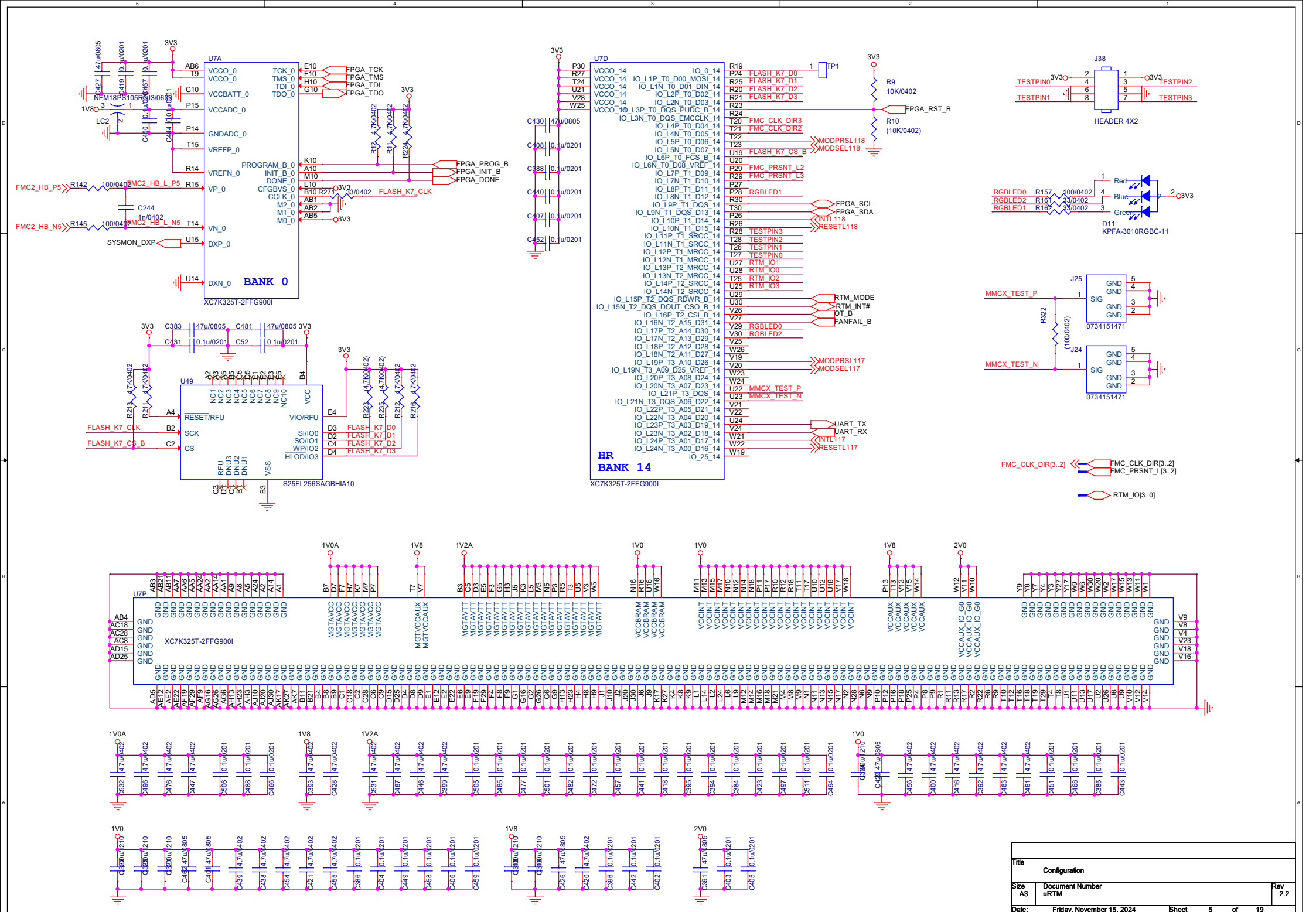
ReDri

FMC3

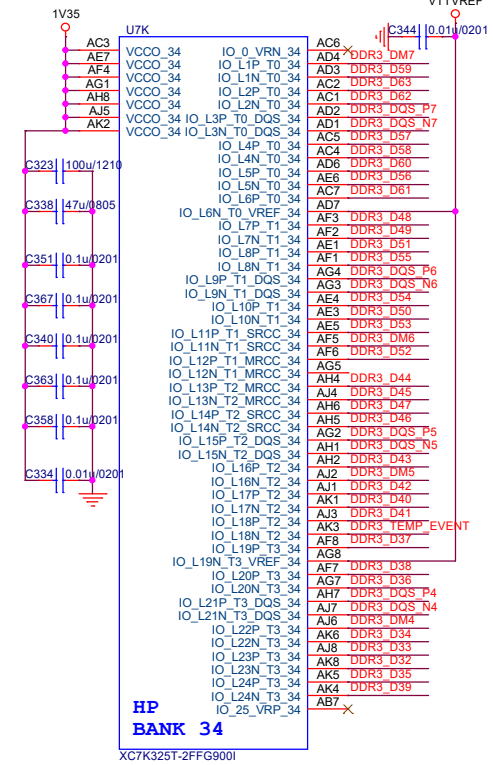
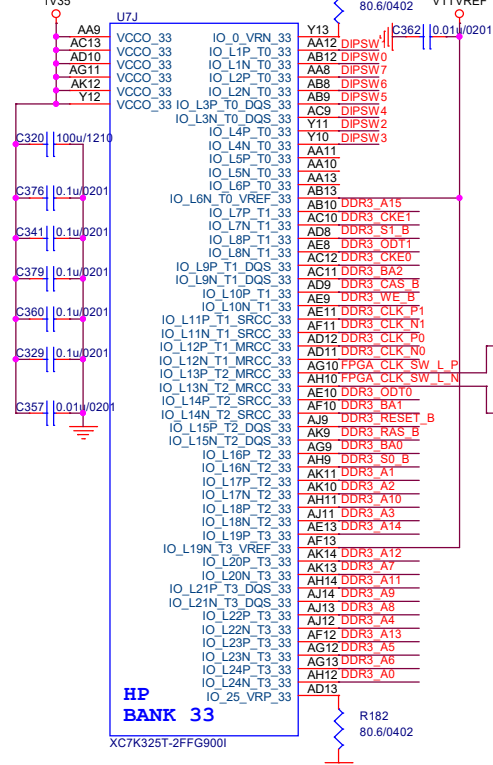
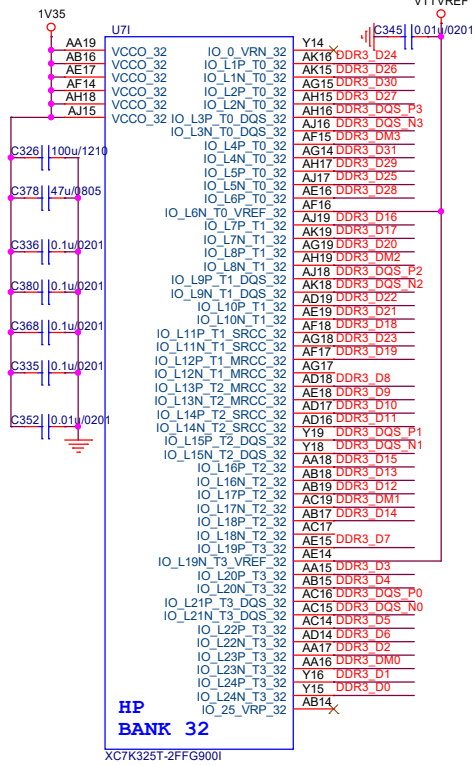
POWER

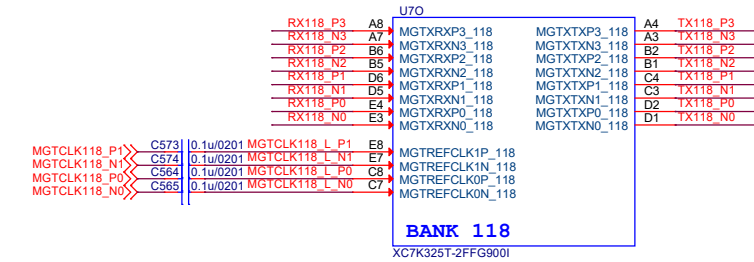
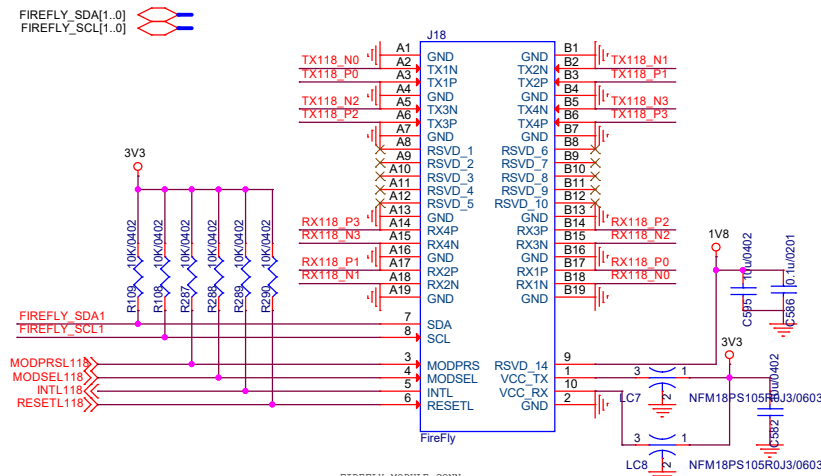
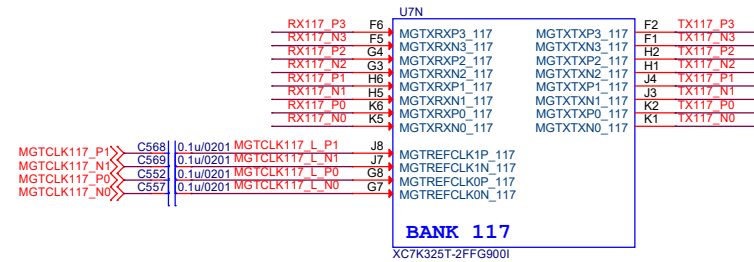
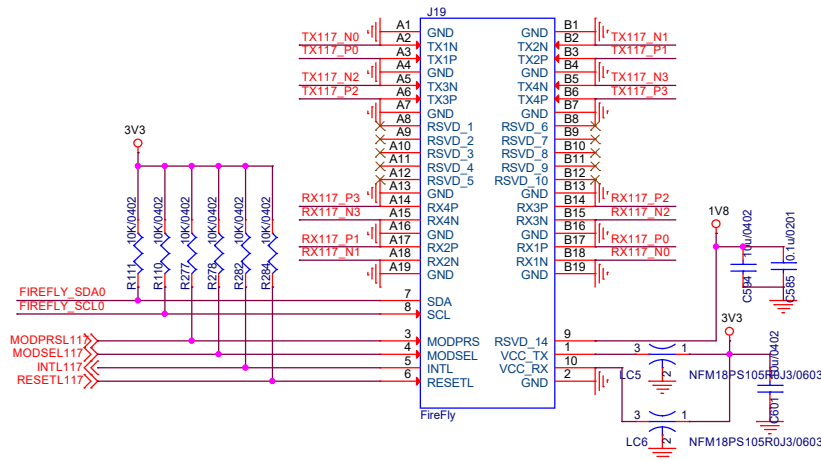
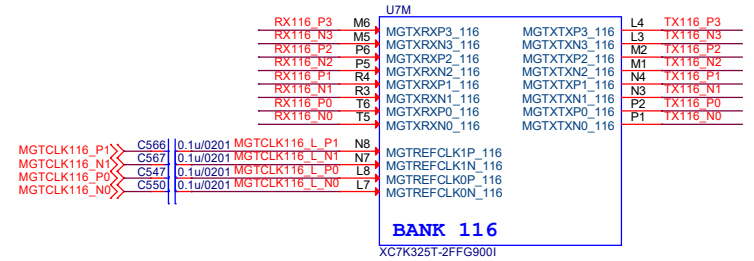
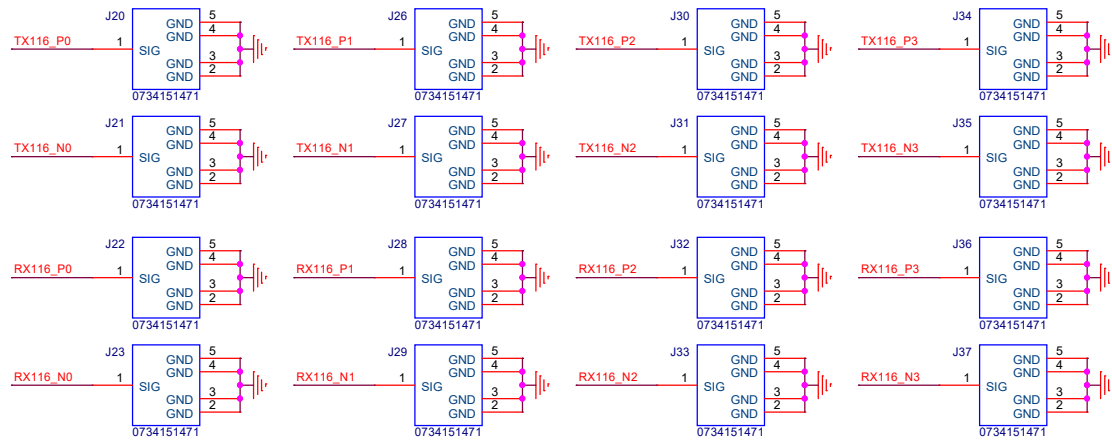
Title			
TOP			
Size	Document Number		Rev
A3	uRTM		2.2
Date:	Sunday, November 10, 2024	Sheet	1 of 19





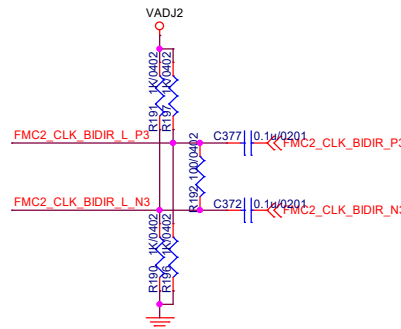
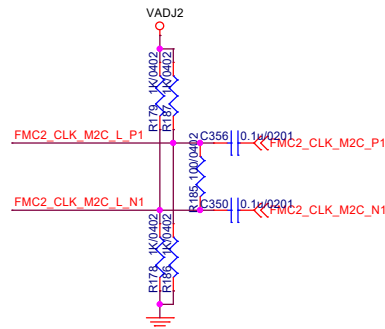
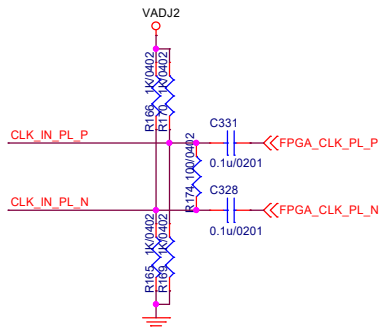
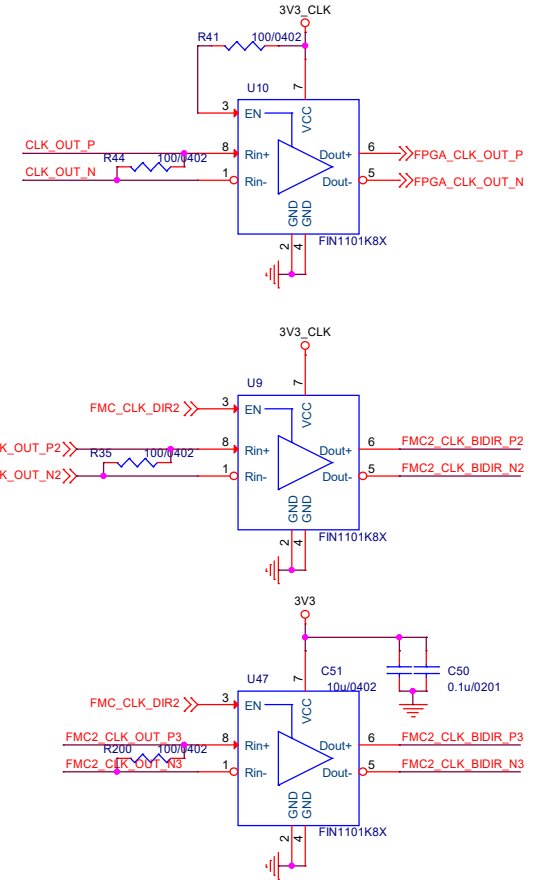
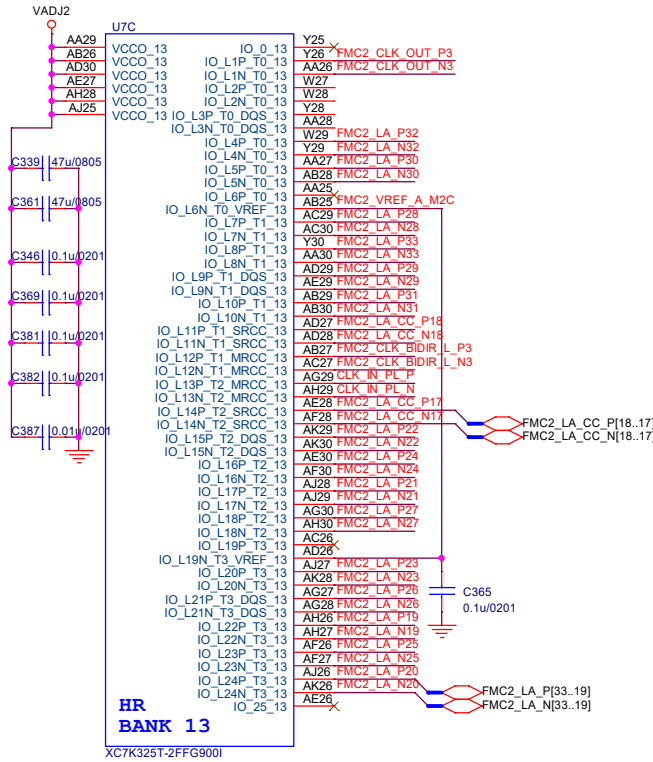
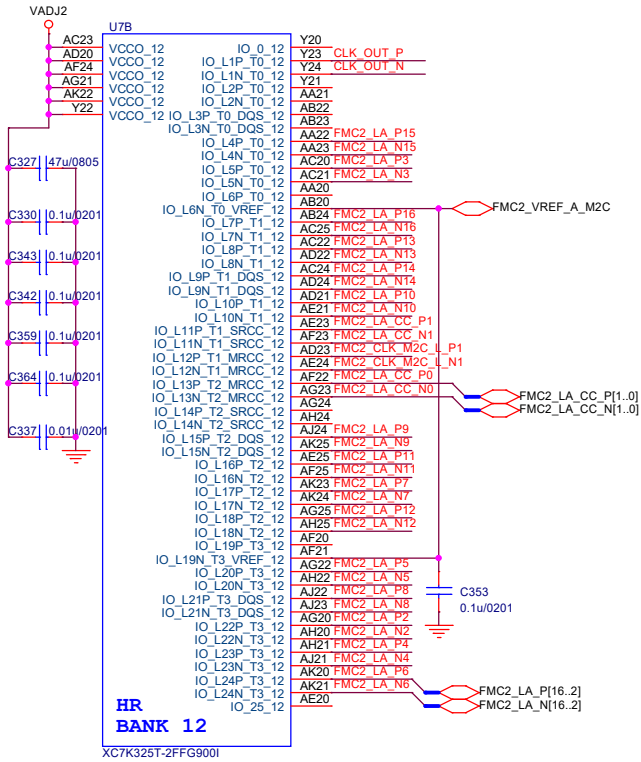
Title				
Configuration				
Size	Document Number			Rev
A3	uRTM			2.2
Date:	Friday, November 15, 2024		Sheet 5 of 19	





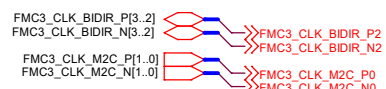
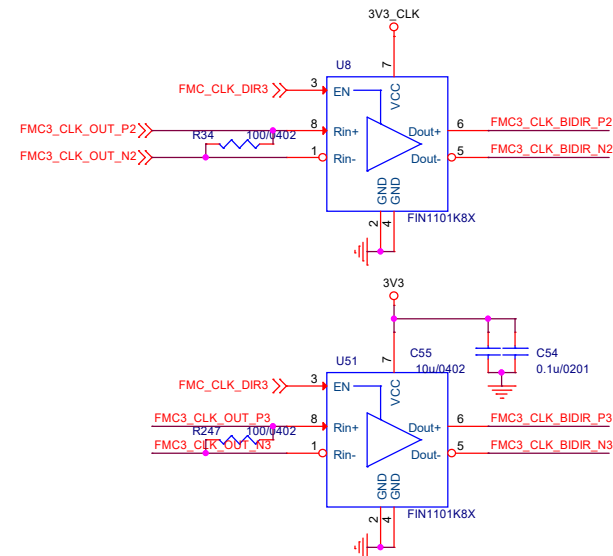
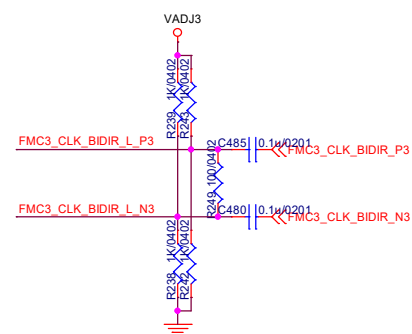
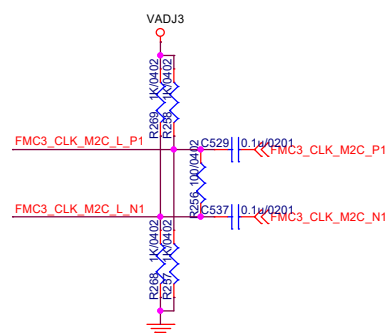
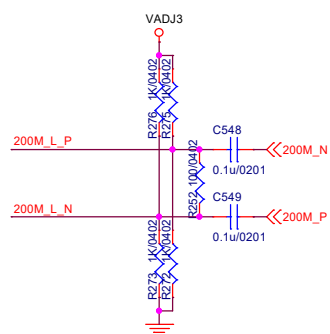
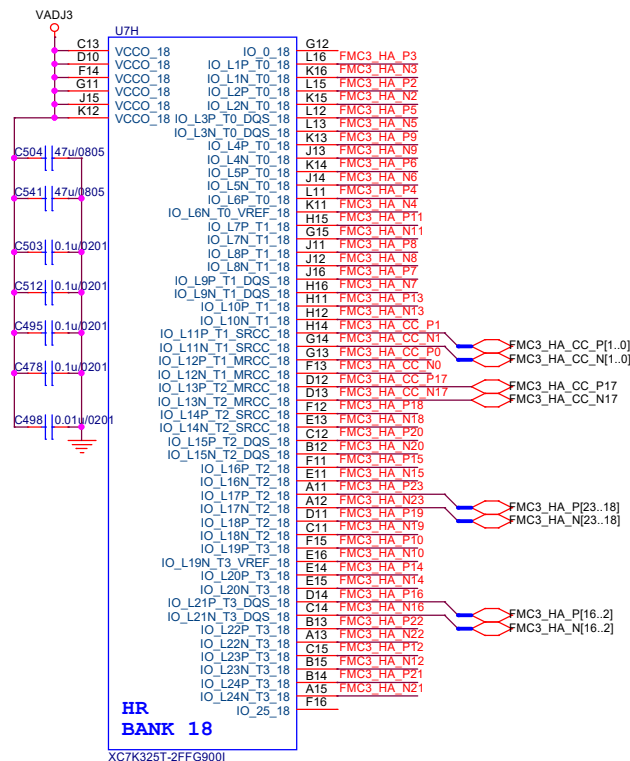
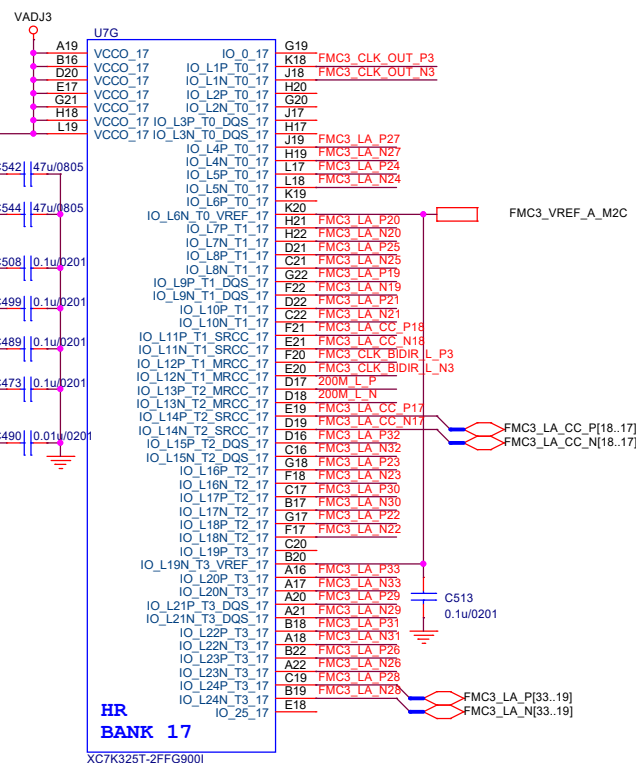
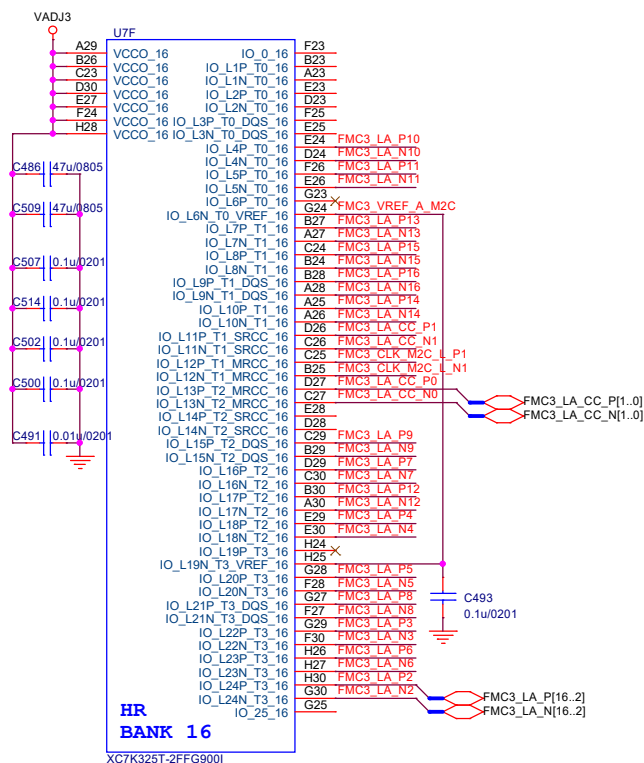
FIREFLY MODULE CONN.
High Speed Signal Connector: UEC5-019-2-H-D-RA-1
Power Connector: UCC8-010-1-H-8-1-A

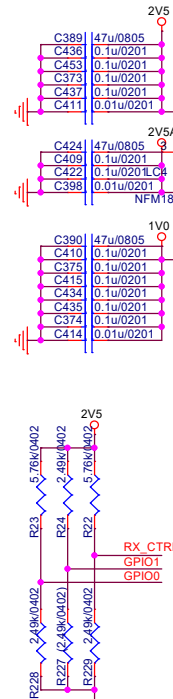
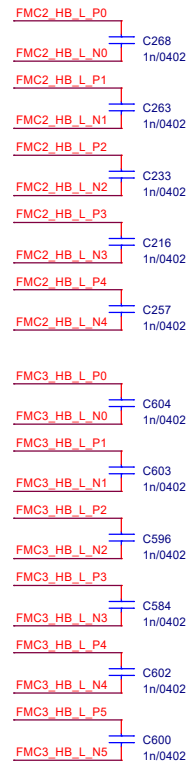
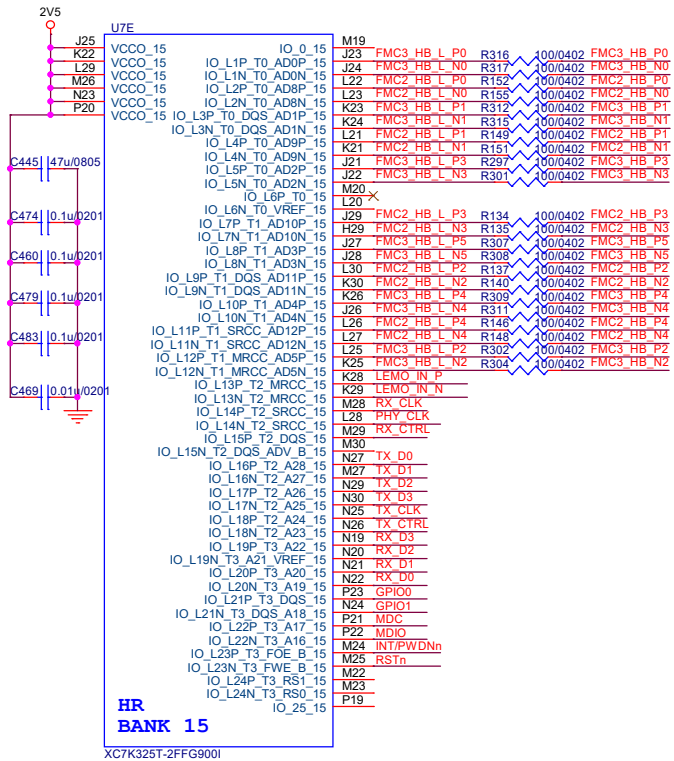
Title			FireFly
Size	Document Number	Rev	
A3	uRTM	2.2	
Date:	Friday, November 15, 2024	Sheet	7 of 19



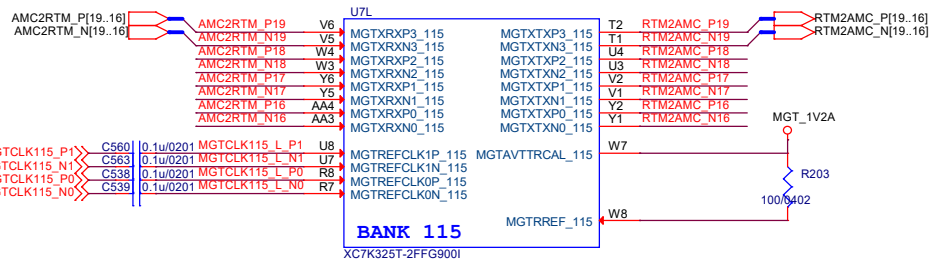
FMC2_CLK_BIDIR_P[3..2]
FMC2_CLK_BIDIR_N[3..2] >> FMC2_CLK_BIDIR_P2
FMC2_CLK_BIDIR_N2
FMC2_CLK_M2C_P[1..0]
FMC2_CLK_M2C_N[1..0] >> FMC2_CLK_M2C_P0
FMC2_CLK_M2C_N0

Title		
FMC2		
Size	Document Number	Rev
A3	uRTM	2.2
Date:	Sunday, November 10, 2024	Sheet 8 of 19



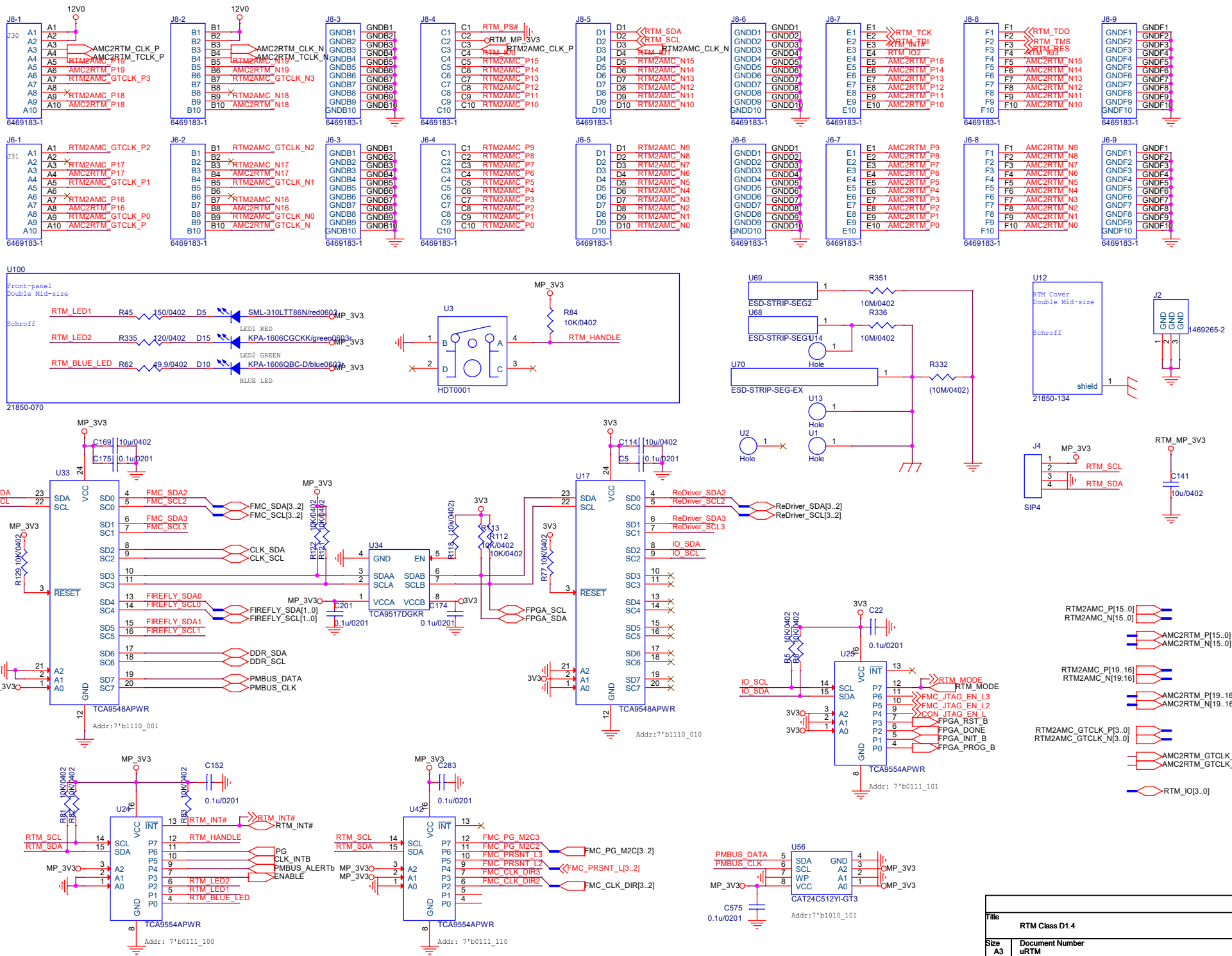


PHY_ADD = 0x0
Auto-negotiation Enable
RGMII Clock Skew TX = 2.5ns
RGMII Clock Skew RX = 2.5ns
SPEED_SEL = 100/1000
Mirror disable
SGMII disable



Trace length from the resistor pins to the
FPGA pins MGTREF and MGTAVTRCAL
must be equal in length.
from: UG476 p.303

Title			
Ethernet			
Size		Document Number	
A3		uRTM	
Date:		Sunday, November 10, 2024	
Sheet		10 of 19	
Rev		2.2	



Title			RTM Class D1.4
Size	A3	Document Number	uRTM
Date:	Friday, November 15, 2024	Sheet	12 of 19