TI81xx-HDVPSS-01.00.01.37 Feature Performance Guide

TI81xx HD-VPSS Drivers

This section provides brief overview of the device drivers supported in HDVPSS release. Drivers are mainly classified into three categories:

- Display Drivers
- Memory-to-Memory(M2M) Drivers.
- Capture Driver

HDVPSS Driver Features

1. Supports TI816x, TI814x and TI8107 SoC
2. Most of the drivers runs on VPSS-M3 core with BIOS operating system and FVID2 interface.
3. FBDEV/V4L2 driver is hosted on Cortex-A8 core with Linux as operating system using proxy server
4. Ships with sample applications and documentation.

VPDMA List Usage

VPDMA had 8 lists which are shared across all drivers:

VPDMA usage

Driver	DMA usage
Capture	One list for the capture driver
Display	One List for each TV output used
M2M	Depends on the path used (1-6 lists)

Setup Details

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	Details	TI816X ES1.1/ES2.0	TI814x ES 1	TI814x ES 2.1	TI8107
SoC Details	Core	VPSS-M3	VPSS-M3	VPSS-M3	VPSS-M3
	Operating speed of Core	250 MHz	200 MHz	200 MHz	200 MHz
	Operating speed of HD-VPSS	250 Mpixels/sec	200 Mpixels/sec	200 Mpixels/sec	200 Mpixels/sec
	EVM Configuration	Ducati, HDVPSS, 2 EMIFs Interleaved, DDR3 @ 796.5MHz	Ducati, HDVPSS, 2 EMIFs Interleaved, DDR2 @ 666MHz	Ducati, HDVPSS, 2 EMIFs Interleaved, DDR3 @ 333MHz	Ducati, HDVPSS, 1 EMIF non-Interleaved, DDR3 @ 400MHz

Optimization Details	Is the Ducati cache enabled?	Yes	Yes	Yes	Yes
	Profile	whole program debug	whole program debug	whole program debug	whole program debug
	Is the code and data placed in L2/L3 memory?	No	No	No	No
	Is the L3 interconnect optimized?	No	No	No	No

Video Display Drivers

This section describes the display drivers' performance numbers - throughput and CPU load.

Introduction

Display drivers takes the video buffers from the application and display the videos on VENCs at specified frame rate and resolution. Display drivers follows the FVID2 interface.

Bypass Path 0/1 and Secondary 1 Path Display Driver

Bypass path display driver controls the two bypass paths in the hardware. It configures only up to the muxes. The rest of the hardware below the mux/switch like CIG, COMP, VENC etc is controlled by display controller driver.

Secondary path 1 driver displays NTSC video on SD-DAC by feeding video data to display controller using secondary1 path. It configures the chroma up-sampler block. The rest of the hardware below the mux/switch like VENC etc is controlled by display controller driver.

Setup Details

- TI816x EVM, TI814x ES 2.1 EVM, TI8107 EVM
- TV - Samsung HD TV Model#LA32B550K1R
- DVD Player - Samsung Model#DVDC550

Video Display performance values

Output Display (Resolution)	TI816x From VPSS-M3		TI814x From VPSS-M3		TI8107 From VPSS-M3	
	Frame Rate (in Frames/sec)	CPU Load (in %)	Frame Rate (in Frames/sec)	CPU Load (in %)	Frame Rate (in Frames/sec)	CPU Load (in %)
Off-Chip HDMI - DVO2 (With Hardware Mosaic)	(30 FPS for 1080P30, 1080i60), (60FPS for 1080P60, 720P60), (25FPS for 1080i50), (50FPS for 1080P50, 720P50), (60FPS for 480P), (50FPS for 576P)	1%	(30 FPS for 1080P30, 1080i60), (60FPS for 1080P60, 720P60), (25FPS for 1080i50), (50FPS for 1080P50, 720P50), (60FPS for 480P), (50FPS for 576P)	1% - 2%	(30 FPS for 1080P30, 1080i60), (60FPS for 1080P60, 720P60), (25FPS for 1080i50), (50FPS for 1080P50, 720P50), (60FPS for 480P), (50FPS for 576P)	1% - 2%
On-Chip HDMI (With Hardware Mosaic)	(30 FPS for 1080P30, 1080i60), (60FPS for 1080P60, 720P60), (25FPS for 1080i50), (50FPS for 1080P50, 720P50), (60FPS for 480P), (50FPS for 576P)	1%	(30 FPS for 1080P30, 1080i60), (60FPS for 1080P60, 720P60), (25FPS for 1080i50), (50FPS for 1080P50, 720P50), (60FPS for 480P), (50FPS for 576P)	1% - 2%	(30 FPS for 1080P30, 1080i60), (60FPS for 1080P60, 720P60), (25FPS for 1080i50), (50FPS for 1080P50, 720P50), (60FPS for 480P), (50FPS for 576P)	1% - 2%

HD-DAC - HDCOMP (With Hardware Mosaic)	(30 FPS for 1080P30, 1080i60), (60FPS for 1080P60, 720P60), (25FPS for 1080i50), (50FPS for 1080P50, 720P50), (60FPS for 480P), (50FPS for 576P)	1%	NA	NA	(30 FPS for 1080P30, 1080i60), (60FPS for 1080P60, 720P60), (25FPS for 1080i50), (50FPS for 1080P50, 720P50), (60FPS for 480P), (50FPS for 576P)	NRY
SD-DAC	(30FPS for NTSC), (25FPS for PAL)	1%	(29FPS for NTSC), (25FPS for PAL)	1%	(30FPS for NTSC), (25FPS for PAL)	1%

Graphics Path 0/1/2 Driver

Graphics path display driver controls the three graphics paths in the hardware to display graphics planes including multi-regions support. The rest of the hardware below like COMP, VENC etc is controlled by display controller driver.

Graphics Planes performance values

Output Display (Resolution)	TI816x VPSS-M3		TI816x Cortex-A8			TI814x VPSS-M3		TI814x Cortex-A8			TI8107 VPSS-M3		TI8107 Cortex-A8		
	Frame Rate (in Frames/sec)	**CPU Load (in %)**	**Frame Rate (in Frames/sec)**	**CPU Load M3 (in %)**	**CPU Load A8 (in %)**	**Frame Rate (in Frames/sec)**	**CPU Load (in %)**	**Frame Rate (in Frames/sec)**	**CPU Load M3 (in %)**	**CPU Load A8 (in %)**	**Frame Rate (in Frames/sec)**	**CPU Load (in %)**	**Frame Rate (in Frames/sec)**	**CPU Load M3 (in %)**	**CPU Load A8 (in %)**
DVO2	(30 FPS for 1080P30), (60FPS for 1080P60, 1080i60, 720P60), (50FPS for 1080P50, 1080i50, 720P50)	1%	NRY	NRY	NRY	(30 FPS for 1080P30), (60FPS for 1080P60, 1080i60, 720P60), (50FPS for 1080P50, 1080i50, 720P50)	1% - 2%	NRY	NRY	NRY	(30 FPS for 1080P30), (60FPS for 1080P60, 1080i60, 720P60), (50FPS for 1080P50, 1080i50, 720P50)	1%	NRY	NRY	NRY
HD DAC	(30 FPS for 1080P30), (60FPS for 1080P60, 1080i60, 720P60), (50FPS for 1080P50, 1080i50, 720P50)	1%	NRY	NRY	NRY	NA	NA	NA	NA	NA	(30 FPS for 1080P30), (60FPS for 1080P60, 1080i60, 720P60), (50FPS for 1080P50, 1080i50, 720P50)	NRY	NRY	NRY	NRY
SD-DAC	(60 FPS for NTSC), (50 FPS for PAL)	1%	NRY	NRY	NRY	(59 FPS for NTSC), (50 FPS for PAL)	1% - 2%	NRY	NRY	NRY	(59 FPS for NTSC), (50 FPS for PAL)	1%	NRY	NRY	NRY

Video Capture Driver

This section describes the video capture driver performance numbers - throughput and CPU load.

Introduction

VIP capture driver makes use of VIP hardware block in HDVPSS to capture data from external video source like video decoders (example, TVP5158, TVP7002). The video data is captured from the external video source by the VIP Parser sub-block in the VIP block. The VIP Parser then sends the captured data for further processing in the VIP block which can include color space conversion, scaling, chroma down sampling and finally writes the video data to external DDR memory.

Setup Details

- TI816x EVM#NEA_1006005
- TV - Samsung HD TV Model#LA32B550K1R
- DVD Player - Samsung Model#DVDC550

Video Capture (Video Decoder - TVP5148) performance values

Video (Resolution)	TI816x M3 Core		TI814x M3 Core		TI8107 M3 Core	
	Field Rate per Channel (in Frames/sec)	CPU Load (in %)	Field Rate per Channel (in Frames/sec)	CPU Load (in %)	Field Rate per Channel (in Frames/sec)	CPU Load (in %)
16 ch D1 NTSC resolution	60	5%	60 (8CH D1 NTSC)	4%	60 (8CH D1 NTSC)	3%

Video Capture 1080P VIP input performance values

Output Display (Resolution)	TI816x M3 Core		TI814x M3 Core		TI8107 M3 Core	
	Frame Rate (in Frames/sec)	CPU Load (in %)	Frame Rate (in Frames/sec)	CPU Load (in %)	Frame Rate (in Frames/sec)	CPU Load (in %)
1080P60 single in; single disp	60	2%	60	2-3%	NRY	NRY
1080P60 dual in; dual disp	NRY	NRY	NRY	NRY	NRY	NRY
1080P60 single in; single disp, with scaling	60	2%	60	2-3%	NRY	NRY
1080P60 dual in; dual disp, with scaling	NRY	NRY	NRY	NRY	NRY	NRY

Memory to Memory Drivers

This section describes the memory-to-memory drivers' performance numbers - throughput and CPU load.

Introduction

M2M drivers takes the video buffer from the memory, optionally process the buffer, (processing done on the buffer depends on the specific M2M driver) and puts it back to memory. M2M driver follows the FVID2 interface for the applications.

Secondary 0 Or Bypass path 0/1 to SC5 and Sec 0/1 to SC3/SC4 M2M driver

This driver takes video data from one of the three paths(SEC0/BP0/BP1), does scaling(SC5) and writes output video to memory. Other variants take data from secondary path 0/1(SEC0/SEC1) and scales via VIP path scalars (SC3/SC4) and writes output videoto memory.

Setup Details:

- Calculate time required for single scaling operation and for CPU load, issue scaling operation in contiguous loop with queuing buffer for each resize.

Scalar Driver Performance values

Scaling Factor (Resolution)	TI816x VPSS-M3		TI814x VPSS-M3		TI8107 VPSS-M3	
	Max Frames per Sec	CPU Load (in %)	Max Frames per Sec	CPU Load (in %)	Max Frames per Sec	CPU Load (in %)
SEC0-SC5 Single Ch (Option 18, 720x480YUV420 => 720X480YUV422 interleaved)	675	5%	516	3%	543	4%
SEC0-SC5 Single Ch (Option 1, 720x480 YUV420 => 1920x1080 YUV422 interleaved)	118	2%	93	3%	94	2%
SEC0-SC5 Single Ch (Option 12, 1920x1080YUV420 => 720x480 YUV422 interleaved)	118	2%	93	3%	94	2%
BP0-SC5 Single Ch (720x480 YUV420 => 1920x1080 YUV422 interleaved)	NRY	NRY	NRY	NRY	NRY	NRY
BP1-SC5 Single Ch (Option 3, 720x480 YUV422 interleaved => 1920x1080 YUV422 interleaved)	118	2%	94	3%	94	2%
SEC0-SC3-VIP0 Single Ch (Option 5, 720x480 YUV420 => 1920x1080 YUV422 interleaved)	118	2%	93	3%	94	2%
SEC1-SC4-VIP1 Single Ch (Option 4, 720x480 YUV420 => 1920x1080 YUV422 Interleaved)	118	2%	93	3%	94	2%
SEC0-SC5 Multi Ch(8) (Option 10, 720x480 YUV420 => 1920x1080 YUV422 Interleaved)	271	1%	215	2%	216	2%
SEC0-SC5 Multi Ch(16) (Option 11, 720x480 YUV420 => 1920x1080 YUV422 Interleaved)	289	1%	230	2%	231	2%
SEC0-SC5 Single Ch 1/3x (1920x1080 YUV420 => 640x360 YUV422 Interleaved)	NRY	NRY	NRY	NRY	NRY	NRY
MultiCh - 3Ch (720x480 => 720xXXX)	NRY	NRY	NRY	NRY	NRY	NRY
8D1@60fps	NRY	NRY	NRY	NRY	NRY	NRY

SubFrame level processing in Secondary 0 Or Bypass path 0/1 to SC5 M2M driver

This driver takes video data from one of the three paths(SEC0/BP0/BP1), does scaling(SC5) subfframe by sub-frame and writes output video to memory.Frame is divided into multiple subframes and processed.

Setup Details:

- Calculate time required for single scaling operation and for CPU load, issue scaling operation in contiguous loop with queuing buffer for each resize.

Scalar Driver Performance values

Scaling Factor (Resolution)	TI816x VPSS-M3			TI814x VPSS-M3		TI8107 VPSS-M3	
	Num of SubFrames per Frame	Max Frames per Sec	CPU Load (in %)	Max Frames per Sec	CPU Load (in %)	Max Frames per Sec	CPU Load (in %)
SEC0-SC5 Single Ch 4x (720x480 YUV420 => 1920x1080 YUV422 interleaved)	4	108	9%	79	17%	87	9%
SEC0-SC5 Single Ch 4x (720x480 YUV422 interleaved => 1920x1080 YUV422 interleaved)	4	NRY	NRY	NRY	NRY	NRY	NRY
BP0-SC5 Single Ch 4x (720x480 YUV422 interleaved => 1920x1080 YUV422 interleaved)	4	111	8%	82	16%	89	8%
BP1-SC5 Single Ch 4x (720x480 YUV422 interleaved => 1920x1080 YUV422 interleaved)	4	111	8%	82	16%	89	8%

DEIH/DEI M2M Driver

This driver takes YUYV422/YUV420 interlaced/progressive input via the DEI path and provide one/two scaled version of the deinterlaced/bypassed outputs - one via writeback path 0/1 and another via VIP 0/1.

Setup Details

- CPU Idle - Disabled
- Tool Used for measurement - LFTB
- Calculate time required for single resize operation and for CPU load, issue resize operation in contiguous loop with queuing buffer for each resize.

DEI/DEIH Scalar Driver Performance values

Scaling Factor (Resolution)	TI816x VPSS-M3		TI814x VPSS-M3		TI8107 VPSS-M3	
	Max Frames per Sec	CPU Load (in %)	Max Frames per Sec	CPU Load (in %)	Max Frames per Sec	CPU Load (in %)
DEIH-WB0 - Single Ch 720x240 YUV420 => scaled to 360x240 YUYV422 via WB0	640	8%	NA	NA	NA	NA
DEI-WB1 - Single Ch 720x240 YUV420 => scaled to 360x240 YUYV422 via WB1	654	7%	NA	NA	NA	NA
DEIH-WB0-VIP0 - Single Ch 720x240 YUV420 => dual scaled to 360x240 YUYV422 via WB0 and 704x480 YUV420 via VIP0	635	8%	NA	NA	NA	NA

DEI-WB1-VIP1 - Single Ch 720x240 YUV420 => dual scaled to 360x240 YUYV422 via WB1 and 704x480 YUV420 via VIP1	649	8%	NA	NA	NA	NA
DEI-WB0-VIP0 - Single Ch 720x240 YUV420 Interlaced=> dual scaled to 360x240 YUYV422 via WB0 and 720x480 YUV420 via VIP0	NA	NA	492	14%	523	7%
SC-WB1-VIP1 – Single Ch 720x240 YUV420 SP Progressive=> dual scaled to 360x240 YUYV422 via WB1 and 704x480 YUV420 via VIP1	NA	NA	515	10%	538	5%
Single o/p writeback path 4x (720x480 => 1920x1080)	NRY	NRY	NRY	NRY	NRY	NRY
Single o/p VIP path 4x (720x480 => 1920x1080)	NRY	NRY	NRY	NRY	NRY	NRY
Single o/p writeback path 1/4x (1920x1080 => 720x480)	NRY	NRY	NRY	NRY	NRY	NRY
Single o/p VIP path 1/4x (1920x1080 => 720x480)	NRY	NRY	NRY	NRY	NRY	NRY

Noise Filter (NSF) M2M Driver

Noise filter driver allows user to filter noise from video data by processing them through the noise filter hardware. This driver can also be used for only YUV422 to YUV420 chroma downsampling.

Noise filter Driver Performance values

Mode	TI816x VPSS-M3		TI814x VPSS-M3		TI8107 VPSS-M3	
	Max Frames per Sec	CPU Load (in %)	Max Frames per Sec	CPU Load (in %)	Max Frames per Sec	CPU Load (in %)
Single Ch Chroma downsampling (640X480YUV422 interleaved => 640X480 YUV420 Semiplanar)	659	3%	511	5%	518	4%
NF spatial (1080P input)	NRY	NRY	NRY	NRY	NRY	NRY
NF temporal (1080P input)	NRY	NRY	NRY	NRY	NRY	NRY
MultiCh NF spatial (480P input)	NRY	NRY	NRY	NRY	NRY	NRY
MultiCh NF temporal (480P input)	NRY	NRY	NRY	NRY	NRY	NRY
16 Ch Chroma downsampling (720X240YUV422 interleaved => 720X240 YUV420 Semiplanar)	NRY	NRY	NRY	NRY	NRY	NRY

Calculating Performance for different Memory to memory paths

The description below is based on actual performance seen with SW drivers and whole multi-CH DVR system (including codecs) on actual Si.

Since DVR use-case is sort of worst case scenario (from processing performance, channel density and DDR BW) as compared to other use-cases, below description will hold true for most pratical use-case's.

Performance of Scalar (SC) Path

This is applicable for all SC's (SC_1 to SC_5) in TI816x, TI814x & TI8107.

Here DEI, whereever applicable, is assumed to be in bypass mode.

When DEI is not in bypass mode the performance description is given in subsequent section.

Each SC operates at 250Mhz clock (in TI816x) and 200Mhz (in TI814x/TI8107).
In theory it can process 1 pixel per clock, i.e
- about 250 mega pixel per second. (MP/s) in TI816x.
- about 200 mega pixel per second. (MP/s) in TI814x/TI8107.

But due to inherent overheads due to overlapping needed for various filtering operations, the practical standalone (i.e only SC running in system) speed would be
- about 230-240 MP/s (mega pixels/sec) in TI816x
- about 180-190 MP/s (mega pixels/sec) in TI814x/TI8107

When SC is run with other modules like other driver, or codecs the performance may drop further due to DDR BW.

SW overheads will also reduce SC performance, but with TI HDVPSS driver we see very little impact of SW overheads.

Taking DVR kind of use-case, each SC can safely do
- about 170MP/s processing (in TI816x).
- about 130MP/s processing (in TI814x/TI8107).

Number of pixel processed when doing SC for a 1 D1 CH of 720x480 @ 30frames per second, is 720x480x30(frames per second) = 10.3MP/s

Here Output from SC is <= 720x480

Thus SC can safely do about 16CHs of D1 (in TI816x) and about 12CH D1 (in TI814x/TI8107) when its output size is <= 720x480, i.e only downscaling is done in the scaler.

In practice with HDVPSS only applications we found that measured SC performance is
- about 20 D1 CHs (about 210MP/s) in TI816x
- about 13 D1 CHs (about 140MP/s) in TI814x/TI8107

With other activity like codec, performance should drop but we know each SC will safely give
- 16CH D1 performance (170MP/s) in TI816x
- 12CH D1 performance (130MP/s) in TI814x/TI8107

When scalar upsampling is used the results would be bit different.
For use-case of scaling 720x480 to 960x540 output size, the performance for 1CH would be,
960x540(since 960x540 > 720x480) x30(frames per second) = 15.5MP/s

In TI816x, assuming SC performance is 170MP/s, thats about 10-11 CHs
In TI814x/TI8107, assuming SC performance is 130MP/s, thats about 8 CHs

Performance of De-interlacer (DEI) Path

This is applicable for both DEI-HQ (in TI816x) as well as DEI (in TI816x, TI814x & TI8107)

Each DEI operates at 250Mhz clock (in TI816x) and 200Mhz (in TI814x/TI8107) .

In theory it can process 1 pixel per clock, i.e
- about 250 mega pixel per second. (MP/s) in TI816x
- about 200 mega pixel per second. (MP/s) in TI814x/TI8107

But due to inherent overheads due to overlapping needed for various filtering operations, the practical standalone (only DEI running in system) speed would be
- about 200-210 MP/s (mega pixels/sec) in TI816x
- about 150-160 MP/s (mega pixels/sec) in TI814xTI8107

When DEI is run with other modules like other driver, or codecs the performance may drop further due to DDR BW.

SW overheads will also reduce DEI performance, but with TI HDVPSS drivers we see very little impact of SW overheads.

Taking DVR kind of use-case, each DEI can safely do
- about 170MP/s processing in TI816x
- about 130MP/s processing in TI814x/TI8107

Number of pixel processed when doing DEI for a 1 D1 CH of 720x240 @ 60fields per second, is

720x240x2(since DEI results in 1 line becoming two lines)x60(frames per second) = 20.7MP/s

Here Output from DEI is <= 720x480

Thus DEI can safely do,
- about 8CHs of D1 in TI816x
- about 6CHs of D1 in TI814x/TI8107

when its output size is <= 720x480, i.e only downscaling is done in the scaler after DEI.

In practice with HDVPSS only applications we found that measured DEI performance is
- about 10-11 D1 CHs (about 200MP/s) in TI816x
- about 6-7 D1 CHs (about 140MP/s) in TI814x/TI8107

With other activity like codec, performance should drop but we know each DEI will safely give
- 8CH D1 performance in TI816x.
- 6CH D1 performance in TI814x/TI8107.

Above is when scalar downsampling is used after DEI.

When scalar upsampling is used the results would be bit different.
For use-case of 960x540 output size, the performance for 1CH would be,

960x540(since 960x540 > 720x480) x60(fields per second) = 31.1MP/s

In TI816x, assuming DEI performance is 170MP/s, thats about 5-6 CHs
In TI816x, assuming DEI performance is 130MP/s, thats about 4 CHs

Performance of Noise Filter (NF) Path

NF operates at 250Mhz clock (in TI816x) and 200Mhz clock (in TI814x/TI8107).
In theory it can process 1 pixel per clock, i.e about 250 mega pixel per second. (MP/s).

But due to inherent overheads due to overlapping needed for various filtering operations, the practical standalone (only NF running in system) speed would be
- about 180-190 MP/s (mega pixels/sec) in TI816x
- about 130-140 MP/s (mega pixels/sec) in TI814x/TI8107

When NF is run with other modules like other driver, or codecs the performance may drop further due to DDR BW.

SW overheads will also reduce NF performance, but with our driver we see very little impact of SW overheads.

Taking DVR kind of use-case, each NF can safely do
- about 170MP/s processing in TI816x
- about 130MP/s processing in TI814x/TI8107

Number of pixel processed when doing NF for a 1 D1 CH of 720x240 @ 60fields per second, is

720x240x60(fields per second) = 10.3MP/s

Thus NF can safely do
- about 16CHs of D1 in TI816x.
- about 12CHs of D1 in TI814x/TI8107

In practice with HDVPSS only applications we found that measured NF performance is also
- about 17.5 D1 CHs (about 180 MP/s) in TI816x
- about 12 D1 CHs (about 130 MP/s) in TI816x

With other activity like codec performance should drop but we know each NF will safely give
- 16CH D1 performance (170MP/s) in TI816x
- 12CH D1 performance (130MP/s) in TI814x/TI8107

Overall System Performance

HDVPSS BIOS package is having Links and Chains example. It shows the typical use cases exercising many different HDVPSS drivers. Below table shows the performance numbers for the different combination of the HDVPSS drivers. Details of each of the different combination can be found in the Links and Chains UserGuide

System Performance Values

Mode	TI816x VPSS-M3	TI814x VPSS-M3	TI8107 VPSS-M3
	CPU Load (in %)	CPU Load (in %)	CPU Load (in %)
16 channel D1 Capture + Noise-Filter (NSF) + De-interlacer (DEIHQ + DEI) + Mosaic Display Option 7	27%	NRY	NRY
8 channel D1 Capture + Noise-Filter (NSF) + De-interlacer (DEI) + Scalar + Display Option 5	13%	NRY	15%
4 channel D1 Capture + De-interlacer + Scalar + Display Option 4	8%	NRY	14%
16 channel(8 channels in case of TI814x/TI8107) D1 Capture + Noise-filter + Scalar + Display Option 3	10%	13%	7%

Article Sources and Contributors

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