H.264 Encoder
Version 02.00.07

Release Notes

November 2013

Build ID: 02.00.07.01

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- Support for higher vertical search range for motion estimation.

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

- This release is dependent on the following components
  - Code Composer Studio (CCSv4) version 4.2.0.09000
  - Code Generation Tool version 4.5.1 for HDVICP2 processor
  - Code Generation Tool version 5.0.3 for Media Controller processor
  - Framework Component version 3.20.00.22
  - HDVICP2 API (01.00.00.23)
  - HDVICP2 CSP (Containing CSL) version 00.05.02.00
- This release is validated on DM816x REV-A2 DDR2 EVM using following components
  - BIOS version 6.30.02.42
  - Codec Engine (CE) version 3.20.00.16
  - XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00105360	Higher search range support for motion estimation	IVAHD_001
SDOCM00103164	Encoder's persistent data is shuffled between different channels in multi-instance scenario and hence a codec hang observed	IVAHD_001
SDOCM00103161	Wait for DM data Tx(vDMA Descriptors push from SL2 to vDMA using DM) is missing in the routine of frame level bit stream Tx	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00089009	In interlaced case, only first field ROI co-ordinates are considered	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00095744	Bit mismatch with CPP in case of H264 Lite Configurations with force skip frames	IVAHD_001

H.264 Encoder
Version 02.00.06

Release Notes

May 2013

Build ID: 02.00.06.01

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- Encoder supports image width that is non-multiple of 16 pixels. Refer User's Guide for more details.
- Parameter extErrorCode has been added as part of IH264ENC_Status structure and IH264ENC_OutArgs structure.
- Added IH264ENC_ExtErrBits enumeration data type. Refer User's Guide for more details.

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1 for HDVICP2 processor
- Code Generation Tool version 5.0.3 for Media Controller processor
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.21)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00

- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00099576	XDM_GETSTATUS control call returns wrong status/information for intra coding parameters	IVAHD_001
SDOCM00100214	XDM_RESET for successive pictures renders standard noncompliance bit stream	IVAHD_001
SDOCM00099575	Even though ROI is supported by the Encoder, User's Guide table 4-2 says that IH264_REGION_OF_INTEREST is not supported	IVAHD_001
SDOCM00099577	Encoder does not give refined error codes in case of creation fail or run time parameter set fail	IVAHD_001
SDOCM00101205	Encoder returns an error for maxPicSizeRatiol parameter value more than 960	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00089009	In interlaced case, only first field ROI co-ordinates are considered	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00095744	Bit mismatch with CPP in case of H264 Lite Configurations with force skip frames	IVAHD_001

H.264 Encoder
Version 02.00.05

Release Notes

February 2013

Build ID: 02.00.05.00

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- The data type of parameter sliceUnitSize as a part of IH264ENC_SliceCodingParams structure has been changed from XDAS_Int16 to XDAS_Int32.
- Performance improvements for High Speed preset encoding feature, refer data sheet for details.
- H264 Encoder Media Controller library is compiled with Code Generation tools v5.0.3.

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1 for HDVICP2 processor
- Code Generation Tool version 5.0.3 for Media Controller processor
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.21)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00

- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00099078	Ducati returns an error when setting a slice size larger than 32767	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00089009	In interlaced case, only first field ROI co-ordinates are considered	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00095744	Bit mismatch with CPP in case of H264 Lite Configurations with force skip frames	IVAHD_001

H.264 Encoder
Version 02.00.04

Release Notes

January 2013

Build ID: 02.00.04.02

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- H264 Encoder Media Controller library is compiled with new Code Generation tools v5.0.2 to produce ELF compliant binaries.

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1 for HDVICP2 processor
- Code Generation Tool version 5.0.2 for Media Controller processor
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.20)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16

- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00097206	Slices in a frame are observed even though the Rate Control decides a frame as Full/Partial skip	IVAHD_001
SDOCM00097210	Bottom padding is improper for High Mega Pixel resolutions	IVAHD_001
SDOCM00097211	Inserting an Intra MB as a part of software work around to avoid ECD_SKIP_RUN_REG saturation affects visual quality	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00089009	In interlaced case, only first field ROI co-ordinates are considered	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here	IVAHD_001

Defect ID	Description	Applicable Release Configuration
	average picture size = (target bit rate / frame rate)	
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00095744	Bit mismatch with CPP in case of H264 Lite Configurations with force skip frames	IVAHD_001

H.264 Encoder
Version 02.00.04

Release Notes

October 2012

Build ID: 02.00.04.01

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- None

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00096084	Privacy Masking not supported for resolution greater than 4096x4096	IVAHD_001
SDOCM00094646	Setting MED_SPEED_HIGH_QUALITY intercodingPreset dynamically doesn't set 4MV	IVAHD_001
SDOCM00096848	Memory leak observed with Debug trace level 0	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00089009	In interlaced case, only first field ROI co-ordinates are considered	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00095744	Bit mismatch with CPP in case of H264 Lite Configurations with force skip frames	IVAHD_001

H.264 Encoder
Version 02.00.04

Release Notes

September 2012

Build ID: 02.00.04.00

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- Support for resolutions up to 4352x4096 has been added.

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00096040	vDMA wait for iLF Param stack Transfer and Recon Descriptor Transfer is missing in case of User Force Skip scenario	IVAHD_001
SDOCM00096062	Concurrent use of vDMA Register interface by iCONT1-ARM and iCONT2-ARM, hence leading to vDMA undefined behaviour	IVAHD_001
SDOCM00096077	Extra bytes observed in the bit-stream with data sync enabled	IVAHD_001
SDOCM00093929	The description of few RC parameters and sliceCoding parameters in User's Guide are not aligned to the codec behavior.	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00089009	In interlaced case, only first field ROI co-ordinates are considered	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here	IVAHD_001

Defect ID	Description	Applicable Release Configuration
	average picture size = (target bit rate / frame rate)	
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00095744	Bit mismatch with CPP in case of H264 Lite Configurations with force skip frames	IVAHD_001
SDOCM00096084	Privacy Masking not supported for resolution greater than 4096x4096	IVAHD_001

H.264 Encoder
Version 02.00.03

Release Notes

September 2012

Build ID: 02.00.03.00

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- H264 Lite Configuration (High Speed / 680 cycle configuration) feature support for High Mega Pixel resolutions.
- Redundant exposure of GDR configuration parameters as a part of Extended Dynamic structure are removed (SDOCM00095027).

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16

- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00095027	Redundant exposure of GDR configuration parameters as a part of Extended Dynamic parameters	IVAHD_001
SDOCM00094509	Default value of maxPicSizeRatioI and scalingMatrixPreset are not for best quality setting	IVAHD_001
SDOCM00095344	Codec Hang observed in OMTB test application on Tablet2 with ROI enabled cases	IVAHD_001
SDOCM00095065	Variable overflow observed during the estimation of current pic bits in RC module	IVAHD_001
SDOCM00095013	With default value of QP i.e., QP = -1, the memory access is happening from unwanted location	IVAHD_001
SDOCM00095014	Control on maximum allowed value for frameSkipThMulQ5 is necessary	IVAHD_001
SDOCM00095343	Codec Hang observed in video record usecase for resolutions less then 1080p on tablet2 setup using Omap4 App	IVAHD_001
SDOCM00095625	Artifacts in P frames are observed for non-multiple of 16 vertical search range in sliding window flow	IVAHD_001
SDOCM00095626	Artifacts in P frames are observed in low bit rate CBR cases + cyclic intra-refresh mechanism configurations	IVAHD_001
SDOCM00087396	Unnecessary error check of qpP and qpOffsetB is happening even if B frames are not in use or rate control is disabled	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00089009	In interlaced case, only first field ROI co-ordinates are considered	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00095744	Bit mismatch with CPP in case of H264 Lite Configurations with force skip frames	IVAHD_001

H.264 Encoder
Version 02.00.02

Release Notes

June 2012

Build ID: 02.00.02.02

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- Run time Exposure of current frame's temporal id (temporalId) through IH264ENC_OutArg. For more details, refer User's Guide section 4.2.2.13.

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00091641	expose temporal id of a frame in run-time output Arguments.	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00089009	In interlaced case, only first field ROI co-ordinates are considered	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001

H.264 Encoder
Version 02.00.02

Release Notes

May 2012

Build ID: 02.00.02.01

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- **lateAcquireArg** parameter in the IH264ENC_InArgs has been renamed to **processId.** For more details, refer User's Guide section 4.2.2.10.

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00084179	High megapixel encoding has been tested with maximum of two consecutive B frames (i.e., IBBPBBPBB)	IVAHD_001
SDOCM00091552	Process call does not return when encoder is configured to encode with following parameters enabled 1. stereoInfoPreset 2. topFieldIsLeftViewFlag and 3. viewSelfContainedFlag This is observed in stand-alone test application with SCRATCH_CONTAMINATION enabled.	IVAHD_001
SDOCM00091962	When user is providing max pic size_I/P/B ratio other than default (in this case it was 640) then it was not taking affect.	IVAHD_001
SDOCM00083447	outArgs structure parameters are written before NULL check	IVAHD_001
SDOCM00090614	MV mismatch in interlaced HiMP cases (1968 < width <= 2K && height > 2K)	IVAHD_001
SDOCM00090615	Bit mismatch with CPP in case of ROI with partial frame skip	IVAHD_001
SDOCM00091140	Watermarking key issues observed for few encoder configurations	IVAHD_001
SDOCM00090853	In extreme situation, in valid stream might get generated in HIGH SPEED configuration	IVAHD_001
SDOCM00091342	In High Speed encoder, when intraFrameInterval is zero then intra restriction is more aggressive than required	IVAHD_001
SDOCM00091869	User guide does not mention whether IH264ENC_SVCCodingParams is part of create/dynamic/status structure	IVAHD_001
SDOCM00092202	Hang on Media controller can be observed, if SL2 is accessed through buffered region from Media controller	IVAHD_001
SDOCM00092248	User guide Appendix E (Debug Trace Support) has one wrong line	IVAHD_001
SDOCM00092250	The ordering of elements in Trace structure can be changed for improved tracing	IVAHD_001
SDOCM00092249	User Guide enhancement is required for extracting analytic buffer info given out from encoder	IVAHD_001
SDOCM00092412	Directory name case is not consistent w.r.t previous releases	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00089009	In interlaced case, only first field ROI co-ordinates are considered	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001

H.264 Encoder
Version 02.00.02

Release Notes

April 2012

Build ID: 02.00.02.00

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- Added a parameter **enableErrorCheck** in the structure IH264ENC_ProcessParamsList. This has been added to enable/disable error check for non supported features in N channel scenario. For more details, refer User's Guide section 4.2.2.15.

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00090145 SDOCM00087196	Below features are not supported in multi channel API and doesn't have any error return – so the behavior is undefined with these features - Min Bit Rate - EOS NAL - Sub Frame Synchronization - FramePackSEI and StereoVideoSEI - ROI - B frame - Mixed handle with 1 MV and 4 MV support	IVAHD_001
SDOCM00090144	Below features are not supported in High Speed Encoding Preset– so the behavior is undefined with these features - Partial Frame skip - intra refresh method	IVAHD_001
SDOCM00089010	High Speed Encoding preset is supported only in High Profile and transformBlockSize as `IH264_TRANSFORM_8x8`. No Error Check has been placed inside codec.	IVAHD_001
SDOCM00088662	No error check happens on minBlockSizeP for IPPP sequence	IVAHD_001
SDOCM00084180	Bit-exactness test with PC reference has not been carried out for high megapixel sequences and ROI enabled cases	IVAHD_001
SDOCM00091525	High Speed Encoding preset is not supported for High mega pixel encoding. No Error Check has been placed inside codec.	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00089009	In interlaced case, only first field ROI co-ordinates are considered	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00084179	High megapixel encoding has been tested with maximum of two consecutive B frames (i.e., IBBPBBPBB)	IVAHD_001
SDOCM00091552	Process call does not return when encoder is configured to encode with following parameters enabled 1. stereoInfoPreset 2. topFieldIsLeftViewFlag and 3. viewSelfContainedFlag This is observed in stand-alone test application with SCRATCH_CONTAMINATION enabled.	IVAHD_001
SDOCM00091962	When user is providing max pic size_I/P/B ratio other than default (in this case it was 640) then it was not taking affect.	IVAHD_001

H.264 Encoder
Version 02.00.00

Release Notes

March 2012

Build ID: 02.00.00.10

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues/Limitations

New In This Release

- Performance improvements for below features, refer data sheet for details
  - ROI and Privacy Masking support
  - High Speed preset encoding
- Enhancement in ROI to support below
  - Increased dynamic range of ROI priority from [-4 , 4] to [-8, 8]
  - Support of ROI in fixed Qp mode
- The way Privacy mask data from user is accepted is changed, refer User guide for more details
- Enumeration value of IH264ENC_INTRACODINGBIAS_HIGH_SPEED has been changed, refer User Guide for more details

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs,	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1

- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00090177	In B frame (or layer other than base layer) if GDR is enabled then error is not thrown by codec	IVAHD_001
SDOCM00090176	When base class of InArgs is in use and static parameter is of extended class with watermark enable then error is not thrown	IVAHD_001
SDOCM00090174	EOS NAL will not get inserted in IPPP sequence even if it is enabled.	IVAHD_001
SDOCM00090173	Unnecessary error check of CVBR parameters are happening even if CVBR is disabled	IVAHD_001
SDOCM00090172	Water Mark SEI message is inserted for both field in interlace cases	IVAHD_001
SDOCM00090167	4Kx4K resolution having complete frame skipped by rate control was not handled properly.	IVAHD_001
SDOCM00090166	UUID used in watermarking SEI is not guaranteed to be unique, it is not generated with UUID generator	IVAHD_001
SDOCM00090164	Watermarking key is not coded as part of stream for last frame if EOS is not enabled	IVAHD_001
SDOXT00001465	For 2Kx2K to 2K x 4K interlaced case, quality might not be good	IVAHD_001
SDOCM00090162	No error is being returned if Encoder has been provided NULL pointer for 1D buffers	IVAHD_001
SDOCM00090161	ROI for a frame after a series of Skip frames, might not provide best quality gain of ROI	IVAHD_001
SDOCM00090160	ROI behavior is not correct when partialFrameSkip is enabled	IVAHD_001
SDOCM00090159	For B frames, the ROI input is not buffered internally hence the user provided ROI will not be applied to appropriate frame	IVAHD_001
SDOCM00090140	sliceMode = IVIDEO_SLICEMODE along with H241 and End of stream NALs enabled scenario codec hang might get observed	IVAHD_001
SDOCM00090138	With High Speed preset mode along with CBR rate control at low bit rates, overshooting of target bit rate is observed. No frame skips are being observed in this situation.	IVAHD_001
SDOCM00090136	In case of force skip with ROI being enabled, encoder might hang.	IVAHD_001
SDOCM00089594	User guide information about mv sad exposure need to be corrected	IVAHD_001
SDOCM00089520	Datasheet says Codec can encode max of 2Kx2K whereas Userguide says Codec can encode max of 4Kx4K	IVAHD_001

SDOCM00088996	unexpected Performance degradation when ROI is enabled	IVAHD_001
SDOCM00087396	Unnecessary error check of qpP and qpOffsetB is happening even if B frames are not in use or rate control is disabled	IVAHD_001
SDOCM00084178	For high megapixel sequences, encoded bitstream has visual artifacts in some skipped frames when forceSKIPPeriod is enabled	IVAHD_001

Known Issues/Limitations

Defect ID	Description	Applicable Release Configuration
SDOCM00090145 SDOCM00087196	Below features are not supported in multi channel API and doesn't have any error return – so the behavior is undefined with these features - Min Bit Rate - EOS NAL - Sub Frame Synchronization - FramePackSEI and StereoVideoSEI - ROI - B frame - Mixed handle with 1 MV and 4 MV support	IVAHD_001
SDOCM00090144	Below features are not supported in High Speed Encoding Preset– so the behavior is undefined with these features - Partial Frame skip - intra refresh method	IVAHD_001
SDOCM00089010	High Speed Encoding preset is supported only in High Profile and transformBlockSize as `IH264_TRANSFORM_8x8`. No Error Check has been placed inside codec.	IVAHD_001
SDOCM00089593	Field Merged Encode output is incorrect, seems corrupted.	IVAHD_001
SDOCM00089009	In interlaced case, only first field ROI co-ordinates are considered	IVAHD_001
SDOCM00088662	No error check happens on minBlockSizeP for IPPP sequence	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00084180	Bit-exactness test with PC reference has not been carried out for high megapixel sequences and ROI enabled cases	IVAHD_001
SDOCM00084179	High megapixel encoding has been tested with maximum of two consecutive B frames (i.e., IBBPBBP…)	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00071001	H264 compliance failure for certain checks by MTS4EA 24333:The number of bits of macroblock_layer() data must not exceed 3200 bits 34292: Hypothetical Reference Decoder SchedSelIdx = 0 model has underflowed	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001

H.264 Encoder
Version 02.00.00

Release Notes

February 2012

Build ID: 02.00.00.09

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- None

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00089070	Method for forcing HDVICP status as SAME_CODECTYPE is not working	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00088996	unexpected Performance degradation when ROI is enabled	IVAHD_001
SDOCM00089010	Profile != HIGH and encodingPreset = HIGHSPEED can result in incompliant stream.	IVAHD_001
SDOCM00089009	ROI along with interlaced content type with process call at field level can result in unexpected output	IVAHD_001
SDOCM00087396	Unnecessary error check of qpP and qpOffsetB is happening even if B frames are not in use or rate control is disabled	IVAHD_001
SDOCM00087196	Multi Frame process call is not supported for B frames and mix of 1 & 4 MV frames	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00071001	H264 compliance failure for certain checks by MTS4EA 24333:The number of bits of macroblock_layer() data must not exceed 3200 bits 34292: Hypothetical Reference Decoder SchedSelIdx = 0 model has underflowed	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may	IVAHD_001

Defect ID	Description	Applicable Release Configuration
	appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00084178	For high megapixel sequences, encoded bitstream has visual artifacts in some skipped frames when forceSKIPPeriod is enabled	IVAHD_001
SDOCM00084179	High megapixel encoding has been tested with maximum of two consecutive B frames (i.e., IBBPBBP…)	IVAHD_001
SDOCM00084180	Bit-exactness test with PC reference has not been carried out for high megapixel sequences and ROI enabled cases	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001

H.264 Encoder
Version 02.00.00

Release Notes

February 2012

Build ID: 02.00.00.08

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- Control for maxPicSizeRatio of each picture type
- CVBR rate control enhancements

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00088524	Setting enableAnalyticInfo flag in ProcessN API for H.264 encoder results in IVAHD hang	IVAHD_001
SDOCM00088318	Dependency on intraframeInterval in hierarchical P-frame case needs to be avoided. This will restrict allowed intra frame interval when number of temporal layer is more than one.	IVAHD_001
SDOCM00088757	H264 Encoder crash in customer application framework. This is applicable in multi channel process call scenario.	IVAHD_001
SDOCM00089036	Watermarking is not effective when ROI is not enabled	IVAHD_001
SDOCM00089035	With Content type = interlaced and rate control = VBR the bit rate is not being achieved	IVAHD_001
SDOCM00089034	Control for maxPicSizeRatio of each picture type is needed	IVAHD_001
SDOCM00089037	Constant value of Dynamic Default structure is not in sync with interface header file element so it cannot be used	IVAHD_001
SDOCM00088871	SVC Temporal Layer3 issue after encoding 1000+ frames.	IVAHD_001
SDOCM00089033	maxBitRate >= 1.5*targetBitRate and rate control = CBR can result in bit rate deviation	IVAHD_001
SDOCM00088884	Control call modifies the default static params structure in medium speed high quality encoding. Due to this dynamic change of different intraCodingPreset and interCodingPreset is not achievable.	IVAHD_001
SDOCM00088997	In multi channel use case, with different handle having different profile will result in not achieving best quality	IVAHD_001
SDOCM00088663	Stand-alone package in RTSC gives build error	IVAHD_001
SDOCM00087195	Multi frame process call scenario codec hang might get observed	IVAHD_001
SDOCM00087397	User Guide :: Numbering index of points is wrong in appendix C	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00088996	unexpected Performance degradation when ROI is enabled	IVAHD_001
SDOCM00089010	Profile != HIGH and encodingPreset = HIGHSPEED can result in incompliant stream.	IVAHD_001
SDOCM00089009	ROI along with interlaced content type with process call at field level can result in unexpected output	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00087396	Unnecessary error check of qpP and qpOffsetB is happening even if B frames are not in use or rate control is disabled	IVAHD_001
SDOCM00087196	Multi Frame process call is not supported for B frames and mix of 1 & 4 MV frames	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00071001	H264 compliance failure for certain checks by MTS4EA 24333:The number of bits of macroblock_layer() data must not exceed 3200 bits 34292: Hypothetical Reference Decoder SchedSelIdx = 0 model has underflowed	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00084178	For high megapixel sequences, encoded bitstream has visual artifacts in some skipped frames when forceSKIPPeriod is enabled	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00084179	High megapixel encoding has been tested with maximum of two consecutive B frames (i.e., IBBPBBP…)	IVAHD_001
SDOCM00084180	Bit-exactness test with PC reference has not been carried out for high megapixel sequences and ROI enabled cases	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001

H.264 Encoder
Version 02.00.00

Release Notes

January 2012

Build ID: 02.00.00.06

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- None

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00086544	For multi-instance scenario the sample test application behavior is not proper for some cases	IVAHD_001
SDOCM00087391	IVIDEO_STORAGE rate control preset is not honored	IVAHD_001
SDOCM00087398	HRDBuffer size and initialBuffer Level default value selected by codec is not as per recommendation in a particular scenario	IVAHD_001
SDOCM00087967	Field merge interlace encoder output is not proper	IVAHD_001
SDOCM00088286	Encoder does not return error when H241 is dynamically configured for CABAC entropy mode or Interlaced encoding	IVAHD_001
SDOCM00087969	Bit rate drop is observed when algo is changed from VBR to CBR	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00088318	Dependancy on intraframeInterval in hirarchical P-frame case needs to be avoided	IVAHD_001
SDOCM00088388	Artifacts are observed in HIGH_SPEED preset encoder setting	IVAHD_001
SDOCM00087968	User Guide information is not sufficient to integrate SVC-T in application	IVAHD_001
SDOCM00087196	Multi Frame process call is not supported for B frames and mix of 1 & 4 MV frames	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00071001	H264 compliance failure for certain checks by MTS4EA 24333:The number of bits of macroblock_layer() data must not exceed 3200 bits 34292: Hypothetical Reference Decoder SchedSelIdx = 0 model has underflowed	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00084178	For high megapixel sequences, encoded bitstream has visual artifacts in some skipped frames when forceSKIPPeriod is enabled	IVAHD_001
SDOCM00084179	High megapixel encoding has been tested with maximum of two consecutive B frames (i.e., IBBPBBP…)	IVAHD_001
SDOCM00084180	Bit-exactness test with PC reference has not been carried out for high megapixel sequences and ROI enabled cases	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001

H.264 Encoder
Version 02.00.00

Release Notes

January 2012

Build ID: 02.00.00.05

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- None

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00087966	Encoder hang can be observed in interlace coding, when one field is encoded in single process call. This is applicable when some other codec is running on same IVAHD.	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00087969	Bit rate drop is observed when algo is changed from VBR to CBR	IVAHD_001
SDOCM00087968	User Guide information is not sufficient to integrate SVC-T in application	IVAHD_001
SDOCM00087967	Field merge interlace encoder output is not proper. Problem observed in second field offset width/height is negative.	IVAHD_001
SDOCM00087179	Distortion(Pink patches) observed in encoded bitstreams when LTRP is enabled for H-P cases	IVAHD_001
SDOCM00087196	Multi Frame process call is not supported for B frames and mix of 1 & 4 MV frames	IVAHD_001
SDOCM00087195	Multi frame process call scenario codec hang might get observed	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00071001	H264 compliance failure for certain checks by MTS4EA 24333:The number of bits of macroblock_layer() data must not exceed 3200 bits 34292: Hypothetical Reference Decoder SchedSelIdx = 0 model has underflowed	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00084178	For high megapixel sequences, encoded bitstream has visual artifacts in some skipped frames when forceSKIPPeriod is enabled	IVAHD_001
SDOCM00084179	High megapixel encoding has been tested with maximum of two consecutive B frames (i.e., IBBPBBP…)	IVAHD_001
SDOCM00084180	Bit-exactness test with PC reference has not been carried out for high megapixel sequences and ROI enabled cases	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001

H.264 Encoder
Version 02.00.00

Release Notes

December 2011

Build ID: 02.00.00.04

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- None

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00086501	In multi channel process call scenario IVAHD MHz saving can be improved further	IVAHD_001
SDOCM00086499	In multi channel process call scenario, if one channel parameters are not correct then no channel/frame is encoded	IVAHD_001
SDOCM00086489	Code hang is observed in multi channel use case if force skip is enabled	IVAHD_001
SDOCM00087182	outputDataMode as IVIDEO_SLICEMODE, SPS data might not get encoded	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00087179	Distortion(Pink patches) observed in encoded bitstreams when LTRP is enabled for H-P cases	IVAHD_001
SDOCM00087196	Multi Frame process call is not supported for B frames and mix of 1 & 4 MV frames	IVAHD_001
SDOCM00087195	Multi frame process call scenario codec hang might get observed	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00071001	H264 compliance failure for certain checks by MTS4EA 24333:The number of bits of macroblock_layer() data must not exceed 3200 bits 34292: Hypothetical Reference Decoder SchedSelIdx = 0 model has underflowed	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may	IVAHD_001

Defect ID	Description	Applicable Release Configuration
	appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00084178	For high megapixel sequences, encoded bitstream has visual artifacts in some skipped frames when forceSKIPPeriod is enabled	IVAHD_001
SDOCM00084179	High megapixel encoding has been tested with maximum of two consecutive B frames (i.e., IBBPBBP…)	IVAHD_001
SDOCM00084180	Bit-exactness test with PC reference has not been carried out for high megapixel sequences and ROI enabled cases	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001

H.264 Encoder
Version 02.00.00

Release Notes

November 2011

Build ID: 02.00.00.03

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- None

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00086836	Encoder is not able to meet bit rate due to un initialized variable inside the codec	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00086489	Code hang is observed in multi channel use case if force skip is enabled	IVAHD_001
SDOCM00086544	For multi-instance scenario the sample test application behavior is not proper for some cases	IVAHD_001
SDOCM00086501	In multi channel process call scenario IVAHD MHz saving can be improved further	IVAHD_001
SDOCM00086499	In multi channel process call scenario, if one channel parameters are not correct then no channel/frame is encoded	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00071001	H264 compliance failure for certain checks by MTS4EA 24333:The number of bits of macroblock_layer() data must not exceed 3200 bits 34292: Hypothetical Reference Decoder SchedSelIdx = 0 model has underflowed	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00084178	For high megapixel sequences, encoded bitstream has visual artifacts in some skipped frames when forceSKIPPeriod is enabled	IVAHD_001
SDOCM00084179	High megapixel encoding has been tested with maximum of two consecutive B frames (i.e., IBBPBBP…)	IVAHD_001
SDOCM00084180	Bit-exactness test with PC reference has not been carried out for high megapixel sequences and ROI enabled cases	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001

H.264 Encoder
Version 02.00.00

Release Notes

November 2011

Build ID: 02.00.00.02

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- Dynamic modification of rate control algorithm support

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

Defect ID	Description	Applicable Release Configuration
SDOCM00086498	Dynamic modification of the rate control algorithm is not supported	IVAHD_001
SDOCM00086693	Parameters HRDBufferSize, initialBufferLevel, chromaQPIndexOffset, scalingMatrixPreset are not supported at run time	IVAHD_001
SDOCM00086490	Code hang might observed in multi channel use case if SL2 area is not initialized to zero in first multi process call	IVAHD_001
SDOCM00086690	Unnecessary error check is happening for referencePicMarking parameter when numTemporalLayer equal to 1	IVAHD_001

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00086489	Code hang is observed in multi channel use case if force skip is enabled	IVAHD_001
SDOCM00086544	For multi-instance scenario the sample test application behavior is not proper for some cases	IVAHD_001
SDOCM00086501	In multi channel process call scenario IVAHD MHz saving can be improved further	IVAHD_001
SDOCM00086499	In multi channel process call scenario, if one channel parameters are not correct then no channel/frame is encoded	IVAHD_001
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00071001	H264 compliance failure for certain checks by MTS4EA 24333:The number of bits of macroblock_layer() data must not exceed 3200 bits	IVAHD_001

Defect ID	Description	Applicable Release Configuration
	34292: Hypothetical Reference Decoder SchedSelIdx = 0 model has underflowed	
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00084178	For high megapixel sequences, encoded bitstream has visual artifacts in some skipped frames when forceSKIPPeriod is enabled	IVAHD_001
SDOCM00084179	High megapixel encoding has been tested with maximum of two consecutive B frames (i.e., IBBPBBP…)	IVAHD_001
SDOCM00084180	Bit-exactness test with PC reference has not been carried out for high megapixel sequences and ROI enabled cases	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001

H.264 Encoder
Version 02.00.00

Release Notes

October 2011

Build ID: 02.00.00.01

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- Support for N frame process call
- Support of high speed encoder preset

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

None

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00071001	H264 compliance failure for certain checks by MTS4EA 24333:The number of bits of macroblock_layer() data must not exceed 3200 bits 34292: Hypothetical Reference Decoder SchedSelIdx = 0 model has underflowed	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00084178	For high megapixel sequences, encoded bitstream has visual artifacts in some skipped frames when forceSKIPPeriod is enabled	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00084179	High megapixel encoding has been tested with maximum of two consecutive B frames (i.e., IBBPBBP…)	IVAHD_001
SDOCM00084180	Bit-exactness test with PC reference has not been carried out for high megapixel sequences and ROI enabled cases	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001
SDOCM00085715	Encoder with multi-channel support may not run on Simulator	IVAHD_001

H.264 Encoder
Version 02.00.00

Release Notes

September 2011

Build ID: 02.00.00.00

The release note is divided into the following sections:

- New In This Release
- Validation Information
- Fixed In This Release
- Known Issues

New In This Release

- Support for resolutions up to 4096x4096 has been added

Validation Information

Release Configuration	Description	Validation Platform
IVAHD_ 001	H.264 Encoder, which runs on HDVICP2 and Media Controller based SoCs	DM816x REV-A2 DDR2 EVM [Datasheet][User Guide]

This release is validated on DM816x REV-A2 DDR2 EVM using the following components.

- Code Composer Studio (CCSv4) version 4.2.0.09000
- Code Generation Tool version 4.5.1
- Framework Component version 3.20.00.22
- HDVICP2 API (01.00.00.19)
- HDVICP2 CSP (Containing CSL) version 00.05.02.00
- BIOS version 6.30.02.42
- Codec Engine (CE) version 3.20.00.16
- XDC tools version 3.20.04.68

Fixed In This Release

None

Known Issues

Defect ID	Description	Applicable Release Configuration
SDOCM00064332	Force IDR request fails in certain corner scenarios with B frames	IVAHD_001
SDOCM00064235	Visual artifact in I frame in low delay scenario	IVAHD_001
SDOCM00068087	Compression ratio is not met (Vprove error)	IVAHD_001
SDOCM00069805	During Flush state and generate header case inBufs and inArgs are expected to be having correct data	IVAHD_001
SDOCM00071001	H264 compliance failure for certain checks by MTS4EA 24333:The number of bits of macroblock_layer() data must not exceed 3200 bits 34292: Hypothetical Reference Decoder SchedSelIdx = 0 model has underflowed	IVAHD_001
SDOCM00072547	Above level 4.1 encoder does not check for level compliance for the generated bit stream	IVAHD_001
SDOCM00075211	While using multiple slice generation based upon maximum bytes per slice on simulator following Warning/Error messages may appear *SBOX: Register Write access while running* *Cannot write to ICONT_SBH_EOT register: write discarded* Simulator might also have unpredictable behavior with this usage.	IVAHD_001
SDOCM00078119	Encoder will be able to achieve slightly lower (around 20%) of target bit rate with a situation when very small HRD buffer size (HRD Buffer Size < 3.33* average picture size) is used. Here average picture size = (target bit rate / frame rate)	IVAHD_001
SDOCM00078133	In case of two adjacent scenes with significantly different amount of complexity starting second scene change exactly at I picture boundary may result in video quality degradation	IVAHD_001
SDOCM00078134	Video segment with steadily increasing complexity in nature might result in video quality degradation	IVAHD_001
SDOCM00078135	When qp offset between P and B is smaller than 4, at the beginning of the sequence and around scene changes VQ may degrade	IVAHD_001
SDOCM00084178	For high megapixel sequences, encoded bitstream has visual artifacts in some skipped frames when forceSKIPPeriod is enabled	IVAHD_001

Defect ID	Description	Applicable Release Configuration
SDOCM00084179	High megapixel encoding has been tested with maximum of two consecutive B frames (i.e., IBBPBBP…)	IVAHD_001
SDOCM00084180	Bit-exactness test with PC reference has not been carried out for high megapixel sequences and ROI enabled cases	IVAHD_001
SDOCM00084181	Output is not proper for high megapixel sequences on Simulator. The EVM outputs are proper.	IVAHD_001