X1500

IoT Application Processor

Data Sheet

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北京君正集成电路股份有限公司
Ingenic Semiconductor Co.,Ltd.

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1 Overview

X1500 is a low power consumption, high performance and high integrated application processor, the application is focus on IoT devices. And it can match the requirements of many other embedded products.

NAME	SIP LPDDR
X1500	32MB

1.1 Block Diagram

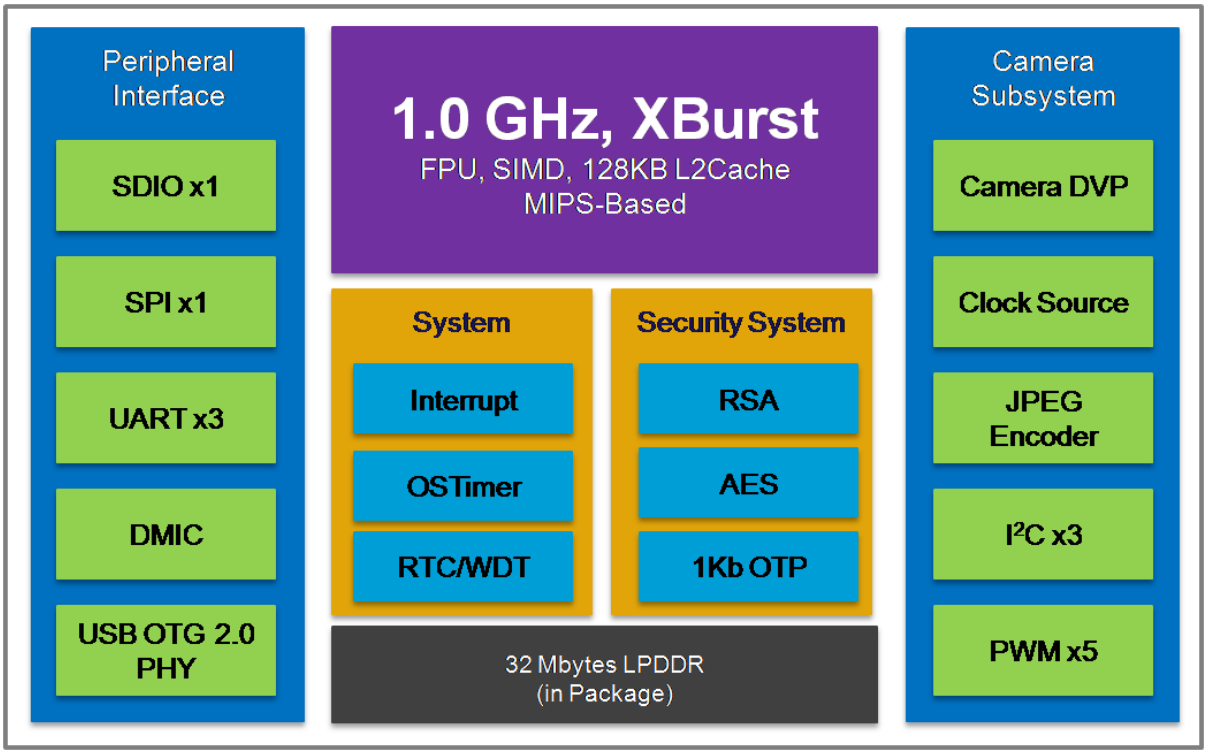


Figure 1-1 X1500 Diagram

1.2 Features

1.2.1 CPU Core

- MIPS-Based XBurst® cores (up to 1.0GHz)
- MIPS-Based XBurst® CPU
  - XBurst® RISC instruction set
  - XBurst® SIMD instruction set
  - XBurst® FPU instruction set supporting both single and double floating point format which are IEEE754 compatible

  - XBurst® 9-stage pipeline micro-architecture
- MMU
  - 32-entry joint-TLB
  - 4 entry Instruction TLB
  - 4 entry data TLB
- L1 Cache
  - 16KB instruction cache
  - 16KB data cache
- Hardware debug support
- 16KB tight coupled memory
- L2 Cache
  - 128KB unify cache
- The XBurst® processor system supports little endian only

1.2.2 Image Core

- Hardware JPEG encoder
  - Baseline ISO/IEC 10918-1 JPEG compliant
  - 8-bit pixel depth support
  - Support for YUY2 ([Y0,U0,Y1,V0]) color
  - Up to four programmable Quantization tables
  - Fully programmable Huffman tables
  - Image size up to 2M pixels

1.2.3 Display/Camera/Audio

- Camera interface module
  - Input image size up to 2M pixels
  - Integrated DMA
  - Supported data format: YCbCr 4:2:2
  - Supports ITU656 (YCbCr 4:2:2) input
  - Configurable VSYNC and HSYNC signals: active high/low
  - Configurable PCLK: active edge rising/falling
  - PCLK max. 80MHz
  - Configurable output order
- Low power DMIC Controller
  - 16 bits data interface and 20bit precision internal controller.
  - SNR: 90dB, THD: -90dB @ FS -20dB
  - Linear high pass filter include. Attenuation: -2.9dB@100Hz, -22dB@27Hz. -36dB@10Hz
  - Low power voice trigger when waiting to start talking.
  - 1 to 4 channel MIC support.
  - Support voice data pre-fetch when trigger enable and the data interface disable, but do not increase the power dissipation.

- Sample rate supported: 8k, 16k.
- Support low power mode

1.2.4 Memory Interface

- DDR Controller
  - Support LPDDR, DDR2, DDR3
  - 16 bit data width
  - Support size up to 1GB (1 chip select, 3-bit Bank,15-bit Row, 11-bit Column,)
  - Asynchornize to system bus and each port.
  - Support clock-stop mode
  - Support auto self-refresh mode
  - Support power-down mode and deep-power-down mode
  - Programmable DDR timing parameters
  - Programmable DDR row and column address width and order

- 32MB SIP LPDDR

- Serial nand/nor flash interface(SFC)
  - SPI protocol support: Standard, Dual, Quad SPI
  - Standard I/O data transfer up to 80Mbits/s
  - Dual I/O data transfer up to 160Mbits/s
  - Quad I/O data transfer up to 240Mbits/s
  - transmit-only or receive-only operation
  - MSB always be first in intra transfer of one byte. Least Significant Byte first for inter transfer of data bytes, and Most Significant Byte first for inter transfer of command or address bytes.
  - one device select
  - Configurable sampling point for reception
  - Configurable timing parameters: tSLCH, tCHSH and tSHSL
  - Configurable flash address wide are supported
  - 7 transfer formats: Standard SPI, Dual-Output/Dual-Input SPI, Quad-Output/Quad-Input SPI, Dual-I/O SPI, Quad-I/O SPI, Full Dual-I/O SPI, Full Quad-I/O SPI
  - two data transfer mode: slave mode and DMA mode
  - Configurable 6 phases for software flow

1.2.5 System Functions

- Clock generation and power management
  - On-chip oscillator circuit (support 24MHz, 26MHz)
  - Two phase-locked loops (PLL) with programmable multiplier
  - CCLK, HHCLK, H2CLK, PCLK, H0CLK, DDR_CLK frequency can be changed separately for software by setting registers
  - Functional-unit clock gating

- Supply block power shut down

- Timer and counter unit with PWM output and/or input edge counter
  - Provide 5 channels, all can generate PWM, two of them have input signal transition edge counter
  - 16-bit A counter and 16-bit B counter with auto-reload function every channel
  - Support interrupt generation when the A counter underflows
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected

- OS timer
  - One channel
  - 32-bit counter and 32-bit compare register
  - Support interrupt generation when the counter matches the compare register
  - Three clock sources: RTCLK (real time clock), EXCLK (external clock input), PCLK (APB Bus clock) selected with 1, 4, 16, 64, 256 and 1024 clock dividing selected

- Interrupt controller
  - Total 64 interrupt sources
  - Each interrupt source can be independently enabled
  - Priority mechanism to indicate highest priority interrupt
  - All the registers are accessed by CPU and PDMA
  - Unmasked interrupts can wake up the chip in sleep mode
  - Another set of source, mask and pending registers to serve for PDMA

- Watchdog timer
  - Generates WDT reset
  - A 16-bit Data register and a 16-bit counter
  - Counter clock uses the input clock selected by software
    - PCLK, EXTAL and RTCCLK can be used as the clock for counter
    - The division ratio of the clock can be set to 1, 4, 16, 64, 256 and 1024 by software

- PDMA Controller
  - Support up to 8 independent DMA channels
  - Descriptor or No-Descriptor Transfer mode
  - A simple Xburst®-1 CPU supports smart transfer mode controlled by programmable firmware
  - Transfer data units: 1-byte, 2-byte, 4-byte, 16-byte, 32-byte, 64-byte, 128-byte
  - Transfer number of data unit: $1 \sim 2^{24} - 1$
  - Independent source and destination port width: 8-bit, 16-bit, 32-bit
  - Fixed three priorities of channel groups: 0~3, highest; 4~11: mid; 12~31: lowest
  - An extra INTC IRQ can be bound to one programmable DMA channel

- RTC (Real Time Clock)
  - Need external 32768Hz oscillator for 32KHz clock generation.
  - RTCLK selectable from the oscillator or from the divided clock of EXCLK, so that 32k crystal can be absent if the hibernating mode is not needed
  - 32-bits second counter
  - Programmable and adjustable counter to generate accurate 1 Hz clock
  - Alarm interrupt, 1Hz interrupt
  - Stand alone power supply, work in hibernating mode
  - Power down controller
  - Alarm wakeup
  - External pin wakeup with up to 2s glitch filter

1.2.6 Peripherals

- General-Purpose I/O ports
  - Each port can be configured as an input, an output or an alternate function port
  - Each port can be configured as an interrupt source of low/high level or rising/falling edge triggering. Every interrupt source can be masked independently
  - Each port has an internal pull-up or pull-down resistor connected. The pull-up/down resistor can be disabled
  - GPIO output 4 interrupts, 1 for every group, to INTC

- Three I2C Controller (I2C0, I2C1, I2C2)
  - Two-wire I2C serial interface – consists of a serial data line (SDA) and a serial clock (SCL)
  - Two speeds
    - Standard mode (100 Kb/s)
    - Fast mode (400 Kb/s)
  - Device clock is identical with pclk
  - Programmable SCL generator
  - Master or slave I2C operation
  - 7-bit addressing/10-bit addressing
  - -level transmit and receive FIFOs
  - Interrupt operation
  - The number of devices that you can connect to the same I2C-bus is limited only by the maximum bus capacitance of 400pF

- One Synchronous serial interfaces (SSI0)
  - 3 protocols support: National's Microwire, TI's SSP, and Motorola's SPI
  - Full-duplex or transmit-only or receive-only operation
  - Programmable transfer order: MSB first or LSB first
  - Configurable normal transfer mode or Interval transfer mode
  - Programmable clock phase and polarity for Motorola's SSI format

- Two slave select signal (SSI0_CE0_ / SSI0_CE1_) supporting up to 2 slave devices
- Back-to-back character transmission/reception mode
- Loop back mode for testing
- Data transfer up to 30Mbits/s

- Three UARTs (UART0, UART1, UART2)
  - Full-duplex operation
  - 5-, 6-, 7- or 8-bit characters with optional no parity or even or odd parity and with 1, 1½, or 2 stop bits
  - Independently controlled transmit, receive (data ready or timeout), line status interrupts
  - Internal diagnostic capability Loopback control and break, parity, overrun and framing-error is provided
  - Separate DMA requests for transmit and receive data services in FIFO mode
  - Supports modem flow control by software or hardware
  - Slow infrared asynchronous interface that conforms to IrDA specification

- One MMC/SD/SDIO controllers
  - Fully compatible with the MMC System Specification version 4.5
  - Support SD Specification 3.0
  - Support SD I/O Specification 1.0 with 1 command channel and 4 data channels
  - Consumer Electronics Advanced Transport Architecture (CE-ATA – version 1.1)
  - Maximum data rate is 50Mbps
  - Both support MMC data width 1bit ,4bit
  - Built-in programmable frequency divider for MMC/SD bus
  - Built-in Special Descriptor DMA
  - Mask-able hardware interrupt for SDIO interrupt, internal status and FIFO status
  - Multi-SD function support including multiple I/O and combined I/O and memory
  - IRQ supported enable card to interrupt MMC/SD controller
  - Single or multi block access to the card including erase operation
  - Stream access to the MMC card
  - Supports SDIO read wait, interrupt detection during 1-bit or 4-bit access
  - Supports CE-ATA digital protocol commands
  - Support Command Completion Signal and interrupt to CPU
  - Command Completion Signal disable feature
  - The maximum block length is 4096bytes

- USB 2.0 OTG interface
  - Complies with the USB 2.0 standard for high-speed (480 Mbps) functions and with the On-The-Go supplement to the USB 2.0 specification
  - Operates either as the function controller of a high- /full-speed USB peripheral or as the host/peripheral in point-to-point or multi-point communications with other USB functions
  - Supports Session Request Protocol (SRP) and Host Negotiation Protocol (HNP)
  - UTMI+ Level 3 Transceiver Interface

- Soft connect/disconnect
- 8 endpoints in device mode, 16 channels for host mode.
- Dedicate FIFO
- Supports control, interrupt, ISO and bulk transfer

- OTP Slave Interface
  - Total 1Kb.

1.2.7 Bootrom

16KB Boot ROM memory

2 Pinout Information

2.1 Pin Map

The X1500 pin to ball assignment is shown in Figure 2-1.

X1500 Ball Assignment Ver1.1

BGA109, 8mm X 8mm X 1.2mm, 0.65pitch, top view

0	1	2	3	4	5	6	7	8	9	10	11	12
A	UART0_TXD_PC11	UART0_CTS_PC12	SFC_CE_SSI0_CE0_PA27	SFC_HOLD_SSI0_GPC_PA31	SFC_WP_SSI0_CE1_PA30	ZQ	VREF0	CIM_D3_PA16	CIM_D1_PA18	CIM_D5_PA14	CIM_D4_PA15	CIM_D7_PA12
B	UART0_RXD_PC10	UART0_RTS_PC13	SFC_CLK_SSI0_CLK_PA26	SFC_DR_SSI0_DR_PA28	SFC_DT_SSI0_DT_PA29				CIM_D2_PA17	CIM_D0_PA19	CIM_D6_PA13	CIM_VSYN_PA10
C	DMIC0_IN_PB22	AVDEFUSE									CIM_MCLK_PA11	CIM_HSYN_PA09
D	I2C0_SDA_PB24	I2C0_SCK_PB23			VDDMEM	VDDMEM	VDDMEM	VSS			CIM_PCLK_PA08	MSC0_CMD_SSI0_CE0_PA25
E	PWM0_PC25	PWM4_PC24		VSS	VSS	VDDMEM	VDDMEM	VSS	VSS		MSC0_D0_SSI0_DR_PA23	MSC0_CLK_SSI0_CLK_PA24
F	I2C1_SDA_PWM2_PC27	I2C1_SCK_PWM1_PC26		VSS	VSS			VDD	VDD		MSC0_D2_SSI0_CE1_PA21	MSC0_D1_SSI0_DT_PA22
G	BOOT_SEL0_PB28	BOOT_SEL1_PB29		VSS	VSS			VDD	VDD		UART1_TXD_PA05	MSC0_D3_SSI0_GPC_PA20
H	UART2_RXD_UART1_RTS_PD05	UART2_TXD_UART1_CTS_PD04		VSS	VSS	VSS	VDDIO	VDDIO	VDD		UART1_RXD_PA04	I2C1_SDA_PA01
J	SSI0_DR_UART1_TXD_PD03	SSI0_DT_UART1_RXD_PD02			VSS	VSS	VDDIO_5V	VDDIO		OTG_VBUS	UART2_RXD_PA02	UART2_TXD_PA03
K	SSI0_CLK_I2C2_SCK_PD00	SSI0_CE0_I2C2_SDA_PD01					VSSRTC	PLL_AVSS	AVSOTG	OTG_ID	PWM3_PB06	I2C1_SCK_PA00
L	I2S_MCLK_PB00	I2S_BCLK_PB01	I2S_LRCLK_PB02	WKUP_PB31	PPRST_	RTCLK	PWRON	DRV_VBUS_PB25	EXCLK_O		OTG_DM	AVDOTG25
M	I2S_DI_PB03	I2S_DO_PB04	DMIC1_IN_PB05	DMIC_CLK_PB21	LDOOUT	XRTCLK	VDDRTC	PLL_AVDD	EXCLK_I	OTG_TXR_RKL	OTG_DP	AVDOTG

Figure 2-1 X1500 pin to ball assignment

2.2 Pin Descriptions

2.2.1 GPIO Group A

Table 2-1 GPIO Group A Pinmux(30)

Ball No.	Ball Name	In/Out	Pull	Pull Default	Driven Strength	Schmitt	Slewrate limitate	GPIO	Func0	Func1	Func2	Extra Func	Power
K12	I2C1_SCK_PA00	IO	PU	Enable	8mA	No		GPA[0]			I2C1_SCK	WKUP	VDDIO
H12	I2C1_SDA_PA01	IO	PU	Enable	8mA	No		GPA[1]			I2C1_SDA	WKUP	VDDIO
J11	UART2_RXD_PA02	IO	PU	Enable	8mA	No		GPA[2]			UART2_RXD	WKUP	VDDIO
J12	UART2_TXD_PA03	IO	PU	Enable	8mA	No		GPA[3]			UART2_TXD	WKUP	VDDIO
H11	UART1_RXD_PA04	IO	PU	Enable	8mA	No		GPA[4]			UART1_RXD	WKUP	VDDIO
G11	UART1_TXD_PA05	IO	PU	Enable	8mA	No		GPA[5]			UART1_TXD	WKUP	VDDIO
D11	CIM_PCLK_PA08	IO	PU	Enable	8mA	No		GPA[8]			CIM_PCLK	WKUP	VDDIO
C12	CIM_HSYN_PA09	IO	PU	Enable	8mA	No		GPA[9]			CIM_HSYN	WKUP	VDDIO
B12	CIM_VSYN_PA10	IO	PU	Enable	8mA	No		GPA[10]			CIM_VSYN	WKUP	VDDIO
C11	CIM_MCLK_PA11	IO	PU	Enable	8mA	No		GPA[11]			CIM_MCLK	WKUP	VDDIO
A12	CIM_D7_PA12	IO	PU	Enable	8mA	No		GPA[12]			CIM_D7	WKUP	VDDIO
B11	CIM_D6_PA13	IO	PU	Enable	8mA	No		GPA[13]			CIM_D6	WKUP	VDDIO
A10	CIM_D5_PA14	IO	PU	Enable	8mA	No		GPA[14]			CIM_D5	WKUP	VDDIO
A11	CIM_D4_PA15	IO	PU	Enable	8mA	No		GPA[15]			CIM_D4	WKUP	VDDIO
A8	CIM_D3_PA16	IO	PU	Enable	8mA	No		GPA[16]			CIM_D3	WKUP	VDDIO
B9	CIM_D2_PA17	IO	PU	Enable	8mA	No		GPA[17]			CIM_D2	WKUP	VDDIO
A9	CIM_D1_PA18	IO	PU	Enable	8mA	No		GPA[18]			CIM_D1	WKUP	VDDIO

B10	CIM_D0_PA19	IO	PU	Enable	8mA	No		GPA[19]			CIM_D0	WKUP	VDDIO
G12	MSC0_D3_SSI0_GPC_PA20	IO	PU	Enable	8mA	No		GPA[20]		MSC0_D3	SSI0_GPC	WKUP	VDDIO
F11	MSC0_D2_SSI0_CE1_PA21	IO	PU	Enable	8mA	No		GPA[21]		MSC0_D2	SSI0_CE1	WKUP	VDDIO
F12	MSC0_D1_SSI0_DT_PA22	IO	PU	Enable	8mA	No		GPA[22]		MSC0_D1	SSI0_DT	WKUP	VDDIO
E11	MSC0_D0_SSI0_DR_PA23	IO	PU	Enable	8mA	No		GPA[23]		MSC0_D0	SSI0_DR	WKUP	VDDIO
E12	MSC0_CLK_SSI0_CLK_PA24	IO	PU	Enable	8mA	No		GPA[24]		MSC0_CLK	SSI0_CLK	WKUP	VDDIO
D12	MSC0_CMD_SSI0_CE0_PA25	IO	PU	Enable	8mA	No		GPA[25]		MSC0_CMD	SSI0_CE0	WKUP	VDDIO
B3	SFC_CLK_SSI0_CLK_PA26	IO	PU	Enable	8mA	No		GPA[26]		SFC_CLK	SSI0_CLK	WKUP	VDDIO
A3	SFC_CE_SSI0_CE0_PA27	IO	PU	Enable	8mA	No		GPA[27]		SFC_CE	SSI0_CE0	WKUP	VDDIO
B4	SFC_DR_SSI0_DR_PA28	IO	PU	Enable	8mA	No		GPA[28]		SFC_DR	SSI0_DR	WKUP	VDDIO
B5	SFC_DT_SSI0_DT_PA29	IO	PU	Enable	8mA	No		GPA[29]		SFC_DT	SSI0_DT	WKUP	VDDIO
A5	SFC_WP_SSI0_CE1_PA30	IO	PU	Enable	8mA	No		GPA[30]		SFC_WP	SSI0_CE1	WKUP	VDDIO
A4	SFC_HOLD_SSI0_GPC_PA31	IO	PU	Enable	8mA	No		GPA[31]		SFC_HOLD	SSI0_GPC	WKUP	VDDIO

2.2.2 GPIO Group B

Table 2-2 GPIO Group B Pinmux(15)

Ball No.	Ball Name	In/Out	Pull	Pull Default	Driven Strength	Schmitt	Slewrate limitate	GPIO	Func0	Func1	Func2	Extra Func	Power
L1	I2S_MCLK_PB00	IO	PU	Enable	8mA	No		GPB[0]		I2S_MCLK		WKUP	VDDIO
L2	I2S_BCLK_PB01	IO	PU	Enable	8mA	No		GPB[1]		I2S_BCLK		WKUP	VDDIO
L3	I2S_LRCLK_PB02	IO	PU	Enable	8mA	No		GPB[2]		I2S_LRCLK		WKUP	VDDIO
M1	I2S_DI_PB03	IO	PU	Enable	8mA	No		GPB[3]		I2S_DI		WKUP	VDDIO
M2	I2S_DO_PB04	IO	PU	Enable	8mA	No		GPB[4]		I2S_DO		WKUP	VDDIO
M3	DMIC1_IN_PB05	IO	PU	Enable	8mA	No		GPB[5]		DMIC1_IN		WKUP	VDDIO

K11	PWM3_PB06	IO	PU	Enable	8mA	No		GPB[6]			PWM3	WKUP	VDDIO
M4	DMIC_CLK_PB21	IO	PU	Enable	8mA	No		GPB[21]	DMIC_CLK			WKUP	VDDIO
C1	DMIC0_IN_PB22	IO	PU	Enable	8mA	No		GPB[22]	DMIC0_IN			WKUP	VDDIO
D2	I2C0_SCK_PB23	IO	PU	Enable	8mA	No		GPB[23]	I2C0_SCK			WKUP	VDDIO
D1	I2C0_SDA_PB24	IO	PU	Enable	8mA	No		GPB[24]	I2C0_SDA			WKUP	VDDIO
L8	DRV_VBUS_PB25	IO	PD	Enable	8mA	No		GPB[25]	DRV_VBUS			WKUP	VDDIO
G1	BOOT_SEL0_PB28	IO	PU	Disable	8mA	No		GPB[28]	BOOT_SEL0			WKUP	VDDIO
G2	BOOT_SEL1_PB29	IO	PU	Disable	8mA	No		GPB[29]	BOOT_SEL1			WKUP	VDDIO
L4	WKUP_PB31	IO	PU	Enable	8mA	Yes		GPB[31]	WKUP			WKUP	VDDRTC

2.2.3 GPIO Group C

Table 2-3 GPIO Group C Pinmux(8)

Ball No.	Ball Name	In/Out	Pull	Pull Default	Driven Strength	Schmitt	Slewrate limitate	GPIO	Func0	Func1	Func2	Extra Func	Power
B1	UART0_RXD_PC10	IO	PU	Enable	8mA	No		GPC[10]	UART0_RXD			WKUP	VDDIO
A1	UART0_TXD_PC11	IO	PU	Enable	8mA	No		GPC[11]	UART0_TXD			WKUP	VDDIO
A2	UART0_CTS_PC12	IO	PU	Enable	8mA	No		GPC[12]	UART0_CTS			WKUP	VDDIO
B2	UART0_RTS_PC13	IO	PU	Enable	8mA	No		GPC[13]	UART0_RTS			WKUP	VDDIO
E2	PWM4_PC24	IO	PU	Enable	8mA	No		GPC[24]	PWM4			WKUP	VDDIO
E1	PWM0_PC25	IO	PD	Enable	8mA	No		GPC[25]	PWM0			WKUP	VDDIO
F2	I2C1_SCK_PWM1_PC26	IO	PU	Enable	8mA	No		GPC[26]	I2C1_SCK	PWM1		WKUP	VDDIO
F1	I2C1_SDA_PWM2_PC27	IO	PU	Enable	8mA	No		GPC[27]	I2C1_SDA	PWM2		WKUP	VDDIO

2.2.4 GPIO Group D

Table 2-4 GPIO Group D Pinmux(6)

Ball No.	Ball Name	In/ Out	Pull	Pull Default	Driven Strength	Schmitt	Slewrate limitate	GPIO	Func0	Func1	Func2	Extra Func	Power
K1	SSI0_CLK_I2C2_SCK_PD00	IO	PU	Enable	8mA	No	5V	GPD[0]	SSI0_CLK	I2C2_SCK		WKUP	VDDIO_5T
K2	SSI0_CE0_I2C2_SDA_PD01	IO	PU	Enable	8mA	No	5V	GPD[1]	SSI0_CE0	I2C2_SDA		WKUP	VDDIO_5T
J2	SSI0_DT_UART1_RXD_PD02	IO	PU	Enable	8mA	No	5V	GPD[2]	SSI0_DT	UART1_RXD		WKUP	VDDIO_5T
J1	SSI0_DR_UART1_TXD_PD03	IO	PU	Enable	8mA	No	5V	GPD[3]	SSI0_DR	UART1_TXD		WKUP	VDDIO_5T
H2	UART2_TXD_UART1_CTS_PD04	IO	PU	Enable	8mA	No	5V	GPD[4]	UART2_TXD	UART1_CTS		WKUP	VDDIO_5T
H1	UART2_RXD_UART1_RTS_PD05	IO	PU	Enable	8mA	No	5V	GPD[5]	UART2_RXD	UART1_RTS		WKUP	VDDIO_5T

2.3 X1500 FUNCTION PIN DESCRIPTION

Table 2-5 X1500 function pin description

Ball No.	Pin Names	IO	Power	Pin Description
Memory				
A6	ZQ			DDR PHY ZQ calibration resistor
A7	VREF0			DDR PHY VREF
Power and Ground				
D5	VDDMEM	P	-	IO digital power for DRAM 1.8V
D6	VDDMEM	P	-	IO digital power for DRAM 1.8V
D7	VDDMEM	P	-	IO digital power for DRAM 1.8V

E6	VDDMEM	P	-	IO digital power for DRAM 1.8V
E7	VDDMEM	P	-	IO digital power for DRAM 1.8V
H7	VDDIO	P	-	IO digital power for none DRAM 1.8~3.3V
H8	VDDIO	P	-	IO digital power for none DRAM 1.8~3.3V
J8	VDDIO	P	-	IO digital power for none DRAM 1.8~3.3V
J7	VDDIO_5T	P	-	IO digital power for none DRAM (5V tolerant)
D8	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
E4	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
E5	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
E8	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
E9	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
F4	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
F5	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
G4	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
G5	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
H4	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
H5	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
H6	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
J5	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
J6	VSS	P	-	Core digital gound for none DRAM and CORE digital ground, 0V
F8	VDD	P	-	CORE digital power, 1.2V
F9	VDD	P	-	CORE digital power, 1.2V
G8	VDD	P	-	CORE digital power, 1.2V
G9	VDD	P	-	CORE digital power, 1.2V
H9	VDD	P	-	CORE digital power, 1.2V
USB OTG				

M11	USB_DP0(OTG_DP)	AIO	AVDOTG	USB OTG data plus
L11	USB_DM0(OTG_DM)	AIO	AVDOTG	USB OTG data minus
J10	USB_VBUS(OTG_VBUS)	AIO	5V	USB 5-V power supply pin for USB OTG. An external charge pump must provide power to this pin
K10	USB_ID(OTG_ID)	AI	AVDOTG25	USB mini-receptacle identifier. It differentiates a mini-A from a mini-B plug. If this signal is not used, internal resistance pulls the signal's voltage level to AVDUSB25.
M10	OTG_TXR_RKL	AIO	AVDOTG25	Transmitter resister tune. It connects to an external resistor of 43.2Ω with 1% tolerance to analog ground, that adjusts the USB 2.0 high-speed source impedance
M12	AVDOTG	P	-	USB analog power.3.3V
K9	AVSOTG	P	-	USB analog ground.
L12	AVDOTG25	P	-	USB OTG analog power, 2.5V
EFUSE				
C2	AVDEFUSE	P	AVEFUSE	EFUSE programming power, 0V/2.5V
CPM				
M9	EXCLK_XI(EXCLK_I)	AI	VDDIO	OSC input.
L9	EXCLK_XO(EXCLK_O)	AO	VDDIO	OSC output.
M8	PLL_AVDD	P	-	PLL analog power, 1.2V
K8	PLL_AVSS	P	-	PLL analog ground
RTC				
L6	RTCLK	AI	VDDRTC	OSC input or 32768Hz clock input
L7	PWRON	O	VDDRTC	Power on/off control of main power
L5	PPRST_	I	VDDRTC	RTC power on reset and RESET-KEY reset input
M5	LDOOUT	P	-	capacitor pin for RTC LDO need a 1nF decoupling capacitor to ground
K7	VSSRTC	P	-	RTC ground
M7	VDDRTC	P	-	VDDRTC: 3.3V power for RTC and hibernating mode controlling that never power down(normally you can use 1.8V instead to reduce power consumption)

2.4 X1500 FUNCTION DESCRIPTION

Table 2-6 X1500 Function Description

Signal Name	In/Out	Description
CIM(Camera Interface)		
CIM_PCLK	Input	CIM pixel clock input
CIM_HSYN	Input	CIM line horizonal sync input
CIM_VSYN	Input	CIM vertical sync input
CIM_MCLK	Output	CIM master clock output
CIM_D7	Input	CIM data input bit 7
CIM_D6	Input	CIM data input bit 6
CIM_D5	Input	CIM data input bit 5
CIM_D4	Input	CIM data input bit 4
CIM_D3	Input	CIM data input bit 3
CIM_D2	Input	CIM data input bit 2
CIM_D1	Input	CIM data input bit 1
CIM_D0	Input	CIM data input bit 0
I2S		
I2S_MCLK	Output	I2S master clock out
I2S_BCLK	Bidirection	I2S bit clock
I2S_LRCLK	Bidirection	I2S LR clock
I2S_DI	Input	I2S data input
I2S_DO	Output	I2S data output
DMIC		
DMIC0_IN	Input	Digital MIC data input(Front/Back channel)
DMIC1_IN	Input	Digital MIC data input(Left/Right channel)

DMIC_CLK	Output	Digital MIC clock output
SFC		
SFC_CLK	Output	Serial Flash clock output
SFC_CE_	Output	Serial Flash chip enable
SFC_DR	Bidirection	Serial Flash data input
SFC_DT	Bidirection	Serial Flash data output
SFC_WP	Bidirection	Serial Flash write protect signal
SFC_HOLD	Bidirection	Serial Flash hold signal
PWM		
PWMn	Bidirection	PWM output or pulse input channel n
I2C		
I2Cn_SCK	Bidirection	I2C n serial clock
I2Cn_SDA	Bidirection	I2C n serial data
SSI		
SSIn_CLK	Output	SSI n clock output
SSIn_CE0_	Output	SSI n chip enable 0
SSIn_CE1_	Output	SSI n chip enable 1
SSIn_GPC	Output	SSI n general-purpose control signal
SSIn_DT	Output	SSI n data output
SSIn_DR	Input	SSI n data input
UART		
UARTn_RXD	Input	UART n receiving data
UARTn_TXD	Output	UART n transmitting data
UARTn_CTS_	Input	UART Clear to send control
UARTn_RTS_	Output	UART Request to send control
MSC		

MSCn_D3	Bidirection	MSC(MMC/SD) n data bit 3
MSCn_D2	Bidirection	MSC(MMC/SD) n data bit 2
MSCn_D1	Bidirection	MSC(MMC/SD) n data bit 1
MSCn_D0	Bidirection	MSC(MMC/SD) n data bit 0
MSCn_CLK	Output	MSC(MMC/SD) n clock output
MSCn_CMD	Bidirection	MSC(MMC/SD) n command
USB 2.0 OTG		
DRV_VBUS	Output	USB OTG VBUS driver control signal

NOTES:

1 The meaning of phases in IO cell characteristics are:

a Bi-dir, Single-end: bi-direction and single-ended DDR IO are used.

b Output, Single-end: output and single-ended DDR IO are used.

c Output, Differential: output and differential signal DDR IO are used.

d Bi-dir, Differential: bi-direction and differential signal DDR IO are used.

e 4mA, 8mA, 16mA out: The IO cell's output driving strength is about 4mA,8mA,16mA.
4/8mA means the IO cell's output driving strength is selected and can be set as 4mA or 8mA.
2/4mA means the IO cell's output driving strength is selected and can be set as 2mA or 4mA.

f Pull-up: The IO cell contains a pull-up resistor.

g Pull-down: The IO cell contains a pull-down resistor.

h Pullup-pe: The IO cell contains a pull-up resistor and the pull-up resistor can be enabled or disabled by setting corresponding register.

i Pulldown-pe: The IO cell contains a pull-down resistor and the pull-down resistor can be enabled or disabled by setting corresponding register.

j rst-pe: these pins are initialed (during reset and after reset) to IO internal pull (up or down) enabled. Otherwise, the pins are initialed to pull disabled

k Schmitt: The IO cell is Schmitt trig input.

l ~SL: The IO cell do not limited slew rate.

2 All GPIO shared pins are reset to GPIO input

3 Electrical Specifications

3.1 Absolute Maximum Ratings

The absolute maximum ratings for the processors are listed in Table 3-1. Do not exceed these parameters or the part may be damaged permanently. Operation at absolute maximum ratings is not guaranteed.

Table 3-1 Absolute Maximum Ratings

Parameter	Min	Max	Unit
Storage Temperature	-65	150	°C
Operation Temperature	-40	85	°C
VDDMEM power supplies voltage	-0.5	1.98	V
VDDIO power supplies voltage	-0.5	3.6	V
VDDIO_5T power supplies voltage	-0.5	3.6	V
VDD core power supplies voltage	-0.2	1.32	V
PLLAVDD power supplies voltage	-0.2	1.32	V
AVDEFUSE power supplies voltage	-0.5	2.75	V
VDDRTC power supplies voltage	-0.5	3.63	V
AVDOTG25 power supplies voltage	-0.5	2.75	V
AVDOTG power supplies voltage	-0.5	3.63	V
Input voltage to VDDMEM supplied non-supply pins	-0.3	1.98	V
Input voltage to VDDIO_5T supplied non-supply pins with 5V tolerance	-0.5	5.5	V
Input voltage to VDDIO supplied non-supply pins without 5V tolerance	-0.5	3.6	V
Input voltage to VDDRTC supplied non-supply pins	-0.5	3.6	V
Input voltage to AVDOTG25 supplied non-supply pins	-0.5	2.75	V
Input voltage to AVDOTG supplied non-supply pins	-0.5	3.63	V
Output voltage from VDDMEM supplied non-supply pins	-0.5	1.98	V
Output voltage from VDDIO supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDIO_5T supplied non-supply pins	-0.5	3.6	V
Output voltage from VDDRTC supplied non-supply pins	-0.5	3.6	V
Output voltage from AVDOTG25 supplied non-supply pins	-0.5	2.75	V
Output voltage from AVDOTG supplied non-supply pins	-0.5	3.6	V
Maximum ESD stress voltage, Human Body Model; Any pin to any supply pin, either polarity, or Any pin to all non-supply pins together, either polarity. Three stresses maximum.		2000	V

3.2 Recommended operating conditions

Table 3-2 Recommended operating conditions for power supplies

Symbol	Description	Min	Typical	Max	Unit
VMEM	VDDMEM voltage for LPDDR	1.65	1.8	1.95	V
	VDDMEM voltage for SSTL18 (DDR2)	1.7	1.8	1.9	V
	VDDMEM voltage for DDR3	1.425	1.5	1.575	V
	VDDMEM voltage for DDR3L	1.28	1.35	1.45	V
VIO(1.8V)	VDDIO voltage, use as 1.8V	1.62	1.8	1.98	V
VIO5(1.8V)	VDDIO_5T voltage, use as 1.8V	1.62	1.8	1.98	V
VIO(2.5V)	VDDIO voltage, use as 2.5V	2.25	2.5	2.75	V
VIO5(2.5V)	VDDIO_5T voltage, use as 2.5V	2.25	2.5	2.75	V
VIO(3.3V)	VDDIO voltage, use as 3.3V	2.97	3.3	3.63	V
VIO5(3.3V)	VDDIO_5T voltage, use as 3.3V	2.97	3.3	3.63	V
VCORE	VDD core voltage	1.08	1.2	1.32	V
VPLL12	PLLAVDD voltage	1.08	1.25	1.32	V
VEFUSE	AVDEFUSE voltage	2.25	2.5	2.75	V
VRTC33	VDDRTC voltage	1.8	1.8	3.63	V
VUSB25	AVDOTG25 voltage	2.25	2.5	2.75	V
VUSB33	AVDOTG voltage	3.0	3.3	3.6	V

Table 3-3 Recommended operating conditions for VDDMEM supplied pins

Symbol	Parameter	Min	Typical	Max	Unit
VI18	Input voltage for LPDDR applications	0	1.8	1.9	V
VO18	Output voltage for LPDDR applications	0	1.8	1.9	V

Table 3-4 Recommended operating conditions for VDDIO/VDDIO_5T/VDDRTC supplied pins

Symbol	**Parameter**	**Min**	**Typical**	**Max**	**Unit**
VIH18	Input high voltage for 1.8V I/O application	1.17	1.8	3.6	V
VIL18	Input low voltage for 1.8V I/O application	–0.3	0	0.63	V
VIH25	Input high voltage for 2.5V I/O application	1.7	2.5	3.6	V
VIL25	Input low voltage for 2.5V I/O application	–0.3	0	0.7	V
VIH33	Input high voltage for 3.3V I/O application	2	3.3	3.6	V
VIL33	Input low voltage for 3.3V I/O application	–0.3	0	0.8	V

Table 3-5 Recommended operating conditions for others

Symbol	**Description**	**Min**	**Typical**	**Max**	**Unit**
TA	Ambient temperature	–40		85	℃

3.3 DC Specifications

The DC characteristics for each pin include input-sense levels and output-drive levels and currents. These parameters can be used to determine maximum DC loading, and also to determine maximum transition times for a given load. All DC specification values are valid for the entire temperature range of the device.

Table 3-6 DC characteristics for V_{REFMEM}

Symbol	Parameter	Min	Typical	Max	Unit
VREFM	Reference voltage supply	0.49	0.5	0.51	VMEM

Table 3-7 DC characteristics for VDDmem supplied pins in LPDDR application

Symbol	Parameter	Min	Typical	Max	Unit
$V_{IH(DC)}$	Input logic threshold High	0.7* VMEM		VMEM+0.3	V
$V_{IL(DC)}$	Input logic threshold Low	VMEM-0.3		0.3* VMEM	V
VIH(AC)	AC Input logic High	0.8* VMEM		VMEM+0.3	V
VIL(AC)	AC Input logic Low	VMEM-0.3		0.2* VMEM	V
VOH	DC output logic High (IOH=-0.1mA)	0.9*VMEM			V
VOL	DC output logic Low (IOL=0.1mA)			0.1 *VMEM	V
ILL	Input leakage current		0.01	6.45	uA
IMEM	VMEM quiescent current		0.02	15.03	uA

Table 3-8 DC characteristics for VDDIO/VDDIO_5T/VDDRTC supplied pins for 1.8V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	0.79	0.86	0.94	V
V_{T+}	Schmitt trig low to high threshold point	0.95	1.06	1.16	V
V_{T-}	Schmitt trig high to low threshold point	0.58	0.69	0.79	V
V_{TPU}	Threshold point with pull-up resistor enabled	0.79	0.86	0.94	V
V_{TPD}	Threshold point with pull-down resistor enabled	0.79	0.86	0.94	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled	0.95	1.06	1.16	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled	0.58	0.68	0.78	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled	0.96	1.07	1.17	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled	0.59	0.69	0.79	V
I_L	Input Leakage Current @ V_I=1.8V or 0V			±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V			±10	μA

R_{PU}	Pull-up Resistor		66	114	211	kΩ
R_{PD}	Pull-down Resistor		58	103	204	kΩ
V_{OL}	Output low voltage				0.45	V
V_{OH}	Output high voltage		1.35			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	5.3	9.8	15.8	mA
		16mA	10.8	19.7	31.8	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	3.3	8.3	16.6	mA
		16mA	6.6	16.5	33.2	mA

Table 3-9 DC characteristics for VDDIO/VDDIO_5T/VDDRTC supplied pins for 2.5V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.06	1.17	1.27	V
V_{T+}	Schmitt trig low to high threshold point	1.27	1.40	1.50	V
V_{T-}	Schmitt trig high to low threshold point	0.86	0.98	1.09	V
V_{TPU}	Threshold point with pull-up resistor enabled	1.05	1.16	1.25	V
V_{TPD}	Threshold point with pull-down resistor enabled	1.06	1.17	1.27	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled	1.27	1.39	1.48	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled	0.85	0.97	1.08	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled	1.27	1.41	1.50	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled	0.88	0.99	1.10	V
I_L	Input Leakage Current @ V_I=1.8V or 0V			±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V			±10	μA
R_{PU}	Pull-up Resistor	43	69	120	kΩ
R_{PD}	Pull-down Resistor	41	66	124	kΩ
V_{OL}	Output low voltage			0.7	V
V_{OH}	Output high voltage	1.7			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	11.6	19.4	28.4	mA
		16mA	23.3	39.1	57.2	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	9.3	19.4	34.6	mA
		16mA	18.6	38.7	69.2	mA

Table 3-10 DC characteristics for VDDIO/VDDIO_5T/VDDRTC supplied pins for 3.3V application

Symbol	Parameter	Min	Typical	Max	Unit
V_T	Threshold point	1.39	1.50	1.65	V
V_{T+}	Schmitt trig low to high threshold point	1.62	1.75	1.90	V
V_{T-}	Schmitt trig high to low threshold point	1.18	1.29	1.44	V

V_{TPU}	Threshold point with pull-up resistor enabled		1.36	1.48	1.64	V
V_{TPD}	Threshold point with pull-down resistor enabled		1.40	1.52	1.66	V
V_{TPU+}	Schmitt trig low to high threshold point with pull-up resistor enabled		1.62	1.75	1.89	V
V_{TPU-}	Schmitt trig high to low threshold point with pull-down resistor enabled		1.16	1.28	1.43	V
V_{TPD+}	Schmitt trig low to high threshold point with pull-down resistor enabled		1.64	1.77	1.91	V
V_{TPD-}	Schmitt trig high to low threshold point with pull-up resistor enabled		1.19	1.31	1.45	V
I_L	Input Leakage Current @ V_I=1.8V or 0V				±10	μA
I_{OZ}	Tri-State output leakage current @ V_I=1.8V or 0V				±10	μA
R_{PU}	Pull-up Resistor		34	51	81	kΩ
R_{PD}	Pull-down Resistor		35	51	88	kΩ
V_{OL}	Output low voltage				0.4	V
V_{OH}	Output high voltage		2.4			V
I_{OL}	Low level output current @ V_{OL}(max)	8mA	10.0	15.2	20.2	mA
		16mA	20.2	30.6	40.6	mA
I_{OH}	High level output current @ V_{OH}(min)	8mA	13.9	28.0	48.2	mA
		16mA	27.8	56.0	96.3	mA

3.4 Power On, Reset and BOOT

3.4.1 Power-On Timing

The external voltage regulator and other power-on devices must provide the X1500 processor with a specific sequence of power and resets to ensure proper operation. Figure 3-1shows this sequence and Table 3-11 gives the timing parameters. Following are the name of the power.

- VDDRTC: VDDRTC
- VDD: all 1.25V power supplies, include VDDCORE, PLLAVDD
- VDDIO: all other digital IO, include DDR power supplies: VDDMEM, VDDIO, VDDIO_5T
- AVD: all other analog power supplies: AVDOTG25, AVDOTG
- AVDEFUSE

Table 3-11 Power-On Timing Parameters

Symbol	Parameter	Min	Max	Unit
t_{R_VDDRTC}	VDDRTC rise time[1]	0	5	ms
t_{R_VDDIO}	VDDIO rise time[1]	0	5	ms

t_{D_VDDIO}	Delay between VDD arriving 50% (or 90%) to VDDIO arriving 50% (or 90%)	0	–	ms
t_{R_VDD}	VDD rise time[1]	0	5	ms
t_{D_VDD}	Delay between VDDRTC arriving 50% (or 90%) to VDD arriving 50% (or 90%)	0	1	ms
t_{R_AVD}	AVD rise time[1]	0	5	ms
t_{D_AVD}	Delay between VDDIO arriving 90% to AVD arriving 90%	0	1	ms
$t_{D\_PPRST\_}$	Delay between AVD stable and PPRST_ de-asserted	TBD[3]	–	ms[2]
$t_{D\_AVDEFUSE}$	Delay between PPRST_ finished and E-fuse programming power apply	0	–	ms

NOTES:

1 The power rise time is defined as 10% to 90%.

2 The PPRST_ must be kept at least 100us. After PPRST_ is deasserted, the corresponding chip reset will be extended at least 40ms.

3 It must make sure the EXCLK is stable and all power(except AVDEFUSE) is stable.

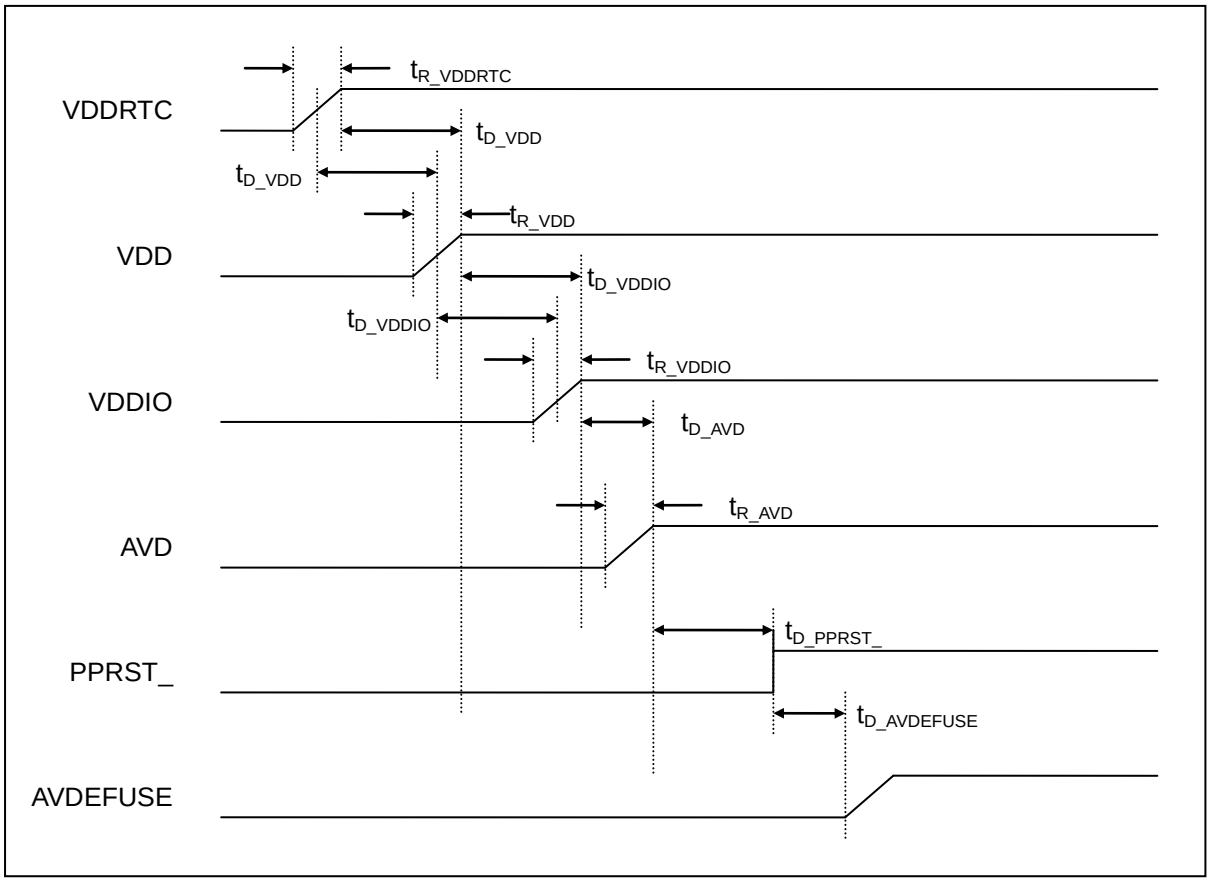


Figure 3-1 Power-On Timing Diagram

3.4.2 Reset procedure

There 3 reset sources: 1 PPRST_ pin reset; 2 WDT timeout reset; and 3 hibernating reset when exiting hibernating mode. After reset, program start from boot.

1 PPRST_ pin reset.
This reset is trigged when PPRST_ pin is put to logic 0. It happens in power on RTC power and RESET-KEY pressed to reset the chip from unknown dead state. The reset end time is about 1M EXCLK cycles after rising edge of PPRST_.

2 WDT reset.
This reset happens in case of WDT timeout. The reset keeps for about a few RTCLK cycles.

3 Hibernating reset.
This reset happens in case of wakeup the main power from power down. The reset keeps for about 1ms ~ 125ms programable, plus 1M EXCLK cycles, start after WKUP_ signal is recognized.

After reset, all GPIO shared pins are put to GPIO input function and most of their internal pull-up/down resistor are set to on, see “2.5 Pin Descriptions” for details. The PWRON is output 1. The oscillators

are on. The USB 2.0 OTG PHY, the audio CODEC DAC/ADC put in suspend mode.

3.4.3 BOOT

The boot sequence of the X1500 is controlled by boot_sel [1:0] pin values. The following table lists them:

Table 3-12 Boot Configuration of X1500

boot_sel[1]	boot_sel[0]	Boot configuration
1	1	Boot from SFC0
0	1	Boot from MSC0
1	0	Boot from USB 2.0 device

X: means "Don't Care"

The boot procedure is showed in the following flow chart:

After reset, the boot program on the internal boot ROM executes as follows:

1 Disable all interrupts and read boot_sel[2:0] to determine the boot method.

2 If it is boot from MMC/SD card at MSC0, its function pins MSC0_D0, MSC0_CLK, MSC0_CMD are initialized, the boot program loads the 12KB code from MMC/SD card to tcsm and jump to it. Only one data bus which is MSC0_D0 is used. The clock EXTCLK/128 is used initially. When reading data, the clock EXTCLK/4 is used.

3 If it is boot from USB, a block of code will be received through USB cable connected with host PC and be stored in tcsm. Then branch to this area in tcsm.

4 If it is boot from SPI nor/nand at SFC, its function pins SFC_CLK,SFC_CE,SFC_DR,SFC_DT, SFC_WP, SFC_HOLD are initialized, the boot program loads the 12KB code from MMC/SD card to tcsm and jump to it.

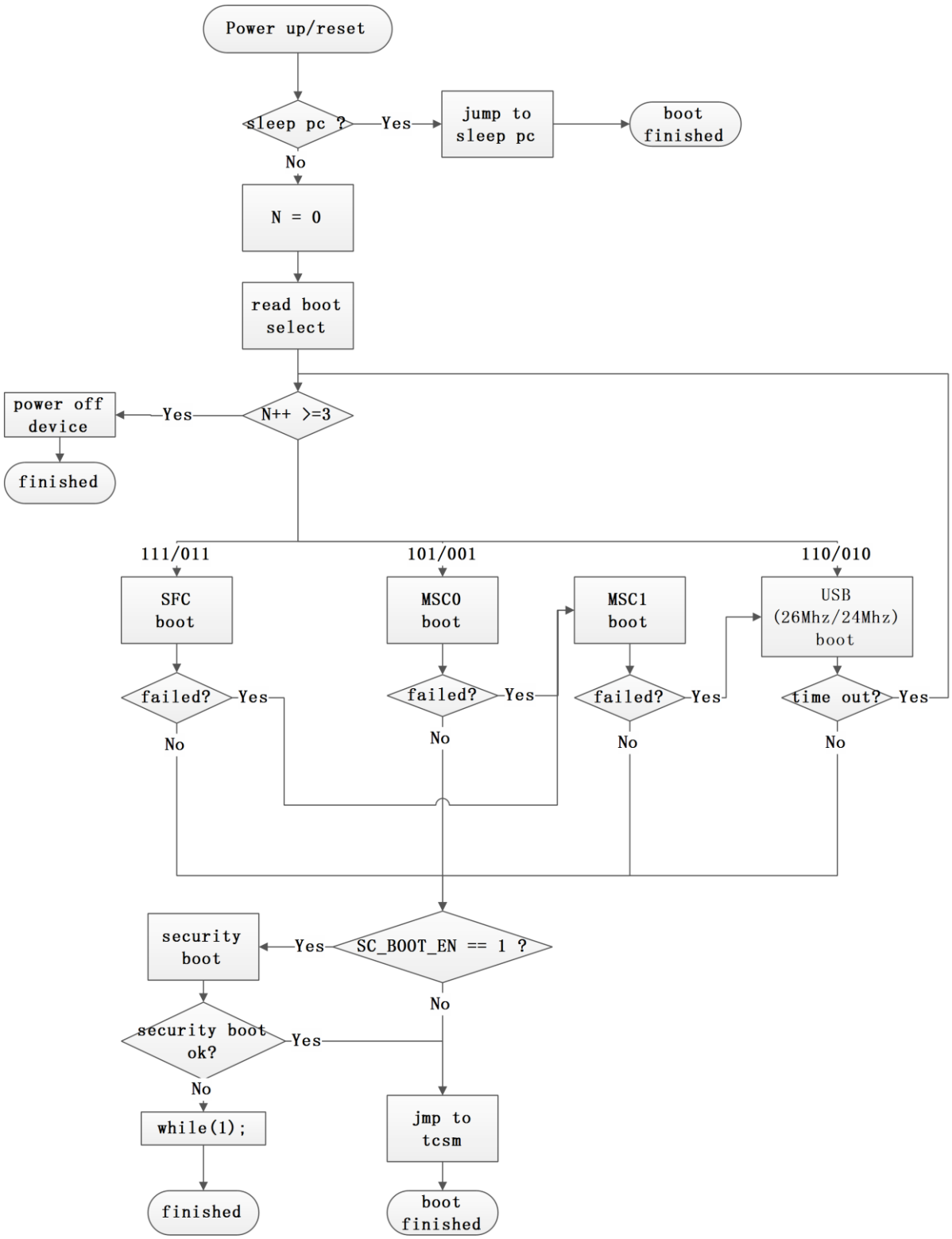


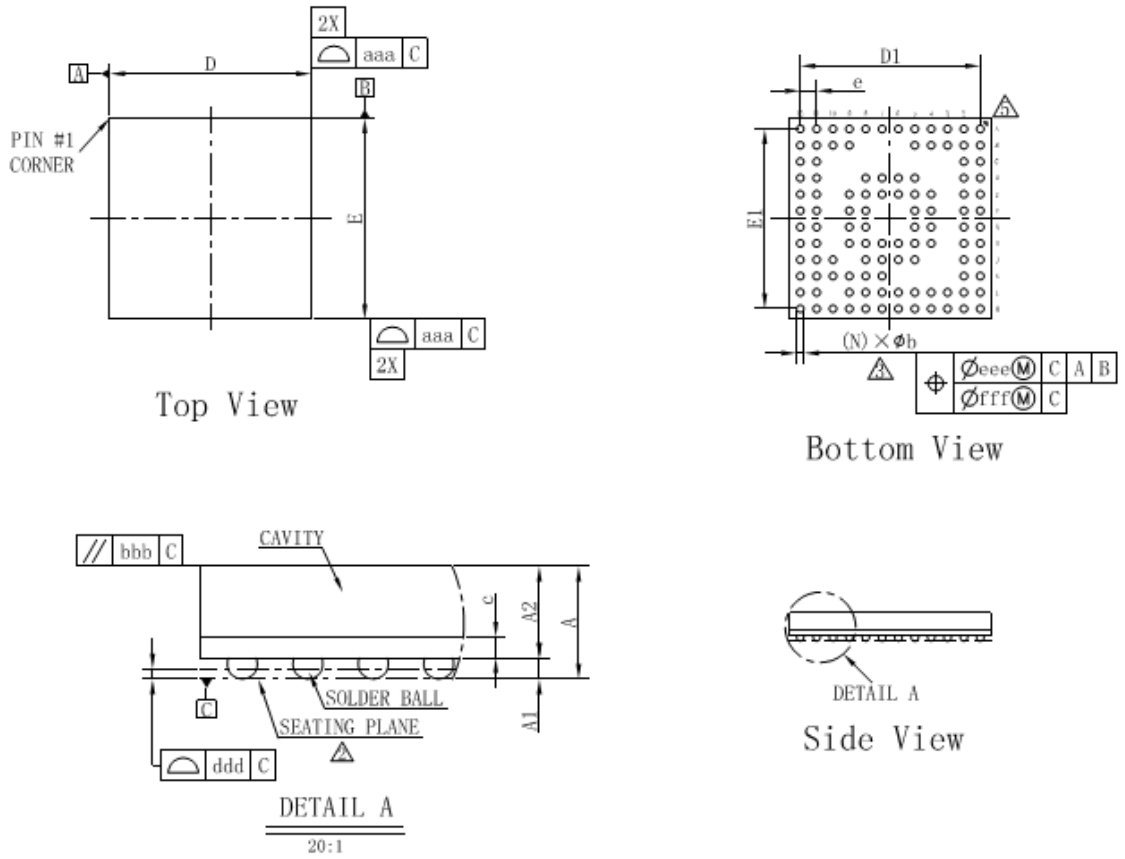
Figure 3-2 Boot flow diagram of X1500

4 Packaging Information

4.1 Overview

X1500 processor is offered in 109-pin BGA package, which is 8mm X 8mm X 1.2mm, 12 x 12 matrix ball grid array and 0.65mm ball pitch, show in Figure 4-1.

4.2 X1500 Device Dimensions



symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	—	—	1.220	---	--	0.048
A1	0.160	0.210	0.260	0.006	0.008	0.010
A2	0.860	0.910	0.960	0.034	0.036	0.038
c	0.170	0.210	0.250	0.007	0.008	0.010
D	7.900	8.000	8.100	0.311	0.315	0.319
E	7.900	8.000	8.100	0.311	0.315	0.319
D1	—	7.150	—	—	0.281	—
E1	--	7.150	--	--	0.281	--
e	—	0.650	—	--	0.026	—
b	0.250	0.300	0.350	0.010	0.012	0.014
aaa	0.100			0.004		
bbb	0.100			0.004		
ddd	0.080			0.003		
eee	0.150			0.006		
fff	0.080			0.003		
Ball Diam	0.300			0.012		
N	109			109		
MD/ME	12/12			12/12		

Figure 4-1 X1500 package outline drawing

Notes:

1. BALL PAD OPENING: 0.270mm；
2. PRIMARY DATUM C AND SEATING PLANE ARE THE SOLDER BALLS；
3. DIMENSION b IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER,PARALLEL TO PRIMARY DATUM C；
4. SPECIAL CHARACTERISTICS C CLASS: bbb,ddd；
5. THE PATTERN OF PIN 1 FIDUCIAL IS FOR REFERENCE ONLY；
6. BAN TO USE THE LEVEL 1 ENVIRONMENT-RELATED SUBSTANCES OF JCET PRESCRIBING；
7. ALL UNITS ARE IN MILLIMETER；

4.3 Solder Ball Materials

Both the top (joint) and bottom solder ball materials of X1500 are SAC105.

4.4 Moisture Sensitivity Level

X1500 package moisture sensitivity is level 3.

5 PCB Mounting Guidelines

5.1 RoHS compliance

TBD.

5.2 Reflow profile

X1500 package is lead-free. It's reflow profile follows the IPC/JEDEC lead-free reflow profile as contained in J-STD-020C.