# Status Register:

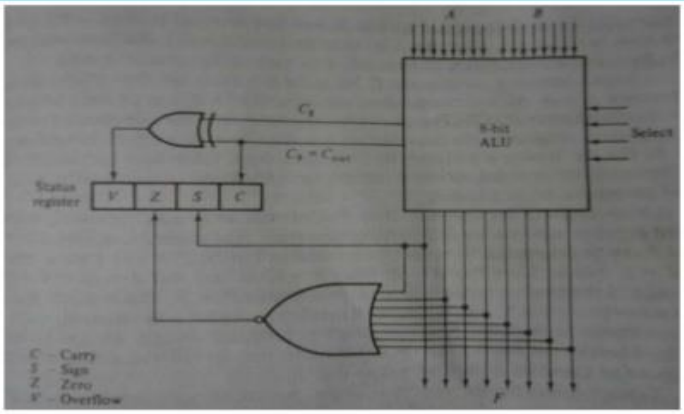
A **status register**, flag **register**, or **condition** code **register** (CCR) is a collection of **status** flag **bits** for a processor. For example, a Z **bit** may be set if the result of the operation is zero and cleared if it is nonzero. Other classes of instructions may also modify the flags to indicate **status**.

The **status register** lets an instruction take action contingent on the outcome of a previous instruction. Typically, flags in the **status register** are modified as effects of arithmetic and bit manipulation operations.

## Status register

- Relative magnitude of two numbers may be determined by subtracting one from the other.
- Also called as flag bits or condition code bits
- Status Bits
  - C – Carry
  - S – Sign bit
  - Z – zero bit
  - V – Overflow bit

## Status register



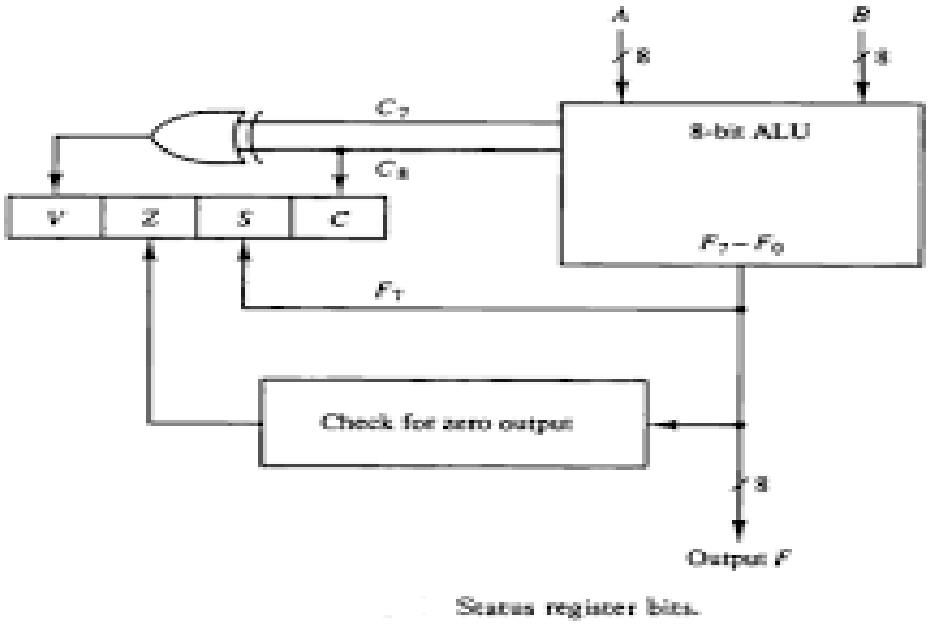
# Status register

- C – Carry bit
  - Set if the output carry of ALU is 1
- S – Sign bit
  - Set if the highest order bit is 1
- Z – Zero bit
  - Set if the ALU's output contains all zeros
- V - Overflow bit
  - Set if there is any overflow. For a 8bit ALU, V is set if the result is greater than 127 and less than -128

# (A-B) of unsigned numbers

A and B are unsigned numbers

| Relation | Condition of status bits | Boolean function |
|---|---|---|
| A>B | C=1 and Z=0 | CZ' |
| A>=B | C=1 | C |
| A<B | C=0 | C' |
| A<=B | C=0 or Z=1 | C'+Z |
| A=B | Z=1 | Z |
| A≠B | Z=0 | Z' |




Status register bits.

## 5.5. ALU status register

The ALU results are characterized by four status bits (C, S, Z, and V), which are defined as follows:

- Bit Cy (carry) is set to 1 only when the operation is an arithmetic operation and its carry output is 1. It is cleared to 0 if the carry is 0.
- Bit S (sign) is set to 1 if the most significant bit of the result C3 is one..
- Bit Z (zero) is set to 1 only if the output of the ALU contains all 0's. It is set to 0 otherwise.
- Bit V (overflow) is set to 1 only when an overflow occurs when performing operations on signed numbers in 2's complement representation (exclusive-OR of the 2 most significant carries).

Derive the logic equations of the status bits and implement them with conventional gates.