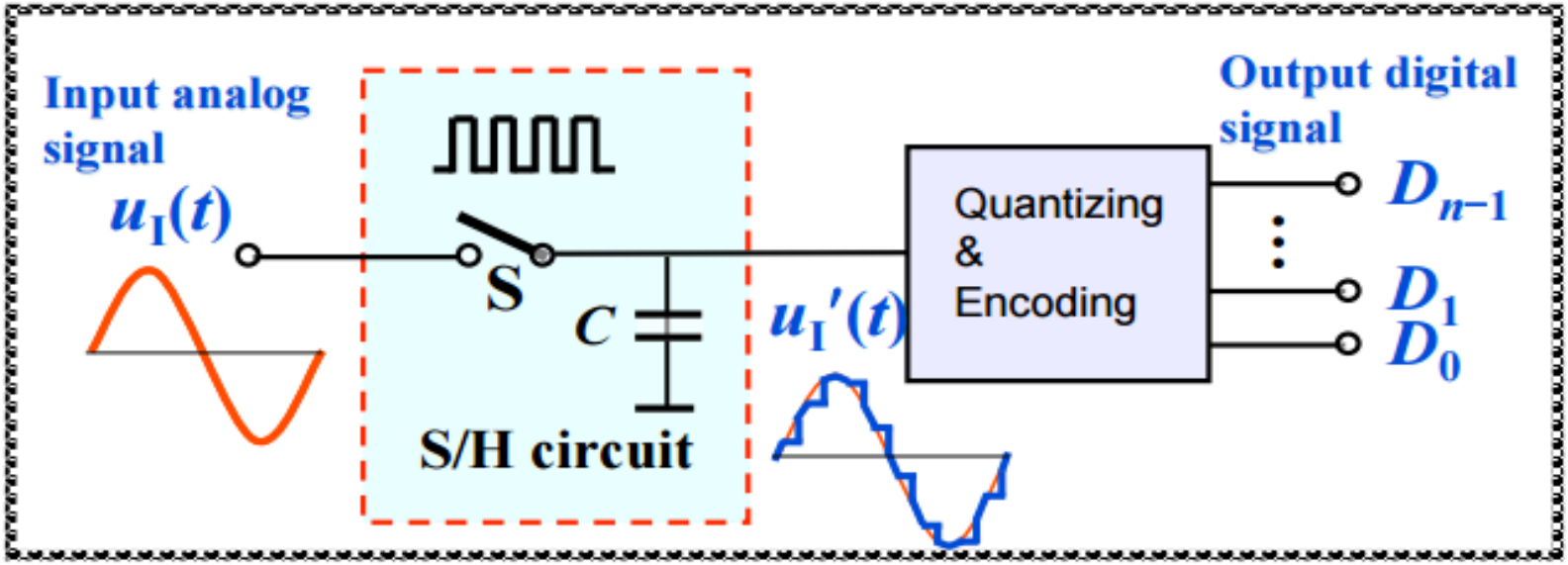
ANALOGUE TO DIGITAL CONVERSION (ADC)

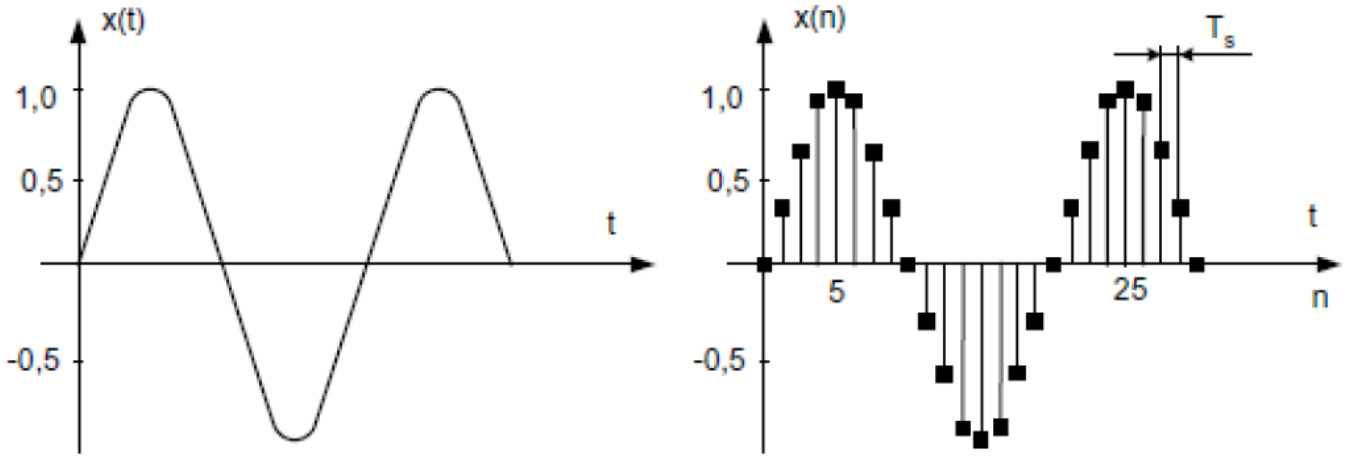
ADC Process



- Sampling and Holding (S/H)
- Quantizing and Encoding (Q/E)

Sampling

Sampling converts analog signal (continuous in time and magnitude) into discrete time signal (discrete in time but can have any magnitude)



The intervals, T_s, must be carefully chosen to ensure an accurate representation of the original analogue signal. To discuss the problem of losing information in the sampling process, it is necessary to recall Nyquist's criteria.

The Nyquist criterion is as follows.

- If $f_s < 2f_m$, than a phenomenon called aliasing will occur.

Quantization

Quantization is breaking down the values of the sampled signal into a set of finite number of quantized values/states.

Example:

We have an analog signal varying in the range from 0-10V. This range is separated into 8 discrete quantized states with 1.25V increments. (How did we get 1.25V?)

Output States	Discrete Voltage Ranges (V)
0	0.00-1.25
1	1.25-2.50
2	2.50-3.75
3	3.75-5.00
4	5.00-6.25
5	6.25-7.50
6	7.50-8.75
7	8.75-10.0

The number of output states (M) that the quantizer can have:

$$M = 2^N$$

where *N* is the number of bits in the A/D converter

- Example: For a 3 bit A/D converter, $M = 2^3 = 8$.

Analog quantization size:

$$q = (V_{max} - V_{min}) / M$$
$$= (10V - 0V)/8 = 1.25V$$

This smallest analog change between each quantization state is called ***resolution.***

Encoding

Here, a unique digital number/word is assigned to each of the quantized states

Output States	Discrete Voltage Ranges (V)	Binary code
0	0.00-1.25	000
1	1.25-2.50	001
2	2.50-3.75	010
3	3.75-5.00	011
4	5.00-6.25	100
5	6.25-7.50	101
6	7.50-8.75	110
7	8.75-10.0	111

Sample and Hold Circuits

- In most ADC, the input analog sample is required to be hold for sometime before its digital output is produced.
- This is achieved by sample and hold circuit.
- By using this it is ensured that the result of conversion will not be affected by a change in the analog signal during the conversion process.

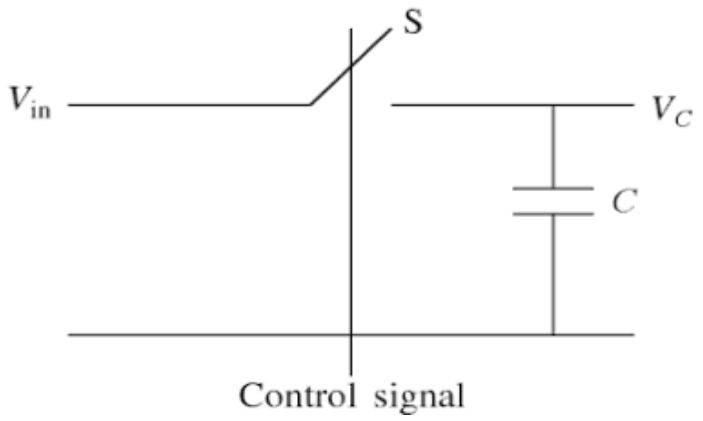
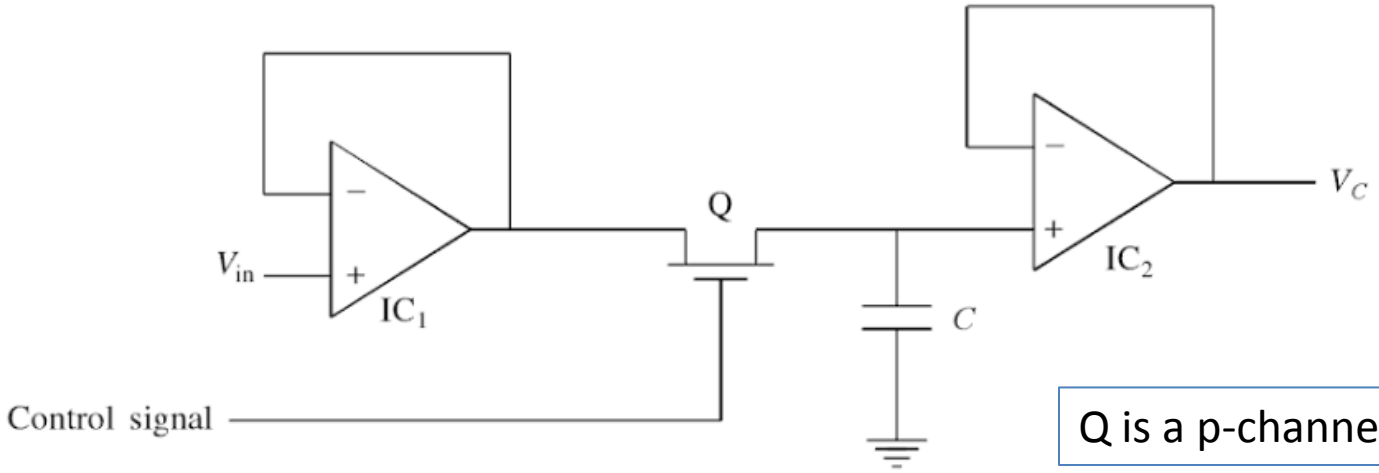


Fig: Basic structure of a sample and hold circuit

When **S** is closed $\mathbf{V_c}$ follows or tracks the applied voltage $\mathbf{V_{in}}$. When **S** is opened capacitor retains the analog voltage applied at that instant of time.



Q is a p-channel MOSFET

Fig: A practical sample and hold circuit

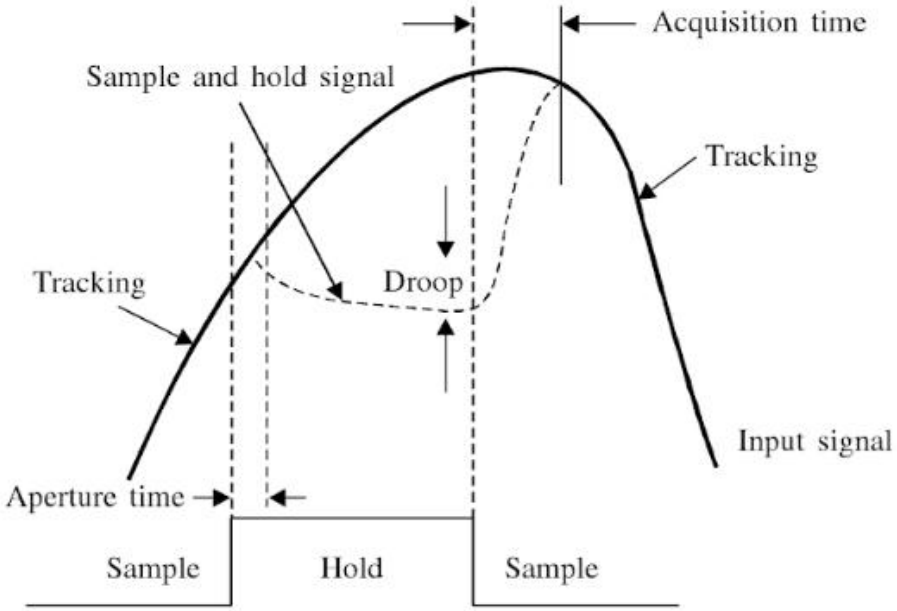


Fig: Response parameters of sample and hold circuit

Response Parameters

- **Aperture time:** time required for the switch to open. This is also called aperture uncertainty
- **Acquisition time:** This is the time the output of the sample and hold circuit takes to track the input signal within specified accuracy
- **Droop rate:** the rate of change of the output voltage when the circuit is in the 'hold' mode, and is a function of the leakage of droop current, $\boldsymbol{i_d}$ and the capacitance, $\boldsymbol{C}$.

$$\frac{dV_C}{dt} = \frac{i_d}{C}$$

Considerations for choosing C

- *C* should be large enough to minimize the 'droop' caused by leakage currents in Q and IC_2
- *C* should be small enough to track the input signal fast, since charging time constant should be as small as possible. [charging time constant = (ON resistance of Q) * *C*]

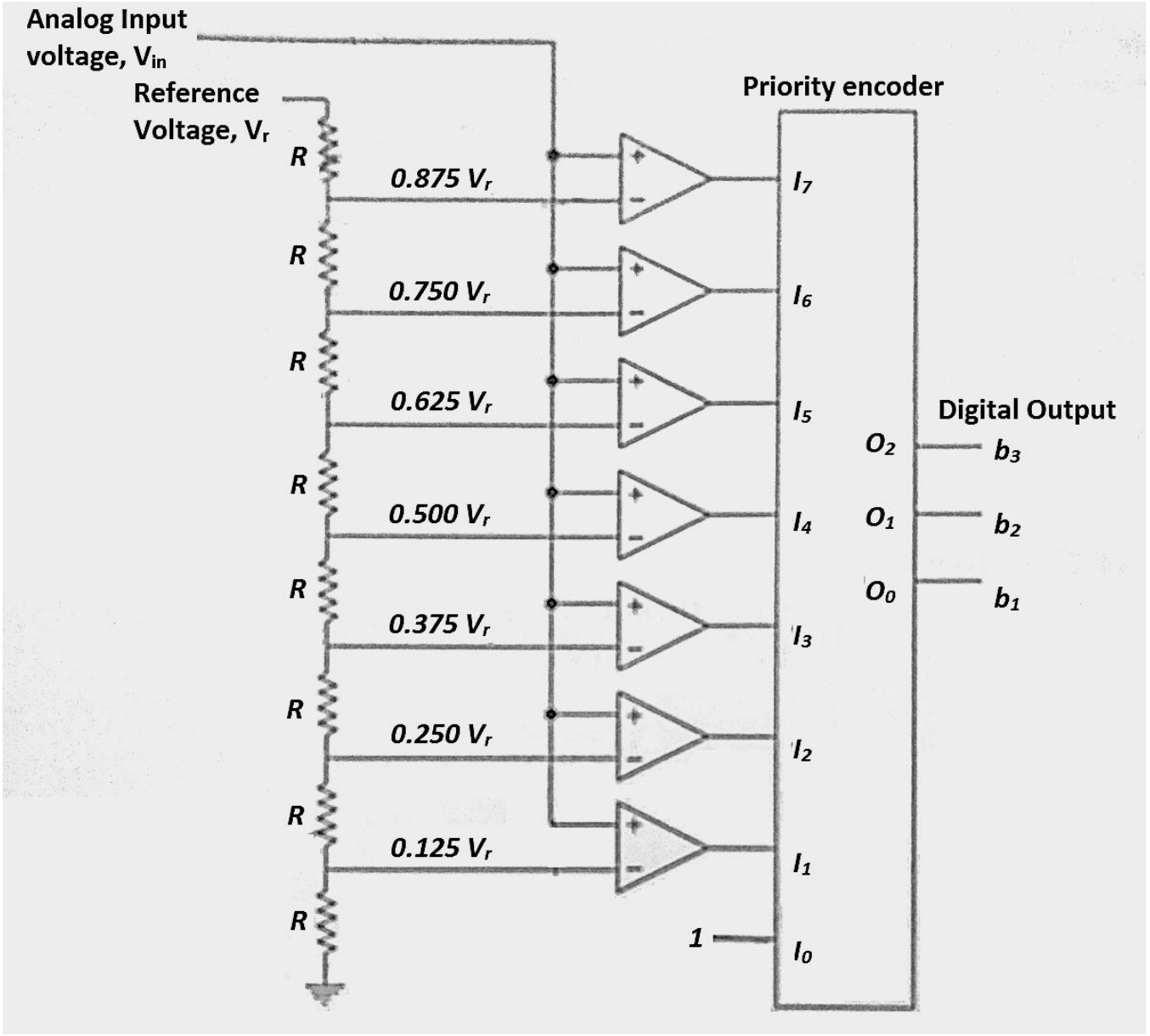
Types of ADC

- Flash A/D Converter
- Successive Approximation A/D Converter
- Dual Slope A/D Converter
- Delta-Sigma A/D Converter

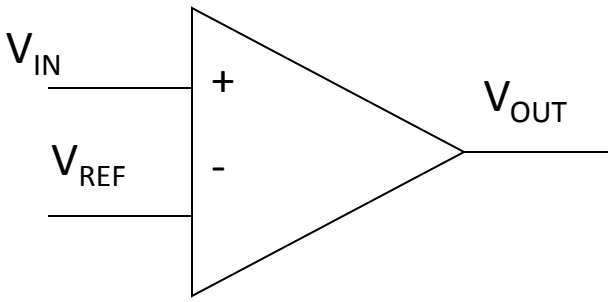
Flash A/D Converter

- Uses the 2^N resistors to form a ladder voltage divider, which divides the reference voltage into 2^N equal intervals.
- Consists of a series of comparators, each one comparing the input signal to a unique reference voltage.
- The comparator outputs connect to the inputs of a priority encoder circuit, which produces a binary output

3-bit Flash A/D Converter

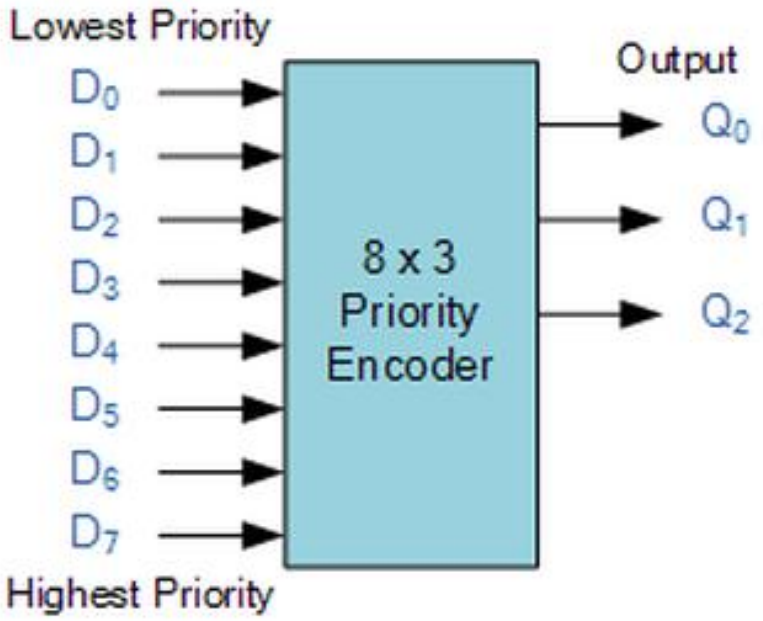


Comparator



If	Output
$V_{IN} > V_{REF}$	High
$V_{IN} < V_{REF}$	Low

Truth Table of Priority Encoder



Inputs								Outputs		
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Q_2	Q_1	Q_0
0	0	0	0	0	0	0	1	0	0	0
0	0	0	0	0	0	1	x	0	0	1
0	0	0	0	0	1	x	x	0	1	0
0	0	0	0	1	x	x	x	0	1	1
0	0	0	1	x	x	x	x	1	0	0
0	0	1	x	x	x	x	x	1	0	1
0	1	x	x	x	x	x	x	1	1	0
1	x	x	x	x	x	x	x	1	1	1

X = dont care

Flash ADC operation

- As the analog input voltage exceeds the reference voltage at each comparator, the comparator outputs will sequentially saturate to a high state.

- The priority encoder generates a binary number based on the highest-order, ignoring all other active inputs.

Advantages and Disadvantages

Advantages:

- Very Fast .
- Very simple operational theory .
- Speed is only limited by gate and comparator propagation delay .

Disadvantages:

- Expensive.
- Each additional bit of resolution requires twice the comparators.

Successive Approximation ADC

- It consists of a successive approximation register (SAR), DAC and comparator.
- The output of SAR is given to n-bit DAC.
- The equivalent analog output voltage of DAC, V_{DA} is applied to the inverting input of the comparator.
- The second input to the comparator is the unknown analog input voltage V_{IN}.
- The output of the comparator is used to activate the successive approximation logic of SAR.

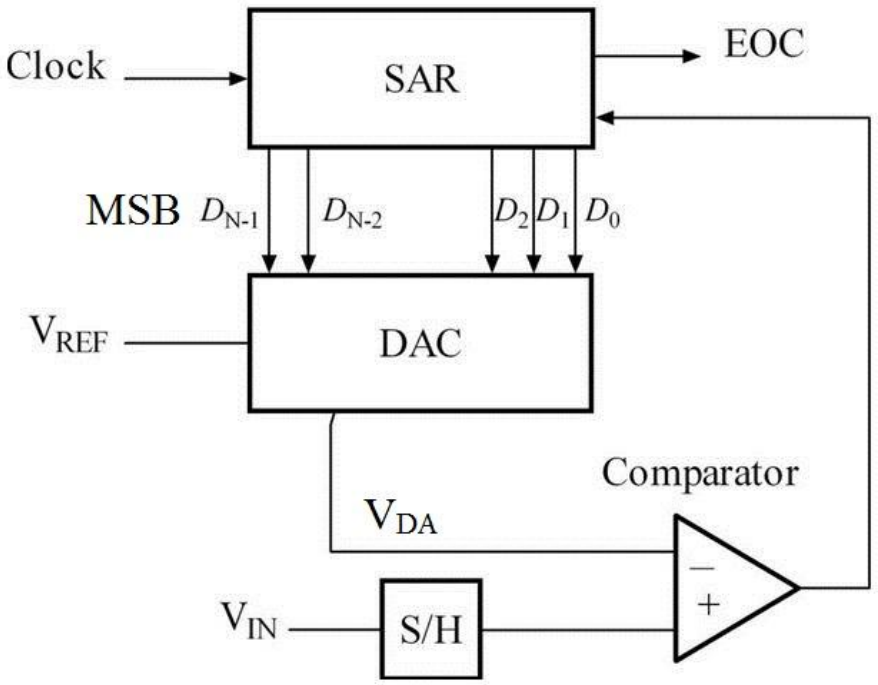


Figure: Block diagram of N-bit Successive Approximation ADC

- A/D conversion begins by setting the MSB = 1 and keeping rest of the bits = 0
- DAC converts the digital output of the SAR to analog signal, V_{DA} which is compared with V_{IN}
- If $V_{IN} > V_{DA}$; then MSB of SAR is kept at 1 and next lower significant bit is set to 1
- If $V_{IN} < V_{DA}$; then MSB of SAR is cleared to 0 and next lower significant bit is set to 1
- Again, DAC converts the digital output of the SAR and comparing V_{DA} with V_{IN} , the respective bit is either kept at 1 or it is cleared to 0
- This process is repeated till all the bits have been checked
- A/D conversion is then completed and the contents of SAR are the Digital representation of V_{IN}

3-bit Successive Approximation ADC (Example)

Let, V_{REF} = 10V

D2	D1	D0	V_{DA}
0	0	0	0.00
0	0	1	1.25
0	1	0	2.50
0	1	1	3.75
1	0	0	5.00
1	0	1	6.25
1	1	0	7.50
1	1	1	8.75

Table 1: Input bit pattern and o/p analog voltage range of 3-bit DAC

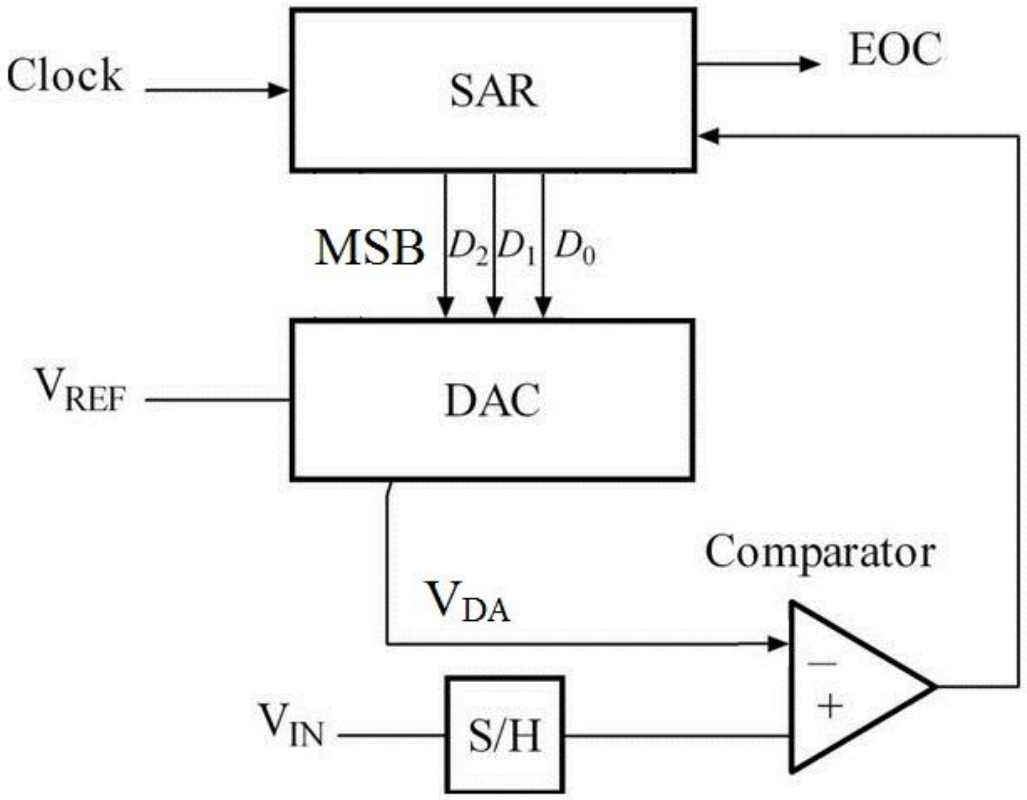


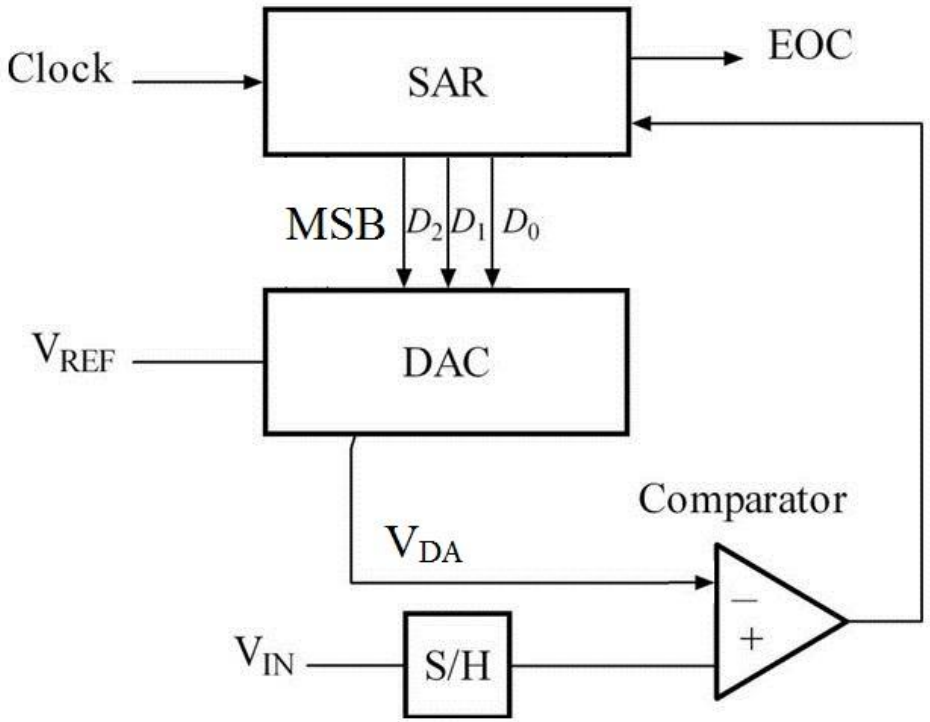
Figure: Block diagram of 3-bit Successive Approximation ADC

Let, V_{IN} = 3.2 V

A/D conversion takes place according to the following 3 cycles:

- MSB (D_2) = 1 , D_1 =0 , D_0 = 0.
  Input to DAC is '*1 0 0*'
  According to **Table 1**
  V_{DA} = 5 V
  As, $V_{IN} < V_{DA}$; D_2 is cleared to 0
  Resulting bit pattern at this stage:

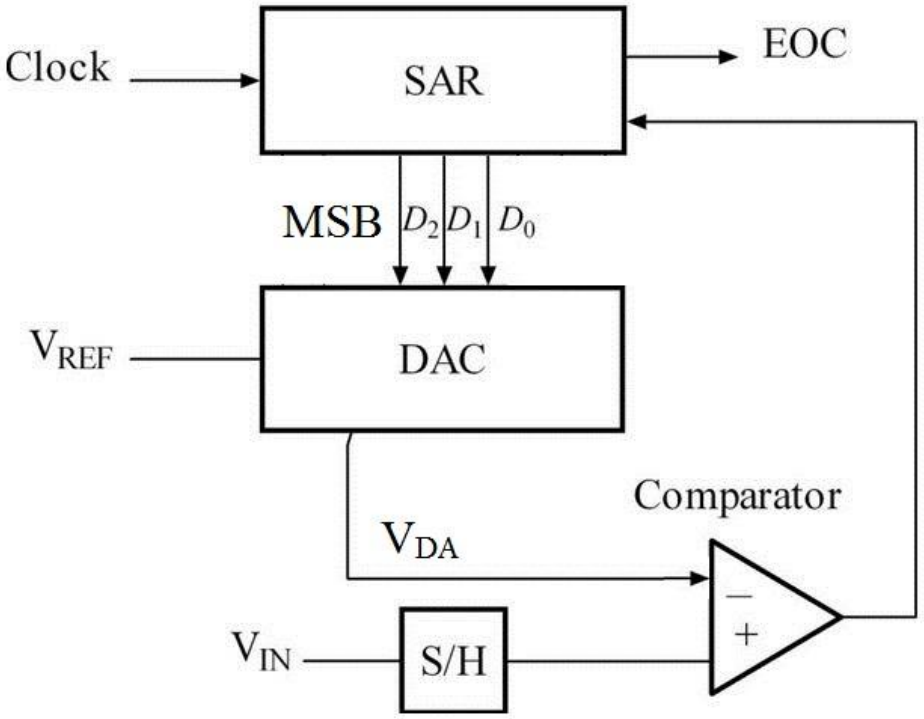
0	0	0



- Next, D_1 is set to 1.
  Input to DAC is '*0 1 0*'
  According to **Table 1**
  V_{DA} = 2.5 V
  As, $V_{IN} > V_{DA}$; D_1 is unchanged

  Updated bit pattern at this stage:

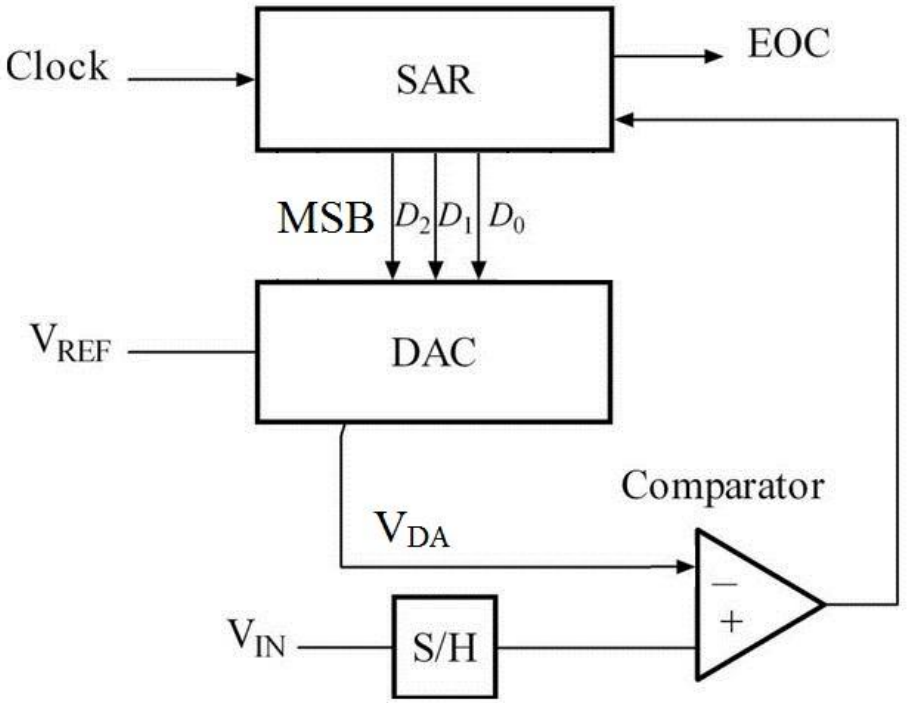
0	1	0



- Next, D_0 is set to 1.
  Input to DAC is *'0 1 1'*
  According to **Table 1**
  V_{DA} = 3.75 V
  As, $V_{IN} < V_{DA}$; D_0 is cleared to 0
  Updated bit pattern at this stage:

0	1	0

- A/D conversion is completed and the digital representation of V_{IN} = 3.2V is *'0 1 0'*



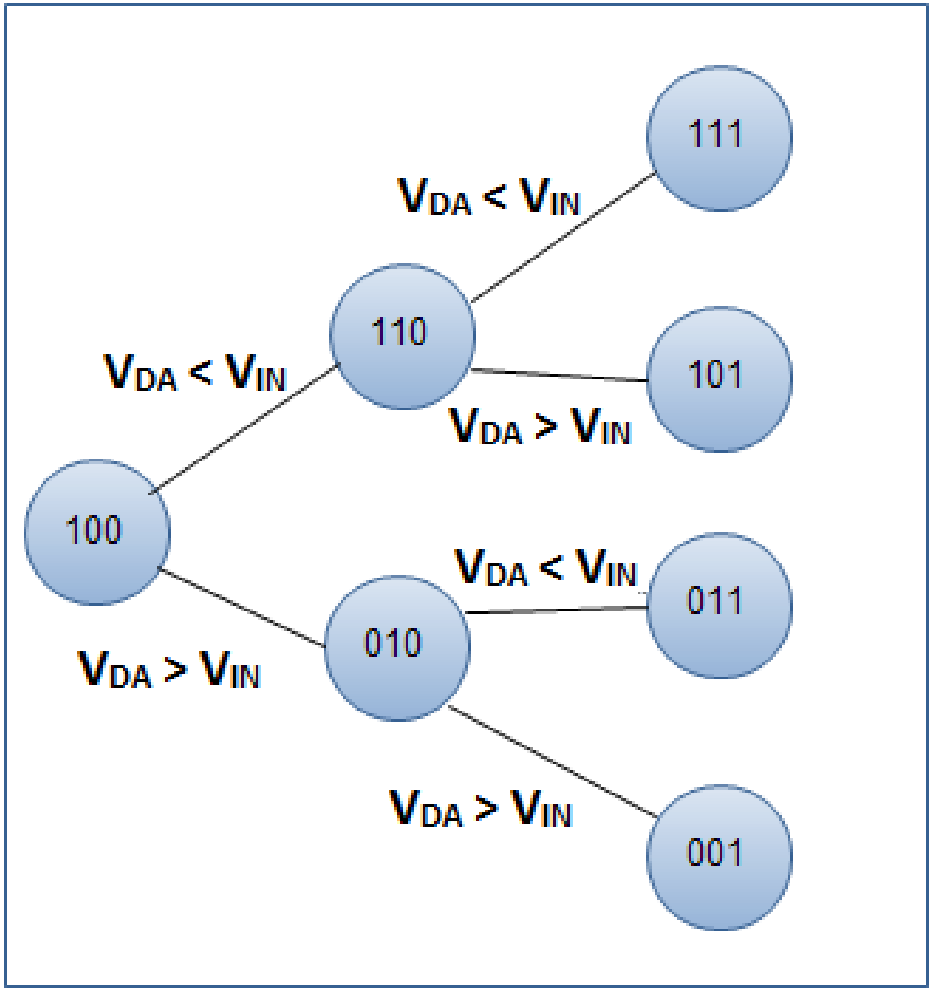


Figure: Conversion sequence of 3-bit successive approximation ADC

Alternative Approach

In the previous example, V_{REF} = 10V

So, voltage contribution from each bit of DAC is:

Table 2

Bit	**D2**	**D1**	**D0**
Voltage Contributed	5 V	2.5 V	1.25 V

The 3 cycles of A/D conversion:

- MSB (D_2) = 1 , D_1 =0 , D_0 = 0.
  Input to DAC is '*1 0 0*'
  According to **Table 2**
  V_{DA} = (5 + 0 + 0) V
  As, $V_{IN} < V_{DA}$; D_2 is cleared to 0

  Resulting bit pattern at this stage:

0	0	0

- Next, D_1 is set to 1.
  Input to DAC is *'0 1 0'*
  According to **Table 2**
  V_{DA} = (0 + 2.5 + 0) V
  As, $V_{IN} > V_{DA}$; D_1 is unchanged

  Updated bit pattern at this stage:

0	1	0

- Next, D_0 is set to 1.
  Input to DAC is *'0 1 1'*
  According to **Table 1**
  V_{DA} = 3.75 V
  As, $V_{IN} < V_{DA}$; D_0 is cleared to 0
  Updated bit pattern at this stage:

0	1	0

A/D conversion is completed and the digital representation of V_{IN} = 3.2V is *'0 1 0'*

Advantages and Disadvantages SA ADC

Advantages :

- Capable of high speed and reliable .
- Medium accuracy compared to other ADC types.
- Good tradeoff between speed and cost.

Disadvantages :

- Higher resolution successive approximation ADC's will be slower

DIGITAL TO ANALOGUE CONVERSION (DAC)

Weighted-Resistor D/A Converter

- Can be designed using an operational amplifier and appropriate combination of resistors
- Resistors connected to data bits are in binary weighted proportion, and each is twice the value of the previous one.
- Each input signal can be connected to the op amp by turning on its switch to the reference voltage that represents logic 1.
- If the switch is off, the input signal is logic 0.

Weighted-Resistor D/A Converter

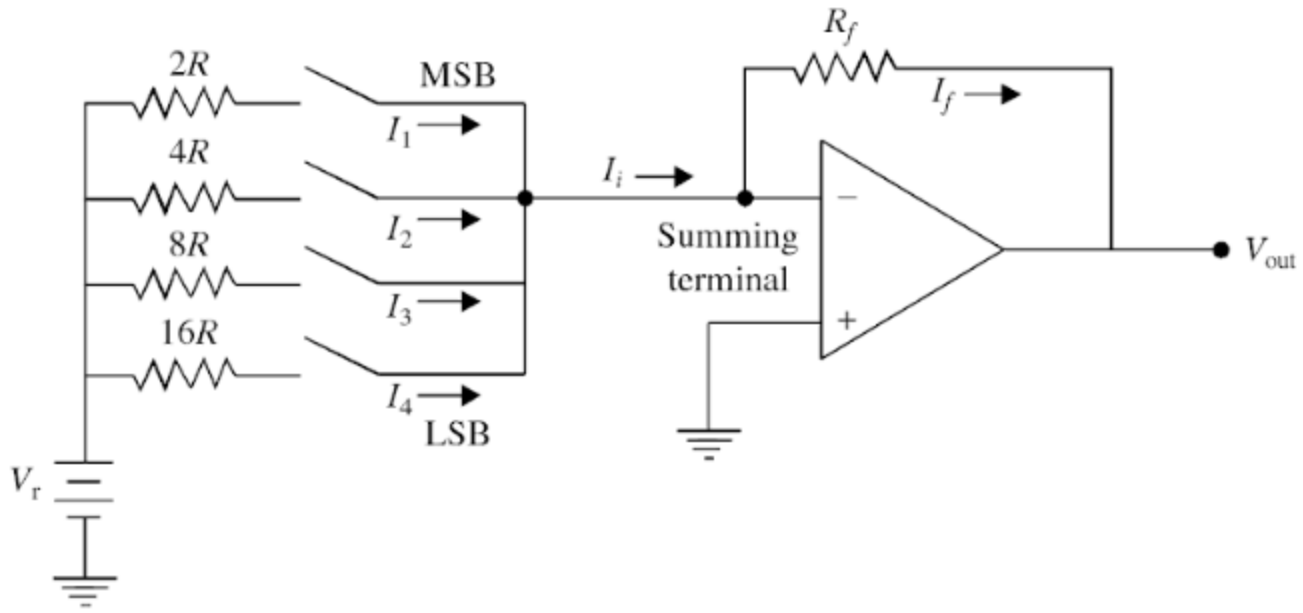


Figure : A 4-bit binary weighted-resistor D/A converter.

Total Current : $I_i = I_1 + I_2 + I_3 + I_4 = I_f$

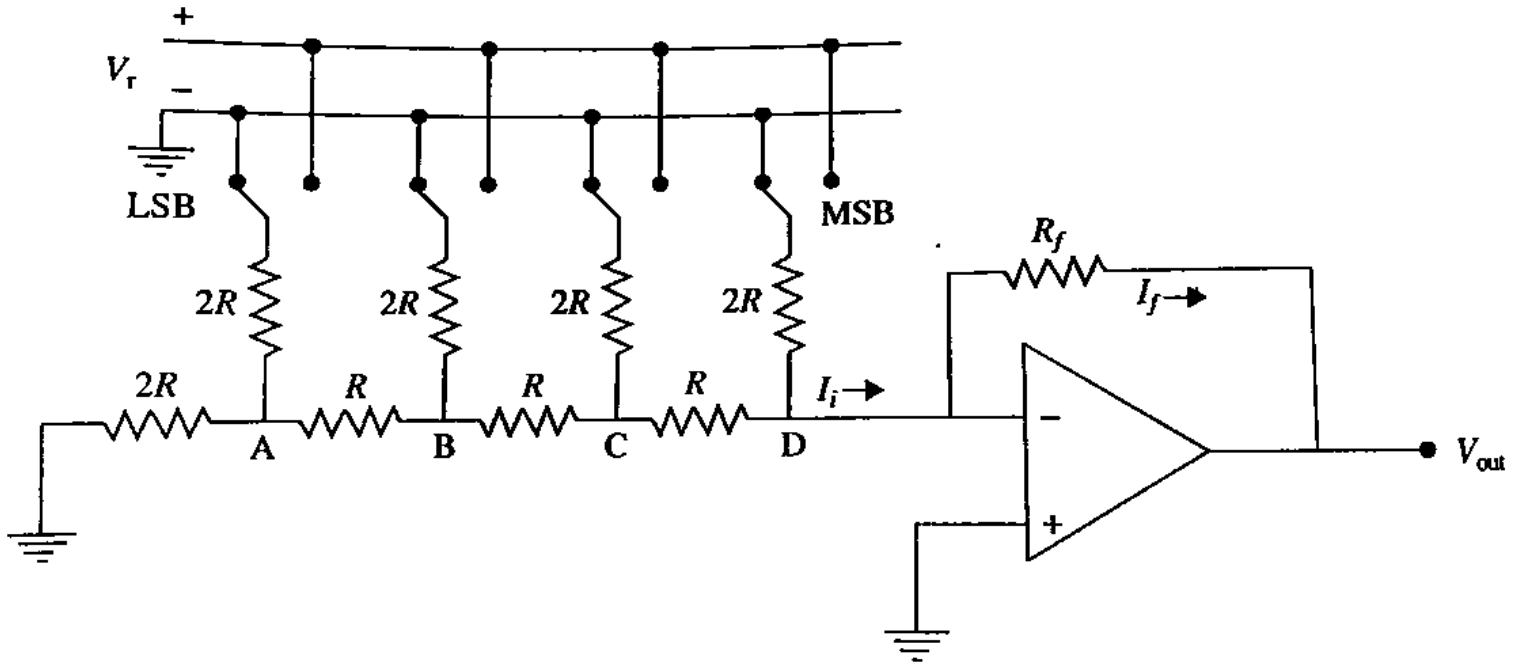
Output Voltage : $V_{out} = -R_f I_f = -R_f V_r \left(\frac{b_1}{2R} + \frac{b_2}{4R} + \frac{b_3}{8R} + \frac{b_4}{16R} \right)$

$$= -\frac{R_f}{R} V_r (b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N})$$

Disadvantages of Binary Weighted DAC

- One disadvantage of this DAC is that N inputs require N binary-weighted resistor values.
- Another is that the circuit require very accurate resistors, as the DAC would require that the error in each resistor be less than the smallest resistor value. This type requires large range of resistors with necessary high precision for low resistors.
- Requires low switch resistances in transistors.
- Can be expensive. Hence resolution is limited to 8-bit size.

R-2R Ladder D/A Converter



- A resistive ladder network is a special type of series-parallel circuit.
- One form of ladder network is commonly used to scale down voltages to certain weighted values for digital-to-analog conversion
  - Called R/2R Ladder Network
- To find total resistance of a ladder network, start at the point farthest from the source and reduce the resistance in steps.

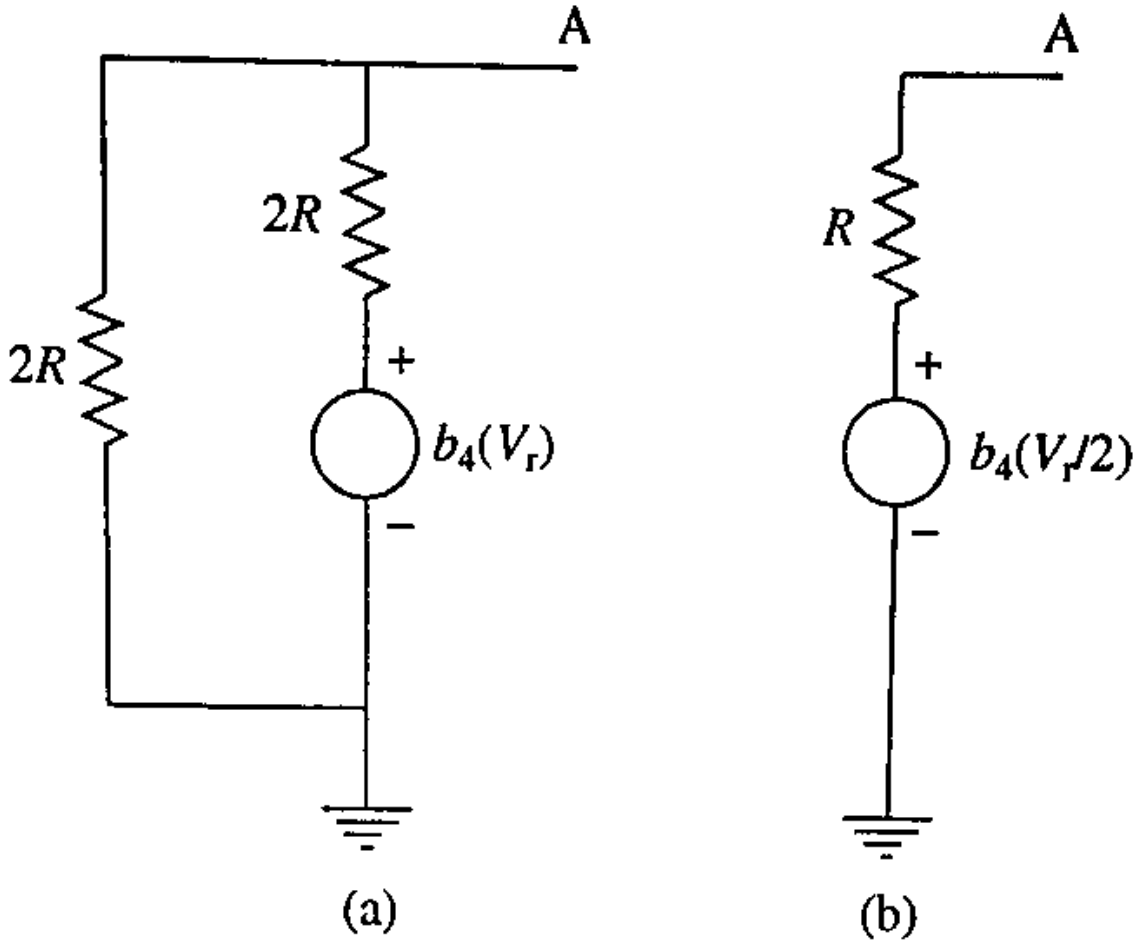


Figure: Thevenin equivalent to the left of point A

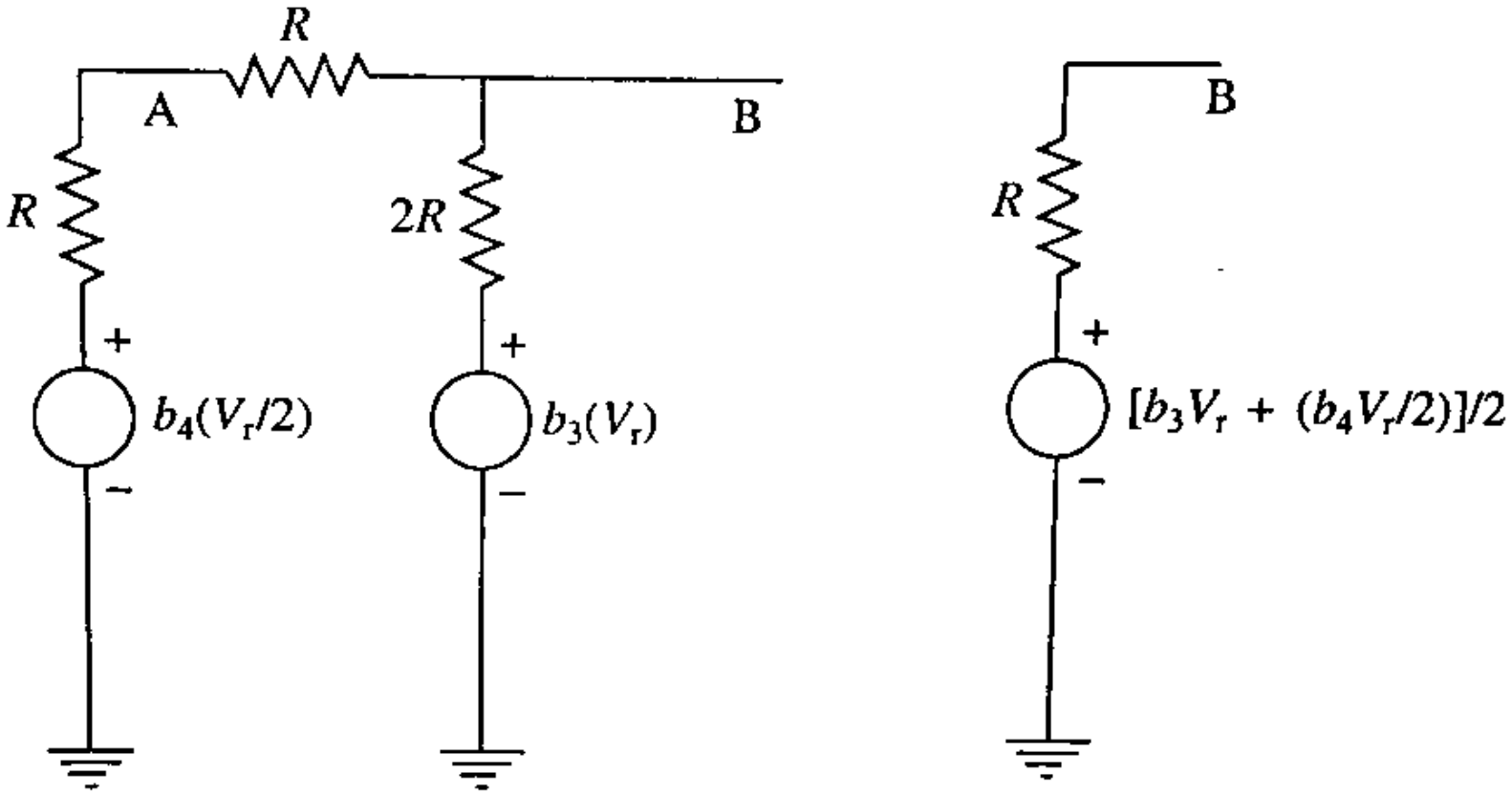


Figure: Thevenin equivalent to the left of point B

Thevenin's equivalent voltage can be determined using superposition theorem

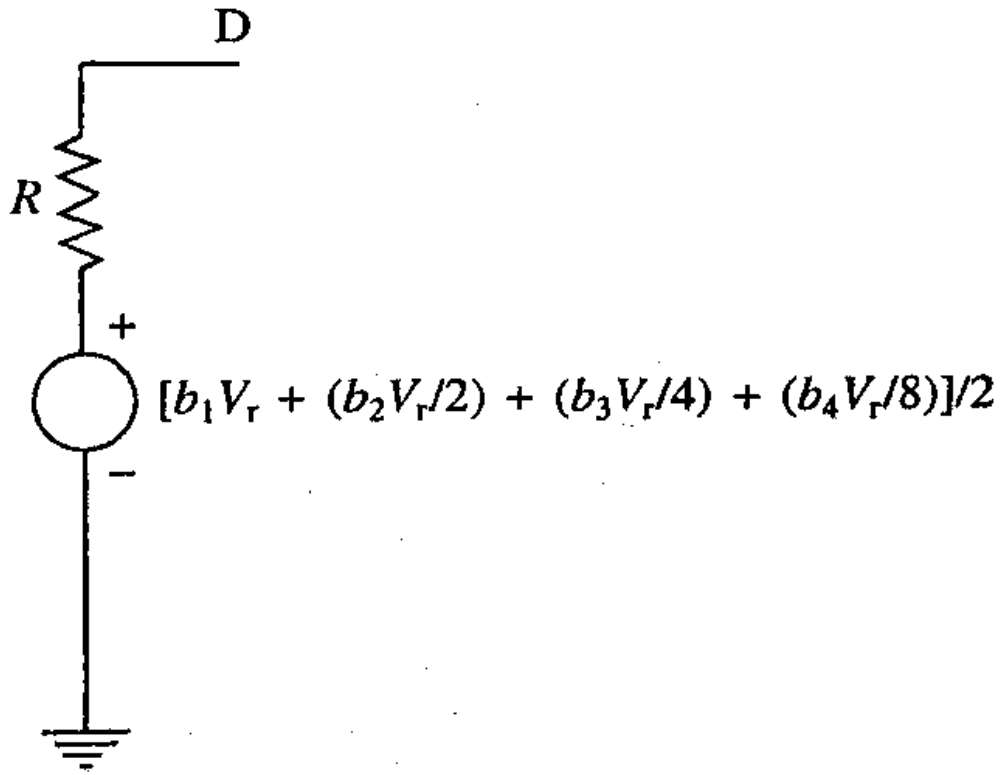


Figure: Thevenin equivalent to the left of point D

$$V_{\text{out}} = -R_f I_f = -R_f V_r \left(\frac{b_1}{2R} + \frac{b_2}{4R} + \frac{b_3}{8R} + \frac{b_4}{16R} \right)$$

$$= -\frac{R_f}{R} V_r \left(b_1 2^{-1} + b_2 2^{-2} + \ldots + b_N 2^{-N}\right)$$

Advantages and Disadvantages

Advantages:

- Only two resistor values are used in R-2R ladder type.
- It does not need as precision resistors as Binary weighted DACs.
- It is cheap and easy to manufacture.

Disadvantages:

- It has slower conversion rate.