Course Instructor

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JK Flip Flop Review

Counter Design Steps

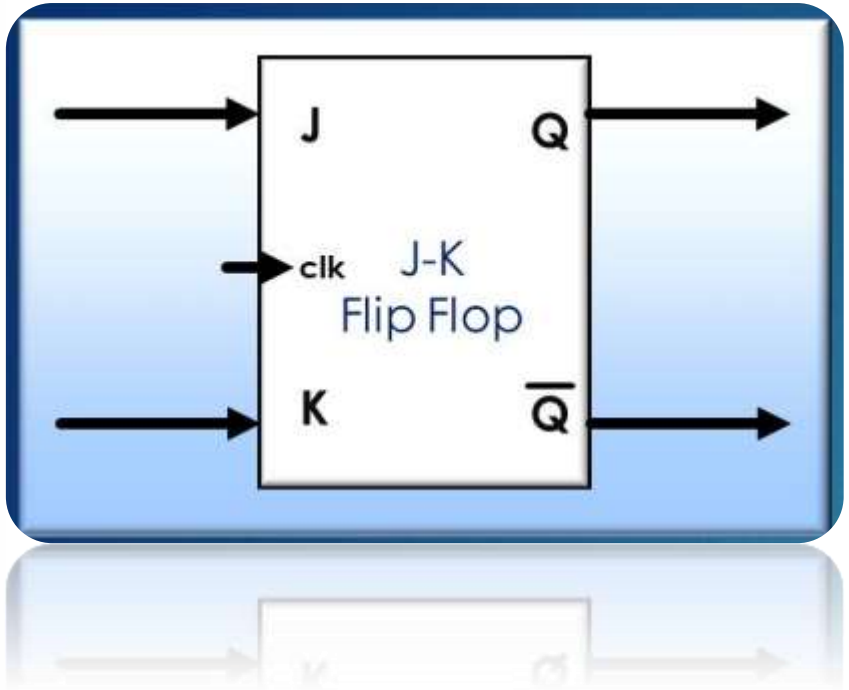
Design of MOD-4 Synchronous Up-Counter

Design of Synchronous Random Counter

Video Link of this Lecture:
Will be Updated After the Class

Q(t)	J	K	Q(t+1)
0	0	0	0 (Hold)
0	0	1	0 (reset)
0	1	0	1 (Set)
0	1	1	1 (Toggle)
1	0	0	1 (Hold)
1	0	1	0 (reset)
1	1	0	1 (Set)
1	1	1	0 (Toggle)

Characteristics Table

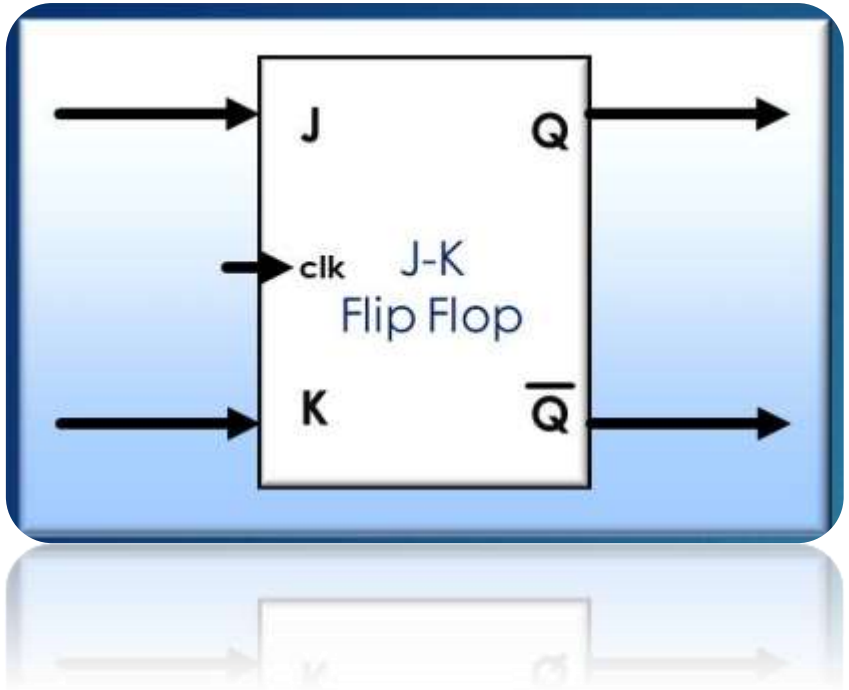


J	K	Q
0	0	Hold
0	1	0 (Reset)
1	0	1 (SET)
1	1	Toggle

Truth Table

Present Qn	Next State Qn+1	J	K
0	0		
0	1		
1	0		
1	1		

Excitation Table

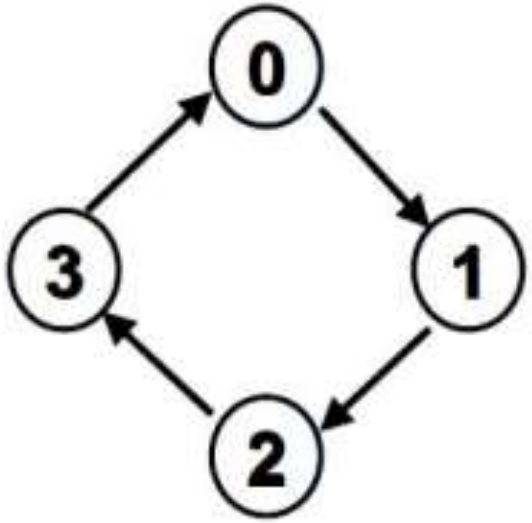


J	K	Q
0	0	Hold
0	1	0 (Reset)
1	0	1 (SET)
1	1	Toggle

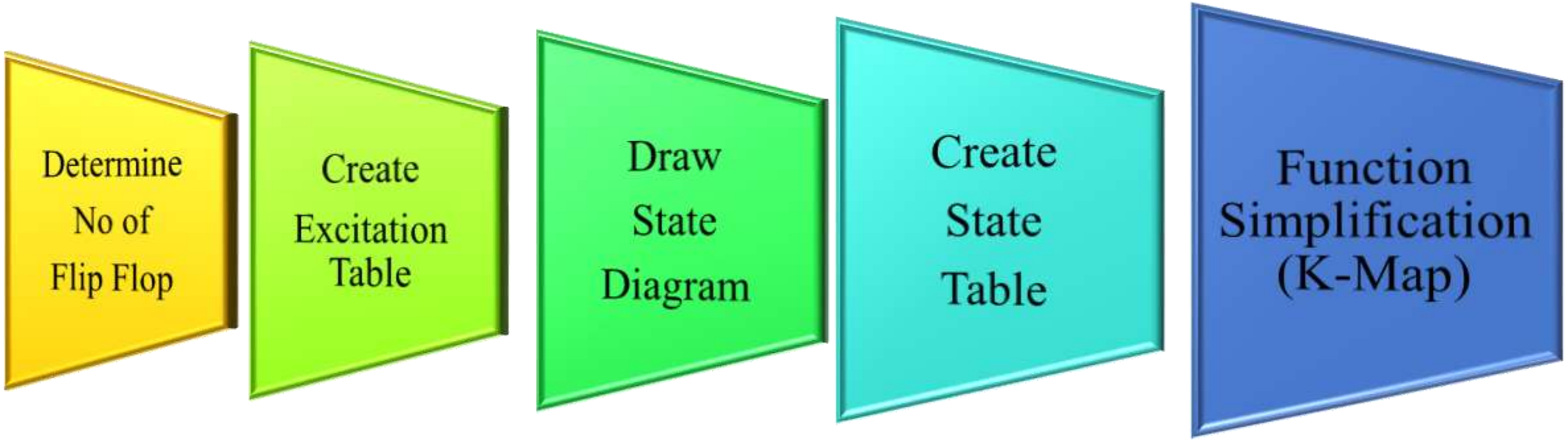
Truth Table

MOD-4 synchronous down-counter

MOD-4 synchronous up-counter



State Diagram


Determine No of Flip Flop
Create Excitation Table
Draw State Diagram
Create State Table
Function Simplification (K-Map)

Determine No of Flip Flop

0, 1, 2, 3, 0, 1, 2, 3, 0, 1, 2, 3,

Maximum Digit

3

Covert Binary

11

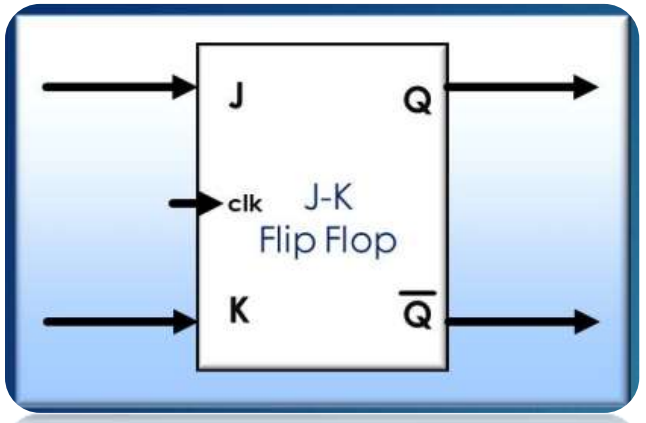
No of FF = 2

Maximum 2 Bit is Needed

Create Excitation Table

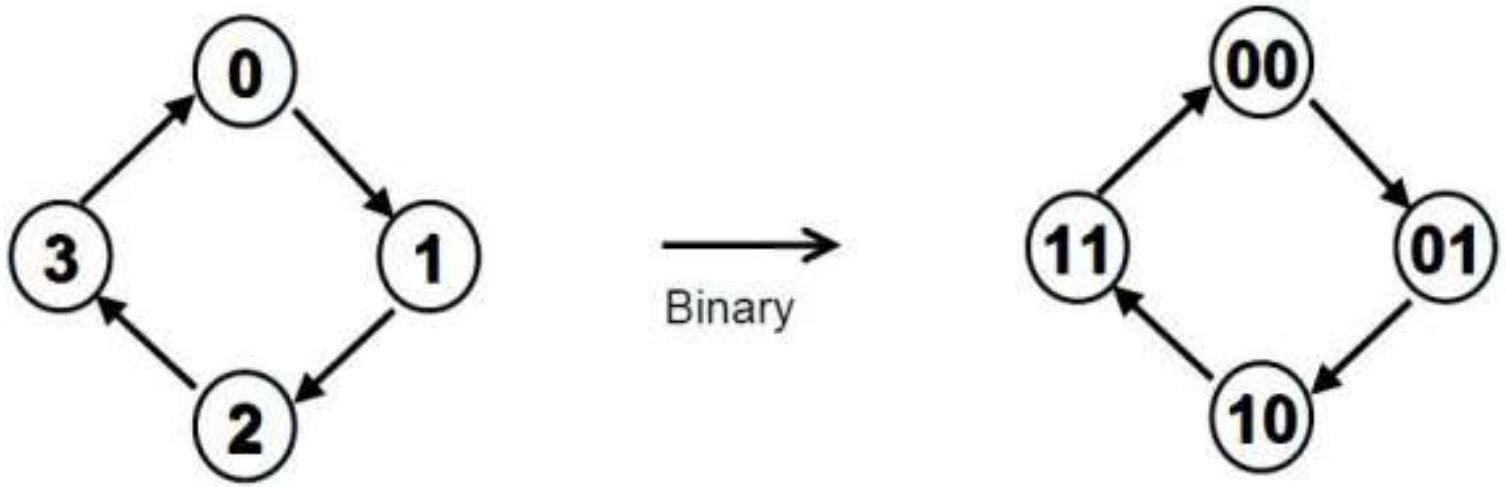
Present Qn	Next State Qn+1	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

Excitation Table



J	K	Q
0	0	Hold
0	1	0 (Reset)
1	0	1 (SET)
1	1	Toggle

Draw State Diagram



Create State Table

Present State	
B	A
0	0
0	1
1	0
1	1

Next State	
B	A
0	1
1	0
1	1
0	0

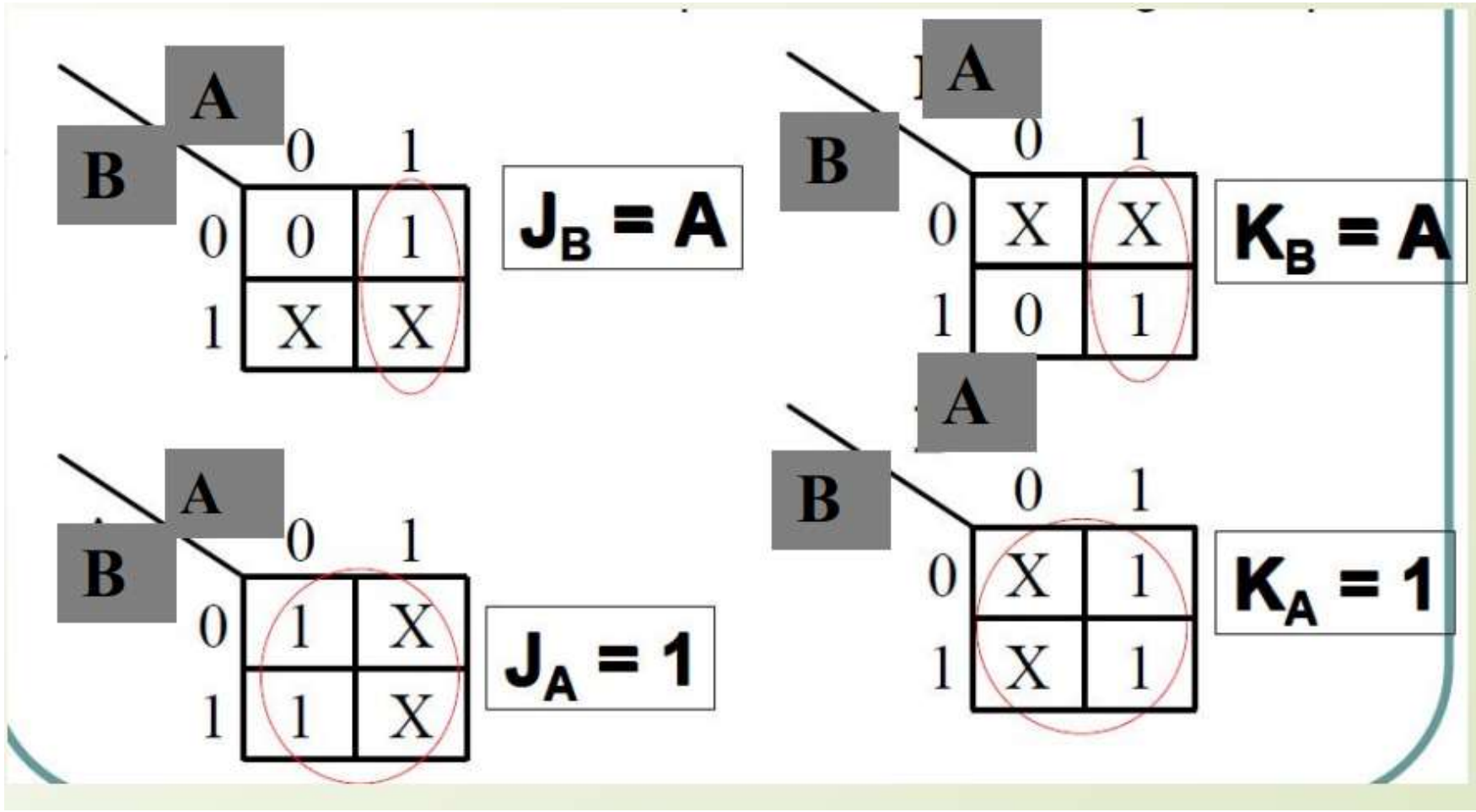
Input, J K			
J_B	K_B	J_A	K_A
0	X	1	X
1	X	X	1
X	0	1	X
X	1	X	1

Present Qn	Next State Qn+1	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

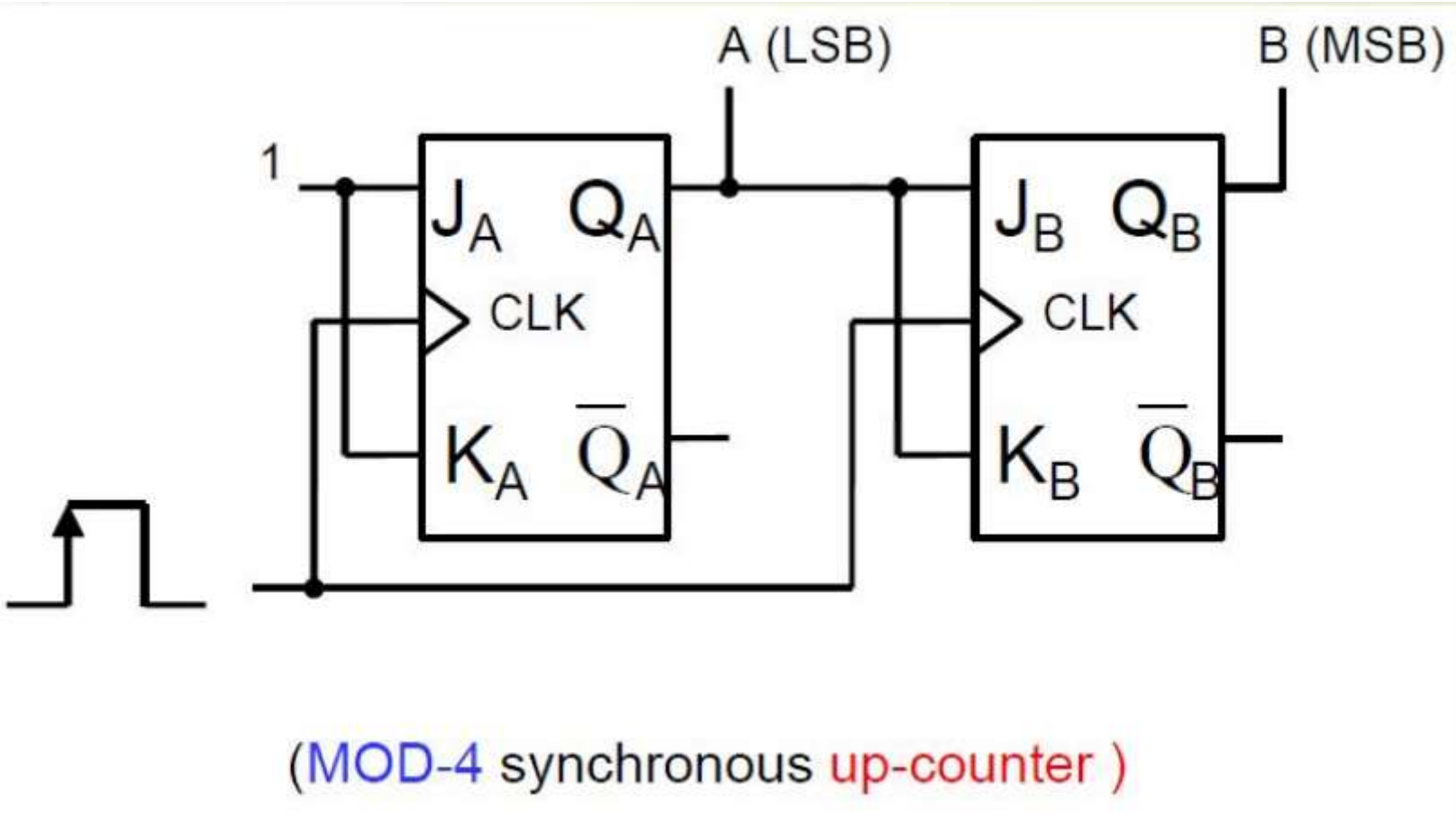
Excitation Table

Function Simplification (K-Map)

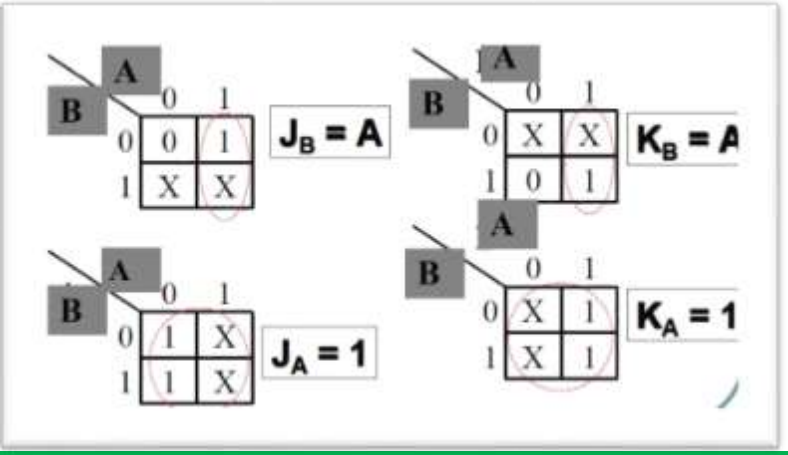
Input, J K	
J_B K_B	J_A K_A
0 X	1 X
1 X	X 1
X 0	1 X
X 1	X 1



Circuit Connection



(MOD-4 synchronous up-counter)

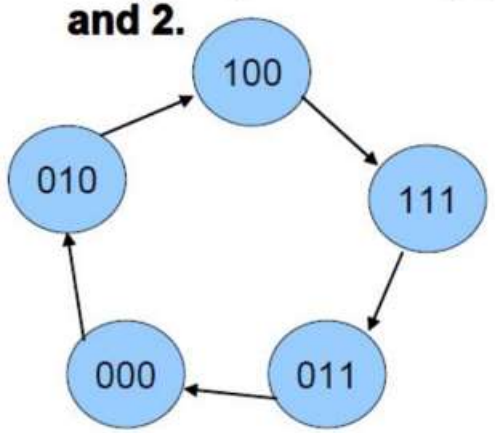


Design a Synchronous Counter to Count 4,7,3,0 and 2 respectively using JKFlip Flop negative trigered by showing:

n = 3 bit = 3 Flip Flop

Present Qn	Next State Qn+1	J	K
0	0	0	x
0	1	1	x
1	0	x	1
1	1	x	0

State Transation Diagram, to count 4, 7, 3, 0 and 2.



Decimal	Present State			Next State			JC	KC	JB	KB	JA	KA
	QC	QB	QA	QC	QB	QA						
4	1	0	0	1	1	1	x	0	1	x	1	x
7	1	1	1	0	1	1	x	1	x	0	x	0
3	0	1	1	0	0	0	0	x	x	1	x	1
0	0	0	0	0	1	0	0	x	1	x	0	x
2	0	1	0	1	0	0	1	x	x	1	0	x

Design a Synchronous Counter to Count 4,7,3,0 and 2 respectively using JKFlip Flop negative trigered by showing:

Decimal	Present State			Next State			JC	KC	JB	KB	JA	KA
	QC	QB	QA	QC	QB	QA						
4	1	0	0	1	1	1	x	0	1	x	1	x
7	1	1	1	0	1	1	x	1	x	0	x	0
3	0	1	1	0	0	0	0	x	x	1	x	1
0	0	0	0	0	1	0	0	x	1	x	0	x
2	0	1	0	1	0	0	1	x	x	1	0	x

K Map for JA

C B A

4=100

5=101

7=111

6=110

C \ BA	00	01	11	10
0	0	X	X	0
1	1	X	X	X

$J_A = C = Q_C$

Design a Synchronous Counter to Count 4,7,3,0 and 2 respectively using JKFlip Flop negative trigered by showing:

Decimal	Present State			Next State			JC	KC	JB	KB	JA	KA
	QC	QB	QA	QC	QB	QA						
4	1	0	0	1	1	1	x	0	1	x	1	x
7	1	1	1	0	1	1	x	1	x	0	x	0
3	0	1	1	0	0	0	0	x	x	1	x	1
0	0	0	0	0	1	0	0	x	1	x	0	x
2	0	1	0	1	0	0	1	x	x	1	0	x

K Map for K_A

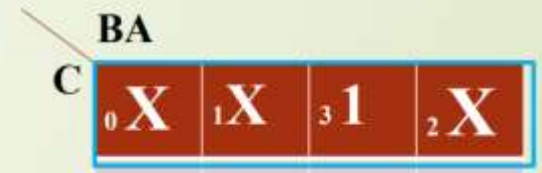
C B A

0=000

1=001

3=011

2=010



$K_A = \overline{C}\,\overline{Q_C}$

Design a Synchronous Counter to Count 4,7,3,0 and 2 respectively using JKFlip Flop negative trigered by showing:

Decimal	Present State			Next State			JC	KC	JB	KB	JA	KA
	QC	QB	QA	QC	QB	QA						
4	1	0	0	1	1	1	x	0	1	x	1	x
7	1	1	1	0	1	1	x	1	x	0	x	0
3	0	1	1	0	0	0	0	x	x	1	x	1
0	0	0	0	0	1	0	0	x	1	x	0	x
2	0	1	0	1	0	0	1	x	x	1	0	x

K Map for J_B

$J_B=1$

C \ BA				
	0	1	3	2
0	1	X	X	X
1	1	X	X	X

Design a Synchronous Counter to Count 4,7,3,0 and 2 respectively using JKFlip Flop negative trigered by showing:

Decimal	Present State			Next State			JC	KC	JB	KB	JA	KA
	QC	QB	QA	QC	QB	QA						
4	1	0	0	1	1	1	x	0	1	x	1	x
7	1	1	1	0	1	1	x	1	x	0	x	0
3	0	1	1	0	0	0	0	x	x	1	x	1
0	0	0	0	0	1	0	0	x	1	x	0	x
2	0	1	0	1	0	0	1	x	x	1	0	x

K Map for K_B

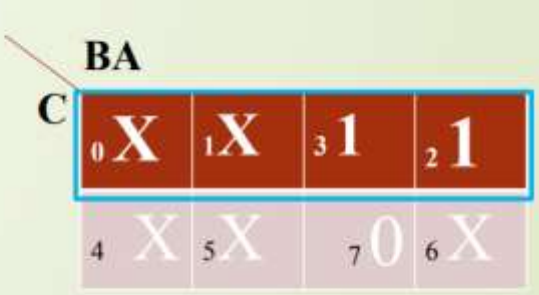
C B A

0=000

1=001

3=011

2=010



$K_B = \overline{C} = \overline{Q_C}$

Design a Synchronous Counter to Count 4,7,3,0 and 2 respectively using JKFlip Flop negative trigered by showing:

K Map for K_c

C B A

2=010
3=011
7=111
6=110

C \ BA	00	01	11	10
0	X	X	X	X
1	0	X	1	X

$K_c = B = Q_B$

K Map for J_c

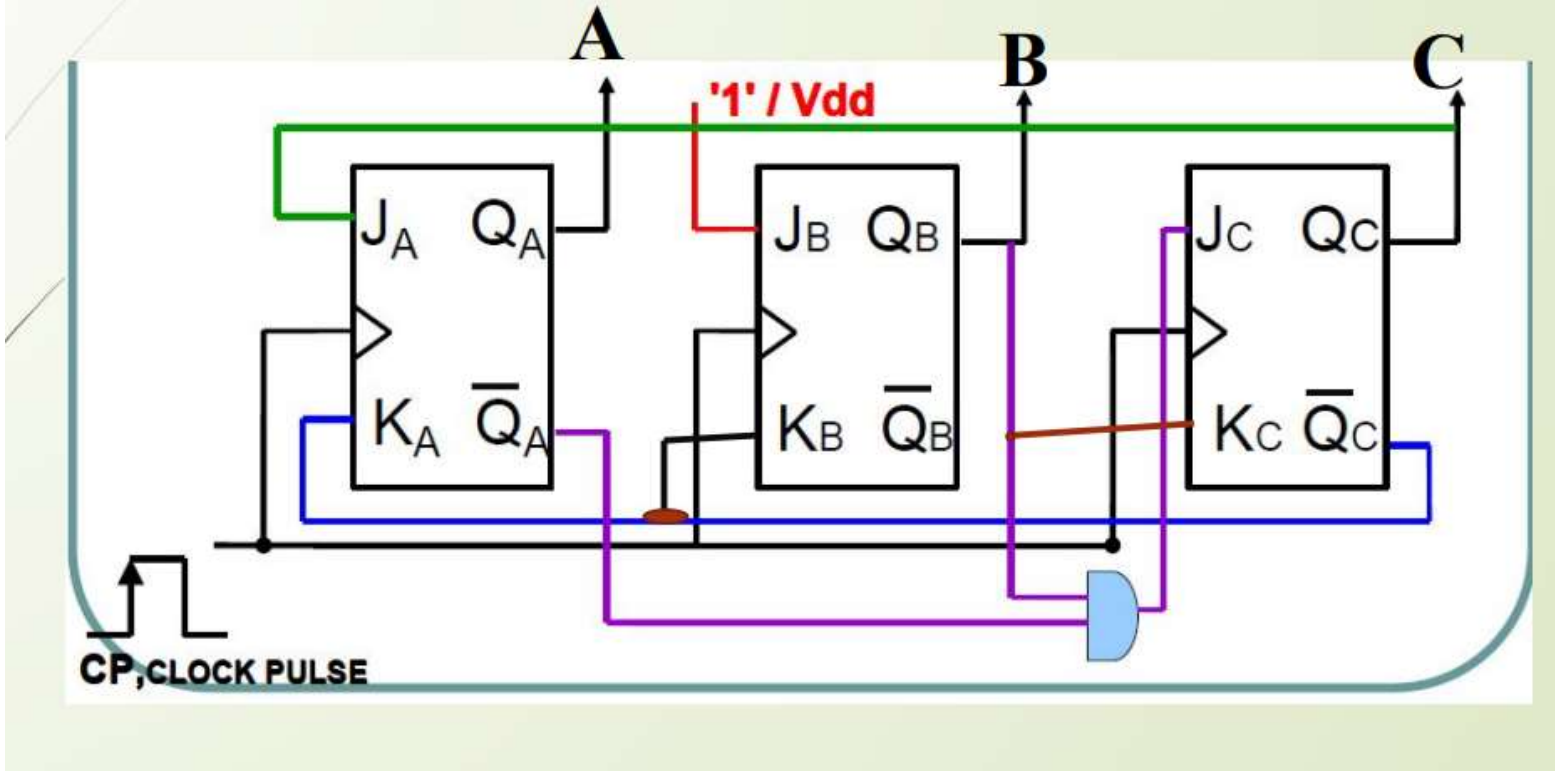
C B A

2=010
6=110

C \ BA	00	01	11	10
0	0	X	0	1
1	X	X	X	X

$J_c = B\overline{A} = Q_B\overline{Q}_A$

Design a Synchronous Counter to Count 4,7,3,0 and 2 respectively using JKFlip Flop negative trigered by showing:



Thank You