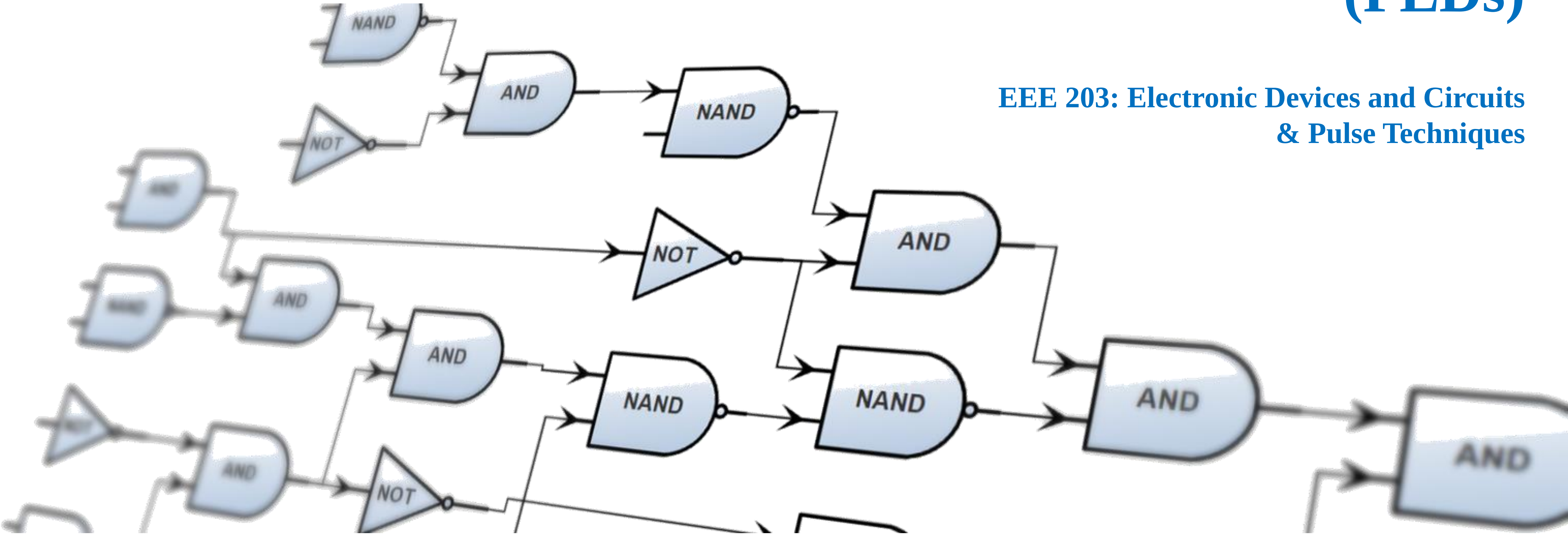
Programmable Logic Devices (PLDs)

EEE 203: Electronic Devices and Circuits & Pulse Techniques



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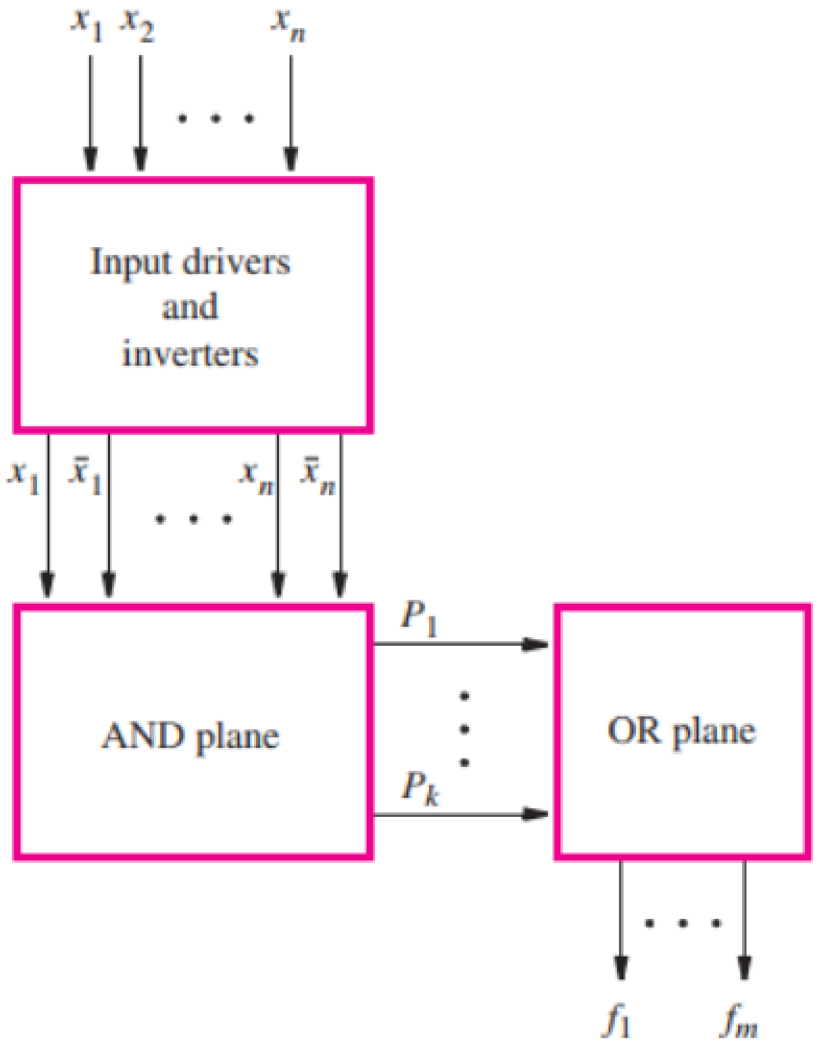
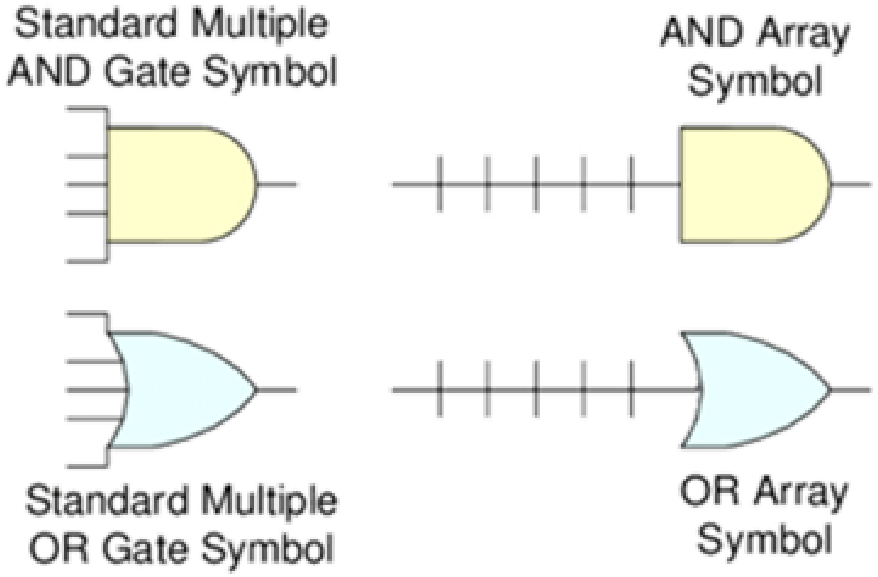
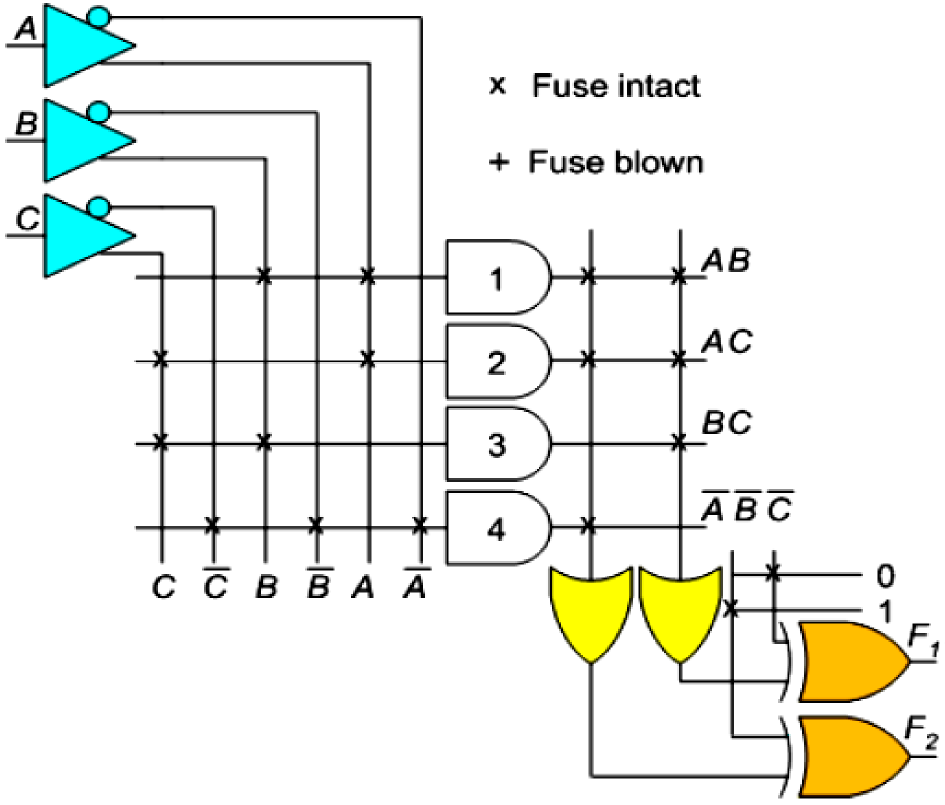
Definition


x_1 x_2 . . . x_n
Input drivers and inverters
x_1 $\bar{x}_1$ . . . x_n $\bar{x}_n$
AND plane
P_1
P_k
OR plane
f_1 . . . f_m

PLD is an integrated circuit with **programmable gates** divided into an **AND** array and an **OR** array to provide an AND-OR **sum of product** implementation.

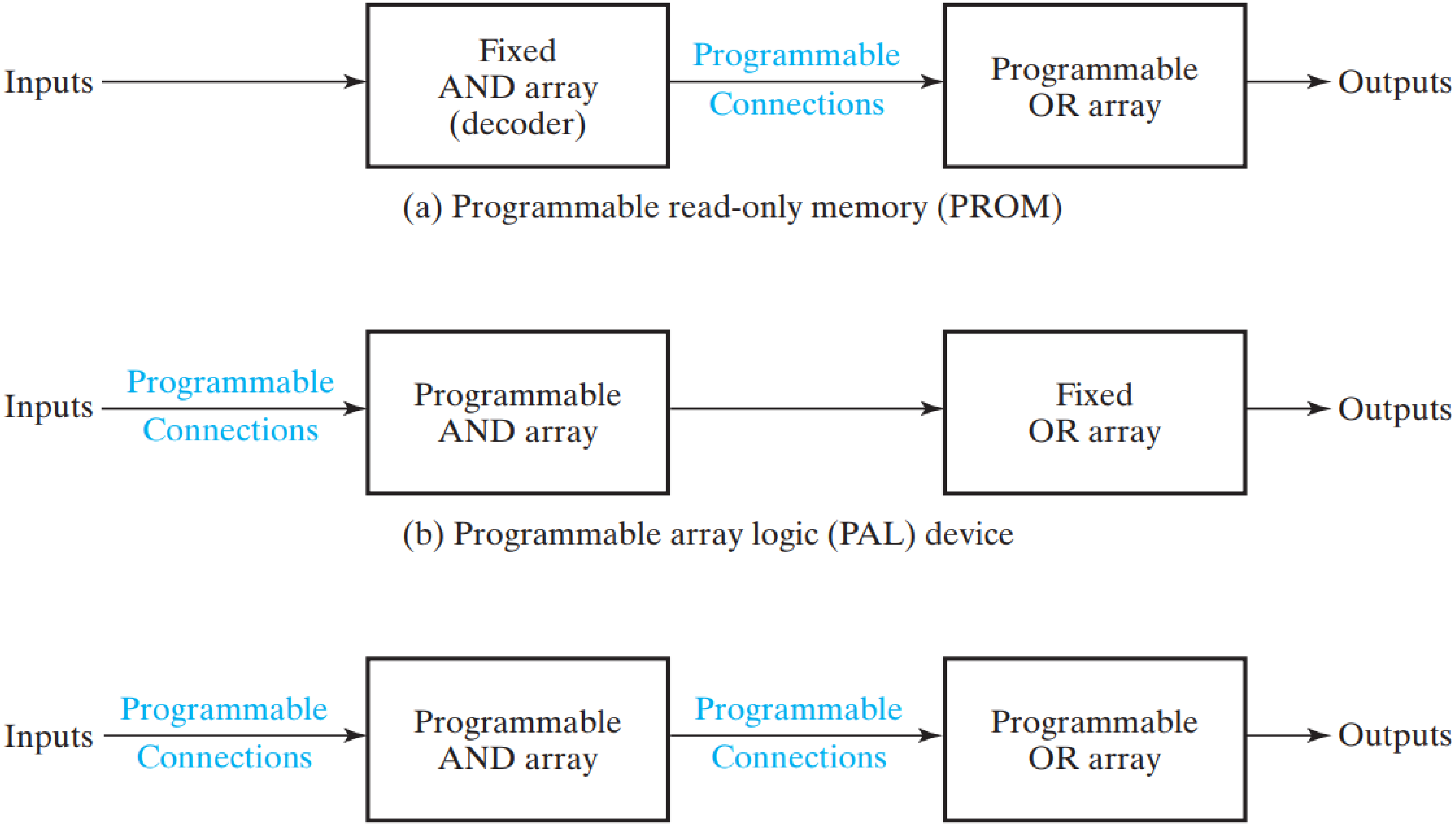
Convention


Standard Multiple AND Gate Symbol
AND Array Symbol
Standard Multiple OR Gate Symbol
OR Array Symbol


A
B
C
x Fuse intact
+ Fuse blown
1
2
3
4
AB
AC
BC
$\overline{A}\,\overline{B}\,\overline{C}$
C
$\overline{C}$
B
$\overline{B}$
A
$\overline{A}$
0
1
F_1
F_2

Classification

Major types of PLDs include PROM, PAL, and PLA



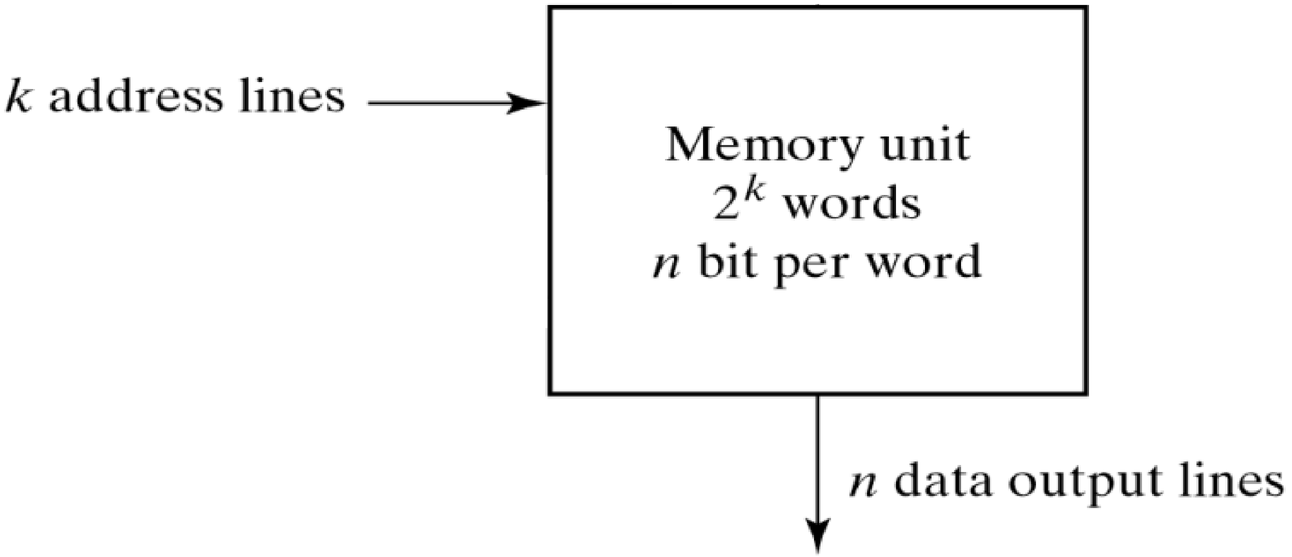
(a) Programmable read-only memory (PROM)

(b) Programmable array logic (PAL) device

(c) Programmable logic array (PLA) device

PROM

PROM is essentially consisted of a **Decoder** and a **Programmable OR plane.** The decoder is made of **Fixed AND plane.**



PROM Gate Plane

Address Lines, $k = 5$

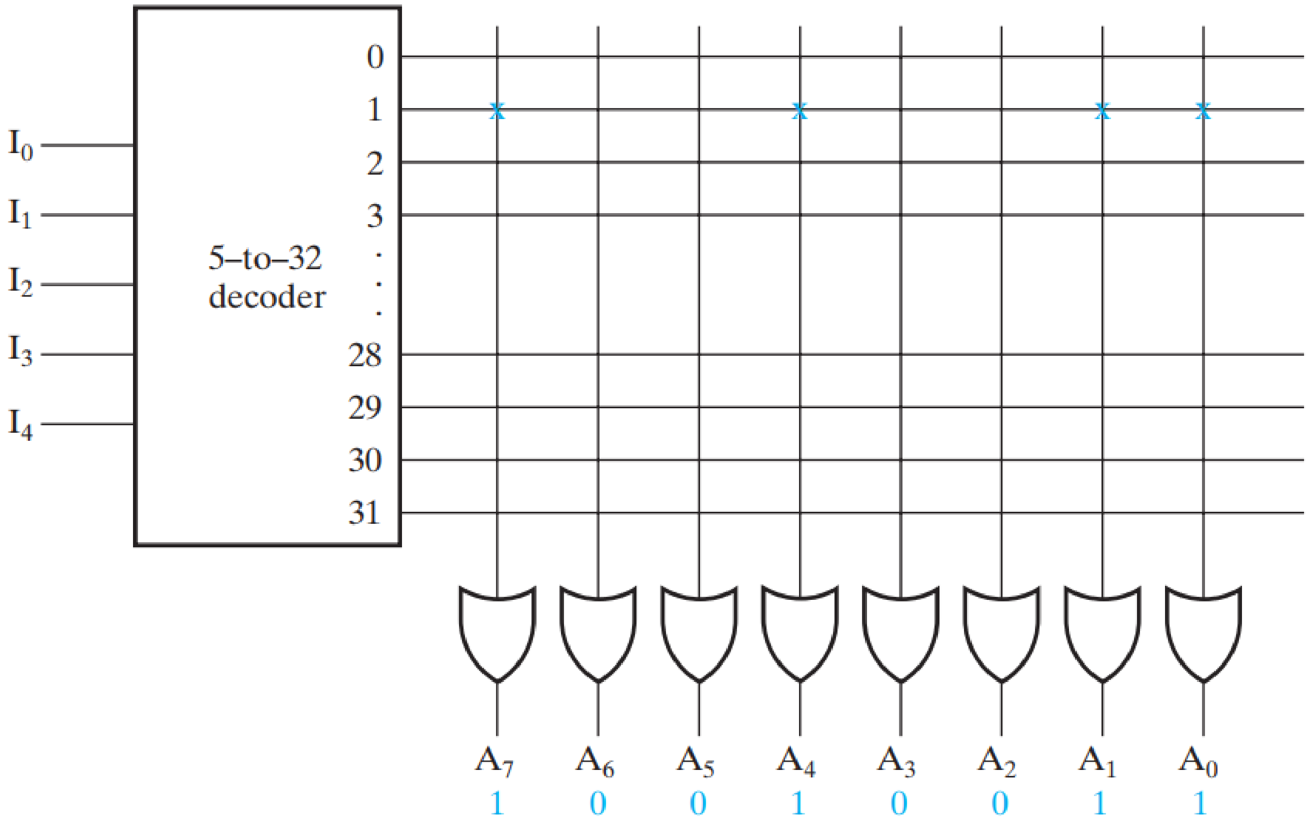
Address number= $2^k = 2^5 = 32$

Decoder dimension= $k - to - 2^k$ = 5-to-32 Decoder

Length of each word, n $= 8\ bits$

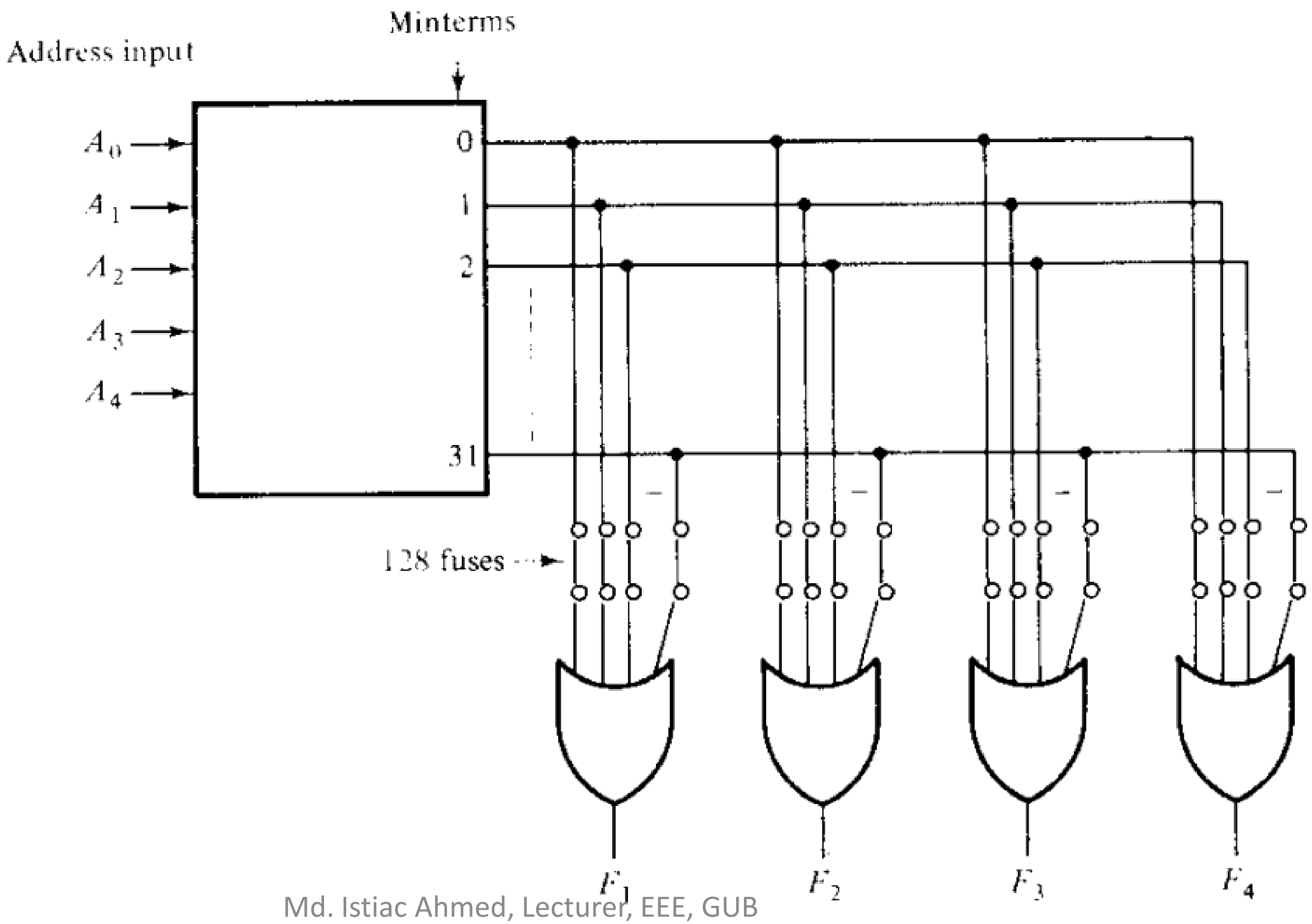
Each OR gate input line = $2^k = 2^5 = 32$

Total Programmable Internal Connections = $2^k \times n = 2^5 \times 8 = 256$



PROM Gate Plane Example

Address Lines =?
Address number = ?
Decoder dimension = ?
Length of each word =?
Each OR gate input line =?
Total Programmable Internal Connections =?



Designing with PROM

Implement the following Boolean functions with PROM

$$F_1(A_0, A_1) = \sum(1, 2, 3)$$

$$F_2(A_0, A_1) = \sum(0, 2)$$

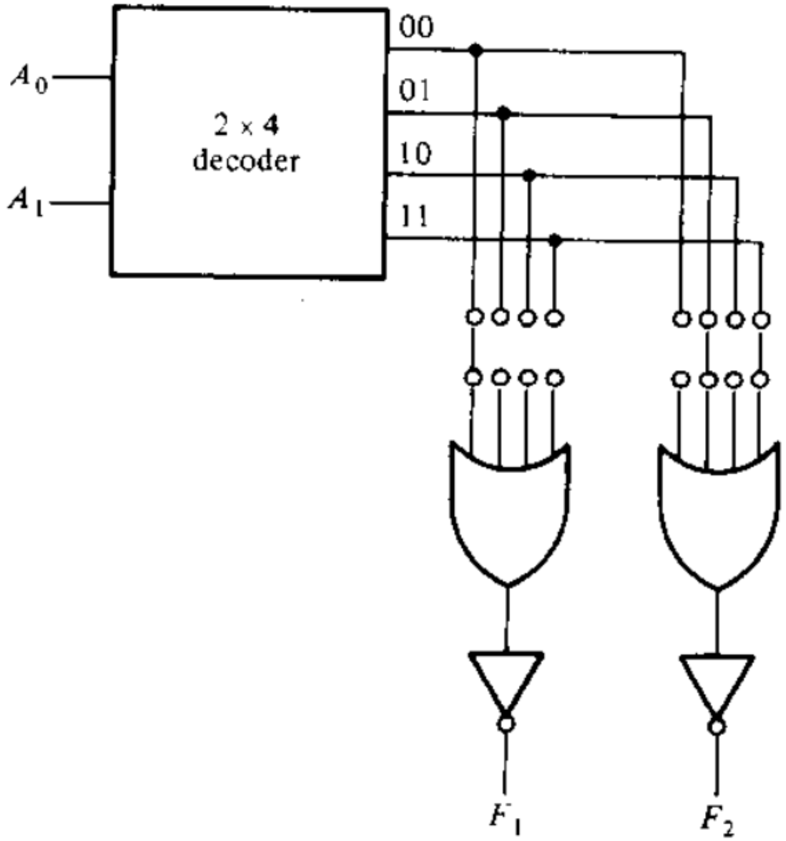
A_0	A_1	F_1	F_2
0	0	0	1
0	1	1	0
1	0	1	1
1	1	1	0

A_1 \ A_0	0	1
0	0	1
1	1	1

F_1

A_1 \ A_0	0	1
0	1	0
1	1	0

F_2



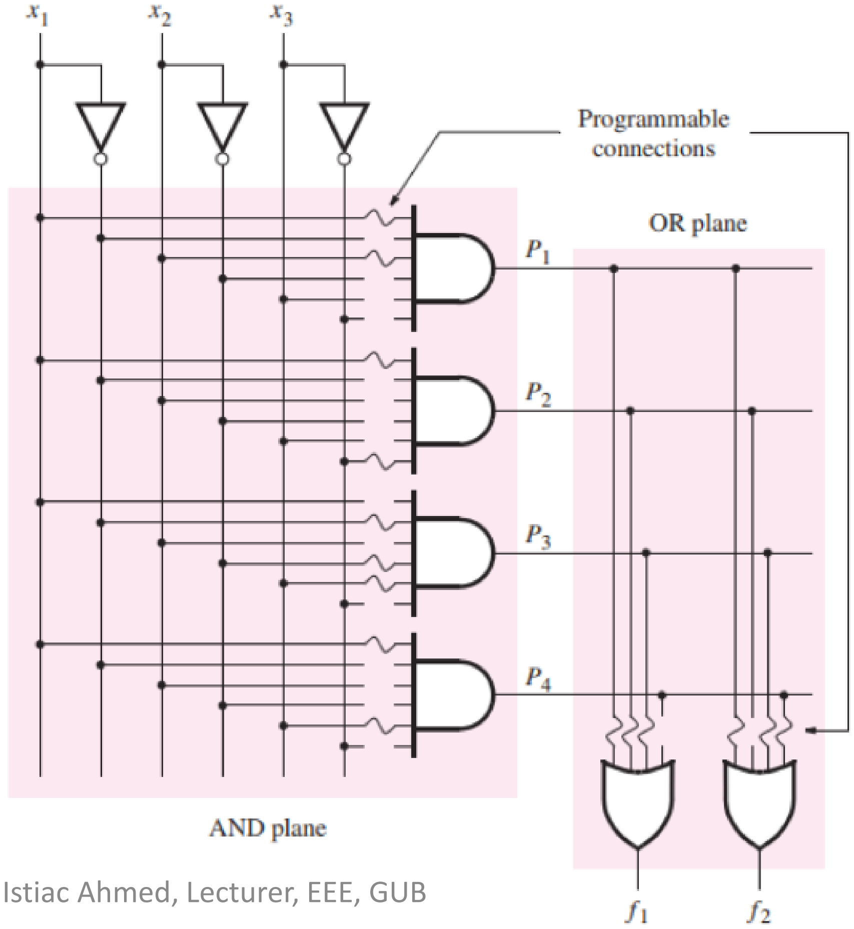
Class Task

Design a combinational circuit using PROM that accepts a 3-bit number and generates an output binary number equal to the square of the input number with necessary tabulations and illustrations.

PLA

Programmable Logic Array (PLA) has a **programmable AND array** and a **programmable OR array**.

No. of **AND** gates = No. of **Product terms**
No. of **OR** gates = No. of **Output functions**
No. of **NOT** gates = No. of **Inputs**



Implement the following functions using PLA.

$$F_1 = A\bar{B} + AC + \bar{A}B\bar{C}$$
$$F_2 = \overline{AC + BC}$$

Step 01: Simplification:

Step 02: Calculations:

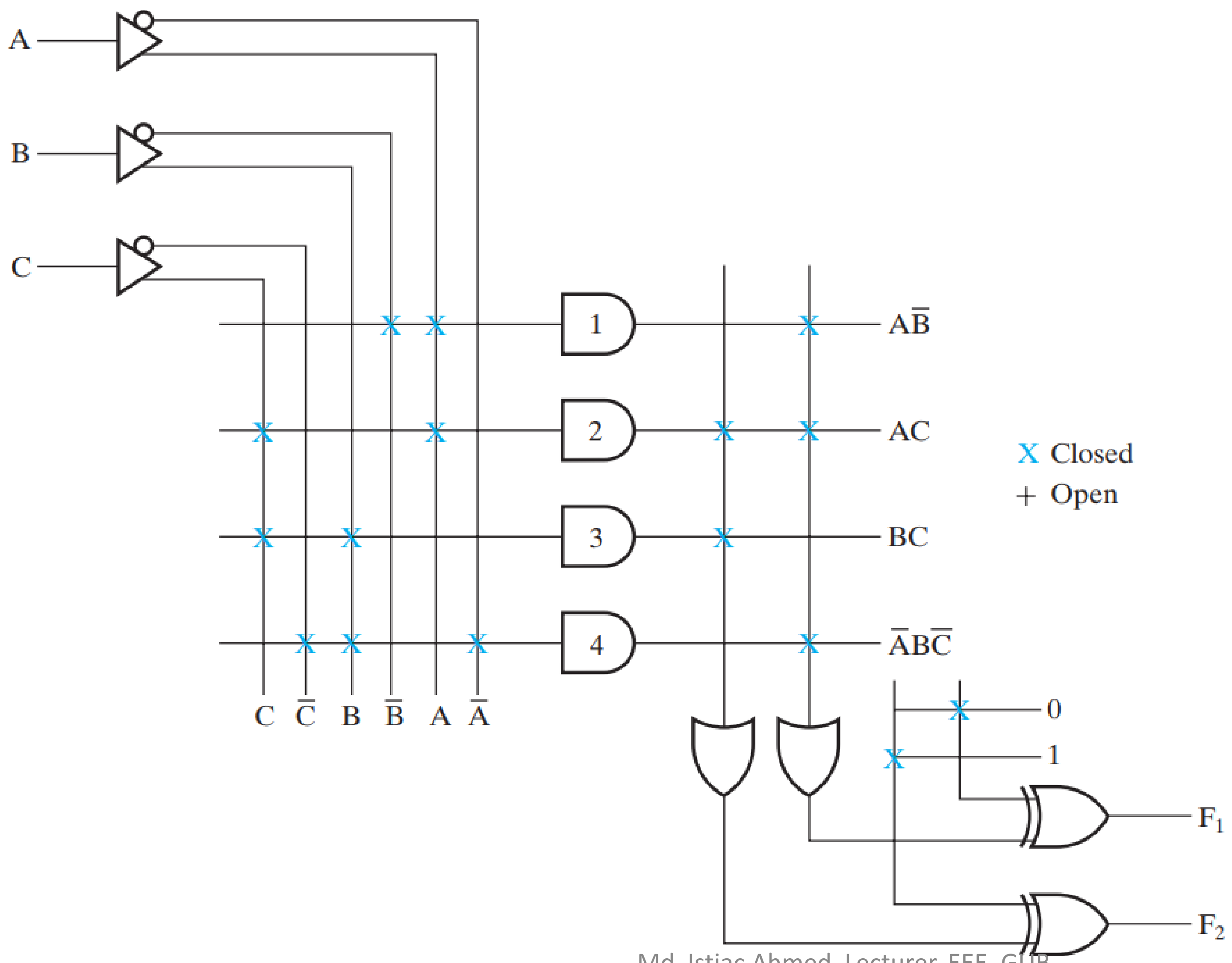
No. of **AND** gates = No. of **Product terms = 4**

No. of **OR** gates = No. of **Output functions = 2**

No. of **NOT** gates = No. of **Inputs = 3**

PLA Example

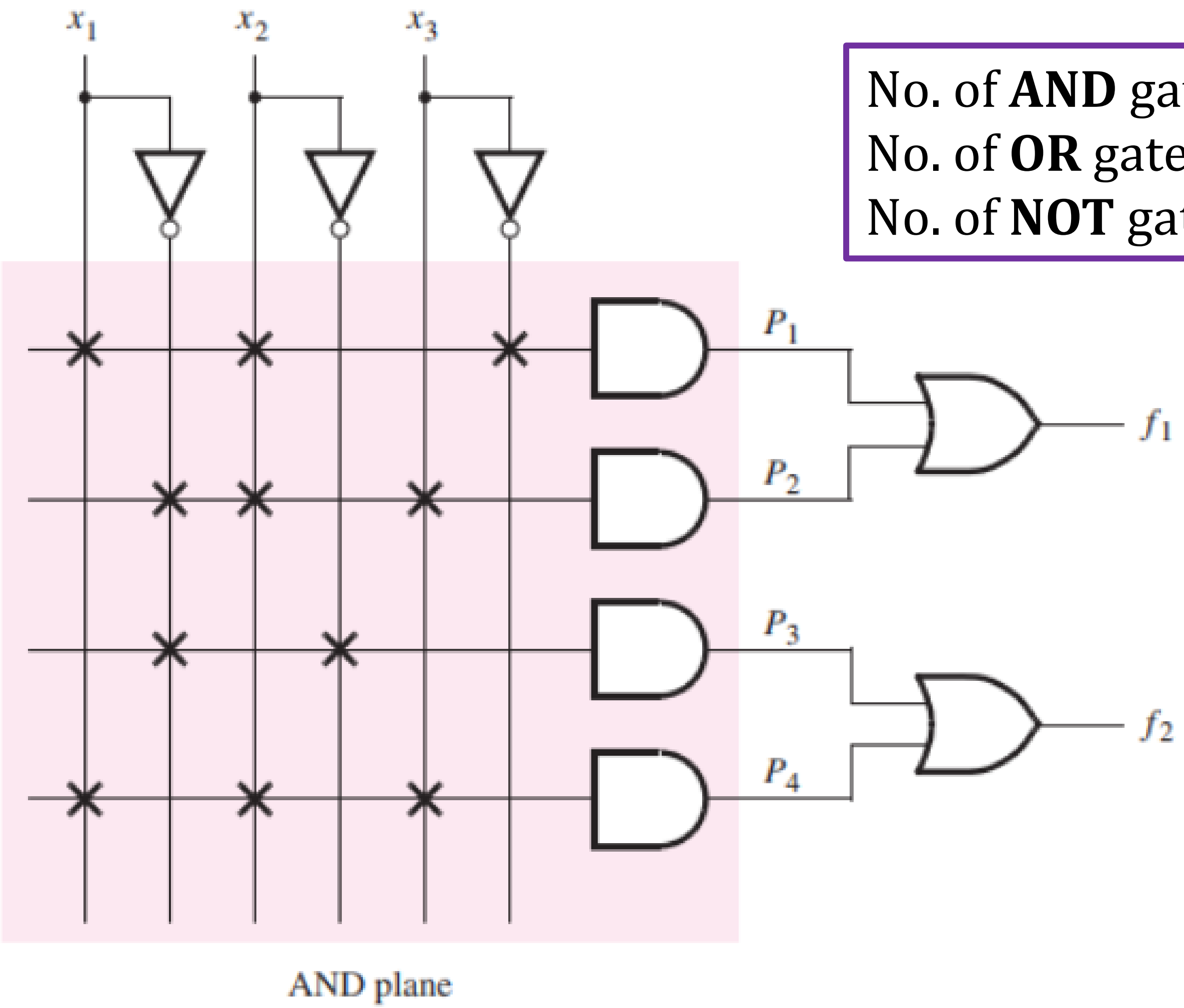
Step 03: Diagram:



PLA Example

PAL

Programmable Array Logic (PAL) has a **programmable AND array** and a **fixed OR array**.



No. of **AND** gates = No. of **Product terms**
No. of **OR** gates = No. of **Output functions**
No. of **NOT** gates = No. of **Inputs**

PAL or PLA
?

Design a 4-bit Adder-Subtractor using PLA & PAL

Thank You!