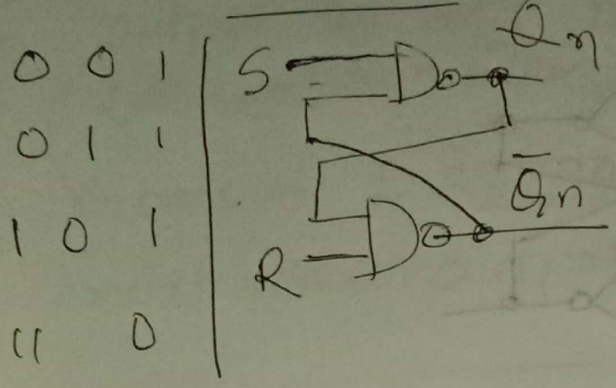
Part-1 → S-R Latch

(n+1) next state

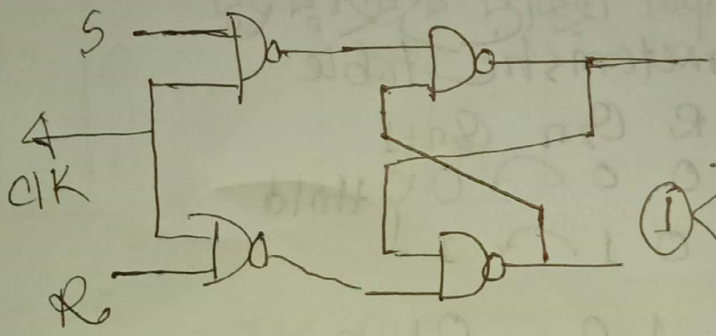
S	R	$Q_{(n+1)}$
0	0	Invalid (stated)
0	1	1
1	0	0
1	1	Hold stated



Part-2 → S-R ff:

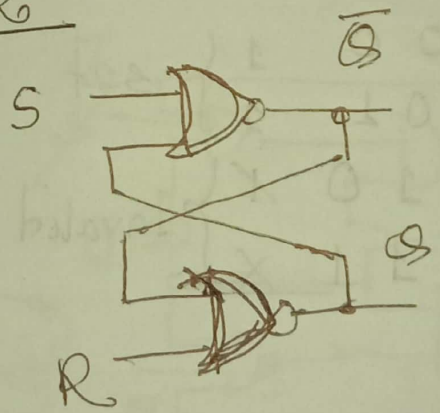
Truth → next output

clk	S	R	Q_{n+1}
Not trigger	x	x	Q_n
trigger	0	0	Hold
	0	1	0 (Reset)
	1	0	1 (set)
	1	1	Invalid



part-3 NOR

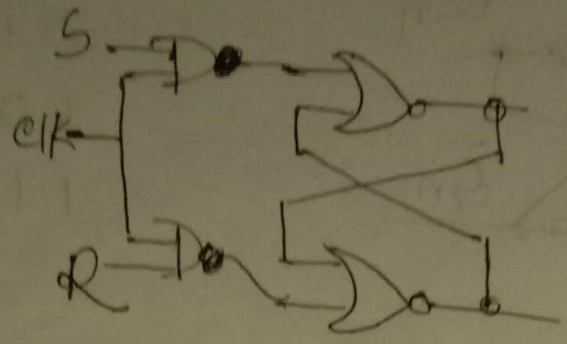
0 0	1
0 1	0
1 0	0
1 1	0



out বসাবো Q এর value

S	R	Q_{n+1}
0	0	Hold
0	1	0
1	0	1
1	1	Invalid

Part-4 S-R ff NOR gate



S-R ff characteristic & Excitation Table

↓

S, R input এবং present output কে input হিসাবে ব্যবহার করে

truth table

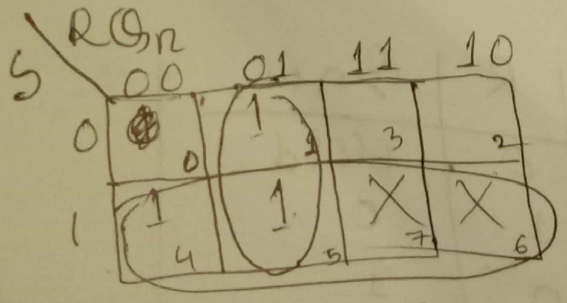
S	R	Q_{n+1}
0	0	Hold
0	1	0
1	0	1
1	1	Invalid

memory

characteristic table

S	R	Q_n	Q_{n+1}	
0	0	0	0	Hold
0	0	1	1	
0	1	0	0	Reset
0	1	1	0	
1	0	0	1	set
1	0	1	1	
1	1	0	X	Invalid
1	1	1	X	

characteristic eqn:



$Q_{n+1} = S + \bar{R} Q_n$

Excitation table;

↓

output এর উপর base input কি হবে সেটার জন্য excitation table বলে।

output 2 ধরনের হয় present state & next state output

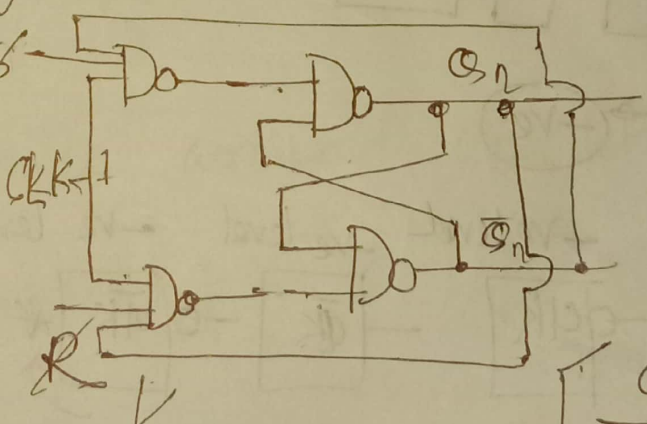
Q_n	Q_{n+1}	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

Part - 05

JK FF

আগের 75% SR FF

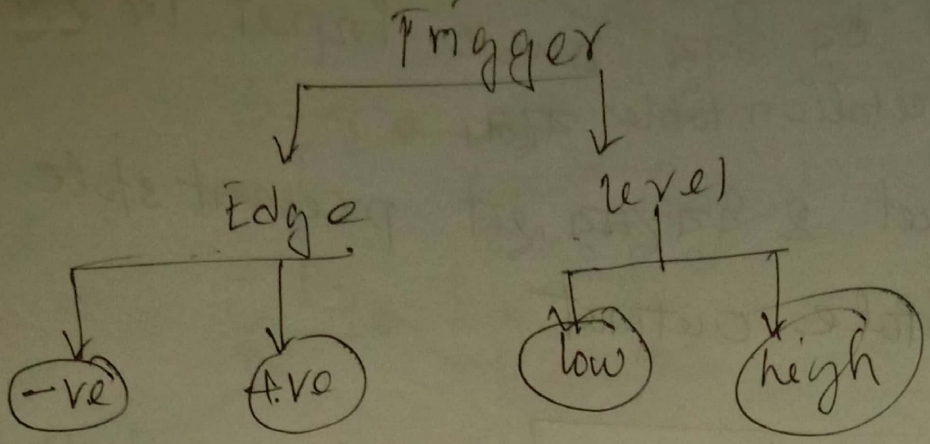
J	K	Q_{n+1}
0	0	→ Hold
0	1	→ 0
1	0	→ 1
1	1	→ Invalid → toggle → $\overline{Q_n}$



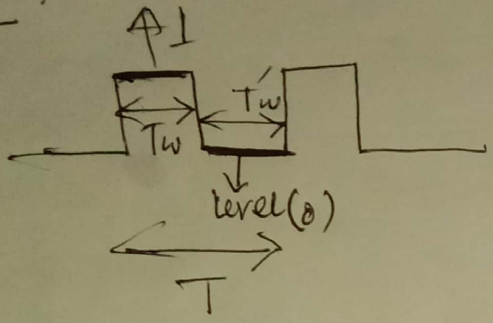
Case-1: $Q_n = 0$, $Q_{n+1} = 0$

Case-2: $Q_n = 0$, $Q_{n+1} = 1$

part-6

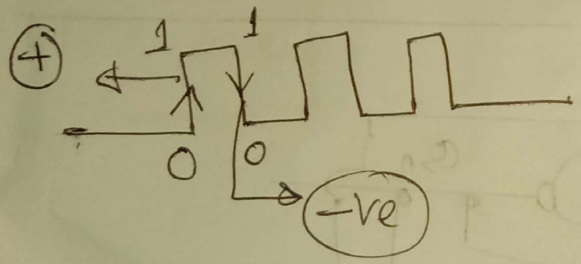


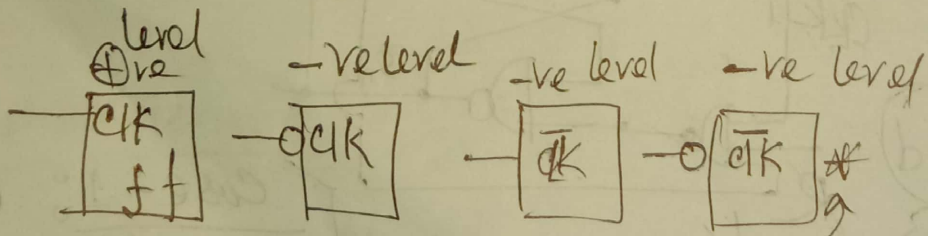
Ex:

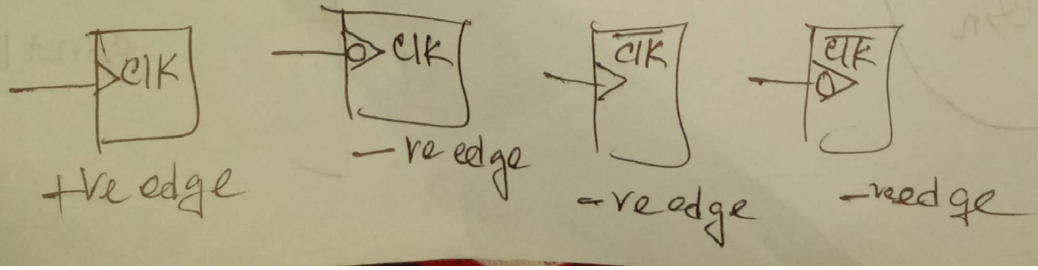


$T_w = \frac{T}{2}$

$T_w' = 2 * T_w$







Part-07 JK FF C table Ex table

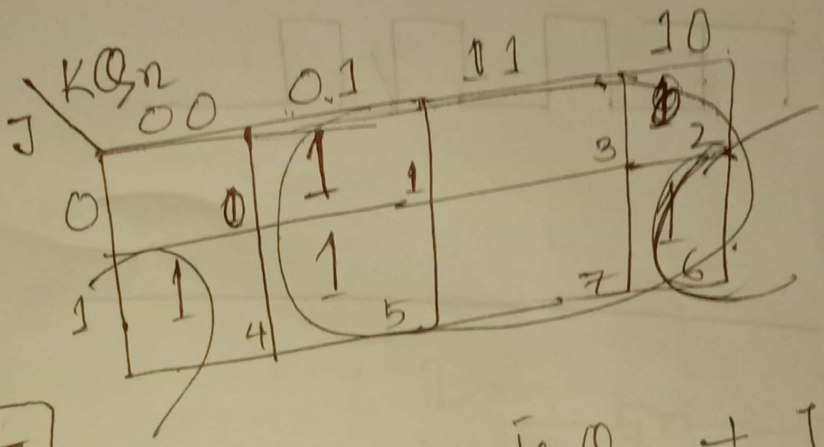
C table

J	K	Q_n	Q_{n+1}	
0	0	0	0	} Hold
0	0	1	1	
0	1	0	0	} Reset
0	1	1	0	
1	0	0	1	} set
1	0	1	1	
1	1	0 → 1		} toggle
1	1	1 → 0		

Ex table

Q_n	Q_{n+1}	J	K
0	0	0	×
0	1	1	×
1	0	×	1
1	1	×	0

J	K	Q_{n+1}
0	0	Hold
0	1	0
1	0	1
1	1	Toggle $\oplus \bar{Q}$



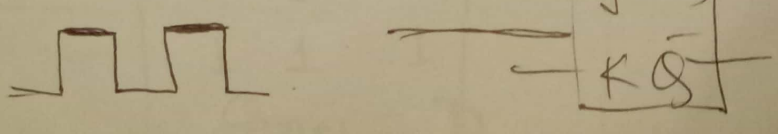
$$Q_{n+1} = \bar{K}Q_n + J\bar{Q}_n$$

Part-08 Race around condition

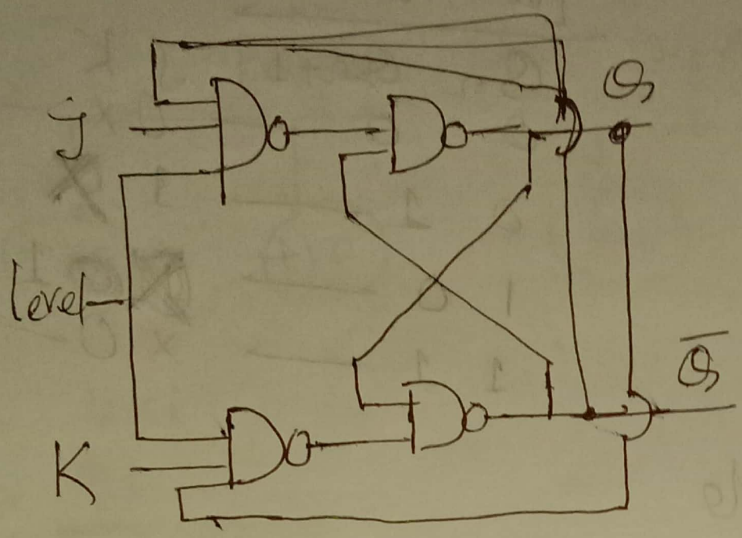
C_1 : level trigger J-K FF

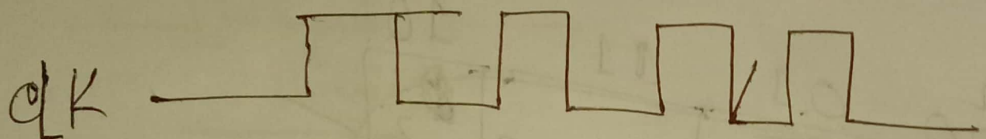
C_2 : When J=K=1 (Toggle mode)

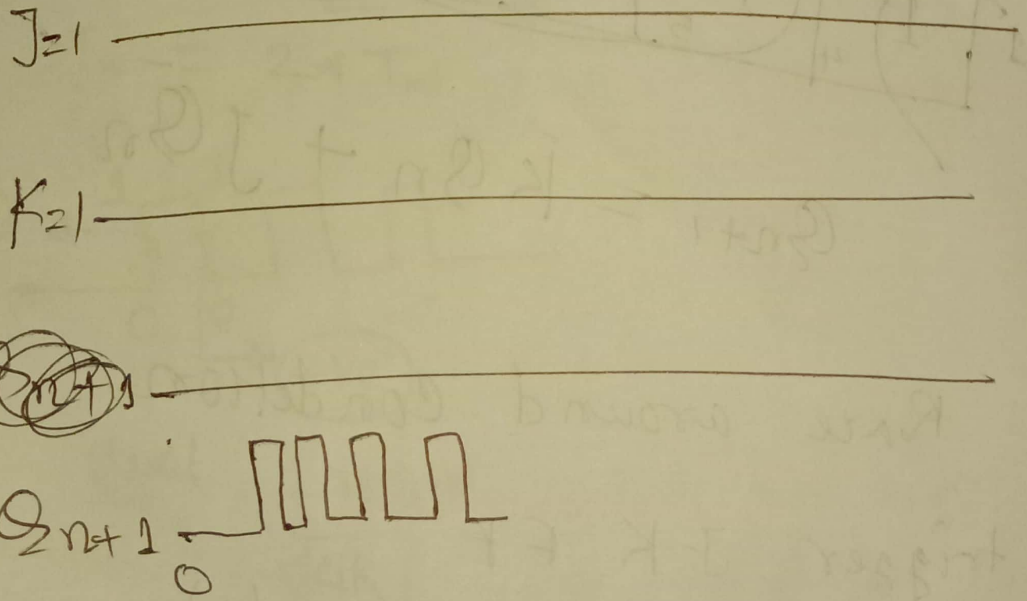
C_3 : $T_W >> T_d$ → Time taken from input → main circuit

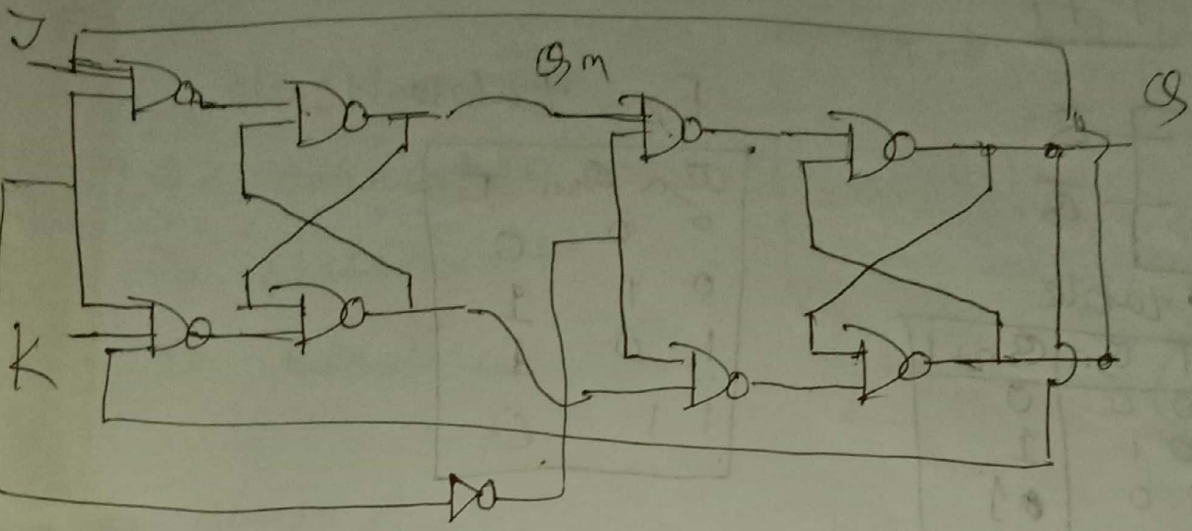


Part-9 master ff JK









J=1, K=1

Qm → active

Q → inactive

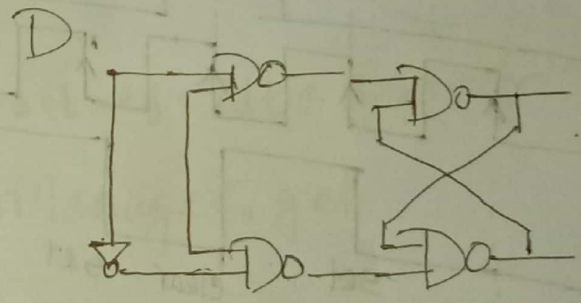
CLK

J = 1

K = 1

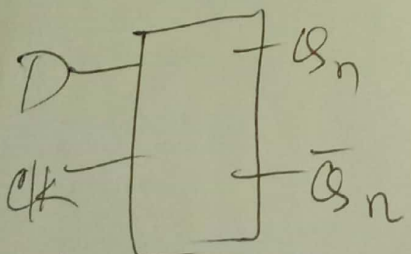
Qm

Q



Part - 10

D - FF



Truth table

D	Q_{n+1}
0	0
1	1

C table

D	Q_n	Q_{n+1}
0	0	0
0	1	0
1	0	1
1	1	1

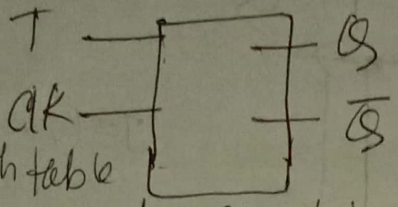
$Q_{n+1} = D$

Ex table

Q_n	Q_{n+1}	D
0	0	0
0	1	1
1	0	0
1	1	1

Part II

T-ff



truth table

T	Q_{n+1}
0	Q_n
1	$\bar{Q}_n$

C-table

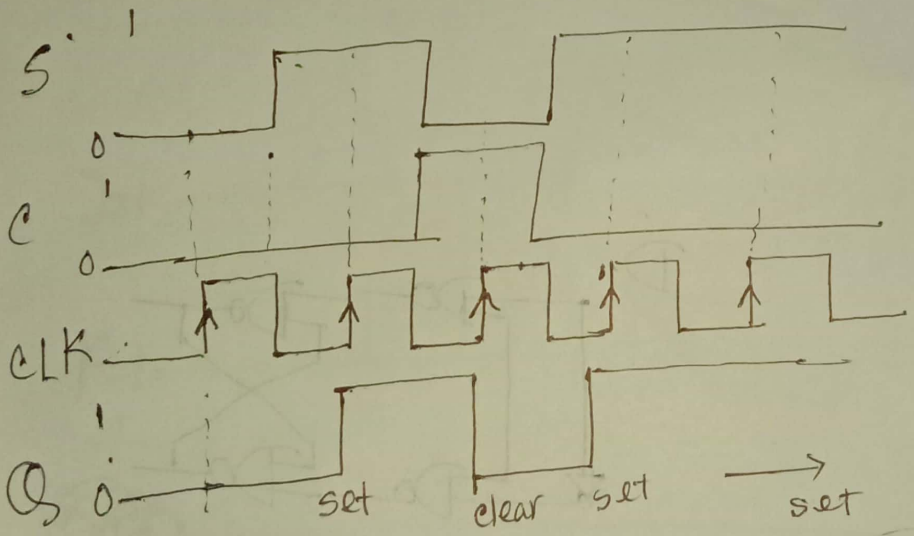
T	Q_n	Q_{n+1}
0	0	0
0	1	1
1	0	1
1	1	0

Ex-table

Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0

$Q_{n+1} = T \oplus Q_n$

Timing Diagram of SR ff



* J-K ff (Time আসবেই)

T-ff Mod 6 counter

Present state			next state				I/Ps of T ff		
Q_A	Q_B	Q_C	Q_{An+1}	Q_{Bn+1}	Q_{Cn+1}		T_A	T_B	T_C
0	0	0	0	0	1	0	0	0	1
0	0	1	0	1	0	1	0	1	1
0	1	0	0	1	1	2	0	0	1
0	1	1	1	0	0	3	1	1	1
1	0	0	1	0	1	4	0	0	1
1	0	1	1	1	0	5	1	0	1
1	1	0	1	1	1	6	1	1	0
1	1	1	0	0	0	7	1	1	1

$T_A = \sum m(3,5,6,7)$

$T_B = \sum m(1,3,6,7)$

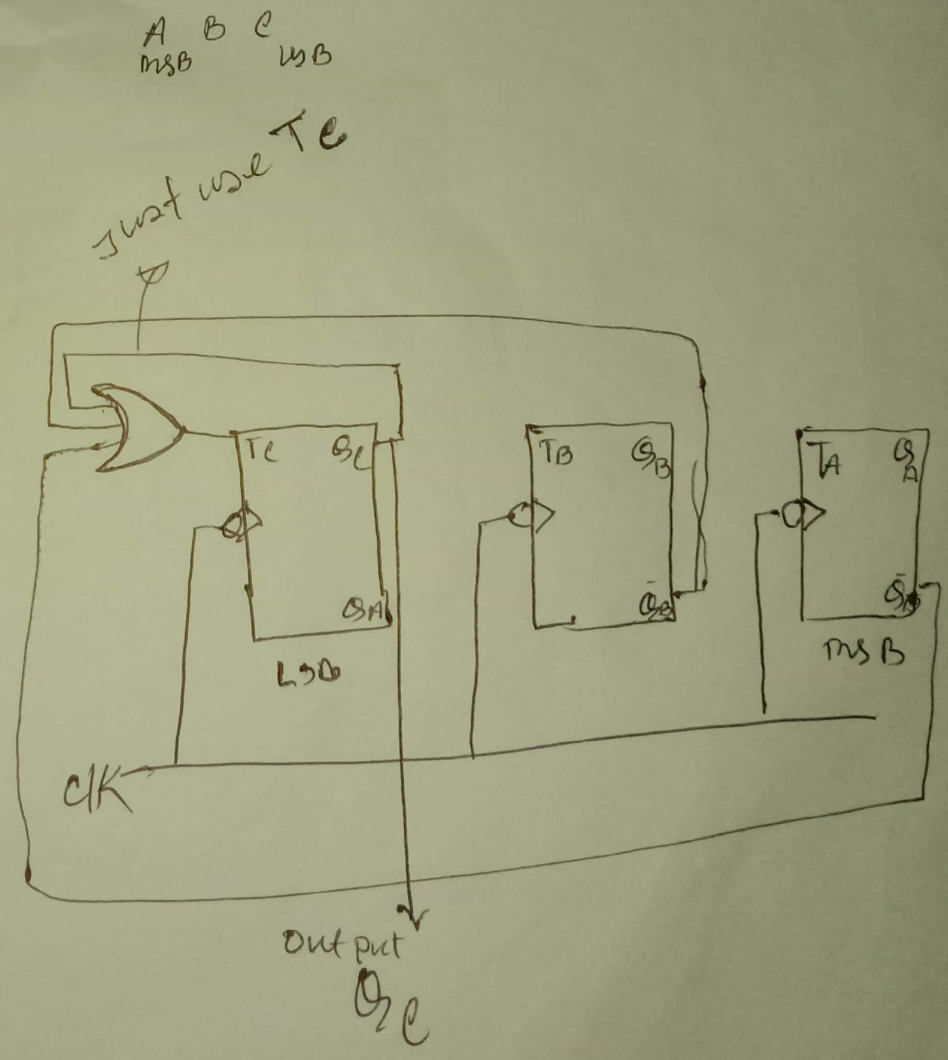
$T_C = \sum m(0,1,2,3,4,5,7)$

$T_A = Q_B Q_C + Q_A Q_C + Q_A Q_B$

$T_B = Q_A' Q_C + Q_A Q_B$

$T_C = Q_B' + Q_C + Q_A'$

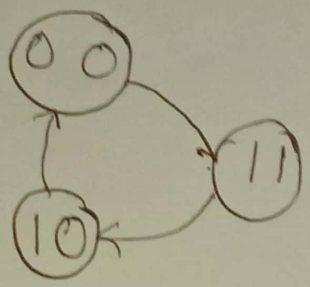
Q_n	Q_{n+1}	T
0	0	0
0	1	1
1	0	1
1	1	0



My ID is 2139022002

∴ Last 3 digit is 002 for this I take = 0 3 2

the state diagram



I have table creat 2 bit because my large digit is 3 this binary 11

Truth table

Present state		Next state	
Q_A	Q_B	Q_{A+1}	Q_{B+1}
0	0	1	1
0	1	X	X
1	0	0	0
1	1	1	0

	T_A	T_B
0	1	1
1	X	X
2	1	0
3	0	1

$$T_A = \sum m(0,2) + d(1)$$

$$T_B = \sum m(0,3) + d(1)$$

K-map

T_A

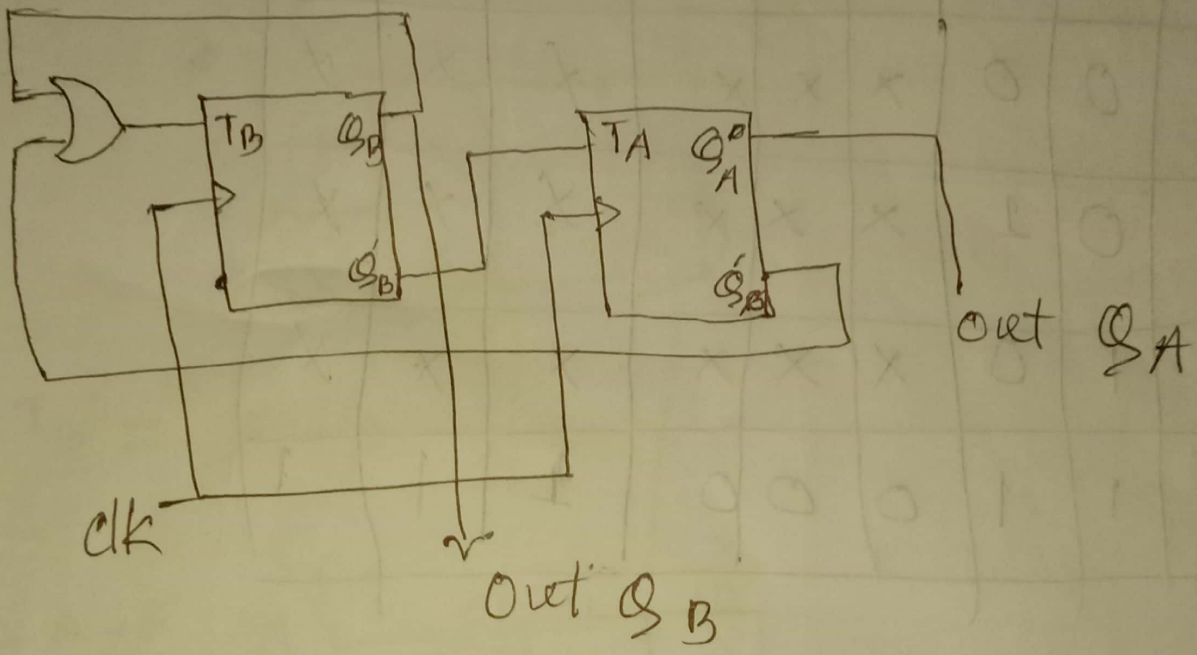
Q_A \ Q_B	0	1
0	1	X
1	1	

$T_A = Q'_B$

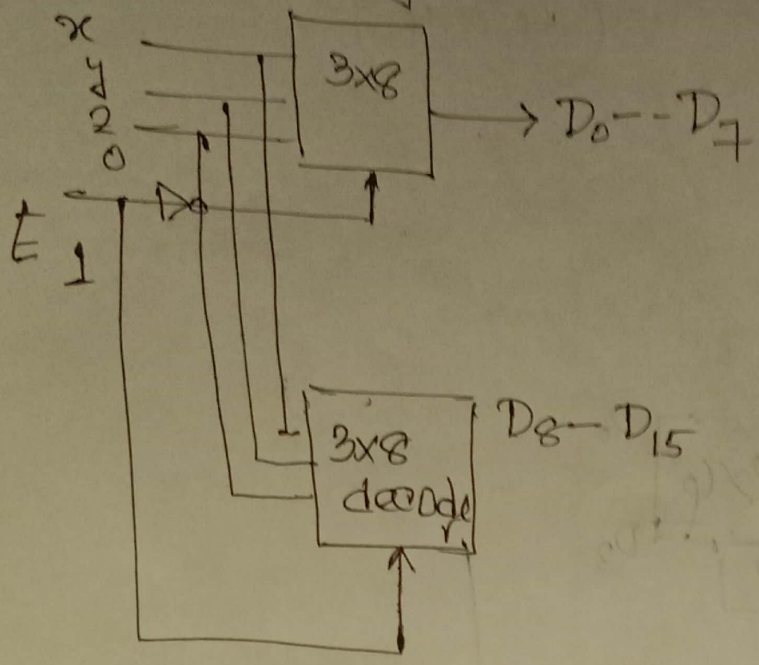
T_B

Q_A \ Q_B	0	1
0	1	X
1		1

$T_B = Q_B + Q'_A$

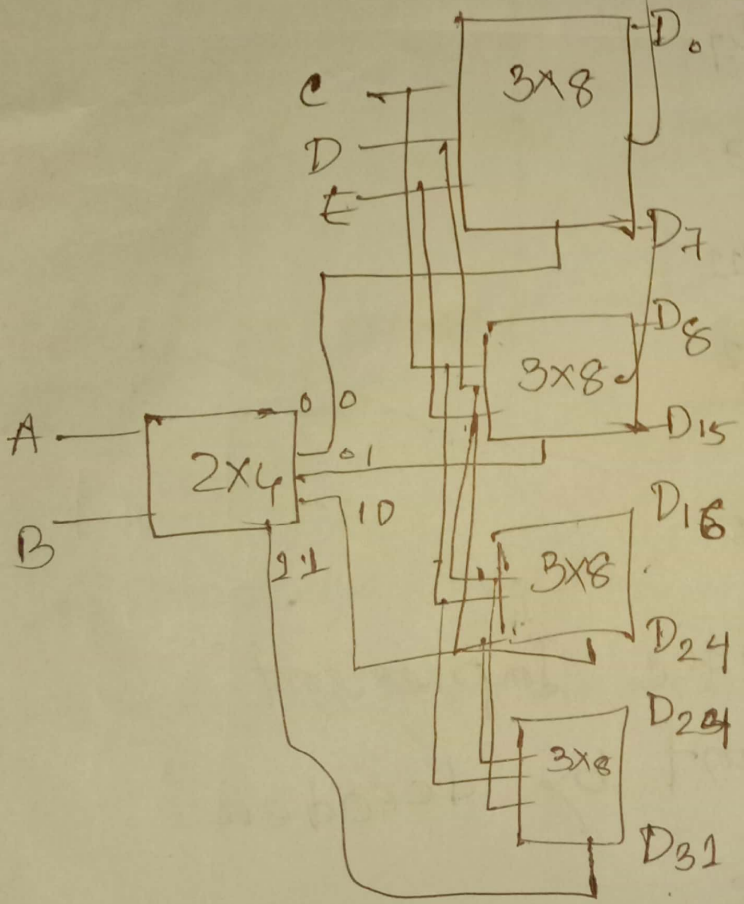


4×16 → making 3×8



5×32 → 3×8 (4)

5×32 → 3×8 (4) → 2×4

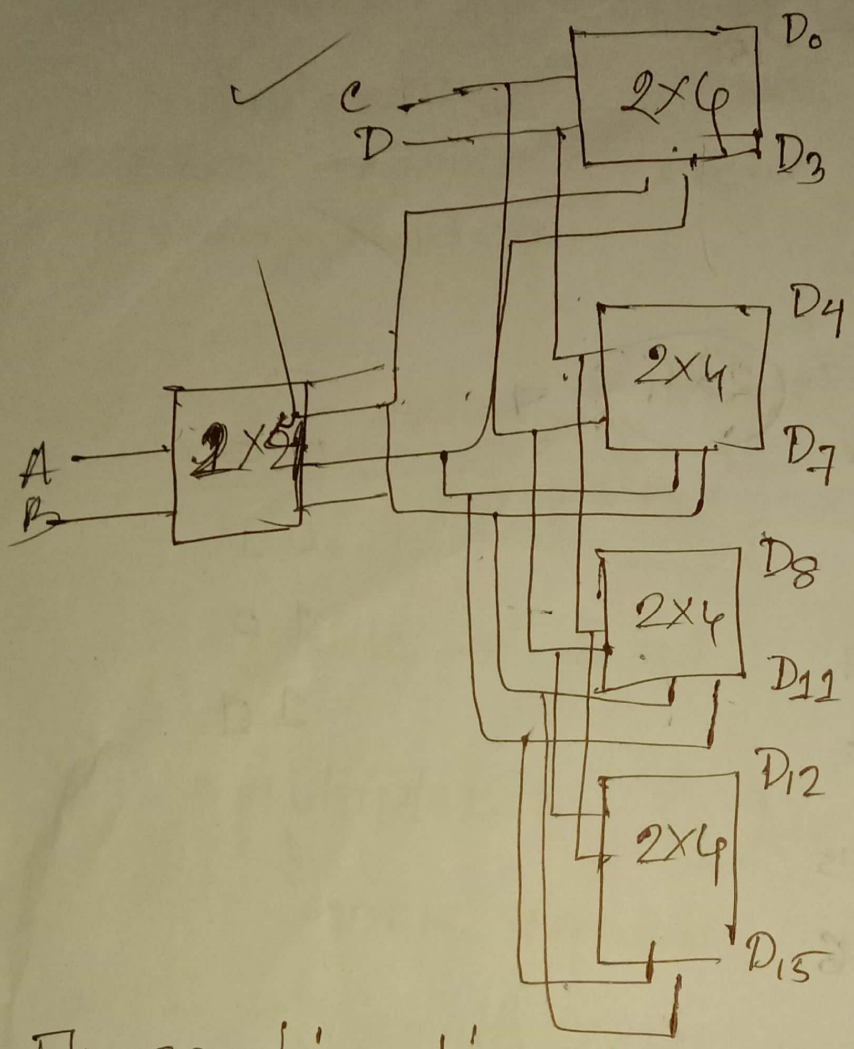


0 0
0 1
1 0
1 1

4 x 16

4 x 4

2x4



Combinational logic Implement

→ Full-adder implement by decoder

→ extra OR gate
↗ minterm

→ $K > 2^n/2$

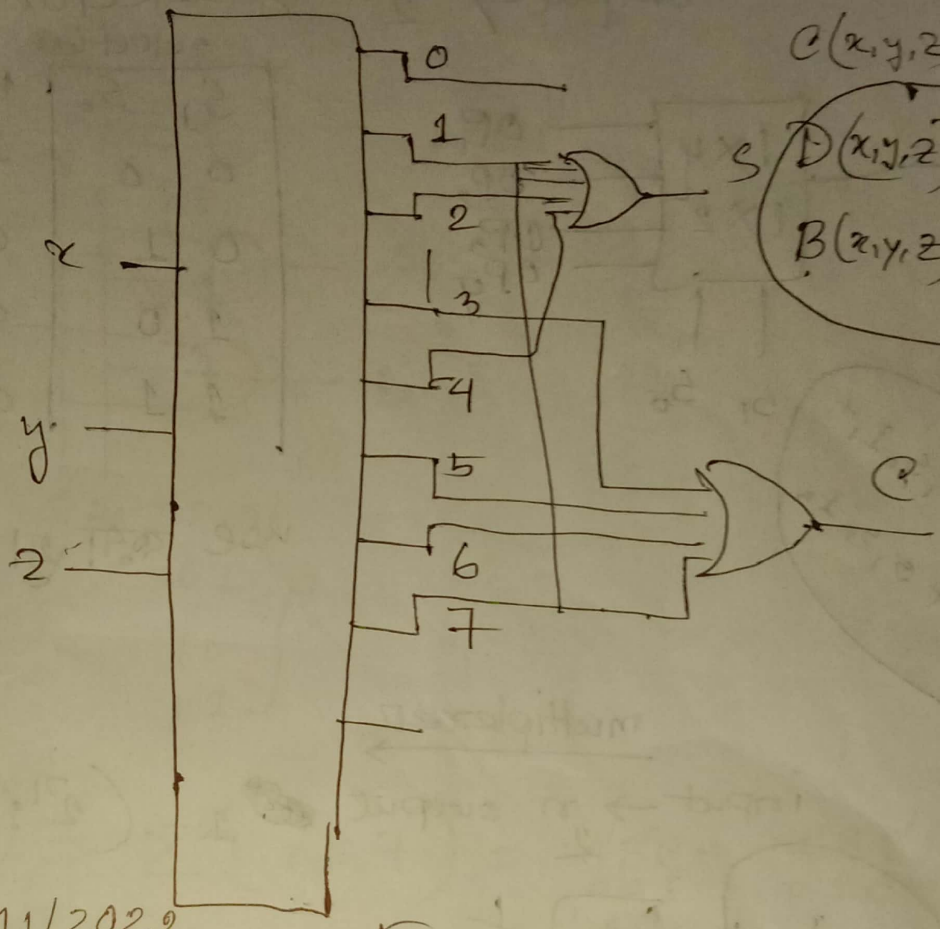
Full - subtractor (How)

$S(x,y,z) = (1,2,4,7)$

$C(x,y,z) = (3,5,6,7)$

$D(x,y,z) = (1,2,4,7)$

$B(x,y,z) = (1,2,3,7)$



Date: 29/11/2022

F_2

Encoder:

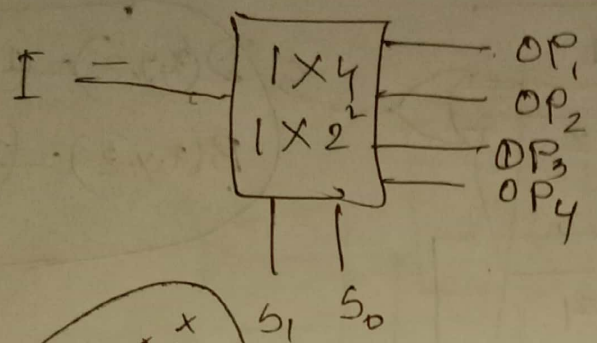
* Priority encoder:

→ multiplexer → Data communication

Demultiplexer

input → 1 :

output → 2^n → selector line



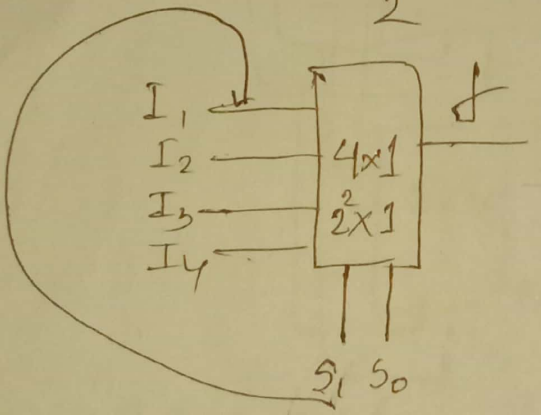
select line		output			
S_1	S_0	P_1	P_2	P_3	P_4
0	0	I	0	0	0
0	1	0	I	0	0
1	0	0	0	I	0
1	1	0	0	0	I

$S_1'S_0'I_0 + S_1'S_0I_1 + S_1S_0'I_2 + S_1S_0I_3$

use করা হয় switch হিসাবে কাজ করে.

multiplexer

input → 2^n output. 1 $(2^n : 1)$



0 0 → output – I_1

0 1 → u – I_2

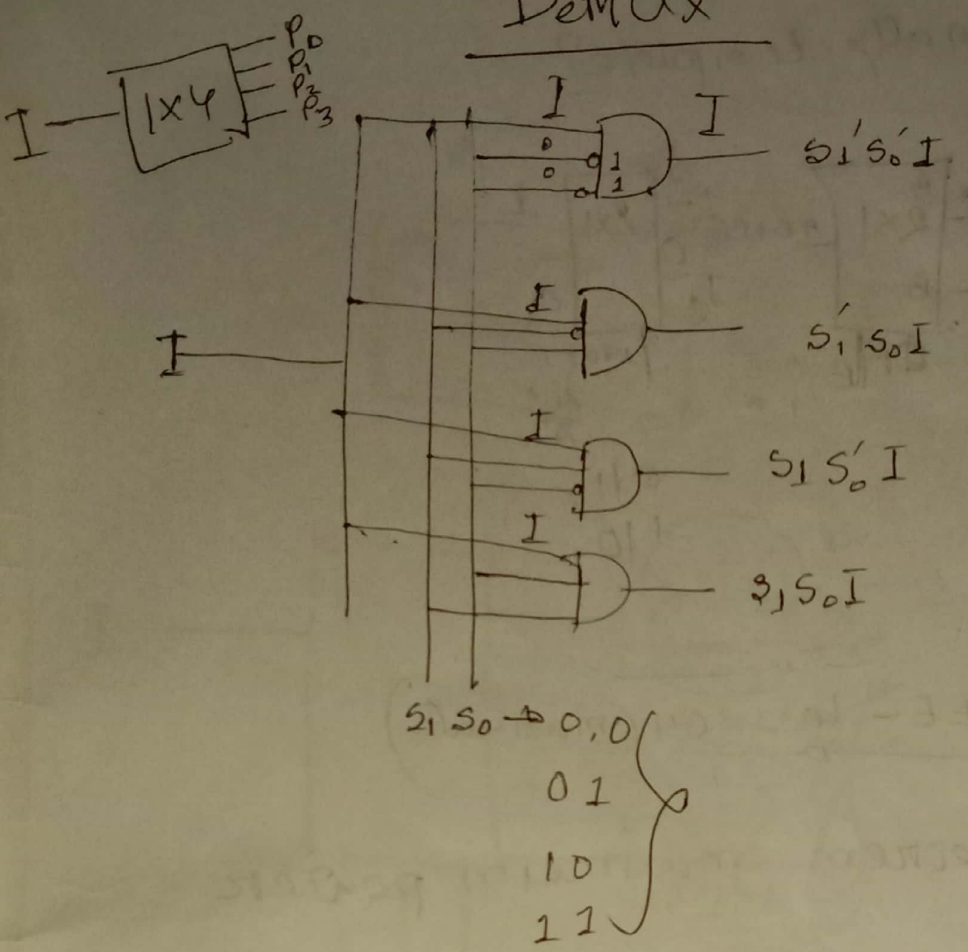
1 0 → u → I_3

1 1 → u → I_4

$f = \bar{S}_1\bar{S}_0I_1 + S_1'S_0I_2 + S_1$

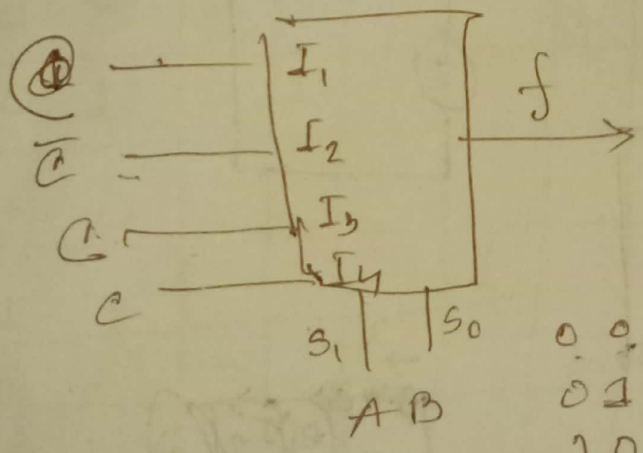
$+ S_1S_0I_4$

DeMUX



$$f(A,B,C) = \Sigma(1,2,5,7) = A'B'C + A'BC' + AB'C + ABC$$

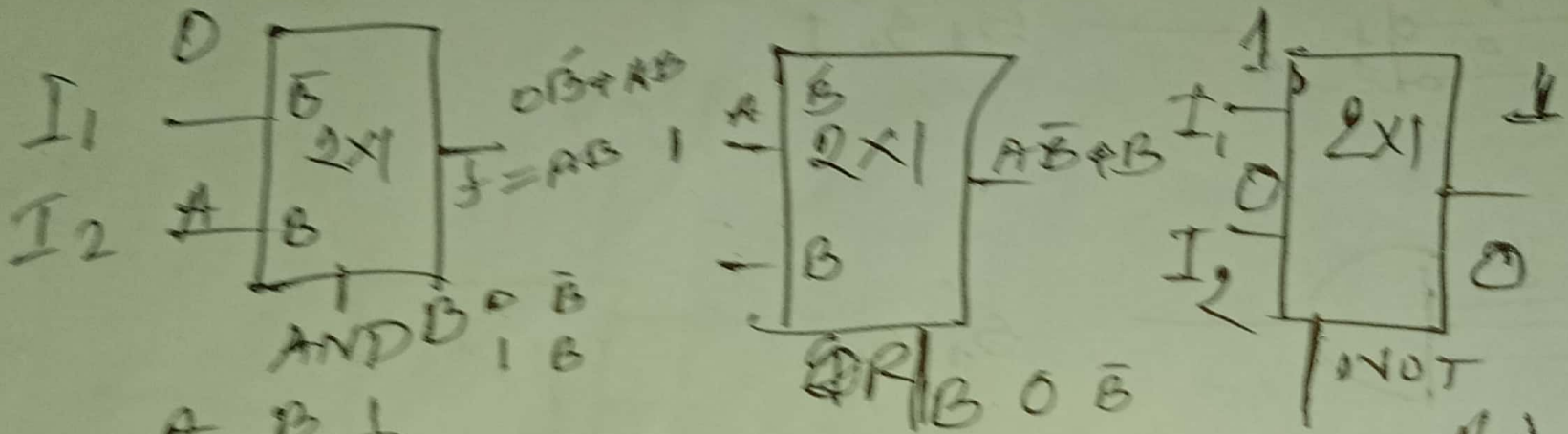
001 010 101 111



$A'B'C + A'B\bar{C} + AB'C + ABC$

0 0 I_1
0 1 I_2
1 0 I_3
1 1 I_4

multiplexer functionally complete?



A	B	F
0	0	0
0	1	0
1	0	0
1	1	1

A	$\bar{A}$
0	1
1	0