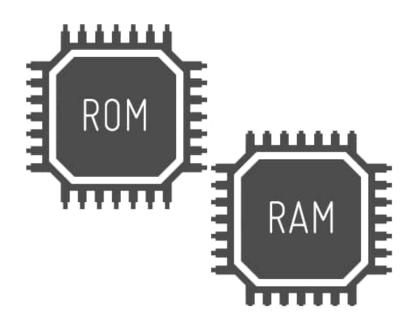
Memory Systems

EEE 203: Electronic Devices and Circuits & Pulse Techniques



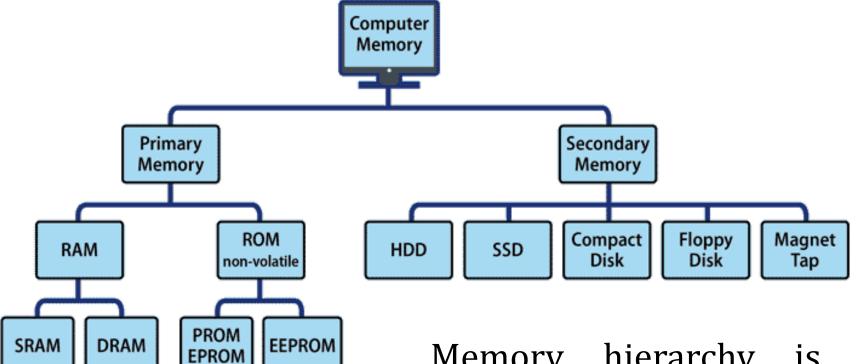


What is Memory?



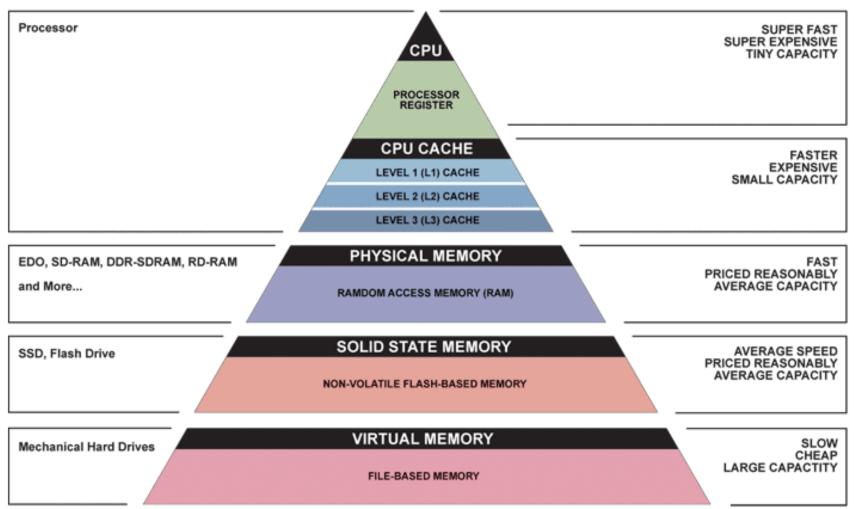
Memory refers to **storages** of **data**. These storings can be **temporary** or **permanent** depending on the design.

Memory Hierarchy



Memory hierarchy is the organized sorting of total memory capacity of different components in a computer

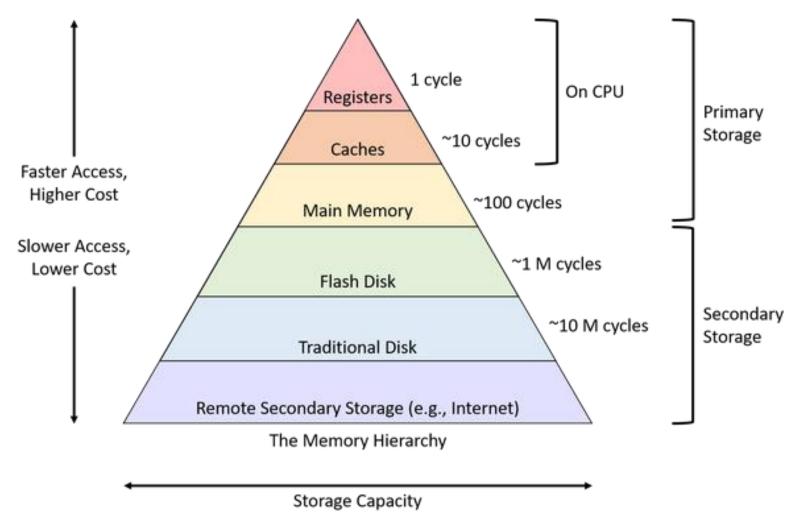
Computer Memory Hierarchy



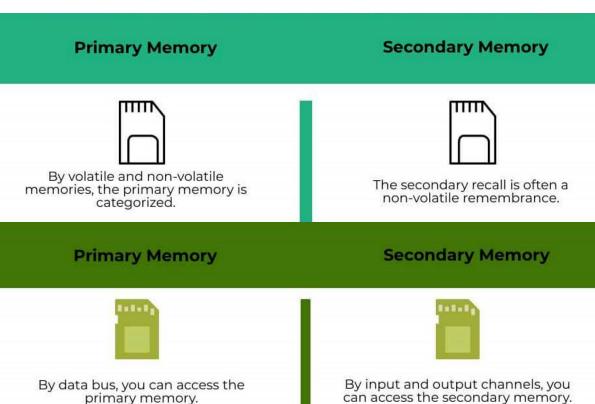
▲ Simplified Computer Memory Hierarchy

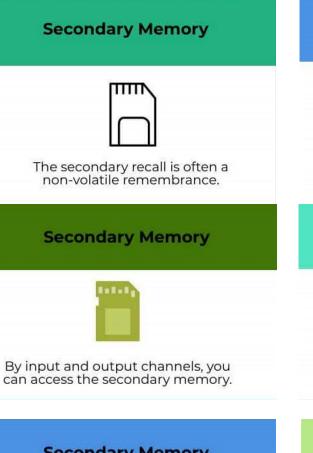
Illustration: Ryan Utilengmed, Lecturer, EEE, GUB

Hierarchy Pyramid Characteristics

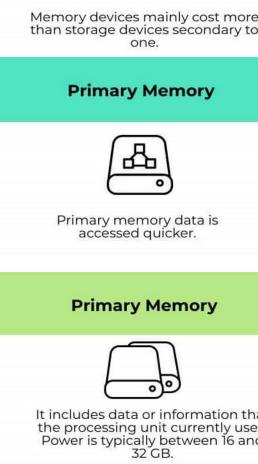


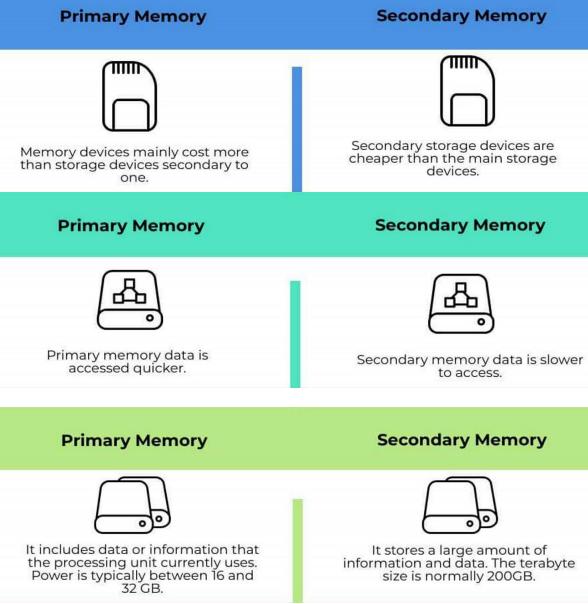
- Capacity
- Access Time
- Cost/bit
- Performance









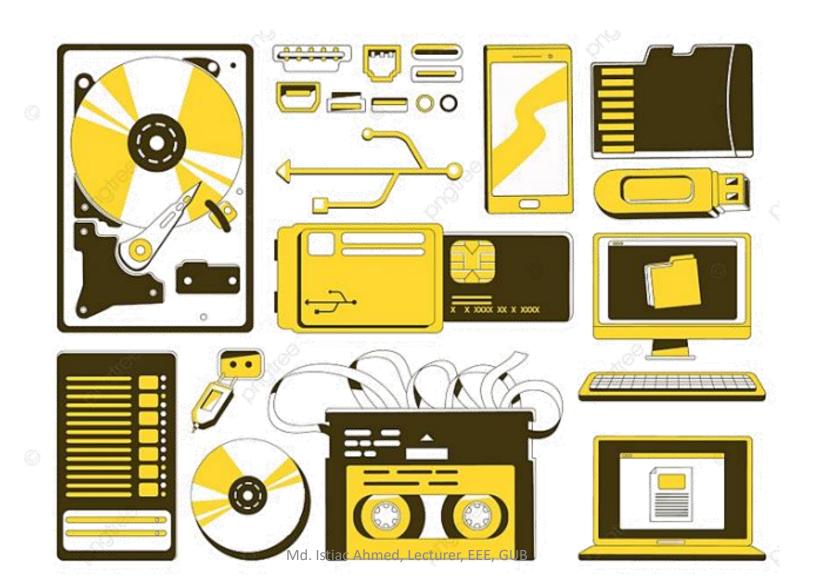






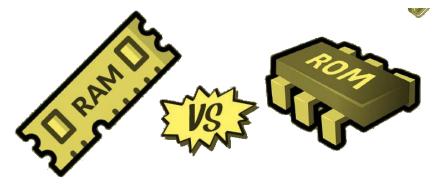
Data
Acquisition
and
Preservation
in Fauna

Digital Memory



Input-output connectors Audio chip PCI extension slots Motherboard power supply connector Processor support Chipset (1) Chipset (2) Processor power supply connector RAM connectors CMOS battery Disk drive and floppy drive connectors Case fastipower supply urer, EEE, GUB

Primary Memory



Difference Between



RAM VERSUS ROM

2 KEY DIFFERENCES

Data can be both stored and retrieved from RAM (Random-Access Memory) Data can be only read from ROM (Read-Only Memory)

RAM is a volatile memory, so once the voltage supply is lost, the data is removed from the memory

Click here to go to main differences

ROM is a non-volatile memory. If it is not erasable, data remains in storage until the hardware is damaged

Visit www.differencebetween.com

- Capacitor-Transistor Model
- Periodic Refreshing

To activate DRAM cell for read/write operation, the access transistor must be turned-on using the WL.

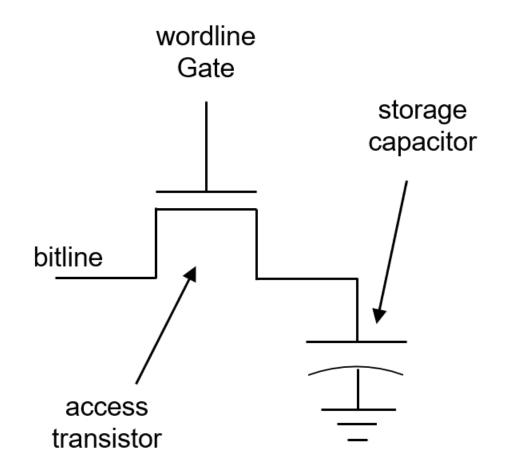
READ Operation

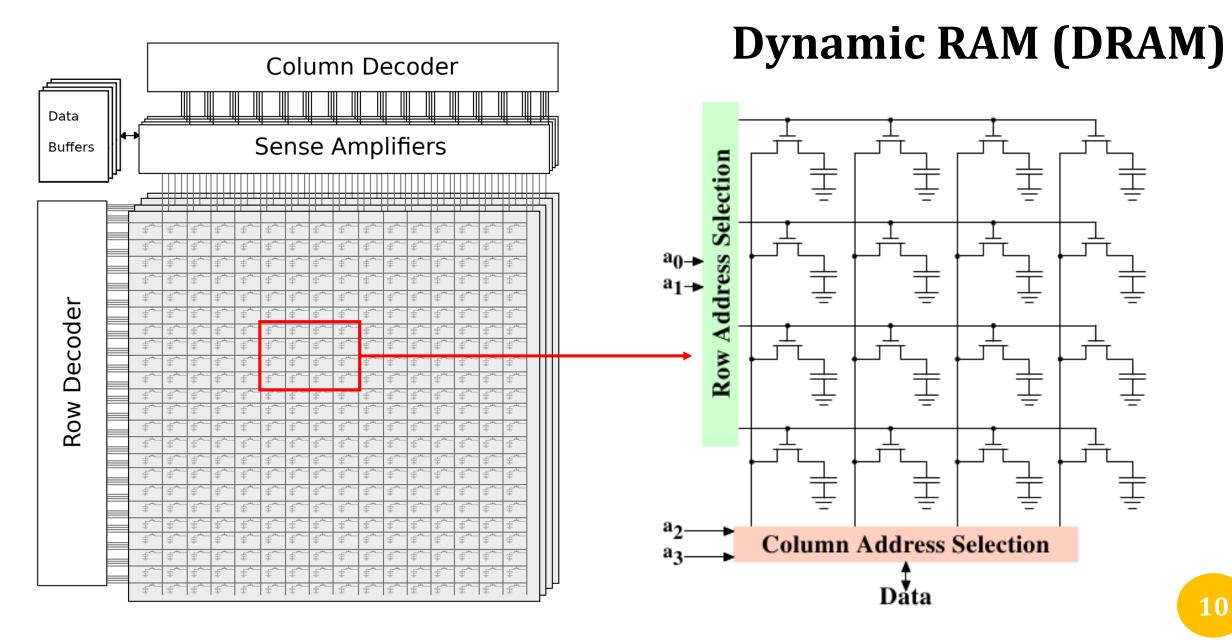
Capacitor voltage is sensed from the BL using the sense amplifier connected to it (not shown in the cell)

WRITE Operation

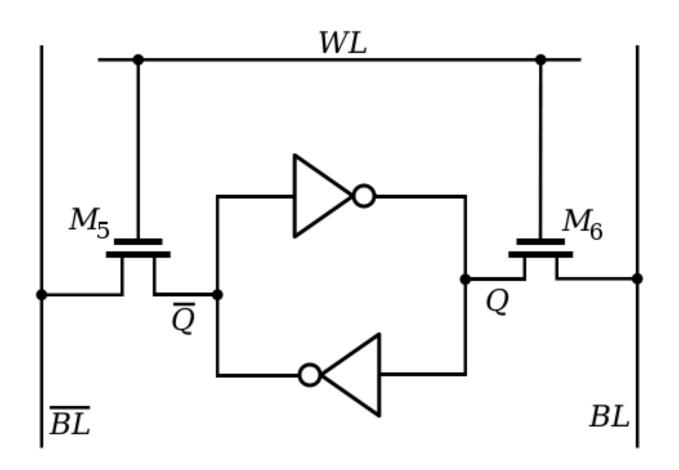
Capacitor is charged to the voltage applied in the BL.

Dynamic RAM (DRAM)





Static RAM (SRAM)



- Transistor Model
- Data is held statically

To activate SRAM cell for read/write operation, the access transistor must be turned-on using the WL.

4T & 6T SRAM Cell

