



**JEPPIAAR**  
INSTITUTE OF TECHNOLOGY  
“Self-Belief | Self Discipline | Self Respect”



## **QUESTION BANK**

Regulation :2017

Year/Semester :III

Semester :05

Batch :2017-2021

**DEPARTMENT OF  
COMPUTER SCIENCE AND ENGINEERING**

## **INSTITUTION VISION**

Jeppiaar Institute of Technology aspires to provide technical education in futuristic technologies with the perspective of innovative, industrial and social application for the betterment of humanity.

## **INSTITUTION MISSION**

- To produce competent and disciplined high quality professionals with the practical skills necessary to excel as innovative professionals and entrepreneurs for the benefit of the society.
- To improve the quality of education through excellence in teaching and learning, research, leadership and by promoting the principles of scientific analysis, and creative thinking.
- To provide excellent infrastructure, serene and stimulating environment that is most conducive to learning
- To strive for productive partnership between the Industry and the Institute for research and development in the emerging fields and creating opportunities for employability
- To serve the global community by instilling ethics, values and life skills among the students needed to enrich their lives.

## **Department Vision**

To produce Engineers with visionary knowledge in the field of Computer Science and Engineering through scientific and practical education in stance of inventive, modern and communal purpose for the improvement of society.

## **Department Mission**

**M1:** Devise students for technical and operational excellence, upgrade them as competent engineers and entrepreneurs for country's development.

**M2:** Develop the standard for higher studies and perpetual learning through creative and critical thinking for the effective use of emerging technologies with a supportive infrastructure.

**M3:** Involve in a constructive, team oriented environment and transfer knowledge to balance the industry-institute interaction.

**M4:** Enrich students with professional integrity and ethical standards that will make them deal social challenges successfully in their life.

## **Program Educational Objectives (PEOs)**

**PEO 1:** To support students with substantial knowledge for developing and resolving mathematical, scientific and engineering problems.

**PEO 2:** To provide students with adequate training and opportunities to work as a collaborator with informative and administrative qualities.

**PEO 3:** To motivate students for extensive learning to prepare them for graduate studies, R&D and competitive exams.

**PEO 4:** To cater students with industrial exposure in an endeavour to succeed in the emerging cutting edge technologies.

**PEO 5:** To shape students with principled values and to follow the code of ethics in social and professional life.

## **Program Specific Outcomes (PSOs)**

**PSO 1** : Students are able to analyse, design, implement and test any software with the programming and testing skills they have acquired.

**PSO 2:** Students are able to design and develop algorithms for real time problems, scientific and business applications through analytical, logical and problems solving skills.

**PSO 3:** Students are able to provide security solution for network components and data storage and management which will enable them to work efficiently in the industry.

## BLOOM'S TAXONOMY

### Definition:

- A theory to identify cognitive levels (Levels of thinking)
- Represents the full range of cognitive functions.

### Objectives:

- To classify educational learning objectives into levels of complexity and specificity. The classification covers the learning objectives in cognitive, affective and sensory domains.
- To structure curriculum learning objectives, assessments and activities.

### Levels in Bloom's Taxonomy:

- **BTL 1 – Remember** - The learner is able to recall, restate and remember learned information.
- **BTL 2 – Understand** - The learner grasps the meaning of information by interpreting and translating what has been learned.
- **BTL 3 – Apply** - The learner makes use of information in a context similar to the one in which it was learned.
- **BTL 4 – Analyze** - The learner breaks learned information into its parts to best understand that information.
- **BTL 5 – Evaluate** - The learner makes decisions based on in-depth reflection, criticism and assessment.
- **BTL 6 – Create** - The learner creates new ideas and information using what has been previously learned.

## TABLE OF CONTENT

<b>MA8551 – ALGEBRA AND NUMBER THEORY</b>		
<b>Unit No.</b>	<b>Topic</b>	<b>Page No.</b>
	Syllabus	1.1
I	Groups And Rings	1.3
II	Finite Fields And Polynomials	1.15
III	Divisibility Theory And Canonical Decompositions	1.21
IV	Diophantine Equations And Congruences	1.28
V	Classical Theorems And Multiplicative Functions	1.36
<b>CS8591 – COMPUTER NETWORKS</b>		
	Syllabus	2.1
I	Introduction And Physical Layer	2.2
II	Data-Link Layer & Media Access	2.12
III	Network Layer	2.25
IV	Transport Layer	2.33
V	Application Layer	2.40
<b>EC8691- MICROPROCESSORS AND MICROCONTROLLERS</b>		
	Syllabus	3.1
I	The 8086 Microprocessor	3.3
II	8086 System Bus Structure	3.17
III	I/O Interfacing	3.26
IV	Microcontroller	3.38
V	Interfacing Microcontroller	3.48
<b>CS8501-THEORY OF COMPUTATION</b>		
	Syllabus	4.1
I	Automata Fundamentals	4.2
II	Regular Expressions And Languages	4.10
III	Context Free Grammar And Languages	4.16
IV	Properties Of Context Free Languages	4.22
V	Undecidability	4.28
<b>CS8592 - OBJECT ORIENTED ANALYSIS AND DESIGN</b>		
	Syllabus	5.1
I	Unified Process And Use Case Diagrams	5.2
II	Static Uml Diagrams	5.10
III	Dynamic And Implementation Uml Diagrams	5.16
IV	Design Patterns	5.23
V	Testing	5.31

OMD551- BASICS OF BIOMEDICAL INSTRUMENTATION		
	Syllabus	6.1
I	Bio Potential Generation And Electrode Types	6.3
II	Bio signal Characteristics And Electrode Configurations	6.15
III	Signal Conditioning Circuit	6.31
IV	Measurement Of Non-Electrical Parameters	6.42
V	Bio-Chemical Measurement	6.63

**MA8551****Algebra and Number Theory****LPTC  
4004****OBJECTIVES:**

- To introduce the basic notions of groups, rings, fields which will then be used to solve related problems.
- To introduce and apply the concepts of rings, finite fields and polynomials.
- To understand the basic concepts in number theory
- To examine the key questions in the Theory of Numbers.
- To give an integrated approach to number theory and abstract algebra, and provide a firm basis for further reading and study in the subject.

<b>UNIT I</b>	<b>GROUPS AND RINGS</b>	<b>12</b>
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Groups: Definition - Properties - Homomorphism - Isomorphism - Cyclic groups - Cosets - Lagrange's theorem. Rings: Definition - Sub rings - Integral domain - Field - Integer modulo n - Ring homomorphism.

<b>UNIT II</b>	<b>FINITE FIELDS AND POLYNOMIALS</b>	<b>12</b>
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Rings - Polynomial rings - Irreducible polynomials over finite fields - Factorization of polynomials over finite fields.

<b>UNIT III</b>	<b>DIVISIBILITY THEORY AND CANONICAL DECOMPOSITIONS</b>	<b>12</b>
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Division algorithm – Base - b representations – Number patterns – Prime and composite numbers – GCD – Euclidean algorithm – Fundamental theorem of arithmetic – LCM.

<b>UNIT IV</b>	<b>DIOPHANTINE EQUATIONS AND CONGRUENCES</b>	<b>12</b>
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Linear Diophantine equations – Congruence's – Linear Congruence's - Applications : Divisibility tests - Modular exponentiation-Chinese remainder theorem – 2 x 2 linear systems.

<b>UNIT V</b>	<b>CLASSICAL THEOREMS AND MULTIPLICATIVE FUNCTIONS</b>	<b>12</b>
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Wilson's theorem – Fermat's little theorem – Euler's theorem – Euler's Phi functions – Tau and Sigma functions.

**TOTAL: 60 PERIODS****OUTCOMES :**

**Upon successful completion of the course, students should be able to:**

- Apply the basic notions of groups, rings, fields which will then be used to solve related problems.
- Explain the fundamental concepts of advanced algebra and their role in modern mathematics and applied contexts.
- Demonstrate accurate and efficient use of advanced algebraic techniques.
- Demonstrate their mastery by solving non - trivial problems related to the concepts, and by proving simple theorems about the, statements proven by the text.

- Apply integrated approach to number theory and abstract algebra, and provide a firm basis for further reading and study in the subject.

**TEXTBOOKS:**

1. Grimaldi, R.P and Ramana, B.V., "Discrete and Combinatorial Mathematics", Pearson Education, 5<sup>th</sup> Edition, New Delhi, 2007.
2. Koshy, T., -Elementary Number Theory with Applications , Elsevier Publications, New Delhi, 2002.

**REFERENCES :**

1. Lidl, R. and Pitz, G, "Applied Abstract Algebra", Springer Verlag, New Delhi, 2<sup>nd</sup> Edition, 2006.
2. Niven, I., Zuckerman.H.S., and Montgomery, H.L., -An Introduction to Theory of Numbers John Wiley and Sons , Singapore, 2004.
3. San Ling and Chaoping Xing, -Coding Theory – A first Course , Cambridge Publications, Cambridge, 2004.

**Subject Code:** MA8551  
**Subject Name:** ALGEBRA AND NUMBER THEORY

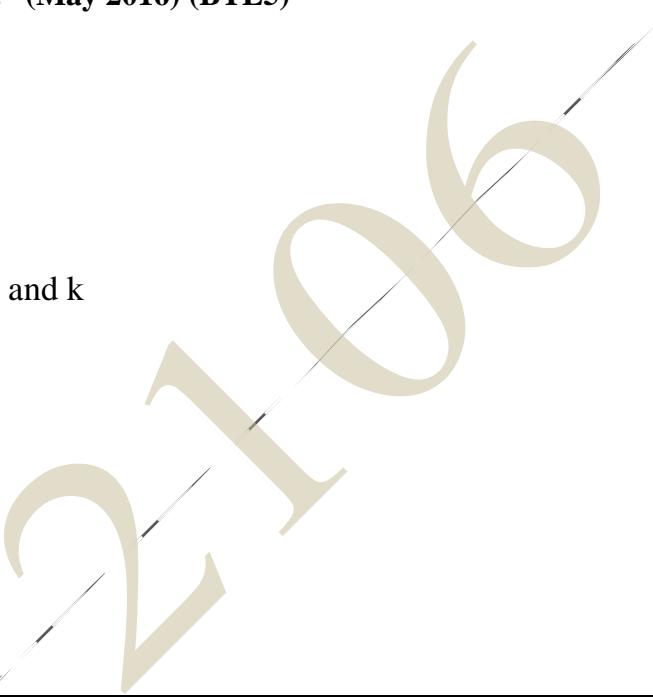
**Year/Semester:** III /V  
**Subject Handler:** Dr.S.Suresh

<b>UNIT I – GROUPS AND RINGS</b>	
Groups : Definition - Properties - Homomorphism - Isomorphism - Cyclic groups - Cosets - Lagrange's theorem. Rings: Definition - Sub rings - Integral domain - Field - Integer modulo n - Ring homomorphism.	
	<b>PART A</b>
<b>Q.No.</b>	<b>Questions</b>
1.	<p><b>Define Group. (BTL1)</b>  A non-empty set <math>G</math> with a binary operation <math>*</math> defined on it is called a group if it satisfies the following:</p> <ul style="list-style-type: none"> <li>(1) <b>Closure:</b> Let <math>a, b \in G</math> then <math>a * b \in G, \forall a, b \in G</math></li> <li>(2) <b>Associative:</b> Let <math>a, b, c \in G</math> then <math>a * (b * c) = (a * b) * c \in G</math></li> <li>(3) <b>Identity:</b> There exists an element <math>e \in G</math> such that <math>a * e = e * a = a, \forall a \in G</math> where ‘e’ is the identity element.</li> <li>(4) <b>Inverse:</b> For each <math>a \in G</math> there exists an element <math>a^{-1}</math> such that <math>a * a^{-1} = a^{-1} * a = e</math>, where <math>a^{-1}</math> is the identity element.</li> </ul>
2	<p><b>Define abelian group. (BTL1)</b>  If a group <math>(G, *)</math> satisfies <math>a * b = b * a \quad \forall a, b \in G</math>, then <math>G</math> is abelian group</p>
3	<p><b>Define semigroup with an example (Nov 2014, Nov 2016, Apr 2018) (BTL1)</b>  A non-empty set <math>S</math> together with a binary operation <math>*</math> satisfying</p> <ul style="list-style-type: none"> <li>(1) <b>Closure:</b> Let <math>a, b \in G</math> then <math>a * b \in G, \forall a, b \in G</math></li> <li>(2) <b>Associative:</b> Let <math>a, b, c \in G</math> then <math>a * (b * c) = (a * b) * c \in G</math></li> </ul> <p>then the set with binary operation is called a semi group.</p> <p><b>Example :</b> ‘N’ the set of all natural numbers is a group under addition.</p>
4	<p><b>Define monoid with an example (Nov 2014) (BTL1)</b>  A non-empty set ‘M’ with a binary operation <math>*</math> satisfying</p> <ul style="list-style-type: none"> <li>(1) <b>Closure:</b> Let <math>a, b \in G</math> then <math>a * b \in G, \forall a, b \in G</math></li> </ul>

	<p>(2) <b>Associative:</b> Let <math>a, b, c \in G</math> then <math>a * (b * c) = (a * b) * c \in G</math></p> <p>(3) <b>Identity:</b> There exists an element <math>e \in G</math> such that <math>a * e = e * a = a, \forall a \in G</math> where 'e' is the identity element.</p> <p>Then the set with binary operation is called a monoid.</p> <p><b>Example:</b> 'Z' set of all integers is a monoid under multiplication.</p>
5	<p><b>Let Z be the group of integers with the binary operation * defined by <math>a * b = a + b - 2, \forall a, b \in Z</math>. Find the identity element of the group <math>\langle Z, * \rangle</math>.</b> (Apr 2017) (BTL3)</p> <p>Let <math>e</math> be the identity element</p> <p>Then <math>a * e = e * a = a</math></p> <p>Now, <math>a * e = a</math></p> <p><math>a + e - 2 = a</math></p> <p><math>e - 2 = 0</math></p> <p><math>e = 2</math></p> <p>2 is the identity element.</p>
6	<p><b>Prove that identity element of a group is unique.</b> (Nov 2015) (BTL5)</p> <p><b>Given:</b> <math>(G, *)</math> is a group</p> <p><b>To Prove:</b> identity element is unique</p> <p>Let <math>e_1</math> and <math>e_2</math> be two identity elements of <math>G</math>.</p> <p>Suppose <math>e_1</math> is the identity element</p> <p><math>e_1 * e_2 = e_2 * e_1 = e_2</math> ----- (1)</p> <p>Suppose <math>e_2</math> is the identity element</p> <p><math>e_2 * e_1 = e_1 * e_2 = e_1</math> ----- (2)</p> <p>From (1) and (2) <math>e_1 = e_2</math></p> <p>Therefore identity element is unique</p>
7	<p><b>Prove that inverse element of a group is unique.</b> (BTL5)</p> <p><b>Given:</b> <math>(G, *)</math> is a group</p> <p><b>To Prove:</b> identity element is unique</p> <p>Let <math>a \in G</math> and <math>e</math> is the identity element</p>

	<p>Let <math>a_1^{-1}</math> and <math>a_2^{-1}</math> be two inverse elements</p> $a_1^{-1} * a = a * a_1^{-1} = e \quad \dots\dots\dots(1)$ $a_2^{-1} * a = a * a_2^{-1} = e \quad \dots\dots\dots(2)$ <p><b>To Prove:</b> <math>a_1^{-1} = a_2^{-1}</math></p> $\begin{aligned} L.H.S &= a_1^{-1} = a_1^{-1} * e \\ &= a_1^{-1} * (a * a_2^{-1}) \quad (\text{by (2)}) \\ &= (a_1^{-1} * a) * a_2^{-1} \quad (\text{by associative}) \\ &= e * a_2^{-1} \quad (\text{by (1)}) \\ &= a_2^{-1} \end{aligned}$ <p>Therefore inverse element is unique.</p>
8	<p><b>For any group G, if <math>a^2 = e, \forall a \in G</math> then G is abelian. (BTL2)</b></p> <p><b>Given:</b> <math>a^2 = e, \forall a \in G</math></p> <p><b>To Prove:</b> G is abelian</p> $\begin{aligned} a^{-1} * a^2 &= a^{-1} * e \\ (a^{-1} * a) * a &= a^{-1} * e \\ e * a &= a^{-1} \\ a &= a^{-1}, \forall a \in G \\ (\text{i.e.}) \text{ Every element has its own inverse} \\ \text{Therefore } G \text{ is abelian} \end{aligned}$
9	<p><b>Prove that in a group idempotent law is true for the identity element. (Apr 2018) (BTL5)</b></p> <p><b>Given:</b> <math>(G, *)</math> is a group</p> <p>Assume that <math>a \in G</math> is an idempotent element</p> <p>Then, <math>a * a = a</math></p> $\begin{aligned} a &= a * e \\ &= a * (a * a^{-1}) \\ \text{Now, } &= (a * a) * a^{-1} \\ &= a * a^{-1} \\ &= e \end{aligned}$

	<p>Therefore <math>a=e</math> Therefore the only idempotent element in a group is its identity element.</p>
10	<p><b>State Lagrange's theorem (May 2008, Nov 2015) (BTL1)</b> The order of a group H of a finite group G divides the order of the group. (i.e) <math>O(H)</math> divides <math>O(G)</math></p>
11	<p><b>Find the left cosets of <math>\{[0],[3]\}</math> in the group <math>(Z_6, +_6)</math> (May 2016, May 2017) ( BTL3)</b></p> <p>Let <math>Z_6 = \{[0], [1], [2], [3], [4], [5]\}</math> be a group  <math>H = \{[0], [3]\}</math> be subgroup  The left cosets are,</p> <p><math>[0] + H = \{0+h / h \in H\} = \{[0]+[0], [0]+[3]\} = \{[0], [3]\} = H</math></p> <p><math>[1] + H = \{1+h / h \in H\} = \{[1]+[0], [1]+[3]\} = \{[1], [4]\}</math></p> <p><math>[2] + H = \{2+h / h \in H\} = \{[2]+[0], [2]+[3]\} = \{[2], [5]\}</math></p> <p><math>[3] + H = \{3+h / h \in H\} = \{[3]+[0], [3]+[3]\} = \{[3], [0]\} \neq H</math></p> <p><math>[4] + H = \{4+h / h \in H\} = \{[4]+[0], [4]+[3]\} = \{[4], [1]\}</math></p> <p><math>[5] + H = \{5+h / h \in H\} = \{[5]+[0], [5]+[3]\} = \{[5], [2]\}</math></p> <p>Therefore, <math>H = [0] + H = [3] + H, [1] + H = [4] + H, [2] + H = [5] + H</math> are the distinct left cosets of <math>H</math> in <math>(Z_6, +_6)</math></p>
12	<p><b>Find the idempotent elements of <math>G = \{1, i, -1, -i\}</math> under the multiplication operation. (BTL3)</b></p> <p>We know that the identity element is the only idempotent element of a group.  Here 1 is the identity element.  Therefore 1 is the only idempotent element.</p>
13	<p><b>Define Normal subgroup . (BTL1)</b></p> <p>A group <math>(H, *)</math> of <math>(G, *)</math> is called normal subgroup of <math>G</math> if <math>aH = Ha</math>, <math>a \in G</math></p>
14	<p><b>Prove or disprove “Every subgroup of an abelian group is normal”. (BTL5)</b>  <b>(Nov 13)</b></p> <p><b>Given:</b> <math>(G, *)</math> is abelian. <math>H</math> is a subgroup of <math>G</math>  <b>To Prove:</b> <math>H</math> is normal</p> <p>Let <math>(G, *)</math> be an abelian group and <math>(H, *)</math> be a subgroup of <math>G</math>.  Let <math>a \in G</math> be any element, then</p>

	<p><math>aH = \{a * h / h \in H\}</math>  <math>= \{h * a / h \in H\} \quad (\text{since } G \text{ is abelian})</math>          Ha, for all <math>a \in G</math>          Therefore <math>H</math> is a normal subgroup of <math>G</math></p>
15	<p><b>Prove that every cyclic group is abelian. (May 2016) (BTL5)</b></p> <p><b>Given:</b> <math>G</math> is cyclic group  <b>To Prove:</b> <math>G</math> is abelian</p> <p>Let <math>G = \{a^n / n \in \mathbb{Z}\}</math></p> <p>Let <math>x, y \in G</math> be any two elements</p> <p>Then <math>x = a^m</math>, <math>y = a^k</math> for some integers <math>m</math> and <math>k</math></p> $\begin{aligned} x * y &= a^m * a^k = a^{m+k} \\ &= a^{k+m} \\ &= a^k * a^m \\ &= y * x \end{aligned}$ <p>Therefore <math>x * y = y * x</math>, for all <math>x, y \in G</math></p> <p>Therefore <math>G</math> is abelian.</p> 
16	<p><b>Define Group homomorphism with an example. (Nov 2014) (BTL1)</b></p> <p>Let <math>(G, *)</math> and <math>(G', \bullet)</math> be two groups. A mapping <math>f : G \rightarrow G'</math> is called a group homomorphism if for all <math>a, b \in G</math>, <math>f(a * b) = f(a) \bullet f(b)</math>.</p> <p><b>Example:</b> Consider the group <math>(R, +)</math> and <math>(R^*, \bullet)</math> where <math>R^* = R - \{0\}</math>. Let <math>f : R \rightarrow R^*</math> be defined by <math>f(a) = 2^a \forall a \in R</math>. Then <math>f</math> is a homomorphism.</p>
17	<p><b>Define Kernel of a homomorphism in a group. (Nov 2017) (BTL1)</b></p> <p>Let <math>(G, *)</math> and <math>(G', \bullet)</math> be groups with <math>e'</math> as the identity element of <math>G'</math>. Let <math>f : G \rightarrow G'</math> be a homomorphism. The <math>\ker f = \{a \in G / f(a) = e'\}</math></p>
18	<p><b>Define Rings. (BTL1)</b></p> <p>A non-empty set <math>R</math> with two binary operations denoted by ‘+’ and ‘.’ is called a ring if</p> <ol style="list-style-type: none"> <li>(1) <math>(R, +)</math> is an abelian group with 0 as identity</li> <li>(2) <math>(R, .)</math> is a semigroup</li> </ol>

	(3) The operation ‘.’ is distributive over ‘+’  (i.e.) $a.(b+c) = a.b + a.c$  and $(b+c).a = b.a + c.a$ , for all $a,b,c \in R$
19	<b>Define a field in an algebraic system. (Apr 2015) (BTL1)</b>  A commutative ring $(R, +, .)$ with identity in which every non-zero element has a multiplicative inverse is called a field.
20	<b>Give an example of a ring which is not a field. (Nov 2013) (BTL3)</b>  $(Z, +, .)$ is a ring but not a field because integers does not contain its multiplicative inverse.
21	<b>If <math>(R, +, .)</math> is a ring then prove that <math>a.0=0</math>, <math>\forall a \in R</math> and 0 is the identity element in R under addition. (Nov 2017) (BTL2)</b>  <b>Given:</b> $(R, +, .)$ is a ring  <b>To Prove:</b> $a.0=0, \forall a \in R$  $\begin{aligned} a.0 &= a.(0+0) \\ &= a.0+a.0 \\ \text{If } a \in R \text{ then } &\Rightarrow a.0+0 = a.0+a.0 \\ &\Rightarrow 0 = a.0 \end{aligned}$ <p>Similarly <math>0.a = (0+0).a = 0.a + 0.a</math></p> $0.a = 0$
22	<b>Prove that if G is abelian, then <math>\forall a,b \in G, (a * b)^2 = a^2 * b^2</math>. (May 2011, Nov 2010, May 2013) (BTL5)</b>  <b>Given:</b> G is abelian  <b>To Prove:</b> $(a * b)^2 = a^2 * b^2$  $\begin{aligned} \text{L.H.S} &= (a * b)^2 = (a * b) * (a * b) \\ &= a * ((b * a) * b) \quad (\text{since associativity}) \\ &= a * ((a * b) * b) \quad (\text{since abelian}) \\ &= a * (a * (b * b)) \quad (\text{since associativity}) \\ &= (a * a) * (b * b) \\ &= a^2 * b^2 \end{aligned}$
23	<b>Give an example of semi group but not a monoid. (BTL3)</b>

	The set of all positive integers over addition form a semi group but it is not a monoid because identity axiom is not satisfied.
24	<p><b>If 'a' is a generator of a cyclic group G, then show that 'a<sup>-1</sup>' is also a generator of G. (BTL4)</b></p> <p><b>Given:</b> 'a' is a generator of G</p> <p><b>To prove:</b> a<sup>-1</sup> is also a generator</p> <p>Let <math>G = \langle a \rangle</math> be a cyclic group generated by 'a'</p> <p>If <math>x \in G</math>, then <math>x = a^n</math> for some <math>n \in \mathbb{Z}</math></p> <p><math>\therefore x = a^n = (a^{-1})^{-n}, (-n \in \mathbb{Z})</math></p> <p><math>\therefore a^{-1}</math> is also a generator of G.</p>
25	<p><b>Give an example to show that union of two subgroups need not be a subgroup. (BTL3)</b></p> <p>We know that <math>(\mathbb{Z}, +)</math> is a group</p> <p>Let <math>H_1 = 2\mathbb{Z}</math> and <math>H_2 = 3\mathbb{Z}</math></p> <p><math>\therefore (H_1, +)</math> and <math>(H_2, +)</math> are subgroups of <math>\mathbb{Z}</math></p> <p>Now <math>2 \in H_1</math> and <math>3 \in H_2</math>, <math>\therefore 2, 3 \in H_1 \cup H_2</math></p> <p>But <math>2, 3 \in H_1 \cup H_2</math></p> <p><math>\because 5 \notin H_1</math> and <math>5 \notin H_2</math></p> <p>So <math>H_1 \cup H_2</math> is not a subgroup of <math>\mathbb{Z}</math></p>
1	<p><b>Part-B</b></p> <p><b>Show that <math>M_2</math>, the set of all <math>2 \times 2</math> non-singular matrices over <math>\mathbb{R}</math> is a group under usual matrix multiplication. Is it abelian? (Apr 2015) (BTL5) (8 Marks)</b></p> <p>(Refer SKD pg.4.38)</p> <p><b>Keypoints:</b></p> <ul style="list-style-type: none"> <li>• Assume a <math>2 \times 2</math> matrix (1mark)</li> <li>• closure <math> AB  =  A  B </math> (1mark)</li> <li>• Associative <math>A(BC) = (AB)C</math> (2mark)</li> <li>• Identity <math>\begin{pmatrix} 1 &amp; 0 \\ 0 &amp; 1 \end{pmatrix}</math> (2mark)</li> <li>• Inverse <math>A^{-1} = \frac{1}{ A } adj A</math> (1mark)</li> </ul>

	<ul style="list-style-type: none"> <li>Commutative is not satisfied. (1mark)</li> </ul>
	<p>Show that <math>(Q^+, *)</math> is an abelian group where <math>*</math> is defined by <math>a * b = \frac{ab}{2}, \forall a, b \in Q^+</math>. (Nov 2016, Apr 2018) (BTL5) (8 Marks)</p> <p>(Refer SKD Pg.4.17)</p> <p>Keypoints:</p> <p>2</p> <ul style="list-style-type: none"> <li>Closure <math>a * b \in G</math> (1mark)</li> <li>Associative <math>a * (b * c) = (a * b) * c</math> (2marks)</li> <li>Identity <math>e=2</math> (2marks)</li> <li>Inverse <math>\frac{4}{a}</math> (2marks)</li> <li>Commutative <math>a * b = b * a</math> (1mark)</li> </ul>
	<p>Prove that <math>\left\{ \begin{bmatrix} 1 &amp; 0 \\ 0 &amp; 1 \end{bmatrix}, \begin{bmatrix} -1 &amp; 0 \\ 0 &amp; 1 \end{bmatrix}, \begin{bmatrix} 1 &amp; 0 \\ 0 &amp; -1 \end{bmatrix}, \begin{bmatrix} -1 &amp; 0 \\ 0 &amp; -1 \end{bmatrix} \right\}</math> forms an abelian group under matrix multiplication. (Nov 2015) (BTL5) (8 Marks)</p> <p>(Refer SKD Pg. 4.15)</p> <p>Keypoints:</p> <p>3</p> <ul style="list-style-type: none"> <li>Closure : all the elements of G are closed under multiplication (1 mark)</li> <li>Associative : Matrix multiplication is always associative (2marks)</li> <li>Identity: I is the identity element (1mark)</li> <li>Inverse : Inverse of I is I, Inverse of A is A, Inverse of B is B, inverse of C is C (2marks)</li> <li>Prove commutative.(2marks)</li> </ul>
	<p>Prove that every cyclic group is an abelian group. (Nov 2013) (BTL5) (8 Marks)</p> <p>( Refer Balaji Pg. 4.54)</p> <p>Keypoints:</p> <p>4</p> <ul style="list-style-type: none"> <li>Consider a cyclic group generated by a. (2marks)</li> <li>Take <math>x = a^n</math> <math>y = a^m</math> (2marks)</li> <li>prove its abelian : <math>x * y = y * x</math> (4marks)</li> </ul>
5	<p>Prove that intersection of any two subgroups of a group <math>(G, *)</math> is again a subgroup of <math>(G, *)</math>. (May 2013, Nov 2013, Nov 2015) (BTL5) (8 Marks)</p>

	(Refer Balaji Pg. 4.56)  Keypoints: <ul style="list-style-type: none"><li>• Consider two subgroups <math>H_1</math> and <math>H_2</math> with same elements in both the groups. (2marks)</li><li>• <math>a * b^{-1} \in H, a * b^{-1} \in k</math> (2marks)</li><li>• <math>a * b^{-1} \in H \cap K</math> (4marks)</li></ul>
6	<b>Show that union of two subgroups of a group G is a subgroup of G iff one is contained in the other.</b> <b>(Apr 2015, Nov 2014) (BTL5) (8 Marks)</b>  (Refer Balaji 4.56)  Keypoints: <ul style="list-style-type: none"><li>• Consider union of two subgroups (2marks)</li><li>• Prove by contrary (3marks)</li><li>• Prove the converse by considering <math>H_1 \subseteq H_2</math> or <math>H_2 \subseteq H_1</math> (3marks)</li></ul>
7	<b>State and Prove Lagrange's theorem for groups. Is the converse true? (May 2015, May 2016, Nov 2016, May 2018, May 2017) (BTL5) (16 Marks)</b>  (Refer Balaji 4.68)  Keypoints: <ul style="list-style-type: none"><li>• Prove the theorem " Let <math>(H, *)</math> be a subgroup of <math>(G, *)</math>. Then the set of all left cosets of <math>H</math> in <math>G</math> form a partition of <math>G</math>. That is every element of <math>G</math> belongs to only one left coset of <math>H</math> in <math>G</math>". (4marks)</li><li>• Prove the theorem " There is a 1-1 correspondence between any two left coset of <math>H</math> in <math>G</math>".(4marks)</li><li>• Using the above two theorems prove order of <math>H</math> divides order of <math>G</math> (4marks)</li><li>• Check if the converse is true. (4marks)</li></ul>
8	<b>If <math>S = NxN</math>, the set of ordered pairs of positive integers with the operation <math>*</math> defined by <math>(a,b)*(c,d)=(ad+bc,bd)</math> and if <math>f:(S,*) \rightarrow (Q,+)</math> is defined by <math>f(a,b)=\frac{a}{b}</math>, show that f is a semigroup homomorphism. (May 2008, Nov 2014) (BTL5) (8 Marks)</b>  (Refer SKD Pg.4.109)  Keypoints: <ul style="list-style-type: none"><li>• Check closure : <math>a * b \in G</math> (3marks)</li><li>• Associative <math>a * (b * c) = (a * b) * c</math> (3marks)</li></ul>

	<ul style="list-style-type: none"> <li>• Check <math>f(x*y) = f(x) + f(y)</math> (2marks)</li> </ul>
9	<p><b>Show that a semigroup with more than one idempotent element cannot be a group. Give an example of a semigroup which is not a group. (Nov 2014) (BTL5) (8 Marks)</b></p> <p>(Refer Balaji 4.17)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>• Consider two idempotent elements <math>a*a=a</math>, <math>b*b=b</math> (2marks)</li> <li>• Prove by contradiction (4marks)</li> <li>• Give an example (2marks)</li> </ul>
10	<p><b>Prove that every subgroup of a cyclic group is cyclic. (May 2016, May 2017) (BTL5) (8 Marks)</b></p> <p>(Refer SKD Pg.4.56)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>• Consider a cyclic group generated by a. (2marks)</li> <li>• Consider a subgroup H of G (2marks)</li> <li>• Prove that H is a cyclic group generated by <math>a^m</math>, <math>x=(a^m)^d</math> (4marks)</li> </ul>
11	<p><b>In any group <math>\langle G, *\rangle</math> show that <math>(a * b)^{-1} = b^{-1} * a^{-1}</math>, <math>\forall a, b \in G</math>. (May 2016) (BTL5) (8 Marks)</b></p> <p>(Refer Balaji Pg. 4.35)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>• Consider two elements in the group G (2marks)</li> <li>• Its inverse also exists in G (2marks)</li> <li>• <math>(a * b)^*(b^{-1} * a^{-1}) = (b^{-1} * a^{-1})^*(a * b) = e</math> (4marks)</li> </ul>
12	<p><b>Prove that kernel of a group homomorphism is a normal subgroup of the group. (May 2017, May 2016, May 2018) (BTL5) (8 Marks)</b></p> <p>(Refer Balaji Pg.4.69)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>• Consider a kernel of the homomorphism (1mark)</li> <li>• Consider two elements in kerf (2marks)</li> <li>• Prove that kerf is a subgroup of G (i.e.,) <math>x * y^{-1} \in Kerf</math> (3marks)</li> <li>• Prove that kerf is normal (i.e.,) <math>f * x * f^{-1} \in Kerf</math> (2marks)</li> </ul>

	<b>Prove that intersection of two normal subgroups of a group G is again a normal subgroup of G.</b> <b>(Nov 2016, Apr 2018) (BTL5) (8 Marks)</b> (Refer Balaji Pg. 4.71)
13	<p>Keypoints:</p> <ul style="list-style-type: none"> <li>• Consider two normal subgroups <math>N_1</math> and <math>N_2</math> (2marks)</li> <li>• <math>ab^{-1} \in N_1 \cap N_2</math></li> <li>• Prove that <math>ana^{-1} \in N_1 \cap N_2</math> (6marks)</li> </ul>
14	<p><b>State and prove Cayley's theorem. (May 2013) (BTL5) (8 Marks)</b> (Refer Balaji Pg. 4.59)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>• “ Every finite group of order n is isomorphic to a permutation group of order n” (2marks)</li> <li>• Define a mapping <math>f : G \rightarrow G</math> (1mark)</li> <li>• Find 1-1 <math>f_a(x)=f_a(y) \Rightarrow x=y</math> (1 mark)</li> <li>• onto if <math>y \in G</math>, <math>y = f_a(a^{-1} * y)</math> (1mark)</li> <li>• Consider a set <math>G'</math>, prove that it's a group (2marks)</li> <li>• Prove <math>G</math> is isomorphic to <math>G'</math>. (1mark)</li> </ul>
15	<p><b>Let <math>f : (G, *) \rightarrow (G', \bullet)</math> be a group homomorphism then prove that</b></p> <p>(1) <math>[f(a)]^{-1} = f(a^{-1})</math>, <math>\forall a \in G</math></p> <p>(2) <b><math>f(e)</math> is an identity of <math>G'</math>, when <math>e</math> is an identity element of <math>G</math>.</b> (Nov 2015) (BTL1) (8 Marks) (Refer SKD Pg. 4.80)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>• (i) <math>f(a).f(e)=f(a).e'</math> (4marks)</li> <li>• (ii) <math>f(a^{-1} * a) = f(e) \Rightarrow f(a^{-1}).f(a) = e'</math> (4marks)</li> </ul>
16	<p><b>State and prove fundamental theorem on group homomorphism of groups. (May 2011, Nov 2013) (8 Marks)</b> (Refer Balaji Pg. 4.70)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>• “Let <math>(G, *)</math> and <math>(G', \bullet)</math> be two groups. Let <math>f : G \rightarrow G'</math> be a homomorphism of groups with kernel K. Then <math>G/K</math> is isomorphic to <math>f(G) \subseteq G'</math> (2marks)</li> </ul>

	<ul style="list-style-type: none"> <li>• Consider a mapping (1mark)</li> <li>• Prove that it is well defined : If <math>ak=bk</math> then <math>f(a)=f(b)</math> (1mark)</li> <li>• 1-1 and onto (2marks)</li> <li>• Prove that it is a homomorphism : <math>\phi(ak \oplus bk) = \phi(ak) \bullet \phi(bk)</math> (2marks)</li> </ul>
17	<p><b>Prove that <math>Z_4 = \{0,1,2,3\}</math> is a commutative ring with respect to the binary operation <math>+_4</math> and <math>\times_4</math>. (Nov 2015). (BTL5) (8 Marks)</b></p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>• Check if <math>Z_4</math> is an abelian group over <math>+</math> (2marks)</li> <li>• Check if <math>Z_4</math> is a semigroup over <math>\times</math> (2marks)</li> <li>• Prove that <math>\times</math> is distributive over <math>+</math> (2marks)</li> <li>• Check if <math>Z_4</math> is commutative (2marks)</li> </ul>
<b>UNIT II – FINITE FIELDS AND POLYNOMIALS</b>	
	Rings - Polynomial rings - Irreducible polynomials over finite fields - Factorization of polynomials over finite fields
<b>Q.No.</b>	<b>PART-A</b>
1.	<p><b>Define rings . (BTL1)</b></p> <p>A nonempty set <math>R</math> is a ring if it has two closed binary operations, addition and multiplication, satisfying the following conditions.</p> <ol style="list-style-type: none"> <li>1. <math>a + b = b + a</math> for <math>a, b \in R</math>.</li> <li>2. <math>(a + b) + c = a + (b + c)</math> for <math>a, b, c \in R</math>.</li> <li>3. There is an element <math>0</math> in <math>R</math> such that <math>a + 0 = a</math> for all <math>a \in R</math>.</li> <li>4. For every element <math>a \in R</math>, there exists an element <math>-a</math> in <math>R</math> such that <math>a + (-a) = 0</math>.</li> <li>5. <math>(ab)c = a(bc)</math> for <math>a, b, c \in R</math>.</li> <li>6. For <math>a, b, c \in R</math></li> </ol>
2	<p><b>Define a ring with unity or identity. (Nov 2014, Nov 2015, Nov 2016) (BTL1)</b></p> <p>If there is an element <math>1 \in R</math> such that <math>1 \neq 0</math> and <math>1a = a1 = a</math> for each element <math>a \in R</math>, we say that <math>R</math> is a ring with unity or identity.</p>

3	<p><b>Define commutative ring, integral domain and division ring. (BTL1)</b></p> <ul style="list-style-type: none"> <li>• A ring R for which <math>ab = ba</math> for all <math>a, b</math> in R is called commutative ring.</li> <li>• A commutative ring R with identity is called an integral domain</li> <li>• A division ring is a ring R, with an identity, in which every nonzero element in R is a unit; that is, for each <math>a \in R</math> with <math>a \neq 0</math>, there exists a unique element <math>a^{-1}</math> such that <math>a^{-1}a = aa^{-1} = 1</math>.</li> </ul>
4	<p><b>Define field. (BTL1)</b></p> <p><b>A commutative division ring is called a field</b></p>
5	<p><b>Define zero divisor. (BTL1)</b></p> <p>A nonzero element a in a ring R is called a zero divisor if there is a nonzero element b in R such that <math>ab = 0</math>.</p> <p>Example: <math>5 \bullet 7 \equiv 11 \pmod{12}</math>, <math>3 \bullet 4 \equiv 0 \pmod{12}</math></p>
6	<p><b>Define polynomial rings. (BTL1)</b></p> <p>Assume that R is a commutative ring with identity. Any expression of the form <math>f(x) = \sum_{i=0}^n a_i x^i = a_0 + a_1 x + a_2 x^2 + \dots + a_n x^n</math>, where <math>a_i \in R</math> and <math>a_n \neq 0</math>, is called a polynomial over R with indeterminate x.</p>
7	<p><b>Find the polynomial</b> <math>p(x) = 3 + 3x^3</math> and <math>q(x) = 4 + 4x^2 + 4x^3</math></p> <p>The sum of <math>p(x)</math> and <math>q(x)</math> is <math>7 + 4x^2 + 3x^3 + 4x^4</math>. The product of the two polynomials is the zero polynomial. This example tells us that <math>R[x]</math> cannot be an integral domain if R is not an integral domain.</p>
8	<p><b>Define the Kernel of the evaluation homomorphism (BTL1)</b></p> <p>Let <math>p(x)</math> be a polynomial in <math>F[x]</math> and <math>\alpha \in F</math>. We say that <math>\alpha</math> is a zero or root of <math>p(x)</math> if <math>p(\alpha) = 0</math>. The set of all such <math>\alpha</math> is the kernel of the evaluation homomorphism.</p>
9	<p><b>Define irreducible polynomials (BTL1)</b></p> <p>A nonconstant polynomial <math>f(x) \in F[x]</math> is irreducible over a field F if <math>f(x)</math> cannot be expressed as a product of two polynomials <math>g(x)</math> and <math>h(x)</math> in <math>F[x]</math>, where the degrees of <math>g(x)</math> and <math>h(x)</math> are both smaller than the degree of <math>f(x)</math>. Irreducible polynomials function as the "prime numbers" of polynomial rings.</p>
10	<p><b>Write the example for irreducible polynomial(BTL4)</b></p>

	The polynomial $x^2 - 2 \in Q(x)$ is irreducible since it cannot be factored any further over the rational numbers. Similarly, $x^2 + 1$ is irreducible over the real numbers
11	<b>Define a relatively prime (BTL4)</b> A If $f(x), g(x) \in F(x)$ and their GCD is 1, then $f(x)$ and $g(x)$ are called relatively prime.
12	<b>Define Boolean algebra. (Nov 2007, May 2010) (BTL1)</b> A boolean algebra is a complemented distributive lattice. A non-empty set $B$ together with two binary operations ' $+$ ', ' $\cdot$ ' on $B$ , a unary operation on $B$ ' called complementation and two distinct elements 0 and 1 is called a Boolean algebra if the following axioms are satisfied for all $a, b, c \in B$ . <b>Commutative Law:</b> $a+b = b+a$ and $a.b=b.a$ <b>Associative Law:</b> $a + (b + c) = (a + b) + c$ and $a . (b . c) = (a . b) . c$ <b>Distributive Law:</b> $a + (b . c) = (a + b) . (a + c)$ and $a . (b + c) = (a . b) + (a . c)$ <b>Identity Law:</b> There exists $0, 1 \in B$ such that $a + 0 = a$ and $a . 1 = a$ <b>Complement Law:</b> For each $a \in B$ there exists an element $a' \in B$ such that $a+a'=1$ and $a.a'=0$ The Boolean algebra is usually denoted as 6-tuple $(B, +, ., ', 0, 1)$ .
13	<b>State the De Morgan's law in a Boolean algebra. (Nov 2016)</b> (i) $(a+b)' = a'.b'$ (ii) $(a.b)' = a'+b'$ , $\forall a, b \in B$
14	<b>Show that Absorbtion laws are valid in a Boolean algebra. (May 2016, May 2017) (BTL5)</b> <b>The absorbtion laws are</b> (i) $a . (a + b) = a$ (ii) $a + a . b = a$ $\forall a, b \in B$ (i) L.H.S = $a . (a + b) = (a + 0) . (a + b)$ (by identity law) $= a + (0 . b)$ (by distributive law) $= a + (b . 0)$ (by commutative law) $= a + 0$ (by boundedness law) $= a$ (by identity law) $= R.H.S$ (ii) L.H.S = $a + (a . b) = (a . 1) + (a . b)$ (by identity law)

	$  \begin{aligned}  &= a \cdot (1 + b) && \text{(by distributive law)} \\  &= a \cdot (b + 1) && \text{(by commutative law)} \\  &= a \cdot 1 && \text{(by bounded law)} \\  &= a && \text{(by identity law)} \\  &= \text{R.H.S}  \end{aligned}  $
15	<p><b>Define Freshman's Dreams. (BTL5)</b></p> <p>Let <math>p</math> be prime and <math>D</math> be an integral domain of characteristic <math>p</math>. Then <math>a^{p^n} + b^{p^n} = (a + b)^{p^n}</math> for all positive integers <math>n</math>.</p>
	<p><b>PART-B</b></p>
1	<p>For an example of a noncommutative division ring, let</p> $1 = \begin{pmatrix} 1 & 0 \\ 0 & 1 \end{pmatrix}, i = \begin{pmatrix} 0 & 1 \\ -1 & 0 \end{pmatrix}, j = \begin{pmatrix} 0 & i \\ i & 0 \end{pmatrix}, k = \begin{pmatrix} i & 0 \\ 0 & -i \end{pmatrix}$ <p>where <math>i^2 = -1</math>. These elements satisfy the following relations <math>i^2 = j^2 = k^2 = -1</math>, <math>ij = k</math>, <math>jk = i</math>, <math>ki = j</math>, and <math>ji = -k</math>, <math>kj = -i</math>, <math>ik = -j</math> (BTL5) (8 Marks)</p> <p>(Refer T W.Judson Pg. 255)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>• <math>H</math> can be considered to be the set of all <math>2 \times 2</math> matrices (2marks)</li> <li>• Define addition and multiplication on <math>H</math> either by the usual matrix operations or in terms of the generators <math>1</math>, <math>i</math>, <math>j</math>, and <math>k</math> (3marks)</li> <li>• To show that the quaternions are a division ring, we must be able to find an inverse for each nonzero element. (2 marks)</li> </ul>
2	<p>If <math>f(x) = 3x^5 - 8x^4 + x^3 - x^2 + 4x - 7</math>, <math>g(x) = x + 9</math> and <math>f(x), g(x) \in \mathbb{Z}[x]</math>, find the remainder when <math>f(x)</math> is divided by <math>g(x)</math>. (BTL2)</p> <p>(Refer T W.Judson 247)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>• Product of <math>f(x)</math> and <math>g(x)</math>(4marks)</li> <li>• Find the normal division of <math>f(x)</math> and <math>g(x)</math> (4marks)</li> </ul>
3	<p>Find the remainder when <math>g(x) = 7x^3 - 2x^2 + 5x - 2</math> is divided by <math>(x) = x - 3</math>. (BTL2) (8 Marks)</p> <p>(Refer T W.Judson 280)</p> <p>Keypoints:</p>

	<ul style="list-style-type: none"> <li>Sum of <math>f(x)</math> and <math>g(x)</math>(2marks)</li> <li>Product of <math>f(x)</math> and <math>g(x)</math>(2marks)</li> <li>Find the normal division of <math>f(x)</math> and <math>g(x)</math> (4marks)</li> </ul>
4	<p>Find all roots of <math>f(x) = x^2 + 4x</math> if <math>f(x) \in Z_{12}</math> <b>(BTL2) (8 Marks)</b>  (Refer T W.Judson 255)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>Roots of <math>f(x)</math> (4marks)</li> <li>Find the <math>f(x) \in Z_{12}</math> (4marks)</li> </ul>
5	<p><b>Let <math>R</math> be a commutative ring with identity. Then <math>R[x]</math> is a commutative ring with identity. (BTL5) (8 Marks)</b>  (Refer T W.Judson 280)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>To show <math>R[x]</math> is an abelian group under binomial addition (2marks)</li> <li>The zero polynomial, <math>f(x)=0</math>, is the additive identity. (3marks)</li> <li>Commutativity and associativity (3marks)</li> </ul>
6	<p>Prove that <math>\deg((x)g(x)) = \deg f(x) + \deg g(x)</math>. <b>(BTL5) (8 Marks)</b>  (Refer T W.Judson 281)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>We have two nonzero polynomials <math>p(x)</math> and <math>q(x)</math> (2marks)</li> <li>The degree of zero polynomial, <math>f(x)=0</math>, is the additive identity. (3marks)</li> <li>Commutativity and associativity (3marks)</li> </ul>
7	<p><b>Let <math>F</math> be a field and suppose that <math>d(x)</math> is the greatest common divisor of two polynomials <math>p(x)</math> and <math>q(x)</math> in <math>F[x]</math>. Then there exist polynomials <math>r(x)</math> and <math>s(x)</math> such that <math>d(x) = r(x)p(x) + s(x)q(x)</math>:</b>  <b>Furthermore, the greatest common divisor of two polynomials is unique. (BTL5) (8 Marks)</b>  (Refer T W.Judson 281)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>Let <math>d(x)</math> be the monic polynomial of smallest degree in the set <math>S</math>.(2marks)</li> <li><math>d(x) = r(x)p(x) + s(x)q(x)</math> (3marks)</li> <li>To show that <math>d(x)</math> is a greatest common divisor of <math>p(x)</math> and <math>q(x)</math>, (3marks)</li> </ul>

8	<p>Let <math>p(x) \in Q(x)</math>. then <math>p(x) = \frac{r}{s}(a_0 + a_1x + \dots + a_nx^n)</math>. where <math>r, s, a_0, a_1, \dots, a_n</math> are integers, the <math>a_i</math>'s are relatively prime, and <math>r</math> and <math>s</math> are relatively prime. (8 Marks) (Refer T W.Judson 287)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>Let <math>d</math> be the greatest common divisor (2marks)</li> <li>Reducing <math>d = (c_0 - - - - c_n)</math> to its lowest terms, we can write <math>p(x) = \frac{r}{s}(a_0 + a_1 + \dots + a_nx^n)</math>. Where <math>\gcd(r, s) = 1</math>. (6marks)</li> </ul>
9	<p>Let <math>(L, \wedge, \vee, \leq)</math> be a distributive lattice and <math>a, b \in L</math> if <math>a \wedge b = a \wedge c</math> and <math>a \vee b = a \vee c</math> then show that <math>b=c</math>. (Apr 2018) (BTL5) (8 Marks) (Refer Balaji Pg. 5.23)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li><math>a \vee (b \wedge c) = c</math> (4marks)</li> <li><math>a \wedge (b \vee c) = b</math> (4marks)</li> </ul>
10	<p>Prove that the diamond lattice is distributive or not. (Nov 2015) (BTL5) (8 Marks) (Refer Balaji Pg. 5.24)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>Draw the diamond lattice (2marks)</li> <li>Consider case (i) as <math>(0, b, a)</math> get the answer as 0 (1mark)</li> <li>Consider case (ii) as <math>(0, 1, a)</math> get the answer as <math>a</math> (1mark)</li> <li>Consider case (iii) as <math>(0, a, 1)</math> get the answer as <math>a</math> (1mark)</li> <li>Consider case (iv) as <math>(a, 0, 1)</math> get the answer as <math>a</math> (1mark)</li> <li>Consider case (v) as <math>(a, b, 1)</math> get the answer as 1 (1mark)</li> <li>Conclude with the following cases (1mark)</li> </ul>
11	<p>Let <math>D_{30} = \{1, 2, 3, 5, 6, 10, 15, 30\}</math> with a relation <math>x \leq y</math> iff <math>x</math> divides <math>y</math>. Find</p> <ol style="list-style-type: none"> <li>All lower bounds of 10 and 15</li> <li>All G.L.B of 10 and 15</li> <li>All upper bounds of 10 and 15</li> <li>All L.U.B of 10 and 15</li> </ol>

	<p>(v) <b>Hasse diagram of <math>D_{30}</math> (Nov2015, Apr 2018) (BTL5) (8 Marks)</b></p> <p><b>Keypoints:</b></p> <ul style="list-style-type: none"> <li>• Draw the hasse diagram (4marks)</li> <li>• Find the GLB and LUB (4marks)</li> </ul>
12	<p><b>Show that in a lattice if <math>a \leq b \leq c</math> then</b></p> <p>(1) <math>a \oplus b = b * c</math> (or) <math>a \vee b = b \wedge c</math></p> <p>(2) <math>(a * b) \oplus (b * c) = b = (a \oplus b) * (a \oplus c)</math></p> <p>(or) <math>(a \wedge b) \vee (b \wedge c) = b = (a \vee b) \wedge (a \vee c)</math> . (Nov 2013) (BTL5) (8 Marks)</p> <p>(Refer Balaji Pg. 5.18)</p> <p><b>Keypoints:</b></p> <ul style="list-style-type: none"> <li>• Using <math>a \leq b \leq c</math> prove (1) (4marks)</li> <li>• Using necessary laws prove (2) , <math>(a * b) \oplus (b * c) = b = (a \oplus b) * (a \oplus c)</math> (4marks)</li> </ul>
13	<p><b>If <math>S_n</math> is the set of all divisors of the positive integers n and D is the relation of division, prove that <math>\{S_{30}, D\}</math> is a lattice. Find also all the sublattices of <math>\{S_{30}, D\}</math> that contains six or more elements. (Apr 2015) (BTL5) (8 Marks)</b></p> <p>(Refer Balaji Pg. 5.30)</p> <p><b>Keypoints:</b></p> <ul style="list-style-type: none"> <li>• Draw the Hasse diagram (3marks)</li> <li>• Find GLB and LUB (2marks)</li> <li>• Find all the sub lattices that contain 6 or more elements(3marks)</li> </ul>
14	<p><b>Show that the De Morgan's law holds in a Boolean algebra. (Nov 2014, May 2016) (BTL5) (8 Marks)</b></p> <p>(Refer Balaji Pg. 5.39)</p> <p><b>Keypoints:</b></p> <ul style="list-style-type: none"> <li>• <math>(a + b)' = a' \cdot b'</math> (2marks)</li> <li>• Prove: <math>(a + b) + (a' \cdot b') = 1</math> (2marks)  <math>(a + b) \cdot (a' \cdot b') = 0</math></li> <li>• <math>(a \cdot b)' = a' + b'</math> (2marks)</li> </ul>

	<ul style="list-style-type: none"> <li>• Prove: <math>(a.b) + (a' + b') = 1</math> (2marks)</li> <li><math>(a.b).(a' + b') = 0</math></li> </ul>
15	<p><b>In any Boolean algebra show that <math>(a+b')(b+c')(c+a')=(a'+b)(b'+c)(c'+a)</math>. (Nov 2013) (BTL5) (8 Marks)</b>          (Refer Balaji Pg. 5.50)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>• Consider LHS = <math>(a+b')(b+c')(c+a')</math> (4marks)</li> <li>• prove the RHS = <math>(a'+b)(b'+c)(c'+a)</math> (4marks)</li> </ul>
16	<p><b>If <math>P(S)</math> is the power set of a non-empty set S, prove that <math>\{P(S), \cup, \cap, /, \phi, S\}</math> is a Boolean algebra.</b>          (Nov 2015) (BTL2) (8 Marks)</p> <p>(Refer Balaji Pg. 5.41)</p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>• Consider elements from <math>P(A)</math> (2marks)</li> <li>• prove that the given set is a Boolean algebra (6marks)</li> </ul>
17	<p><b>If <math>a, b \in S = \{1, 2, 3, 6\}</math> and <math>a+b = \text{LCM}(a, b)</math>, <math>a*b = \text{GCD}(a, b)</math> and <math>a' = \frac{6}{a}</math>, show that <math>(B, +, ., ', 1, 6)</math> is a Boolean algebra. (BTL3) (8 Marks)</b></p> <p>Keypoints:</p> <ul style="list-style-type: none"> <li>• Prove Commutative, Associative, (3marks)</li> <li>• Distributive, Identity (3marks)</li> <li>• Complement. (2marks)</li> </ul>
	<b>UNIT-III</b>
	<p><b>DIVISIBILITY THEORY AND CANONICAL DECOMPOSITIONS</b></p> <p>Division algorithm – Base - b representations – Number patterns – Prime and composite numbers – GCD – Euclidean algorithm – Fundamental theorem of arithmetic – LCM.</p>
	<b>PART-A</b>
1.	<p><b>State Division Algorithm BTL1</b></p> <p>Let a be any integer and b a positive integer. Then there exist unique integers q and r such that <math>a=b.q + r</math> where <math>0 \leq r &lt; b</math></p>

2	<b>Find the quotient q and the remainder r when 207 is divided by 15</b> BTL3 $207 = 15 \cdot 13 + 12$ ; so $q = 13$ and $r = 12$ .
3	<b>Find the quotient q and the remainder r when -23 is divided by 5.</b> Since $-23 = 5 \cdot (-4) + (-3)$ , you might be tempted to say that $q = -4$ and $r = -3$ . The remainder, however, can never be negative. But $-23$ can be written as $-23 = 5 \cdot (-5) + 2$ , where $0 \leq r (= 2) < 5$ . Thus, $q = -5$ and $r = 2$ .
4	<b>State the Pigeonhole Principle</b> BTL1 If $m$ pigeons are assigned to $n$ pigeonholes, where $m > n$ , then at least two pigeons must occupy the same pigeonhole.
5	<b>Find the number of positive integers <math>\leq 2076</math> and divisible by neither 4 nor 5.</b> BTL3 Let $A = \{x \in \mathbb{N} \mid x \leq 2076 \text{ and divisible by 4}\}$ and $B = \{x \in \mathbb{N} \mid x \leq 2076 \text{ and divisible by 5}\}$ . Then $\begin{aligned} A \cup B  &=  A  +  B  -  A \cap B  \\&= 2076/4 + 2076/5 - 2076/20 \\&= 519 + 415 - 103 = 831\end{aligned}$ Therefore $2076 - 831 = 1245$ integers not divisible by 4 or 5.
6	<b>Find the number of positive integers <math>\leq 3000</math> and divisible by 3, 5, or 7.</b> BTL3 Let $A$ , $B$ , and $C$ denote the sets of positive integers $\leq 3000$ and divisible by 3, 5, or 7. By the Inclusion–Exclusion Principle, $\begin{aligned} A \cup B \cup C  &=  A  +  B  +  C  -  A \cap B  -  B \cap C  -  C \cap A  +  A \cap B \cap C  \\&= 3000/3 + 3000/5 + 3000/7 - 3000/15 - 3000/35 - 3000/21 + 3000/105 \\&= 1000 + 600 + 428 - 200 - 85 - 142 + 28 = 1629\end{aligned}$
7	<b>Express <math>10110_{\text{two}}</math> in base ten.</b> BTL4 $\begin{aligned}10110_{\text{two}} &= 1(2^4) + 0(2^3) + 1(2^2) + 1(2^1) + 0(2^0) \\&= 16 + 0 + 4 + 2 + 0 = 22\end{aligned}$
8	<b>Add the binary integers <math>10110_{\text{two}}</math> and <math>101_{\text{two}}</math></b> BTL3 First, write the integers one below the other in such a way that the corresponding bits are vertically aligned. Add the corresponding bits from right to left, beginning with the ones column: $0 + 1 = 1$ . Because $1 \bmod 2 = 1$ , enter 1 as the ones bit in the sum. Since $1 \div 2 = 0$ , the resulting carry is 0. Now add the bits 0, 1, and 1 in the twos column: $0 + 1 + 1 = 2$ . Because $2 \bmod 2 = 0$ and $2 \div 2 = 1$ , enter 0 in the twos column and the new carry is 1. Continuing like this, we get the sum $100001_{\text{two}}$ .
9	<b>Multiply <math>1011_{\text{two}}</math> and <math>101_{\text{two}}</math>.</b> BTL3 $\begin{array}{r} 1011 \\ (*) \quad 101 \\ \hline 1011 \\ 0000 \\ 1011 \end{array}$

	1 1 0 1 1 1		
10	<p><b>Show that 111 cannot be a square in any base.</b> BTL4</p> <p>Suppose 111 is a perfect square <math>a^2</math> in some base b, so <math>a^2 = b^2 + b + 1 &lt; (b + 1)^2</math>.</p> <p>Then <math>(b + 1/2)^2 = b^2 + b + 1/4 &lt; b^2 + b + 1</math></p> <p>That is, <math>(b + 1/2)^2 &lt; a^2 &lt; (b + 1)^2</math></p> <p>This yields <math>(b + 1/2) &lt; a &lt; b + 1</math>;</p> <p>That is, a lies between <math>b + 1/2</math> and <math>b + 1</math>, which is impossible.</p> <p>Thus, 111 cannot be a square in any base.</p>		
11	<p><b>Study the number pattern and add two more rows:</b></p> <p><b>1 · 8 + 1 = 9</b></p> <p><b>12 · 8 + 2 = 98</b></p> <p><b>123 · 8 + 3 = 987</b></p> <p><b>1234 · 8 + 4 = 9876</b></p> <p><b>12345 · 8 + 5 = 98765</b></p> <p><b>123456 · 8 + 6 = 987654</b> BTL3</p> <p>The 1<sup>st</sup> factor of the product on the LHS of the nth equation has the form 123 . . . n; the second factor is always 8. The second addend in the equation is n. The number on the RHS of the nth equation contains n digits, each begins with the digit 9, and the digits decrease by 1. Thus the next two lines of the pattern are</p> <p><math>1234567 \cdot 8 + 7 = 9876543</math></p> <p><math>12345678 \cdot 8 + 8 = 98765432</math></p>		
12	<p><b>Determine whether 1601 is a prime number.</b> BTL3</p> <p>First list all the primes <math>\leq \sqrt{1601}</math></p> <p>They are 2, 3, 5, 7, 11, 13, 17, 19, 23, 29, 31, and 37</p> <p>Since none of them is a factor of 1601 ,</p> <p>Therefore 1601 is a prime.</p>		
13	<p><b>Find six consecutive integers that are composites.</b> BTL3</p> <p>By the theorem</p> <p>“For every positive integer n, there are n consecutive integers that are composite numbers.”</p> <p>There are six consecutive integers beginning with <math>(n + 1)! + 2 = (6 + 1)! + 2 = 5042</math>, namely, 5042, 5043, 5044, 5045, 5046, and 5047.</p>		
14	<p><b>Evaluate A74<sub>twelve</sub> – 39B<sub>twelve</sub> and 2076<sub>sixteen</sub> – 1777<sub>sixteen</sub></b> BTL3</p> <p>We can find answers in the following figures</p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td style="text-align: center;"> <math>A</math>  </td> <td style="text-align: center;"> <math>F</math>  </td> </tr> </table>	$A$ 	$F$ 
$A$ 	$F$ 		

15	<p><b>Show that <math>641 f_5</math>.</b> BTL4</p> $641 = 5 \cdot 2^7 + 1$ $\text{So } 2^{25} + 1 = 2^{32} + 1 = 2^4 \cdot 2^{28} + 1$ $16 \cdot 2^{28} + 1 = (641 - 625)2^{28} + 1$ $(641 - 5^4)2^{28} + 1 = 641 \cdot 2^{28} - (5 \cdot 2^7)^4 + 1$ $= 641 \cdot 2^{28} - (641 - 1)^4 + 1,$ $= 641 \cdot 2^{28} - (641^4 - 4 \cdot 641^3 + 6 \cdot 641^2 - 4 \cdot 641 + 1) + 1$ $= 641(2^{28} - 641^3 + 4 \cdot 641^2 - 6 \cdot 641 + 4)$ <p>Thus, <math>641 f_5</math>.</p>
16	<p><b>Express (28, 12) as a linear combination of 28 and 12.</b> BTL2</p> <p>First, notice that <math>\text{GCD}(28, 12) = 4</math>. Next, we need to find integers <math>\alpha</math> and <math>\beta</math> such that <math>\alpha \cdot 28 + \beta \cdot 12 = 4</math>.</p> <p>By trial and error, <math>\alpha = 1</math> and <math>\beta = -2</math> works: <math>1 \cdot 28 + (-2) \cdot 12 = 4</math>.</p>
17	<p><b>Find (12, 18, 28), (12, 36, 60, 108), and (15, 28, 50).</b> BTL3</p> <p>The largest positive integer that divides 12, 18, and 28 is 2, so <math>(12, 18, 28) = 2</math>.</p> <p>12 is the largest factor of 12, and 12 is a factor of 12, 36, 60, and 108; so <math>(12, 36, 60, 108) = 12</math>.</p> <p>Since <math>(15, 28) = 1</math>, the largest common factor of 15, 28, and 50 is 1; that is, <math>(15, 28, 50) = 1</math>.</p>
18	<p><b>Express (12, 15, 21) as a linear combination of 12, 15, and 21</b> BTL2</p> <p>First, we may notice that <math>(12, 15, 21) = 3</math>. Next, find integers <math>\alpha</math>, <math>\beta</math>, and <math>\gamma</math>, by trial and error, such that <math>\alpha \cdot 12 + \beta \cdot 15 + \gamma \cdot 21 = 3</math>; <math>\alpha = -1</math>, <math>\beta = 1</math>, and <math>\gamma = 0</math> is such a Combination: <math>(-1) \cdot 12 + 1 \cdot 15 + 0 \cdot 21 = 3</math>.</p>
19	<p><b>Using recursion, evaluate (18, 30, 60, 75, 132).</b> BTL3</p> $(18, 30, 60, 75, 132) = ((18, 30, 60, 75), 132) = (((18, 30, 60), 75), 132)$ $= (((((18, 30), 60), 75), 132) = (((6, 60), 75), 132)$ $= ((6, 75), 132) = (3, 132)$

	$= 3$
20	<p><b>Find the canonical decomposition of 2520.</b> BTL3</p> <p>Beginning with the smallest prime 2, since <math>2 2520</math>, <math>2520 = 2 \cdot 1260</math>. Now 2 is a factor of 1260, so <math>2520 = 2 \cdot 2 \cdot 630</math>; <math>2 630</math> again, so <math>2520 = 2 \cdot 2 \cdot 2 \cdot 315</math>. Now 2 <math>\nmid 315</math>, but 3 does, so <math>2520 = 2 \cdot 2 \cdot 2 \cdot 3 \cdot 105</math>; 3 is a factor of 105 also, so <math>2520 = 2 \cdot 2 \cdot 2 \cdot 3 \cdot 3 \cdot 35</math>. Continuing like this we get</p> $2520 = 2 \cdot 2 \cdot 2 \cdot 3 \cdot 3 \cdot 5 \cdot 7 = 2^3 \cdot 3^2 \cdot 5 \cdot 7$ <p>Which is the desired canonical decomposition.</p>
21	<p><b>Using the canonical decompositions of 168 and 180, find their gcd.</b> BTL3</p> <p>We know that <math>168 = 2^3 \cdot 3 \cdot 7</math> and <math>180 = 2^2 \cdot 3^2 \cdot 5</math>. The only common prime factors are 2 and 3, so 5 or 7 cannot appear in their gcd. Since 2 appears thrice in the canonical decomposition of 168, but only twice in the canonical decomposition of 180, <math>2^2</math> is a factor in the gcd. Similarly, 3 is also a common factor, so <math>(168, 180) = 2^2 \cdot 3 = 12</math>.</p>
22	<p><b>Using the canonical decompositions of 1050 and 2574, find their lcm.</b> BTL3</p> <p><math>1050 = 2 \cdot 3 \cdot 5^2 \cdot 7</math> and <math>2574 = 2 \cdot 3^2 \cdot 11 \cdot 13</math>. Therefore,</p> $\begin{aligned} [1050, 574] &= 2^{\max\{1, 1\}} \cdot 3^{\max\{1, 2\}} \cdot 5^{\max\{2, 0\}} \cdot 7^{\max\{1, 0\}} \cdot 11^{\max\{0, 1\}} \cdot 13^{\max\{0, 1\}} \\ &= 2^1 \cdot 3^2 \cdot 5^2 \cdot 7^1 \cdot 11^1 \cdot 13^1 = 450,450 \end{aligned}$
23	<p><b>Using (252, 360), compute [252, 360].</b> BTL3</p> <p><math>252 = 2^2 \cdot 3^2 \cdot 7</math> and <math>360 = 2^3 \cdot 3^2 \cdot 5</math>, so <math>(252, 360) = 2^2 \cdot 3^2 = 36</math>.</p> $[252, 360] = \frac{252 * 360}{36} = 2520$
24	<p><b>Using recursion, evaluate [24, 28, 36, 40].</b> BTL3</p> $\begin{aligned} [24, 28, 36, 40] &= [[24, 28, 36], 40] = [[[24, 28], 36], 40] \\ &= [[168, 36], 40] = [504, 40] = 2520 \end{aligned}$
25	<p><b>Define Least Common Multiple</b> BTL3</p> <p>The least common multiple of two positive integers <math>a</math> and <math>b</math> is the least positive integer divisible by both <math>a</math> and <math>b</math>; it is denoted by <math>[a, b]</math>.</p>
	<b>PART-B</b>
1.	<p><b>State and Prove Division Algorithm (10M)</b> BTL1</p> <p><b>Answer:</b> Refer Page No:69-70-Elementary number theory with Applications by Koshy</p>

	<ul style="list-style-type: none"> <li>Statement : Let <math>a</math> be any integer and <math>b</math> a positive integer. Then there exist unique integers <math>q</math> and <math>r</math> such that <math>a=b.q + r</math> where <math>0 \leq r &lt; b</math> (2M)</li> <li>Existence Proof (4M)</li> <li>Uniqueness Proof (4M)</li> </ul>
2.	<p><b>Show that the number of leap years after 1600 and not exceeding a given year <math>y</math> is given by <math>l = [y/4] - [y/100] + [y/400] - 388</math>. (8M) BTL2</b></p> <p><b>Answer:</b> Refer Page No:77-78-Elementary number theory with Applications by Koshy</p> <ul style="list-style-type: none"> <li><math>n_1 = [y/4] - 400</math> (2M)</li> <li><math>n_2 = [y/100] - 16</math> (2M)</li> <li><math>n_3 = [y/400] - 4</math> (2M)</li> </ul> <p>For Proving</p> <ul style="list-style-type: none"> <li><math>l = [y/4] - [y/100] + [y/400] - 388.</math> (2M)</li> </ul>
3.	<p><b>Let <math>b</math> be a positive integer <math>\geq 2</math>. Then Prove that every positive integer <math>N</math> can be expressed uniquely in the form <math>N = a_k b^k + a_{k-1} b^{k-1} + \dots + a_1 b + a_0</math>, where <math>a_0, a_1, \dots, a_k</math> are nonnegative integers less than <math>b</math>, <math>a_k = 0</math>, and <math>k \geq 0</math>. (16M) BTL2</b></p> <p><b>Answer:</b> Refer Page No:80-82-Elementary number theory with Applications by Koshy</p> <ul style="list-style-type: none"> <li><math>N = q_1 b^2 + a_1 b + a_0</math> (8M)</li> <li>Uniqueness Proof (8M)</li> </ul>
4.	<p><b>Express 3014 in base eight. (8M) BTL3</b></p> <p><b>Answer:</b> Refer Page No:84-Elementary number theory with Applications by Koshy</p> <ul style="list-style-type: none"> <li><math>3014 = 5 \cdot 512 + 454</math> (4M)</li> <li><math>3014 = 5706_{\text{eight}}</math> (4M)</li> </ul>
5.	<p><b>Add two more rows to the following pattern, conjecture a formula for the <math>n</math>th row, and prove it:</b></p> $9 \cdot 9 + 7 = 88$ $98 \cdot 9 + 6 = 888$ $987 \cdot 9 + 5 = 8888$ $9876 \cdot 9 + 4 = 88888$ $98765 \cdot 9 + 3 = 888888 \quad (8M) \text{ BTL2}$ <p><b>Answer:</b> Refer Page No:100-101-Elementary number theory with Applications by Koshy</p> <ul style="list-style-type: none"> <li><math>987654 \cdot 9 + 2 = 8888888</math> (2M)</li> <li><math>9876543 \cdot 9 + 1 = 88888888</math> (2M)</li> <li>For proving the conjecture (4M)</li> </ul>
6.	<p><b>Prove that Every integer <math>n \geq 2</math> has a prime factor. (8M) BTL2</b></p> <p><b>Answer:</b> Refer Page No:104-Elementary number theory with Applications by Koshy</p> <ul style="list-style-type: none"> <li>If <math>k + 1</math> is a prime, then <math>k + 1</math> is a prime factor of itself. (4M)</li> <li>If <math>k + 1</math> is not a prime, <math>k + 1</math> must be a composite, so it must have a factor <math>d \leq k</math>. Then, by the inductive hypothesis, <math>d</math> has a prime factor <math>p</math>. So <math>p</math> is a factor of <math>k + 1</math>,</li> </ul>

	Thus, by the strong version of induction, the statement is true for every integer $\geq 2$ ; that is, every integer $\geq 2$ has a prime factor. (4M)
7.	<b>Prove that There are infinitely many primes. (8M) BTL2</b> <b>Answer: Refer Page No:104-Elementary number theory with Applications by Koshy</b> • By Proving Contradiction method $\pi 1$ , which is impossible. (8M)
8.	<b>Prove that there is no polynomial <math>f(n)</math> with integral coefficients that will produce primes for all integers <math>n</math>. (8M) BTL2</b> <b>Answer: Refer Page No:109-Elementary number theory with Applications by Koshy</b> • $f(b + tp) = p + pg(t)$ , (4M) • $f(n)$ is a polynomial of degree $k$ , so it <i>cannot</i> assume the same value more than $k$ times, yielding a contradiction. Thus, <i>no</i> polynomial with integral coefficients exists that will generate only primes. (4M)
9.	<b>Find the number of primes <math>\leq 100</math>. (8M) BTL3</b> <b>Answer: Refer Page No:110-Elementary number theory with Applications by Koshy</b> • $\pi(10) = 4$ (4M) • $\pi(100) = 25$ (4M)
10.	<b>Find the formula for <math>\sum_{i=1}^n F_i</math> (8M) BTL3</b> <b>Answer: Refer Page No:132-Elementary number theory with Applications by Koshy</b> • $\sum_{i=1}^n F_i = F_{n+2} - 1$ (4M) • $\sum_{i=1}^{k+1} F_i = F_{k+3} - 1$ (4M)
11.	<b>Let <math>(a, b) = d</math>. Then Prove that</b> $(a/d, b/d) = 1$ $(a, a - b) = d$ . (8M) BTL2 <b>Answer: Refer Page No:158-159-Elementary number theory with Applications by Koshy</b> • For Showing $(a/d, b/d) = 1$ (4M) • For Showing $(a, a - b) = d$ . (4M)
12.	<b>Prove that The gcd of the positive integers <math>a</math> and <math>b</math> is a linear combination of <math>a</math> and <math>b</math>. (8M) BTL2</b> <b>Answer: Refer Page No: 159-Elementary number theory with Applications by Koshy</b> • For Showing $r$ is a linear combination of $a$ and $b$ . (4M) • For proving $d = (a, b)$ (4M)
13.	<b>If <math>a c</math> and <math>b c</math>, and <math>(a, b) = 1</math>, then Prove that <math>ab c</math>. (8M) BTL2</b>

	<b>Answer: Refer Page No: 162-Elementary number theory with Applications by Koshy</b> <ul style="list-style-type: none"> <li>• <math>\alpha a + \beta b = 1</math> for some integers <math>\alpha</math> and <math>\beta</math> (4M)</li> <li>• <math>ab(n\alpha + m\beta) = c</math>, so <math>ab c</math>. (4M)</li> </ul>
14.	<b>State and Prove Lame's Theorem (16M) BTL1</b> <b>Answer: Refer Page No: 172-Elementary number theory with Applications by Koshy</b> <ul style="list-style-type: none"> <li>• Statement : The number of divisions needed to compute <math>(a, b)</math> by the euclidean algorithm is no more than five times the number of decimal digits in <math>b</math>, where <math>a \geq b \geq 2</math>. (2M)</li> <li>• <math>b \geq F_{n+1}</math> (6M)</li> <li>• <math>b &lt; 10^k</math> . Therefore, <math>\log b &lt; k</math> and hence <math>k &gt; (n - 1)/5</math>. Thus, <math>n &lt; 5k + 1</math> or <math>n \leq 5k</math>. (8M)</li> </ul>
	<b>UNIT IV</b>
	<b>DIOPHANTINE EQUATIONS AND CONGRUENCES</b> <span style="float: right;">12</span> Linear Diophantine equations – Congruence's – Linear Congruence's - Applications: Divisibility tests - Modular exponentiation-Chinese remainder theorem – 2 x 2 linear systems.
<b>Q.No.</b>	<b>PART-A</b>
1	<p><b>Twenty-three weary travellers entered the outskirts of a lush and beautiful forest. They found 63 equal heaps of plantains and seven single fruits, and divided them equally. Find the number of fruits in each heap BTL3</b></p> <p>Let <math>x</math> denote the number of plantains in a heap and <math>y</math> the number of plantains received by a traveller. Then we get the LDE <math>63x + 7 = 23y</math> Since both <math>x</math> and <math>y</math> must be positive, we are interested in finding only the positive integral solutions of the LDE . Solving it for <math>y</math>, <math>y = \frac{63x + 7}{23}</math> When <math>x &gt; 0</math>, clearly <math>y &gt; 0</math>. So try the values 1, 2, 3, and so on for <math>x</math> until the value of <math>y</math> becomes an integer .It follows from the table that <math>x = 5</math>, <math>y = 14</math> is a solution. We can verify that <math>x = 28</math>, <math>y = 77</math> is yet another solution. That is, the LDE has infinitely many solutions.</p>
2	<p><b>Does every LDE have a solution? BTL1</b></p> <p>Consider the LDE <math>2x + 4y = 5</math>. No matter what the integers <math>x</math> and <math>y</math> are, the LHS <math>2x + 4y</math> is always even, whereas the RHS is always odd, so the LDE has no solution. Thus, not every LDE has a solution.</p>
3	<p><b>Determine whether the LDEs <math>12x + 18y = 30</math>, <math>2x + 3y = 4</math>, and <math>6x + 8y = 25</math> are solvable. BTL3</b></p> <p><math>(12, 18) = 6</math> and <math>6 30</math>, so the LDE <math>12x + 18y = 30</math> has a solution.</p> <p><math>(2, 3) = 1</math>, therefore LDE has a solution.</p>

	(6, 8) = 2, but $2 \nmid 25$ , so the LDE $6x + 8y = 25$ is not solvable.
4	<b>Twenty-four weary travellers entered the outskirts of a lush and beautiful forest. They found 63 equal heaps of plantains and seven single fruits, and divided them equally. Find the number of fruits in each heap BTL3</b>  With 24 travellers, the Diophantine equation becomes $63x - 24y = -7$ . Since $(63, 24) = 3$ and $3 \nmid 7$ , the Diophantine equation has no integral solutions, so the puzzle has no solutions.
5	<b>Determine whether the LDEs <math>6x + 8y + 12z = 10</math> and <math>6x + 12y + 15z = 10</math> are solvable.</b> BTL3 Since $(6, 8, 12) = 2$ and $2 \mid 10$ , the LDE $6x + 8y + 12z = 10$ is solvable. $(6, 12, 15) = 3$ , but $3 \nmid 10$ , so the $6x + 12y + 15z = 10$ has no integral solutions.
6	<b>Prove that <math>a \equiv b \pmod{m}</math> if and only if <math>a = b + km</math> for some integer k.</b> BTL1  Suppose $a \equiv b \pmod{m}$ . Then $m (a - b)$ , so $a - b = km$ for some integer $k$ ; that is, $a = b + km$ . Conversely, suppose $a = b + km$ for some integer $k$ . Then $a - b = km$ , so $m (a - b)$ and consequently, $a \equiv b \pmod{m}$ .
7	<b>Prove that no prime of the form <math>4n + 3</math> can be expressed as the sum of two squares.</b> BTL1 Let $N$ be a prime of the form $4n + 3$ . Then $N \equiv 3 \pmod{4}$ .  Suppose $N = A^2 + B^2$ for some integers $A$ and $B$ . Since $N$ is odd, one of the squares, say, $A^2$ , must be odd and hence $B^2$ must be even. Then $A$ must be odd and even. Let $A = 2a + 1$ and $B = 2b$ for some integers $a$ and $b$ . Then $\begin{aligned} N &= (2a + 1)^2 + (2b)^2 \\ &= 4(a^2 + b^2 + a) + 1 \\ &\equiv 1 \pmod{4} \end{aligned}$ which is a contradiction, since $N \equiv 3 \pmod{4}$ .
8	<b>Find the remainder when <math>1! + 2! + \dots + 100!</math> is divided by 15</b> BTL3 We know that, when $k \geq 5$ , $k! \equiv 0 \pmod{15}$ . Therefore, $\begin{aligned} 1! + 2! + \dots + 100! &\equiv 1! + 2! + 3! + 4! + 0 + \dots + 0 \pmod{15} \\ &\equiv 1 + 2 + 6 + 24 \pmod{15} \\ &\equiv 1 + 2 + 0 \pmod{15} \\ &\equiv 3 \pmod{15} \end{aligned}$ Thus, when the given sum is divided by 15, the remainder is 3.
9	<b>Find the remainder when <math>16^{53}</math> is divided by 7.</b> BTL3

	<p>First, reduce the base to its least residue: <math>16 \equiv 2 \pmod{7}</math>.</p> <p><math>16^{53} \equiv 2^{53} \pmod{7}</math>. Now express a suitable power of 2 congruent modulo 7 to a number less than 7: <math>2^3 \equiv 1 \pmod{7}</math>. Therefore, <math>2^{53} = 2^{3 \cdot 17 + 2} = (2^3)^{17} \cdot 2^2</math></p> $\begin{aligned} &\equiv 1^{17} \cdot 4 \pmod{7} \\ &\equiv 4 \pmod{7} \end{aligned}$ <p>So <math>16^{53} \equiv 4 \pmod{7}</math>, by the transitive property.</p> <p>Thus, when <math>16^{53}</math> is divided by 7, the remainder is 4.</p>
10	<p><b>Show that <math>11 \cdot 14^n + 1</math> is a composite number. BTL2</b></p> <p>Let <math>N = 11 \cdot 14^n + 1</math>. We shall show that <math>p N</math> for some prime <math>p</math>.</p> <p>Suppose <math>n</math> is even. Since <math>14 \equiv -1 \pmod{3}</math>, <math>14^n \equiv 1 \pmod{3}</math>. Then <math>N \equiv 2 \cdot 1 + 1 \equiv 0 \pmod{3}</math>, so <math>3 N</math>.</p> <p>On the other hand, let <math>n</math> be odd. Since <math>14 \equiv -1 \pmod{5}</math>, <math>14^n \equiv -1 \pmod{5}</math>.</p> <p>Then <math>N \equiv 1 \cdot (-1) + 1 \equiv 0 \pmod{5}</math>, so <math>5 N</math>.</p> <p>Thus, in both cases, <math>N</math> is composite.</p>
11	<p><b>Show that <math>f_5 = 2^{2^5} + 1</math> is divisible by 641. BTL2</b></p> <p><math>640 \equiv -1 \pmod{641}</math>; that is, <math>5 \cdot 2^7 \equiv -1 \pmod{641}</math>. Therefore,</p> $5^4 \cdot 2^{28} \equiv 1 \pmod{641}$ <p>But <math>5^4 = 625 \equiv -16 \equiv -2^4 \pmod{641}</math>, so congruence can be rewritten as <math>(-2^4)(2^{28}) \equiv 1 \pmod{641}</math>; that is, <math>2^{32} \equiv -1 \pmod{641}</math>. Thus, <math>641 f_5</math>.</p>
12	<p><b>Using casting out nines, check if the sum of the numbers 3569, 24,387, and 49,508 is 78,464. BTL1</b></p> <p><math>3569 \equiv 3 + 5 + 6 + 9 \equiv 5 \pmod{9}</math></p> <p><math>24387 \equiv 2 + 4 + 3 + 8 + 7 \equiv 6 \pmod{9}</math></p> <p><math>49508 \equiv 4 + 9 + 5 + 0 + 8 \equiv 8 \pmod{9}</math></p> <p>Their sum <math>\equiv 5 + 6 + 8 \pmod{9}</math></p> <p><math>\equiv 1 \pmod{9}</math></p> <p>Given answer = 78464 <math>\equiv 7 + 8 + 4 + 6 + 4 \pmod{9}</math></p> <p><math>\equiv 2 \pmod{9}</math></p> <p>Thus, the given answer is not congruent to the actual sum modulo 9; consequently, the given sum is definitely wrong. (The correct sum is 77,464.)</p>

	<b>Using casting out nines, determine whether the product of 1976 and 3458 is 6,833,080. BTL1</b>
13	$\begin{array}{rcl} 1976 & \equiv & 1 + 9 + 7 + 6 \equiv 5 \pmod{9} \\ \\ 3458 & \equiv & 3 + 4 + 5 + 8 \equiv 2 \pmod{9} \\ \hline \text{Their product} & & \equiv 1 \pmod{9} \end{array}$ <p>Given answer = <math>6,833,080 \equiv 6 + 8 + 3 + 3 + 0 + 8 + 0 \pmod{9}</math>  <math>\equiv 1 \pmod{9}</math></p> <p>Because the given answer is congruent to the actual product modulo 9, we might be tempted to say that the given answer is correct. In fact, all we can say is, it is probably correct. This is so because any rearrangement of the digits of an integer yields the same least residue modulo 9, an idea used by today's accountants. (The given answer is in fact wrong. The correct answer is 6,833,008.)</p>
14	<b>Find the digital roots of square numbers. BTL3</b>  By the division algorithm, every integer $n$ is of the form $9k + r$ , where $0 \leq r < 9$ . So $n \equiv r \pmod{9}$ and hence $n^2 \equiv r^2 \pmod{9}$ . Since $r \equiv r - 9 \pmod{9}$ , $0^2 \equiv 0 \pmod{9}$ , $(\pm 1)^2 \equiv 1 \pmod{9}$ , $(\pm 2)^2 \equiv 4 \pmod{9}$ , $(\pm 3)^2 \equiv 0 \pmod{9}$ , and $(\pm 4)^2 \equiv 7 \pmod{9}$ . Thus, $n^2$ is congruent to 0, 1, 4, or 7, so its digital root is 1, 4, 7, or 9.
15	<b>Determine whether <math>N = 16,151,613,924</math> can be a square. BTL2</b> Digital root of $N \equiv (1 + 6 + 1 + 5 + 1 + 6 + 1 + 3 + 9 + 2 + 4) \pmod{9} \equiv 3 \pmod{9}$ Because the digital root is 3, $N$ is not a square.
16	<b>Prove that the digital root of the product of twin primes, other than 3 and 5, is 8. BTL2</b> Every prime $> 3$ is of the form $6k - 1$ or $6k + 1$ , so we can take the twin primes to be $6k - 1$ and $6k + 1$ . Their product = $(6k - 1)(6k + 1) = 36k^2 - 1 \equiv 0 - 1 \equiv 8 \pmod{9}$ . So the digital root of the product is 8.
17	<b>Determine the day of the week on which January 13, 2020, falls. BTL3</b>  We know that January 2020 is the eleventh month of year 2019, so here $y = 2019$ , $C = 20$ , $D = 19$ , $m = 11$ , and $r = 13$ . $\begin{aligned} d &\equiv 13 + 2.6 \times 11 - 0.2 - 2 \times 20 + 19 + 20/4 + 19/4 \pmod{7} \\ &\equiv 13 + 28 - 40 + 19 + 5 + 4 \pmod{7} \\ &\equiv 1 \pmod{7} \end{aligned}$ <p>Thus, January 13, 2020, falls on a Monday.</p>
18	<b>Determine whether the following linear system is solvable. <math>x \equiv 3 \pmod{6}</math></b> <b><math>x \equiv 5 \pmod{8}</math> BTL3</b> Since $(6, 8) = 2$ and $2 (3 - 5)$ , the linear system has a solution.

	<b>Determine whether the following linear system is solvable.</b>
19	$x \equiv 7 \pmod{9}$ $x \equiv 11 \pmod{12}$ BTL3 <p>We have <math>(9, 12) = 3</math>, but <math>3 \nmid (7 - 11)</math>, so the system is not solvable.</p>
20	<b>Determine whether the following linear system is solvable:</b> $x \equiv 4 \pmod{6}$ $x \equiv 2 \pmod{8}$ $x \equiv 1 \pmod{9}$ BTL3 <p>Since <math>(6, 8) (4 - 2)</math>, <math>(8, 9) (2 - 1)</math>, and <math>(6, 9) (4 - 1)</math>, the linear system has a solution.</p>
21	<b>Determine whether the following linear system is solvable:</b> $x \equiv 3 \pmod{4}$ $x \equiv 5 \pmod{9}$ $x \equiv 7 \pmod{12}$ BTL3 <p>Since <math>(4, 9) (3 - 5)</math>, and <math>(9, 12) (5 - 8)</math>, but <math>(4, 12) = 4</math> and <math>4 \nmid (3 - 8)</math>; so the system is not solvable.</p>
22	<b>Define <math>2 \times 2</math> linear system</b> BTL1 A $2 \times 2$ linear system is a system of linear congruences of the form $\begin{aligned} ax + by &\equiv e \pmod{m} \\ cx + dy &\equiv f \pmod{m} \end{aligned}$
23	<b>Show that <math>x \equiv 12 \pmod{13}</math> and <math>y \equiv 2 \pmod{13}</math> is a solution of the <math>2 \times 2</math> linear system</b> $2x + 3y \equiv 4 \pmod{13}$ $3x + 4y \equiv 5 \pmod{13}$ BTL2 When $x \equiv 12 \pmod{13}$ and $y \equiv 2 \pmod{13}$ , $2x + 3y \equiv 2(12) + 3(2) \equiv 4 \pmod{13}$ $3x + 4y \equiv 3(12) + 4(2) \equiv 5 \pmod{13}$ Therefore, every pair $x \equiv 12 \pmod{13}$ , $y \equiv 2 \pmod{13}$ is a solution of the system.
	<b>PART-B</b>
1.	<b>If a cock is worth five coins, a hen three coins, and three chicks together one coin, how many cocks, hens, and chicks, totalling 100, can be bought for 100 coins? (8M)</b> BTL1 <b>Answer: Refer Page No: 190-191-Elementary number theory with Applications by Koshy</b> <ul style="list-style-type: none"> <li>• <math>x=4t ; y=25-7t; z=75+3t</math> (4M)</li> </ul>

	<ul style="list-style-type: none"> <li>The riddle has four possible solutions, corresponding to <math>t = 0, 1, 2</math>, and <math>3</math>:  <math>x = 0, y = 25, z = 75</math>; <math>x = 4, y = 18, z = 78</math>; <math>x = 8, y = 11, z = 81</math>; and <math>x = 12, y = 4, z = 84</math>. (4M)</li> </ul>
2.	<p><b>Prove that the LDE <math>ax + by = c</math> is solvable if and only if <math>d c</math>, where <math>d = (a, b)</math>. If <math>x_0, y_0</math> is a particular solution of the LDE, then all its solutions are given by <math>x = x_0 + \left(\frac{b}{d}\right)t</math>; <math>y = y_0 - \left(\frac{a}{d}\right)t</math></b></p> <p>Where <math>t</math> is an arbitrary integer. (16M) BTL2</p> <p><b>Answer: Refer Page No: 192-Elementary number theory with Applications by Koshy</b></p> <ul style="list-style-type: none"> <li>If the LDE is solvable, then <math>d c</math>. (4M)</li> <li>To prove that if <math>d c</math>, then the LDE is solvable (4M)</li> <li>To Show that <math>x = x_0 + \left(\frac{b}{d}\right)t</math>; <math>y = y_0 - \left(\frac{a}{d}\right)t</math> is a solution (4M)</li> <li><math>x' = x_0 + \left(\frac{b}{d}\right)t</math>; <math>y' = y_0 - \left(\frac{a}{d}\right)t</math> (4M)</li> </ul>
3.	<p><b>Five sailors and a monkey are marooned on a desert island. During the day they gather coconuts for food. They decide to divide them up in the morning, but first they retire for the night. While the others sleep, one sailor gets up and divides them into five equal piles, with one left over, which he throws out for the monkey. He hides his share, puts the remaining coconuts together, and goes back to sleep. Later a second sailor gets up, divides the pile into five equal shares with one coconut left over, which he discards for the monkey. One by one the remaining sailors repeat the process. In the morning, they divide the pile equally among them with one coconut left over, which they throw out for the monkey. Find the smallest possible number of coconuts in the original pile. (8M) BTL3</b></p> <p><b>Answer: Refer Page No: 197-Elementary number theory with Applications by Koshy</b></p> <ul style="list-style-type: none"> <li><math>15625 \cdot [(-11529) \cdot 313] - 1024 \cdot [4776 \cdot (-11529)] = -11529</math> (4M)</li> <li>The least number of coconuts in the original pile is 15,621. (4M)</li> </ul>
4.	<p><b>Solve the LDE <math>1076x + 2076y = 3076</math> by Euler's method. (16M) BTL3</b></p> <p><b>Answer: Refer Page No: 199-Elementary number theory with Applications by Koshy</b></p> <ul style="list-style-type: none"> <li><math>u=-1, v=1, x=-1, y=2</math> (8M)</li> <li>The general solution is <math>x = 519t - 1</math>, <math>y = -269t + 2</math> (8M)</li> </ul>
5.	<p><b>A six-digit positive integer is cut up in the middle into two three-digit numbers. If the square of their sum yields the original number, find the number. (8M) BTL3</b></p> <p><b>Answer: Refer Page No: 201-Elementary number theory with Applications by Koshy</b></p> <ul style="list-style-type: none"> <li><math>27 c</math> and <math>37 (c - 1)</math>, or <math>27 (c - 1)</math> and <math>37 c</math> (4M)</li> </ul>

	<ul style="list-style-type: none"> <li>there are two six-digit positive integers satisfying the required property: 998,001 and 494,209 (4M)</li> </ul>
6.	<p><b>Find the general solution of the LDE <math>6x + 8y + 12z = 10</math> (8M) BTL3</b></p> <p><b>Answer: Refer Page No: 203-Elementary number theory with Applications by Koshy</b></p> <ul style="list-style-type: none"> <li><math>x = 5 + 2t</math></li> <li><math>y = -10 - 6t + 3t'</math></li> <li><math>z = 5 + 3t - 2t'</math></li> </ul> <p style="text-align: right;">(8M)</p>
7.	<p><b>Prove that <math>a \equiv b \pmod{m}</math> if and only if <math>a</math> and <math>b</math> leave the same remainder when divided by <math>m</math>. (8M) BTL2</b></p> <p><b>Answer: Refer Page No: 214-Elementary number theory with Applications by Koshy</b></p> <ul style="list-style-type: none"> <li>For Proving <math>a</math> and <math>b</math> leave the same remainder when divided by <math>m</math> (4M)</li> <li>For Proving <math>a \equiv b \pmod{m}</math> (4M)</li> </ul>
8.	<p><b>Let <math>a \equiv b \pmod{m}</math> and <math>c \equiv d \pmod{m}</math>. Then Prove that <math>a + c \equiv b + d \pmod{m}</math> and <math>ac \equiv bd \pmod{m}</math>. (8M) BTL2</b></p> <p><b>Answer: Refer Page No: 218-Elementary number theory with Applications by Koshy</b></p> <ul style="list-style-type: none"> <li>For Proving <math>a + c \equiv b + d \pmod{m}</math> (4M)</li> <li>For Proving <math>ac \equiv bd \pmod{m}</math>. (4M)</li> </ul>
9.	<p><b>Find the positive integers <math>n</math> for which <math>\sum_{k=1}^n k!</math> is a square. (8M) BTL3</b></p> <p><b>Answer: Refer Page No: 219-Elementary number theory with Applications by Koshy</b></p> <ul style="list-style-type: none"> <li>If <math>n \geq 5</math>, <math>S</math> cannot be a square. (4M)</li> <li>There are exactly two positive integers <math>n</math> for which <math>S</math> is a square, namely, 1 and 3. (4M)</li> </ul>
10.	<p><b>If <math>a \equiv b \pmod{m}</math>, then Prove that <math>a^n \equiv b^n \pmod{m}</math> for any positive integer <math>n</math>. (4M) BTL3</b></p> <p><b>Answer: Refer Page No: 220-Elementary number theory with Applications by Koshy</b></p> <ul style="list-style-type: none"> <li>For Proving by induction method <math>a^{k+1} \equiv b^{k+1} \pmod{m}</math>. (4M)</li> </ul>
11.	<p><b>Show that 1919 cannot be expressed as the sum of the cube of an integer and the fourth power of another integer (8M) BTL2</b></p> <p><b>Answer: Refer Page No: 220-Elementary number theory with Applications by Koshy</b></p> <ul style="list-style-type: none"> <li>For Proving by contradiction method <math>19^{19}</math> cannot be expressed as the sum of the cube of an integer and the fourth power of another integer (8M)</li> </ul>
12.	<p><b>Prove that no integer of the form <math>8n + 7</math> can be expressed as a sum of three squares. (8M) BTL2</b></p> <p><b>Answer: Refer Page No: 220-Elementary number theory with Applications by Koshy</b></p>

	<ul style="list-style-type: none"> <li>For Proving by contradiction method no integer of the form <math>8n + 7</math> can be expressed as a sum of three squares. (8M)</li> </ul>
13.	<p><b>Find the remainder when <math>3^{247}</math> is divided by 17.</b> (8M) BTL3  <b>Answer:</b> Refer Page No: 221-Elementary number theory with Applications by Koshy</p> <ul style="list-style-type: none"> <li><math>3^{247} = 3^{24 \cdot 10 + 7} = (3^{24})^{10} \cdot 3^7 \equiv 1^{10} \cdot 3^7 \equiv 3^7 \pmod{17}</math> (4M)</li> <li>The remainder is 11 (4M)</li> </ul>
14.	<p><b>Find the remainder when <math>3^{247}</math> is divided by 25.</b> (8M) BTL3  <b>Answer:</b> Refer Page No: 222-Elementary number theory with Applications by Koshy</p> <ul style="list-style-type: none"> <li>For <math>3^{247} = 3^{128+64+32+16+4+2+1} \equiv 3^{128} \equiv 1 \pmod{25}</math> (4M)</li> <li>The remainder is 12 (4M)</li> </ul>
15.	<p><b>Find the remainder when <math>(n^2 + n + 41)^2</math> is divided by 12.</b> (8M) BTL3  <b>Answer:</b> Refer Page No: 225-Elementary number theory with Applications by Koshy</p> <ul style="list-style-type: none"> <li><math>(n^2 + n + 41)^2 \equiv (n^2 + n + 5)^2 \pmod{12}</math> (4M)</li> <li><math>(n^2 + n + 41)^2</math> is divided by 12, the remainder is 1. (4M)</li> </ul>
16.	<p><b>Prove that the linear congruence <math>ax \equiv b \pmod{m}</math> is solvable if and only if <math>d b</math>, where <math>d = (a, m)</math>.</b>  <b>If <math>d b</math>, then it has <math>d</math> incongruent solutions.</b> (16M) BTL2  <b>Answer:</b> Refer Page No: 231-Elementary number theory with Applications by Koshy</p> <ul style="list-style-type: none"> <li>For Proving the linear congruence <math>ax \equiv b \pmod{m}</math> is solvable (8M)</li> <li>For Proving If <math>d b</math>, then it has <math>d</math> incongruent solutions. (8M)</li> </ul>
17.	<p><b>Solve the congruence <math>12x \equiv 48 \pmod{18}</math>.</b> (8M) BTL3  <b>Answer:</b> Refer Page No: 232-Elementary number theory with Applications by Koshy</p> <ul style="list-style-type: none"> <li>The solutions of this congruence are of the form <math>x = 1 + 3t</math> (8M)</li> </ul>
18.	<p><b>State and Prove the Chinese Remainder Theorem</b> (16M) BTL3  <b>Answer:</b> Refer Page No: 297-Elementary number theory with Applications by Koshy</p> <ul style="list-style-type: none"> <li>Statement :The linear system of congruences <math>x \equiv a_i \pmod{m_i}</math>, where the moduli are pairwise relatively prime and <math>1 \leq i \leq k</math>, has a unique solution modulo <math>m_1 m_2 \cdots m_k</math>. (2M)</li> <li>To show that <math>x</math> is a solution of the linear system (6M)</li> <li>To show that the solution is unique modulo <math>M</math> (6M)</li> </ul>

	<b>UNIT V CLASSICAL THEOREMS AND MULTIPLICATIVE FUNCTIONS</b>
	Wilson's theorem – Fermat's little theorem – Euler's theorem – Euler's Phi functions – Tau and Sigma functions.
	<b>PART –A</b>
Q.No.	<b>Questions</b>
1.	<p><b>State Wilson's Theorem.</b> BTL1 If <math>p</math> is a prime, then <math>(p - 1)! \equiv -1 \pmod{p}</math>.</p>
2.	<p><b>Prove that, A positive integer <math>a</math> is self-invertible modulo <math>p</math> if and only if <math>a \equiv \pm 1 \pmod{p}</math>.</b> BTL2 Suppose <math>a</math> is self-invertible. Then <math>a^2 \equiv 1 \pmod{p}</math>; that is, <math>p (a^2 - 1)</math>; so <math>p (a - 1)(a + 1)</math>. Then, <math>p a - 1</math> or <math>p a + 1</math>; thus, either <math>a \equiv 1 \pmod{p}</math> or <math>a \equiv -1 \pmod{p}</math>. Conversely, Suppose <math>a \equiv 1 \pmod{p}</math> or <math>a \equiv -1 \pmod{p}</math>. In either case, <math>a^2 \equiv 1 \pmod{p}</math> so <math>a</math> is self-invertible modulo <math>p</math>.</p>
3.	<p><b>Prove that, If <math>n</math> is a positive integer such that <math>(n - 1)! \equiv -1 \pmod{n}</math>, then <math>n</math> is a prime.</b> BTL2 Suppose <math>n</math> is composite, say, <math>n = ab</math>, where <math>1 &lt; a, b &lt; n</math>. Since <math>a n</math> and <math>n [(n - 1)! + 1]</math>, <math>a [(n - 1)! + 1]</math>. Since <math>1 &lt; a &lt; n</math>, <math>a</math> is one of the integers 2 through <math>n - 1</math>, so <math>a (n - 1)!</math>. Therefore, <math>a [(n - 1)! + 1 - (n - 1)!]</math>; that is, <math>a 1</math>. So <math>a = 1</math>, a contradiction. Thus, <math>n</math> must be a prime.</p>
4	<p><b>State Fermat's Little Theorem</b> BTL1 Let <math>p</math> be a prime and <math>a</math> any integer such that <math>p \nmid a</math>. Then <math>a^{p-1} \equiv 1 \pmod{p}</math></p>
5	<p><b>Find the remainder when <math>24^{1947}</math> is divided by 17.</b> BTL3 We know that <math>24 \equiv 7 \pmod{17}</math> Therefore, <math>24^{1947} \equiv 7^{1947} \pmod{17}</math> But, by Fermat's little theorem, <math>7^{16} \equiv 1 \pmod{17}</math>. So <math>7^{1947} = 7^{16 \cdot 121 + 11} = (7^{16})^{121} \cdot 7^{11}</math> <math>\equiv 1^{121} \cdot 7^{11} \equiv 7^{11} \pmod{17}</math> But <math>7^2 \equiv -2 \pmod{17}</math>, so <math>7^{11} \equiv (7^2)^5 \cdot 7 \equiv (-2)^5 \cdot 7 \equiv -32 \cdot 7 \equiv 2 \cdot 7 \equiv 14 \pmod{17}</math> Thus, when <math>24^{1947}</math> is divided by 17, the remainder is 14.</p>
6	<p><b>Let <math>p</math> be a prime and <math>a</math> any integer such that <math>p \nmid a</math>. Then prove that <math>a^{p-2}</math> is an inverse of <math>a</math> modulo <math>p</math>.</b> BTL2 By Fermat's little theorem, <math>a^{p-1} \equiv 1 \pmod{p}</math>. That is, <math>a \cdot a^{p-2} \equiv 1 \pmod{p}</math>, so <math>a^{p-2}</math> is an inverse of <math>a</math> modulo <math>p</math></p>

	<b>Solve the linear congruence <math>12x \equiv 6 \pmod{7}</math>. BTL3</b> 12 <sup>5</sup> ≡ 3 (mod 7) is an inverse of 12 modulo 7. Multiply both sides of the congruence by 3: 7 $3(12x) \equiv 3 \cdot 6 \pmod{7}$ $x \equiv 4 \pmod{7}$
8	<b>Verify that 33 is a composite number. BTL2</b> If 33 were a prime, then $2^{33} \equiv 2 \pmod{33}$ . But $2^{33} = (2^5)^6 \cdot 2^3 \equiv (-1)^6 \cdot 8 \equiv 8 \pmod{33}$ $\equiv 2 \pmod{33}$ Therefore, 33 is not a prime. Hence 33 is a composite number.
9	<b>Show that <math>2^{341} \equiv 2 \pmod{341}</math>. BTL2</b> By Fermat's little theorem, $2^{10} \equiv 1 \pmod{11}$ , so $2^{341} = (2^{10})^{34} \cdot 2 \equiv 1^{34} \cdot 2 \equiv 2 \pmod{11}$ . Also, $2^5 \equiv 1 \pmod{31}$ , so $2^{341} = (2^5)^{68} \cdot 2 \equiv 1^{68} \cdot 2 \equiv 2 \pmod{31}$ . Therefore, $2^{341} \equiv 2 \pmod{[11, 31]}$ ; that is, $2^{341} \equiv 2 \pmod{341}$
10	<b>Let <math>m</math> and <math>n</math> be positive integers such that <math>m n</math>. Then Prove that <math>2^m - 1 2^n - 1</math>. BTL2</b> Since $m n$ , $n = km$ for some positive integer $k$ . Then $2^n - 1 = 2^{km} - 1$ $= (2^m - 1)[2^{(k-1)m} + 2^{(k-2)m} + \dots + 2^m + 1]$ Therefore, $2^m - 1 2^n - 1$ .
11	<b>Compute <math>\phi(11)</math> and <math>\phi(18)</math>. BTL3</b> Since 11 is a prime, every positive integer < 11 is relatively prime to 11, so $\phi(11) = 10$ . And there are six positive integers $\leq 18$ and relatively prime to it, namely, 1, 5, 7, 11, 13, and 17. Therefore, $\phi(18) = 6$ .
12	<b>State Euler's Theorem BTL2</b> Let $m$ be a positive integer and $a$ any integer with $(a, m) = 1$ . Then $a^{\phi(m)} \equiv 1 \pmod{m}$ .
13	<b>Find the remainder when <math>245^{1040}</math> is divided by 18. BTL3</b> Since $245 \equiv 11 \pmod{18}$ , $245^{1040} \equiv 11^{1040} \pmod{18}$ . Since $(11, 18) = 1$ , by Euler's theorem, $11^{\phi(18)} \equiv 11^6 \equiv 1 \pmod{18}$ . Therefore, $11^{1040} = (11^6)^{173} \cdot 11^2$ $\equiv 1^{173} \cdot 13 \equiv 13 \pmod{18}$ . Thus, the desired remainder is 13.

14	<p><b>Solve the linear congruence <math>35x \equiv 47 \pmod{24}</math>.</b> BTL3</p> <p>The congruence can be simplified as <math>11x \equiv -1 \pmod{24}</math>. Since <math>(11, 24) = 1</math>,</p> $x \equiv 11^{\phi(24)-1} \cdot (-1) \equiv 11^7 \cdot (-1) \pmod{24}$ $\equiv (11^2)^3 \cdot 11 \cdot (-1) \equiv 1^3 \cdot (-11) \pmod{24} \equiv 13 \pmod{24}$
15	<p><b>Compute <math>\phi(8)</math>, <math>\phi(81)</math>, and <math>\phi(15,625)</math>.</b> BTL3</p> $\phi(8) = \phi(2^3) = 2^3 - 2^2 = 8 - 4 = 4$ $\phi(81) = \phi(3^4) = 3^4 - 3^3 = 54$ $\phi(15,625) = \phi(5^6) = 5^6 - 5^5 = 12,500$
16	<p><b>Verify that <math>\sum_{d 18} \phi(d) = 18</math>.</b> BTL2</p> <p>The positive divisors of 18 are 1, 2, 3, 6, 9, and 18. So</p> $\sum_{d 18} \phi(d) = \phi(1) + \phi(2) + \phi(3) + \phi(6) + \phi(9) + \phi(18) = 1 + 1 + 2 + 2 + 6 + 6 = 18$
17	<p><b>Evaluate <math>\tau(18)</math> and <math>\tau(23)</math>.</b> BTL3</p> <p>The positive divisors of 18 are 1, 2, 3, 6, 9, and 18, so <math>\tau(18) = 6</math>.</p> <p>And 23 being a prime, has exactly two positive divisors, so <math>\tau(23) = 2</math>.</p>
18	<p><b>Evaluate <math>\sigma(12)</math> and <math>\sigma(28)</math>.</b> BTL3</p> <p>The positive divisors of 12 are 1, 2, 3, 4, 6, and 12;  <math>\sigma(12) = 1 + 2 + 3 + 4 + 6 + 12 = 28</math></p> <p>The positive divisors of 28 are 1, 2, 4, 7, 14, and 28;  <math>\sigma(28) = 1 + 2 + 4 + 7 + 14 + 28 = 56</math></p>
19	<p><b>Compute <math>\tau(36)</math> and <math>\sigma(36)</math>.</b> BTL3</p> <p>Since <math>36 = 4 \cdot 9</math>, where <math>(4, 9) = 1</math>,  <math>\tau(36) = \tau(4) \cdot \tau(9) = 3 \cdot 3 = 9</math>  and <math>\sigma(36) = \sigma(4) \cdot \sigma(9) = (1 + 2 + 4)(1 + 3 + 9) = 91</math></p>
20	<p><b>Compute <math>\tau(6120)</math> and <math>\sigma(6120)</math>.</b> BTL3</p> <p>First, we find the canonical decomposition of 6120: <math>6120 = 2^3 \cdot 3^2 \cdot 5 \cdot 17</math>. Therefore,</p> $\tau(6120) = (3 + 1)(2 + 1)(1 + 1)(1 + 1) = 48$ $\sigma(6120) = 15 \cdot 13 \cdot 6 \cdot 18 = 21060$
	<b>Part B</b>
1	<b>State and Prove Wilson's Theorem. (8M)</b> BTL2

	<b>Answer: Refer Page No: 323-Elementary number theory with Applications by Koshy</b> <ul style="list-style-type: none"> <li>Statement :If <math>p</math> is a prime, then <math>(p - 1)! \equiv -1 \pmod{p}</math>. (2M)</li> <li>For Proving <math>(p - 1)! \equiv -1 \pmod{p}</math>. (6M)</li> </ul>
2	<b>Let <math>p</math> be a prime and <math>n</math> any positive integer. Prove that</b> $\frac{np!}{n! p^n} = (-1)^n \pmod{p}$ (8M) BTL2 <b>Answer: Refer Page No: 324-Elementary number theory with Applications by Koshy</b> <ul style="list-style-type: none"> <li><math>a(a + 1) \cdots [a + (p - 2)] \equiv (p - 1)! \equiv -1 \pmod{p}</math>. (4M)</li> <li>For Proving <math>\frac{np!}{n! p^n} = (-1)^n \pmod{p}</math> (4M)</li> </ul>
3	<b>Let <math>p</math> be a prime and <math>a</math> any integer such that <math>p \nmid a</math>. Then prove that the least residues of the integers <math>a, 2a, 3a, \dots, (p - 1)a</math> modulo <math>p</math> are a permutation of the integers <math>1, 2, 3, \dots, (p - 1)</math>. (8M) BTL2</b> <b>Answer: Refer Page No: 327-Elementary number theory with Applications by Koshy</b> <ul style="list-style-type: none"> <li>To show that <math>ia \equiv 0 \pmod{p}</math>, where <math>1 \leq i \leq p - 1</math> (4M)</li> <li>To show that if <math>ia \equiv ja \pmod{p}</math>, where <math>1 \leq i, j \leq p - 1</math> then <math>i = j</math> (4M)</li> </ul>
4	<b>State and Prove Fermat's Little Theorem. (8M) BTL2</b> <b>Answer: Refer Page No: 328-Elementary number theory with Applications by Koshy</b> <ul style="list-style-type: none"> <li>Statement :Let <math>p</math> be a prime and <math>a</math> any integer such that <math>p \nmid a</math>. Then <math>a^{p-1} \equiv 1 \pmod{p}</math> (2M)</li> <li>For Proving <math>a^{p-1} \equiv 1 \pmod{p}</math> (6M)</li> </ul>
5	<b>Let <math>p</math> be a prime and <math>a</math> any positive integer. Then prove that <math>a^p \equiv a \pmod{p}</math>. (8M) BTL2</b> <b>Answer: Refer Page No: 333-Elementary number theory with Applications by Koshy</b> <ul style="list-style-type: none"> <li>Suppose <math>p \nmid a</math> then proving <math>a^{p-1} \equiv 1 \pmod{p}</math>, so <math>a^p \equiv a \pmod{p}</math>. (4M)</li> <li>Suppose <math>p \mid a</math> then proving <math>a^{p-1} \equiv 1 \pmod{p}</math>, so <math>a^p \equiv a \pmod{p}</math>. (4M)</li> </ul>

	<b>If n is an odd pseudo prime, then Prove that N = 2<sup>n</sup> – 1 is also an odd pseudo prime. (8M)</b> BTL2
6	<b>Answer:</b> Refer Page No: 338-Elementary number theory with Applications by Koshy <ul style="list-style-type: none"> <li>• <math>2^{N-1} - 1 = 2^{kn} - 1</math>. (4M)</li> <li>• For Proving <math>2^n - 1</math> is a larger odd pseudo prime (4M)</li> </ul>
7	<b>Prove that There are infinitely many pseudo primes.(8M) BTL2</b> <b>Answer:</b> Refer Page No: 338-Elementary number theory with Applications by Koshy <ul style="list-style-type: none"> <li>• <math>n_{i+1} = 2^{n_i} - 1</math> for <math>i = 0, 1, 2, \dots</math> (4M)</li> <li>• For Proving There are infinitely many pseudo primes (4M)</li> </ul>
8	<b>Prove that A positive integer p is a prime if and only if <math>\phi(p) = p - 1</math>. (8M) BTL2</b> <b>Answer:</b> Refer Page No: 338-Elementary number theory with Applications by Koshy <ul style="list-style-type: none"> <li>• For Proving A positive integer p is a prime (4M)</li> <li>• <math>\phi(p) = p - 1</math> (4M)</li> </ul>
9	<b>State and Prove Euler's Theorem. (8M) BTL2</b> <b>Answer:</b> Refer Page No: 344-Elementary number theory with Applications by Koshy <ul style="list-style-type: none"> <li>• Statement : Let m be a positive integer and a any integer with <math>(a, m) = 1</math>.then  <math display="block">a^{\phi(m)} \equiv 1 \pmod{m}. \quad (2M)</math> </li> <li>• For Proving <math>a^{\phi(m)} \equiv 1 \pmod{m}</math>. (6M)</li> </ul>
10	<b>Let p be a prime and e any positive integer. Then Prove that <math>\phi(p^e) = p^e - p^{e-1}</math> (8M) BTL2</b> <b>Answer:</b> Refer Page No: 356-Elementary number theory with Applications by Koshy <ul style="list-style-type: none"> <li>• <math>\phi(p^e)</math> = number of positive integers <math>\leq p^e</math> and relatively prime to it (4M)</li> <li>• For Proving <math>\phi(p^e) = p^e - p^{e-1}</math> (4M)</li> </ul>
11	<b>Prove that the function <math>\phi</math> is multiplicative. (8M) BTL2</b> <b>Answer:</b> Refer Page No: 360-Elementary number theory with Applications by Koshy <ul style="list-style-type: none"> <li>• Let <math>d = (r, m)</math>. Then <math>d r</math> and <math>d m</math>, so <math>d km</math> (4M)</li> <li>• For Proving <math>\phi</math> is multiplicative (4M)</li> </ul>

**OBJECTIVES:** The student should be made to:

- To understand the protocol layering and physical level communication.
- To analyze the performance of a network.
- To understand the various components required to build different networks.
- To learn the functions of network layer and the various routing protocols.
- To familiarize the functions and protocols of the Transport layer.

**UNIT I INTRODUCTION AND PHYSICAL LAYER**

Networks – Network Types – Protocol Layering – TCP/IP Protocol suite – OSI Model – Physical Layer: Performance – Transmission media – Switching – Circuit-switched Networks – Packet Switching.

9

**UNIT II DATA-LINK LAYER & MEDIA ACCESS**

9

Introduction – Link-Layer Addressing – DLC Services – Data-Link Layer Protocols – HDLC – PPP - Media Access Control - Wired LANs: Ethernet - Wireless LANs – Introduction – IEEE 802.11, Bluetooth – Connecting Devices.

**UNIT III NETWORK LAYER**

9

Network Layer Services – Packet switching – Performance – IPV4 Addresses – Forwarding of IP Packets - Network Layer Protocols: IP, ICMP v4 – Unicast Routing Algorithms – Protocols – Multicasting Basics – IPV6 Addressing – IPV6 Protocol.

**UNIT IV TRANSPORT LAYER**

9

Introduction – Transport Layer Protocols – Services – Port Numbers – User Datagram Protocol – Transmission Control Protocol – SCTP.

**UNIT V APPLICATION LAYER**

9

WWW and HTTP – FTP – Email –Telnet –SSH – DNS – SNMP.

**TOTAL: 45 PERIODS****OUTCOMES:**

**At the end of the course, the student should be able to:**

- Identify the components required to build different types of networks
- Choose the required functionality at each layer for given application
- Identify solution for each functionality at each layer
- Trace the flow of information from one node to another node in the network

**TEXT BOOK:**

1. Behrouz A. Forouzan, Data Communications and Networking, Fifth Edition TMH, 2013.

**UNIT I – INTRODUCTION AND PHYSICAL LAYER**

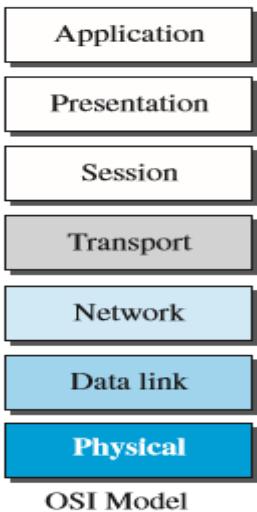
Networks – Network Types – Protocol Layering – TCP/IP Protocol suite – OSI Model – Physical Layer: Performance – Transmission media – Switching – Circuit-switched Networks – Packet Switching

**PART \* A**

<b>Q.No.</b>	<b>Questions</b>
1.	<p><b>Group the OSI layers by function? (NOV/DEC 2013) BTL1</b></p> <p>The seven layers of the OSI model belong to three subgroups. Physical, data link and network layers are the network support layers; they deal with the physical aspects of moving data from one device to another. Session, presentation and application layers are the user support layers; they allow interoperability among unrelated software systems. The transport layer ensures end-to-end reliable data transmission</p>
2	<p><b>What is OSI? BTL1</b></p> <p>A standard that specifies a conceptual model called Open systems Interconnection network interface model, which breaks networked communications into seven layers: Application, Presentation, Session, Transport, Network, Data link, Physical</p>
3	<p><b>Define a layer. NOV/DEC 2013 BTL1</b></p> <p>The ISO defined a common way to connect computers, called the Open Systems Interconnection (OSI) architecture. It defines partitioning of network functionality into seven layers as shown. The bottom three layers, i.e., physical, data link and network are implemented on all nodes on the network including switches</p>
4	<p><b>What is meant by circuit switching? NOV/DEC 2010 BTL1</b></p> <p>Circuit switching is a methodology of implementing a telecommunications network in which two network nodes establish a dedicated communications channel (circuit) through the network before the nodes may communicate. The circuit guarantees the full bandwidth of the channel and remains connected for the duration of the communication session. The circuit functions as if the nodes were physically connected as with an electrical circuit.</p>
5	<p><b>Why protocols needed? BTL1</b></p> <p>In networks, communication occurs between the entities in different systems. Two entities cannot just send bit streams to each other and expect to be understood. For communication, the entities must agree on a protocol. A protocol is a set of rules that govern data communication</p>
6	<p><b>What are the two types of line configuration? BTL1</b></p> <p>Line configuration refers to the way two or more communication devices attached to a link. Line configuration is also referred to as connection. There are two possible types of line configurations or connections.</p> <p>Point-to-point connection and Multipoint connection</p>

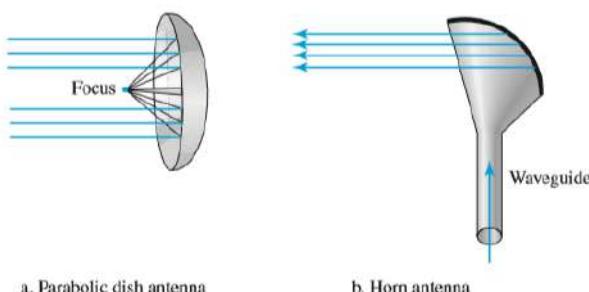
	<b>Differentiate between connection less operation and connection oriented operation</b> BTL1																
7	<table border="1"> <thead> <tr> <th><i>Circuit switching</i></th><th><i>Packet switching</i></th></tr> </thead> <tbody> <tr> <td>Source and destination host are physically connected</td><td>No such physical connection exists</td></tr> <tr> <td>Switching takes place at the physical layer</td><td>Switching takes place at network (datagram) or data link layer (VCN)</td></tr> <tr> <td>Resources such as bandwidth, switch buffer &amp; processing time, are allocated in advance.</td><td>Resources are allocated on demand</td></tr> <tr> <td>Resources remain allocated for the entire duration of data communication.</td><td>Resources can be reallocated when idle.</td></tr> <tr> <td>There is no delay during data transfer.</td><td>Delay exists at each switch during data transfer</td></tr> <tr> <td>Data transferred between the two stations is a continuous flow of signal</td><td>Data is transferred as discrete packets</td></tr> <tr> <td>Example: <i>Telephony</i></td><td>Example: <i>Internet</i></td></tr> </tbody> </table>	<i>Circuit switching</i>	<i>Packet switching</i>	Source and destination host are physically connected	No such physical connection exists	Switching takes place at the physical layer	Switching takes place at network (datagram) or data link layer (VCN)	Resources such as bandwidth, switch buffer & processing time, are allocated in advance.	Resources are allocated on demand	Resources remain allocated for the entire duration of data communication.	Resources can be reallocated when idle.	There is no delay during data transfer.	Delay exists at each switch during data transfer	Data transferred between the two stations is a continuous flow of signal	Data is transferred as discrete packets	Example: <i>Telephony</i>	Example: <i>Internet</i>
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8	<p><b>Distinguish between Packet Switched and Circuit Switched Networks.</b> Apr/May 2017 BTL1</p> <p>Circuit switching consists of a set of switches connected by physical links A connection between two stations is a dedicated path made of one more links Each connection uses only one dedicated channel on each link, Each link is divided into n channels by using TDM or FDM.</p> <p>In a packet-switched network, there is no resource reservation; resources are allocated on demand.</p>																
9	<p><b>Mention the different physical media?</b> BTL1</p> <ul style="list-style-type: none"> <li>• Twisted pair.</li> <li>• Coaxial cable.</li> <li>• Optical fiber.</li> </ul>																
10	<p><b>What are the functions of a DTE? What are the functions of a DCE?</b> BTL1</p> <p>Data terminal equipment is a device that is an information source or an information sink. It is connected to a network through a DCE .Data circuit-terminating equipment is a device used as an interface between a DTE and a network.</p>																
11	<p><b>What are the two interfaces provided by protocols?</b> BTL1</p> <p>Service interface Peer interface</p> <p>Service interface- defines the operations that local objects can perform on the protocol. Peer interface- defines the form and meaning of messages exchanged between protocol peers to implement the communication service</p>																
12	<p><b>Distinguish between peer-to-peer relationship and a primary-secondary relationship.</b> BTL1</p> <p>Peer-to-peer relationship: All the devices share the link equally. Primary-secondary relationship: One device controls traffic and the others must transmit through it.</p>																

13	<b>Define Signals? BTL1</b> Signals are actually electromagnetic waves traveling at the speed of light. The speed of light is, however, medium dependent-electromagnetic waves traveling through copper and fiber do so at about two-thirds the speed of light in vacuum
14	<b>Define flow control? NOV/DEC 2011,APR/MAY 2015 BTL1</b> Flow control refers to a set of procedures used to restrict the amount of data. The sender can send before waiting for acknowledgment.
15	<b>What is mean by data communication? BTL1</b> Data communication is the exchange of data (in the form of 1s and 0s) between two devices via some form of transmission medium (such as a wire cable).
16	<b>What are the three criteria necessary for an effective and efficient network? BTL1</b> The most important criteria are performance, reliability and security. Performance of the network depends on number of users, type of transmission medium, the capabilities of the connected h/w and the efficiency of the s/w. Reliability is measured by frequency of failure, the time it takes a link to recover from the failure and the network's robustness in a catastrophe. Security issues include protecting data from unauthorized access and viruses.
17	<b>What are the three fundamental characteristics determine the effectiveness of the data communication system? BTL1</b> The effectiveness of the data communication system depends on 3 fundamental characters: Delivery: The system must deliver data to the correct destination. Accuracy: The system must deliver data accurately. Timeliness: The system must deliver data in a timely manner.
18	<b>Why are standards needed? BTL1</b> Co-ordination across the nodes of a network is necessary for an efficient communication. If there are no standards, difficulties arise. A standard provides a model or basis for development to which everyone has agreed.
19	<b>For n devices in a network, what is the number of cable links required for a mesh and ring topology? BTL1</b> Mesh topology – $n(n-1)/2$ Ring topology – $n$
20	<b>Assume 6 devices are arranged in a mesh topology. How many cables are needed? How many ports are needed for each device? BTL1</b> Number of cables = $n(n-1)/2 = 6(6-1)/2 = 15$ Number of ports per device = $n-1 = 6-1 = 5$
21	<b>What are the three criteria necessary for an effective and efficient network? BTL2</b> The most important criteria are performance, reliability and security. Performance of the network depends on number of users, type of transmission medium, the capabilities of the connected h/w and the efficiency of the software .Reliability is measured by frequency of failure, the time it takes a link to recover from the failure and the network's robustness
	<b>PART * B</b>
1	<b>Discuss in detail about the layers in OSI model. or Draw the OSI network architecture and explain the functionalities of every layer in detail. (13M) BTL2</b> <b>Answer Page:26- Larry L. Peterson</b> <b>Definition.</b> (2M) ISO defines a common way to connect computer by the architecture called Open System Interconnection (OSI) architecture. Network functionality is divided into seven layers.

<p><b>Architecture</b></p>  <p><b>OSI Model</b></p> <p><b>OSI Layers</b></p> <ol style="list-style-type: none"> <li>1. Physical layer</li> <li>2. Data link layer</li> <li>3. Network layer</li> <li>4. Transport layer</li> <li>5. Session layer</li> <li>6. Presentation layer</li> </ol>	<span style="font-size: 100px;">10<sup>6</sup></span>
<p>(4M)</p> <p>(7M)</p> <p>(1M)</p> <p>(1M)</p> <p>(1M)</p> <p>(1M)</p>	

	<p>The presentation layer is layer 6 of the 7-layer Open Systems Interconnection (OSI) model. It is used to present data to the application layer (layer 7) in an accurate, well-defined and standardized format. The presentation layer is sometimes called the syntax layer.</p> <p><b>7.Application layer</b> (1M)</p> <p>The application layer is a layer in the Open Systems Interconnection (OSI) seven-layer model and in the TCP/IP protocol suite. It consists of protocols that focus on process-to-process communication across an IP network and provides a firm communication interface and end-user services.</p>																		
	<p><b>Explain about TCP/IP architecture or Internet Architecture. (May/June 2015) (13M) BTL2</b></p> <p><b>Answer Page:28- Larry L. Peterson</b></p> <p><b>Definition of TCP</b> (2M)</p> <p><b>Transmission Control Protocol (TCP)</b></p> <p>TCP is one of the main protocols in TCP/IP networks. Whereas the IP protocol deals only with packets, TCP enables two hosts to establish a connection and exchange streams of data.</p> <p><b>Definition of IP</b> (1M)</p> <p>An Internet Protocol address (IP address) is a numerical label assigned to each device connected to a computer network that uses the Internet Protocol for communication. An IP address serves two principal functions: host or network interface identification and location addressing.</p>																		
2	<p><b>Header Format</b> (5M)</p> <table border="1"> <thead> <tr> <th>Packet names</th> <th>Layers</th> <th>Addresses</th> </tr> </thead> <tbody> <tr> <td>Message</td> <td>Application layer</td> <td>Names</td> </tr> <tr> <td>Segment / User datagram</td> <td>Transport layer</td> <td>Port numbers</td> </tr> <tr> <td>Datagram</td> <td>Network layer</td> <td>Logical addresses</td> </tr> <tr> <td>Frame</td> <td>Data-link layer</td> <td>Link-layer addresses</td> </tr> <tr> <td>Bits</td> <td>Physical layer</td> <td></td> </tr> </tbody> </table> <p><b>Explanation &amp;Diagram</b> (3M)</p>	Packet names	Layers	Addresses	Message	Application layer	Names	Segment / User datagram	Transport layer	Port numbers	Datagram	Network layer	Logical addresses	Frame	Data-link layer	Link-layer addresses	Bits	Physical layer	
Packet names	Layers	Addresses																	
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Frame	Data-link layer	Link-layer addresses																	
Bits	Physical layer																		
3.	<p><b>Explain Different types of Networks with neat Architecture (13M)</b></p> <p><b>Answer Page : 208 Behrouz A. Forouzan</b></p> <p><b>Definition of Network</b> (2M)</p>																		

	<p>A network is the interconnection of a set of devices capable of communication. In this definition, a device can be a host (or an end system as it is sometimes called) such as a large computer, desktop, laptop, workstation, cellular phone, or security system</p> <p><b>a).Local Area Network (LAN)</b> (4M)</p> <p>A local area network (LAN) is usually privately owned and connects some hosts in a single office, building, or campus. Depending on the needs of an organization, a LAN can be as simple as two PCs and a printer in someone's home office, or it can extend throughout a company and include audio and video devices. Each host in a LAN has an identifier, an address, that uniquely defines the host in the LAN. A packet sent by a host to another host carries both the source host's and the destination host's addresses.</p> <p><b>b).Wide Area Network (WAN)</b> (4M)</p> <p>A wide area network (WAN) is also an interconnection of devices capable of communication. However, there are some differences between a LAN and a WAN. A LAN is normally limited in size, spanning an office, a building, or a campus; a WAN has a wider geographical span, spanning a town, a state, a country, or even the world. A LAN interconnects hosts; a WAN interconnects connecting devices such as switches, routers, or modems.</p> <p><b>c.) Switching</b> (3M)</p> <p>An internet is a switched network in which a switch connects at least two links together. A switch needs to forward data from a network to another network when required. The two most common types of switched networks are circuit-switched and packet-switched networks. We discuss both next.</p>
4.	<p><b>Briefly Explain different types of Unguided Media with architecture (13M)</b> <b>Answer Page : 197 Behrouz A. Forouzan</b></p> <p><b>Definition.</b> <b>UNGUIDED MEDIA:</b> <b>WIRELESS</b></p> <p>Unguided medium transport electromagnetic waves without using a physical conductor. This type of communication is often referred to as wireless communication. Signals are normally broadcast through free space and thus are available to anyone who has a device capable of receiving them.</p> <p><b>1.Radio Waves</b></p> <p>Electromagnetic waves ranging in frequencies between 3 kHz and 1 GHz are normally called radio waves; waves ranging in frequencies between 1 and 300 GHz are called microwaves. However, the behavior of the waves, rather than the frequencies, is a better criterion for classification. Radio waves, for the most part, are omnidirectional. When an antenna transmits radio waves, they are propagated in all directions. This means that the sending and receiving antennas do not have to be aligned.</p> <p><b>2.Microwaves</b></p> <p>Electromagnetic waves having frequencies between 1 and 300 GHz are called microwaves. Microwaves are unidirectional. When an antenna transmits microwaves, they can be narrowly focused. This means that the sending and receiving antennas need to be aligned. The unidirectional property has an obvious advantage. A pair of antennas can be aligned without interfering with another pair of aligned antennas.</p>

**Figure 7.20 Unidirectional antennas**

a. Parabolic dish antenna

b. Horn antenna

### 3. Infrared

Infrared waves, with frequencies from 300 GHz to 400 THz (wavelengths from 1 mm to 770 nm), can be used for short-range communication. Infrared waves, having high frequencies, cannot penetrate walls. This advantageous characteristic prevents interference between one system and another; a short-range communication system in one room cannot be affected by another system in the next room. When we use our infrared remote control, we do not interfere with the use of the remote by our neighbors.

### Part- C

**Explain Different types of Transmission media with architecture (15M) BTL2**

**Answer Page :186 Behrouz A. Forouzan**

#### Definition

(2M)

Transmission media are actually located below the physical layer and are directly controlled by the physical layer. We could say that transmission media belong to layer zero.

1.

Architecture

(5M)

Sender

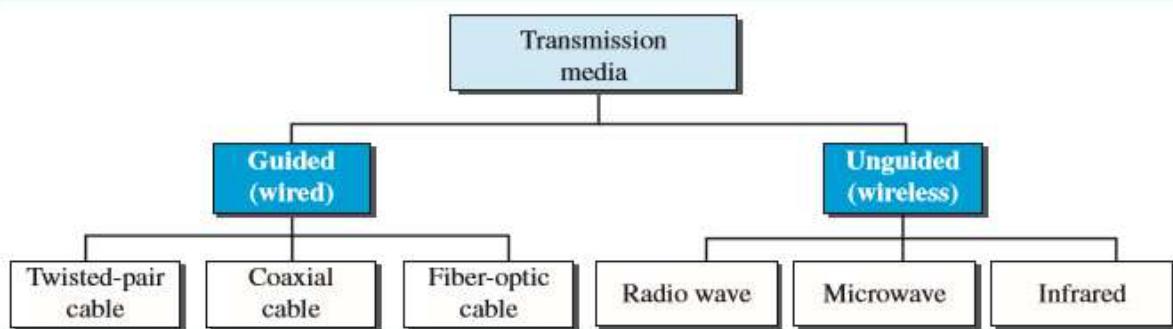
Physical layer

Physical layer

Receiver

Transmission medium

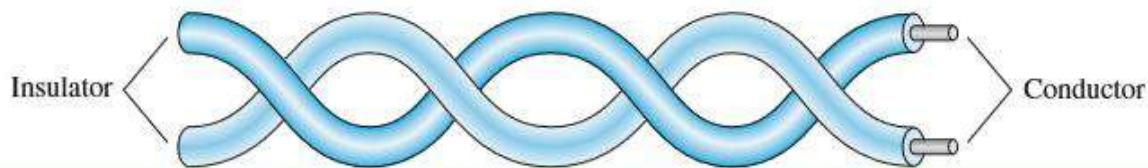
Cable or air

**Figure 7.2** Classes of transmission media**Guided Media**

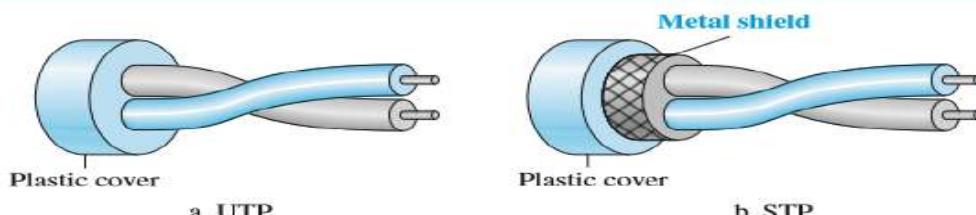
Guided media, which are those that provide a conduit from one device to another, include twisted-pair cable, coaxial cable, and fiber-optic cable. A signal traveling along any of these media is directed and contained by the physical limits of the medium.

**Twisted-Pair Cable**

A twisted pair consists of two conductors (normally copper), each with its own plastic insulation, twisted together, as shown in Figure.

**Figure 7.3** Twisted-pair cable**Unshielded Versus Shielded Twisted-Pair Cable.**

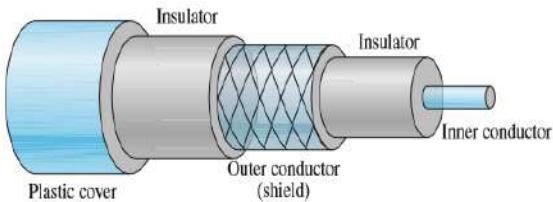
The most common twisted-pair cable used in communications is referred to as unshielded twisted-pair (UTP). IBM has also produced a version of twisted-pair cable for its use, called shielded twisted-pair (STP). STP cable has a metal foil or braided mesh covering that encases each pair of insulated conductors.

**Figure 7.4** UTP and STP cables**Coaxial Cable**

(4M)

Coaxial cable (or coax) carries signals of higher frequency ranges than those in twisted pair cable, in part because the two media are constructed quite differently. Instead of having two wires, coax has a central core conductor of solid or stranded wire (usually copper) enclosed in an insulating sheath, which is, in turn, encased in an outer conductor of metal foil, braid, or a combination of the two.

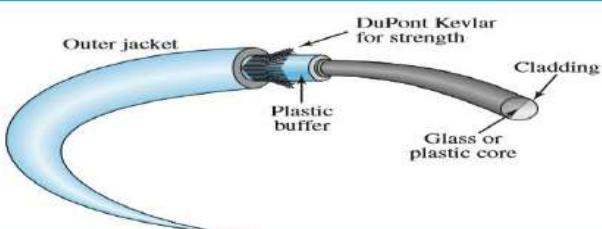
**Figure 7.7 Coaxial cable**



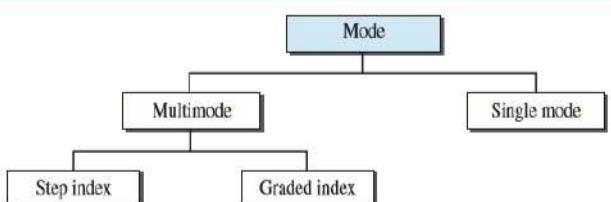
### Fiber-Optic Cable.

A fiber-optic cable is made of glass or plastic and transmits signals in the form of light. To understand optical fiber, we first need to explore several aspects of the nature of light. Light travels in a straight line as long as it is moving through a single uniform substance. If a ray of light traveling through one substance suddenly enters another substance (of a different density), the ray changes direction.

**Figure 7.14 Fiber construction**



**Figure 7.12 Propagation modes**



### Describe Switching concepts with example (15M) BTL2

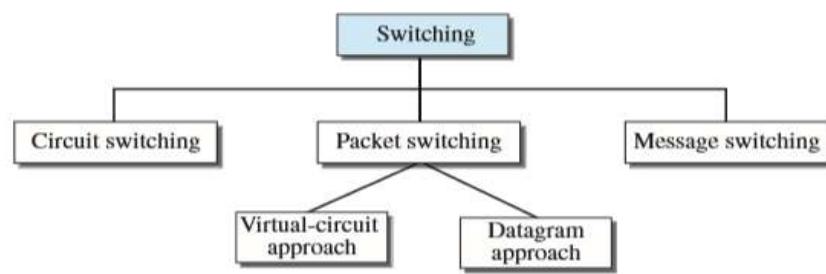
Answer Page : 208 Behrouz A. Forouzan

(2M)

2. Definition  
A switched network consists of a series of interlinked nodes, called switches. Switches are devices capable of creating temporary connections between two or more devices linked to the switch. In a switched network, some of these nodes are connected to the end systems (computers or telephones, for example). Others are used only for routing.

Architecture

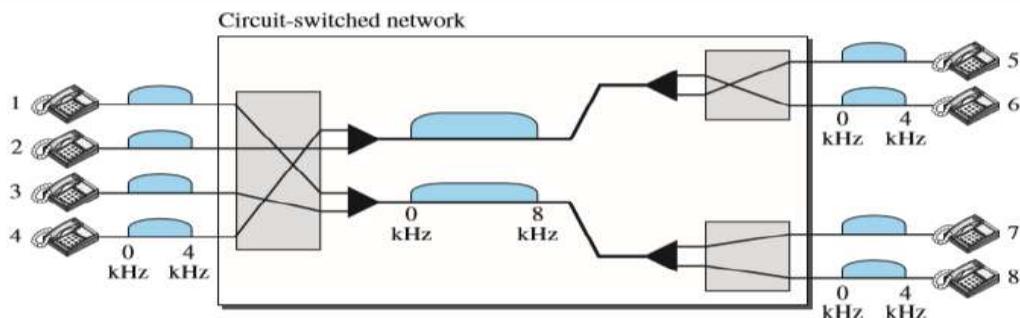
(3M)

**Figure 8.2** Taxonomy of switched networks

### CIRCUIT-SWITCHED NETWORKS.

(4M)

A circuit-switched network consists of a set of switches connected by physical links. A connection between two stations is a dedicated path made of one or more links. However, each connection uses only one dedicated channel on each link. Each link is normally divided into  $n$  channels by using FDM or TDM.

**Figure 8.4** Circuit-switched network used in Example 8.1

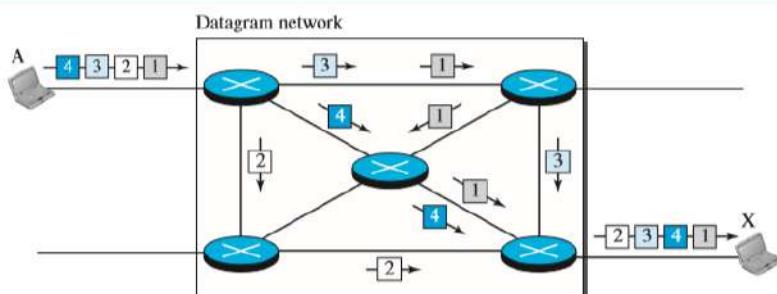
### PACKET SWITCHING

(7M)

In data communications, we need to send messages from one end system to another. If the message is going to pass through a packet-switched network, it needs to be divided into packets of fixed or variable size. The size of the packet is determined by the network and the governing protocol. In packet switching, there is no resource allocation for a packet. This means that there is no reserved bandwidth on the links, and there is no scheduled processing time for each packet. Resources are allocated on demand. The allocation is done on a firstcome, first-served basis. When a switch receives a packet, no matter what the source or destination is, the packet must wait if there are other packets being processed.

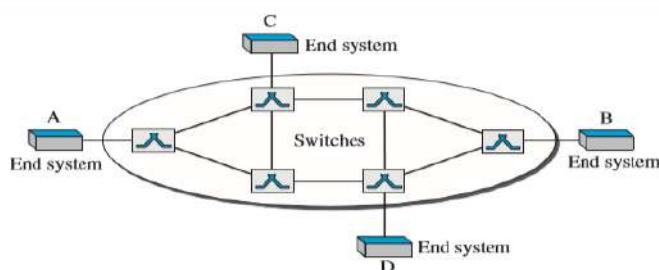
#### Datagram Networks

In a datagram network, each packet is treated independently of all others. Even if a packet is part of a multipacket transmission, the network treats it as though it existed alone. Packets in this approach are referred to as datagrams. Datagram switching is normally done at the network layer. We briefly discuss datagram networks here as a comparison with circuit-switched and virtual-circuit switched networks.

**Figure 8.7** A datagram network with four switches (routers)

### Virtual-Circuit Networks.

A virtual-circuit network is a cross between a circuit-switched network and a datagram network. It has some characteristics of both. A virtual-circuit network is normally implemented in the data-link layer, while a circuit-switched network is implemented in the physical layer and a datagram network in the network layer. But this may change in the future.

**Figure 8.10** Virtual-circuit network

JIT

<b>UNIT II – DATA-LINK LAYER &amp; MEDIA ACCESS</b>	
Introduction – Link-Layer Addressing – DLC Services – Data-Link Layer Protocols – HDLC – PPP - Media Access Control - Wired LANs: Ethernet - Wireless LANs – Introduction – IEEE 802.11, Bluetooth – Connecting Devices.	
<b>PART * A</b>	
Q.No.	Questions
1.	<p><b>What are the functions of MAC? BTL1</b>            MAC sub layer resolves the contention for the shared media. It contains synchronization, flag, flow and error control specifications necessary to move information from one place to another, as well as the physical address of the next station to receive and route a packet.</p>
2	<p><b>What is Ethernet? BTL1</b>            Ethernet is a multiple-access network, meaning that a set of nodes send and receive frames over a shared link.</p>
3	<p><b>List out advantages of Ethernet.BTL1</b>            1.Inexpensive 2.Easy to install 3.Supports various writing technologies.</p>
4	<p><b>What do you mean by ARP? BTL1</b>            ARP stands for Address resolution protocol, maps an IP address to a MAC address</p>
5	<p><b>What do you mean by RARP? BTL1</b>            RARP stands for Reverse Address resolution protocol, maps an MAC address to a IP address.</p>
6	<p><b>Define Tree Traversal and Mention the different binary tree traversal techniques. BTL1</b>            Tree Traversal is an operation which can be performed on a binary tree is visiting all the nodes exactly once.           <ul style="list-style-type: none"> <li>• Inorder: traversing the LST, visiting the root and finally traversing the RST.</li> <li>• Preorder: visiting root, traversing LST and finally traversing RST.</li> <li>• Post- order: traversing LST, then RST and finally visiting root.</li> </ul> </p>
7	<p><b>Contrast fast Ethernet and gigabit ethernet? NOV/DEC 2012 BTL1</b>            Fast Ethernet cards connect to networks at a rate of 100 Mbps while Gigabit network cards can connect at speeds up to 1000mb/s. The main difference between the two is speed. A fast Ethernet card can run on bandwidths at 100mb/s while a gigabit Ethernet can run at ten times that speed. However, the existence of FDDIs around made this technology more like a stepping stone to something better – enter the gigabit card. Gigabit networks are made to run the best at Layer 3 switching meaning it has more route functionality than the 100mbps fast Ethernet. Gigabit Ethernet is backwards compatible meaning that it will support all current applications and requires a minimum of new learning. This goes just the same with the fast Ethernet, fast Ethernet can use 10/100 Mbps and gigabit can run on networks 10/100/1000 Mbps. Hence both cards are basically the same using the same technology except the gigabit card can run on 1000mb/s, an astonishing speed.</p>
8	<p><b>What are the four prominent wireless technologies? BTL1</b></p> <ul style="list-style-type: none"> <li>• Bluetooth</li> <li>• Wi-Fi(formally known as 802.11)</li> </ul>

	<ul style="list-style-type: none"> <li>• WiMAX(802.16)</li> <li>• Third generation or 3G cellular wireless</li> </ul>
9	<b>What do you mean by framing? NOV/DEC 2013 BTL1</b> A frame consists of one complete cycle of time slots, including one or more slot dedicated to each sending device
10	<b>What is the difference between port address, logical address and physical address? M/J 2014 BTL1</b> A physical address is like your hard drive to your computer. A logical address is like a file on the server, with information or instructions that lead to it. A port address is an address assigned by the CPU (0xFFFF) that can be accessed for I/O read/write like RAM
11	<b>What are the functions of LLC? BTL1</b> The IEEE project 802 models take the structure of an HDLC frame and divides it into 2 sets of functions. One set contains the end user portion of the HDLC frame – the logical address, control information, and data. These functions are handled by the IEEE 802.2 logical link control (LLC) protocol.
12	<b>Why Ethernet is said to be a I-persistent protocol? BTL1</b> An adaptor with a frame to send transmits with probability „1 „, whenever a busy line goes idle.
13	<b>How to mediate access to a shared link? BTL1</b> Ethernet, token ring, and several wireless protocols. Ethernet and token ring media access protocols have no central arbitrator of access. Media access in wireless networks is made more complicated by the fact that some nodes may be hidden from each other due to range limitations of radio transmission.
14	<b>Show the Ethernet Frame Format. Nov/Dec 17 BTL1</b> Ethernet is a multiple-access network, meaning that a set of nodes send and receive frames over a shared link. An Ethernet frame is preceded by a preamble and start frame delimiter (SFD), which are both part of the Ethernet packet at the physical layer. Each Ethernet frame starts with an Ethernet header, which contains destination and source MAC addresses as its first two fields. The middle section of the frame is payload data including any headers for other protocols (for example, Internet Protocol) carried in the frame. The frame ends with a frame check sequence (FCS), which is a 32-bit cyclic redundancy check used to detect any in-transit corruption of data
15	<b>What are the ways to address the framing problem? BTL1</b> <ul style="list-style-type: none"> <li>• Byte-Oriented Protocols(PPP)</li> <li>• Bit-Oriented Protocols(HDLC)</li> <li>• Clock-Based Framing (SONET).</li> </ul>
16	<b>What are the responsibilities of data link layer? BTL1</b> Specific responsibilities of data link layer include the following. a) Framing b) Physical addressing c) Flow control d) Error control e) Access control
17	<b>Mention the types of errors. BTL1</b>

	There are 2 types of errors a) Single-bit error. b) Burst-bit error.																												
18	<b>What is redundancy?</b> BTL1 It is the error detecting mechanism, which means a shorter group of bits or extra bits may be appended at the destination of each unit.																												
19	<b>What is selective reject ARQ?</b> BTL1 In selective reject ARQ only the specific damaged or lost frame is retransmitted. If a frame is corrupted in transit, a NAK is returned and the frame is resent out of sequence.																												
20	<b>List the types of stations in HDLC.</b> BTL1 HDLC differentiates between 3 types of stations. a) Primary b) Secondary c) Combined																												
21	<b>What is the access method used by wireless LAN?</b> BTL2 The access method used by wireless LAN is Carrier Sense Multiple Access with Collision Avoidance (CSMA/CA)																												
	<b>PART – B</b>																												
	<b>Write short notes on ARP. Or Explain in detail ARP. (13M) BTL 2</b> <b>Answer Page : 245 Behrouz A. Forouzan</b>																												
	<b>Definition of ARP</b> (3M) <b>ARP:</b> Associates an IP address with physical address. It is used to find the physical address of the node when its Internet address is known. Any time a host/router needs to find the physical address of another host on its network, it formats an ARP query packet that includes the IP address and broadcasts it																												
	<b>Packet Header Format ARP</b> (5M)																												
1	<p><b>Figure 9.8 ARP packet</b></p> <table border="1"> <tr> <td>0</td> <td>8</td> <td>16</td> <td>31</td> </tr> <tr> <td colspan="2">Hardware Type</td> <td colspan="2">Protocol Type</td> </tr> <tr> <td>Hardware length</td> <td>Protocol length</td> <td colspan="2">Operation Request:1, Reply:2</td> </tr> <tr> <td colspan="4">Source hardware address</td> </tr> <tr> <td colspan="4">Source protocol address</td> </tr> <tr> <td colspan="4">Destination hardware address (Empty in request)</td> </tr> <tr> <td colspan="4">Destination protocol address</td> </tr> </table>	0	8	16	31	Hardware Type		Protocol Type		Hardware length	Protocol length	Operation Request:1, Reply:2		Source hardware address				Source protocol address				Destination hardware address (Empty in request)				Destination protocol address			
0	8	16	31																										
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Source hardware address																													
Source protocol address																													
Destination hardware address (Empty in request)																													
Destination protocol address																													
	<b>Explanation</b> (5M)																												
2	<b>Explain DLC Services in detail. (13M) BTL 2</b> <b>Answer Page:294- Behrouz A. Forouzan</b> <p><b>Definition</b> (2M)</p> <p>The data link control (DLC) deals with procedures for communication between two adjacent nodes—node-to-node communication—no matter whether the link is dedicated or broadcast. Data link control functions include framing and flow and error control.</p>																												

	<p><b>Framing</b> (2M)</p> <p>Data transmission in the physical layer means moving bits in the form of a signal from the source to the destination. The physical layer provides bit synchronization to ensure that the sender and receiver use the same bit durations and timing.</p> <p><b>Character-Oriented Framing.</b> (2M)</p> <p>In character-oriented (or byte-oriented) framing, data to be carried are 8-bit characters from a coding system such as ASCII (see Appendix A). The header, which normally carries the source and destination addresses and other control information, and the trailer, which carries error detection redundant bits, are also multiples of 8 bits.</p> <p><b>Flow and Error Control</b> (4M)</p> <p>One of the responsibilities of the data-link control sublayer is flow and error control at the data-link layer. Flow Control Whenever an entity produces items and another entity consumes them, there should be a balance between production and consumption rates. If the items are produced faster than they can be consumed, the consumer can be overwhelmed and may need to discard some items. If the items are produced more slowly than they can be consumed, the consumer must wait, and the system becomes less efficient.</p>
3	<p><b>Figure 11.5 Flow control at the data-link layer</b></p> <pre> graph LR     subgraph Sending_node [ ]         direction TB         S_DL[Data-link layer] --- S_P[Producer]     end     subgraph Receiving_node [ ]         direction TB         R_DL[Data-link layer] --- R_P[Producer]     end     S_P -- "Frames are pushed" --&gt; R_P     R_P -- "Flow control" --&gt; R_DL </pre> <p><b>Error Control</b></p> <p>Since the underlying technology at the physical layer is not fully reliable, we need to implement error control at the data-link layer to prevent the receiving node from delivering corrupted packets to its network layer. Error control at the data-link layer is normally very simple and implemented using one of the following two methods. In both methods, a CRC is added to the frame header by the sender and checked by the receiver.</p> <p><b>Connectionless and Connection-Oriented</b> (3M)</p> <p><b>Connectionless Protocol.</b></p> <p>In a connectionless protocol, frames are sent from one node to the next without any relationship between the frames; each frame is independent. Note that the term connectionless here does not mean that there is no physical connection (transmission medium) between the nodes; it means that there is no connection between frames.</p> <p><b>Connection-Oriented Protocol.</b></p> <p>In a connection-oriented protocol, a logical connection should first be established between the two nodes (setup phase). After all frames that are somehow related to each other are transmitted (transfer phase), the logical connection is terminated (teardown phase). In this type of communication, the frames are numbered and sent in order.</p>

	<p><b>Definition</b> (3M)</p> <p>Traditionally four protocols have been defined for the data-link layer to deal with flow and error control: Simple, Stop-and-Wait, Go-Back-N, and Selective-Repeat. Although the first two protocols still are used at the data-link layer, the last two have disappeared.</p> <p><b>Simple Protocol</b> (5M)</p> <p>Our first protocol is a simple protocol with neither flow nor error control. We assume that the receiver can immediately handle any frame it receives. In other words, the receiver can never be overwhelmed with incoming frames.</p>
	<p><b>Figure 11.7 Simple protocol</b></p> <p>The diagram illustrates the Simple protocol. It shows two nodes: a 'Sending node' on the left and a 'Receiving node' on the right. Each node has a stack of three layers: Network, Data-link, and Physical. A horizontal line labeled 'Logical link' connects the Data-link layers of both nodes. A single blue bar labeled 'Frame' is shown moving from the Physical layer of the Sending node to the Physical layer of the Receiving node. Arrows indicate the flow of frames between the Physical layers.</p>
	<p><b>Stop-and-Wait Protocol</b> (5M)</p> <p>Our second protocol is called the Stop-and-Wait protocol, which uses both flow and error control. In this protocol, the sender sends one frame at a time and waits for an acknowledgment before sending the next one. To detect corrupted frames, we need to add a CRC to each data frame. When a frame arrives at the receiver site, it is checked. If its CRC is incorrect, the frame is corrupted and silently discarded. The silence of the receiver is a signal for the sender that a frame was either corrupted or lost. Every time the sender sends a frame, it starts a timer.</p>
4	<p><b>Figure 11.10 Stop-and-Wait protocol</b></p> <p>The diagram illustrates the Stop-and-Wait protocol. It shows two nodes: a 'Sending node' on the left and a 'Receiving node' on the right. The 'Logical link (duplex)' is shown as a double-headed arrow between their Data-link layers.    - The 'Frame' is sent from the Sending node's Data-link layer to the Receiving node's Data-link layer. The frame is divided into three parts: a header, a payload, and a 'CRC' (Cyclic Redundancy Check).   - An 'ACK' (Acknowledgment) is sent back from the Receiving node's Data-link layer to the Sending node's Data-link layer. Like the frame, it also has a header, payload, and a 'CRC'.   - A small circle with a timer symbol is shown below the Sending node's Data-link layer, indicating that a timer is active while waiting for the ACK.</p>

### Piggybacking

Protocols have been designed in the past to allow data to flow in both directions. However, to make the communication more efficient, the data in one direction is piggybacked with the acknowledgment in the other direction. In other words, when node A is sending data to node B, Node A also acknowledges the data received from node B.

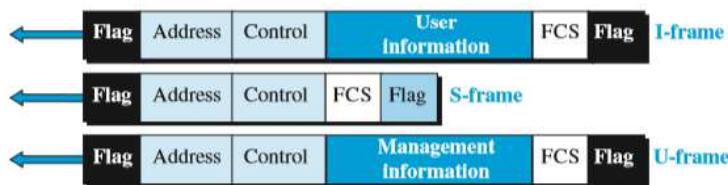
### Explain in detail about HDLC and PPP. (13M) (Nov/Dec 2015) BTL2

#### Answer Page:304- Behrouz A. Forouzan

##### Definition for HDLC (3M)

High-level Data Link Control (HDLC) is a bit-oriented protocol for communication over point-to-point and multipoint links. It implements the Stop-and-Wait protocol we discussed earlier. Although this protocol is more a theoretical issue than practical, most of the concept defined in this protocol is the basis for other practical protocols such as PPP.

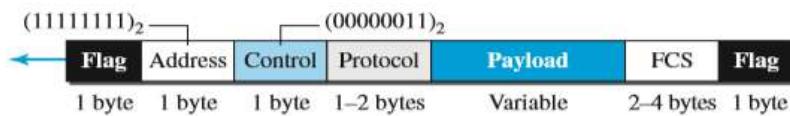
##### Packet Header Format (3M)

**Figure 11.16 HDLC frames****POINT-TO-POINT PROTOCOL (PPP)**

One of the most common protocols for point-to-point access is the Point-to-Point Protocol (PPP). Today, millions of Internet users who need to connect their home computers to the server of an Internet service provider use PPP. The majority of these users have a traditional modem; they are connected to the Internet through a telephone line, which provides the services of the physical layer.

**Services Provided by PPP**

PPP defines the format of the frame to be exchanged between devices. It also defines how two devices can negotiate the establishment of the link and the exchange of data. PPP is designed to accept payloads from several network layers (not only IP). Authentication is also provided in the protocol, but it is optional. The new version of PPP, called Multilink PPP, provides connections over multiple links.

**Figure 11.20 PPP frame format**

**Explain how CSMA work with bandwidth allocation and Access methods. (13M) BTL2**

**Answer Page:331- Behrouz A. Forouzan**

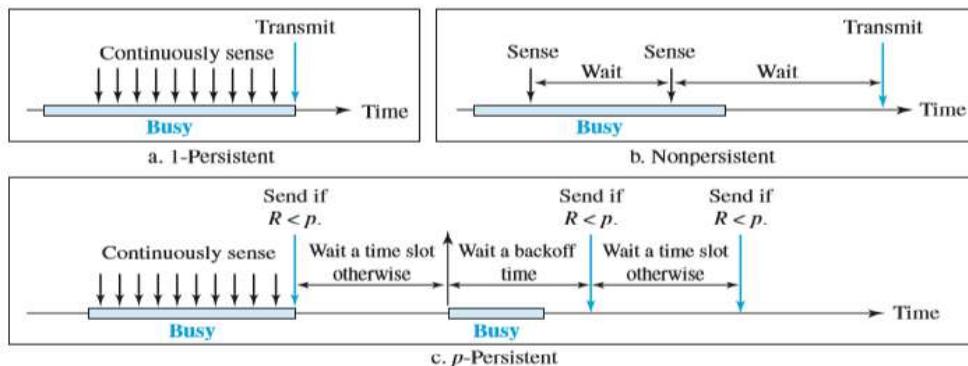
**Definition CSMA**

The chance of collision can be reduced if a station senses the medium before trying to use it. Carrier sense multiple access (CSMA) requires that each station first listen to the medium (or check the state of the medium) before sending.

**Persistence Methods****Architecture**

(4M)

5

**Figure 12.9 Behavior of three persistence methods****1-Persistent**

The 1-persistent method is simple and straightforward. In this method, after the station finds the line idle, it sends its frame immediately (with probability 1). This method has the highest chance of collision because two or more stations may find the line idle and send their frames immediately. (2M)

In the nonpersistent method, a station that has a frame to send senses the line. If the line is idle, it sends immediately. If the line is not idle, it waits a random amount of time and then senses the line again. The nonpersistent approach reduces the chance of collision because it is unlikely that two or more stations will wait the same amount of time and retry to send simultaneously. (2M)

**p-Persistent.**

The p-persistent method is used if the channel has time slots with a slot duration equal to or greater than the maximum propagation time. The p-persistent approach combines the advantages of the other two strategies. It reduces the chance of collision and improves efficiency. (2M)

**How CSMA / CD method working for collision techniques(13M) BTL2**

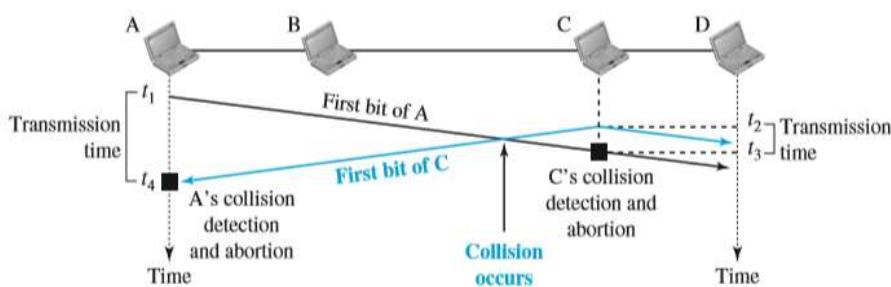
**Answer Page: 334- Behrouz A. Forouzan**

**Definition**

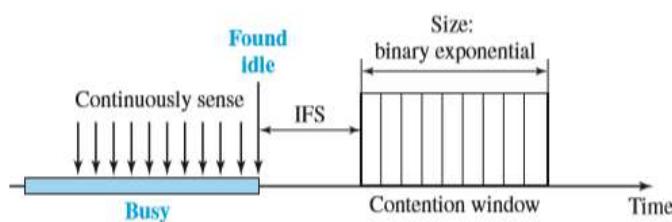
(2M)

Carrier sense multiple access with collision detection (CSMA/CD) augments the algorithm to handle the collision. In this method, a station monitors the medium after it sends a frame to see if the transmission was successful. If so, the station is finished. If, however, there is a collision, the frame is sent again. (3M)

**Architecture**

**Figure 12.11 Collision of the first bits in CSMA/CD****CSMA/CA**

Carrier sense multiple access with collision avoidance (CSMA/CA) was invented for wireless networks. Collisions are avoided through the use of CSMA/CA's three strategies: the interframe space, the contention window, and acknowledgments, as shown in Figure.

**Figure 12.16 Contention window****Contention Window.**

(4M)

The contention window is an amount of time divided into slots. A station that is ready to send chooses a random number of slots as its wait time. The number of slots in the window changes according to the binary exponential back off strategy. This means that it is set to one slot the first time and then doubles each time the station cannot detect an idle channel after the IFS time.

**Hidden-Station Problem.**

The solution to the hidden station problem is the use of the handshake frames (RTS and CTS). It also shows that the RTS message from B reaches A, but not C. However, because both B and C are within the range of A, the CTS message, which contains the duration of data transmission from B to A, reaches C. Station C knows that some hidden station is using the channel and refrains from transmitting until that duration is over.

**PART \*C**

- |   |  |
|---|--|
| 1 | <b>Explain different Evolution of Ethernet with neat architecture.(15M) BTL2</b> |
|---|--|

**Answer Page: 364- Behrouz A. Forouzan**

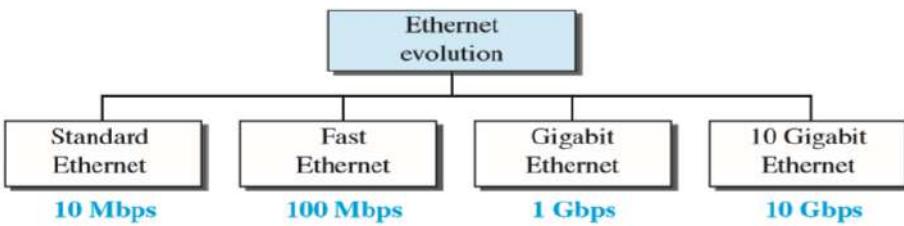
(2M)

**Definition**

The Ethernet LAN was developed in the 1970s by Robert Metcalfe and David Boggs. Since then, it has gone through four generations: Standard Ethernet (10 Mbps), Fast Ethernet (100 Mbps), Gigabit Ethernet (1 Gbps), and 10 Gigabit Ethernet (10 Gbps).

**Architecture**

(3M)

**1. Standard Ethernet.**

(3M)

Ethernet provides a connectionless service, which means each frame sent is independent of the previous or next frame. Ethernet has no connection establishment or connection termination phases. The sender sends a frame whenever it has it; the receiver may or may not be ready for it. The sender may overwhelm the receiver with frames, which may result in dropping frames. If a frame drops, the sender will not know about it. Since IP, which is using the service of Ethernet, is also connectionless, it will not know about it either. If the transport layer is also a connectionless protocol, such as UDP, the frame is lost and salvation may only come from the application layer.

**2. Fast Ethernet (100MBPS)**

(3M)

In the 1990s, some LAN technologies with transmission rates higher than 10 Mbps, such as FDDI and Fiber Channel, appeared on the market. If the Standard Ethernet wanted to survive, it had to compete with these technologies. Ethernet made a big jump by increasing the transmission rate to 100 Mbps, and the new generation was called the Fast Ethernet. The designers of the Fast Ethernet needed to make it compatible with the Standard Ethernet. The MAC sublayer was left unchanged, which meant the frame format and the maximum and minimum size could also remain unchanged.

**3. Gigabit Ethernet (1GBPS)**

(3M)

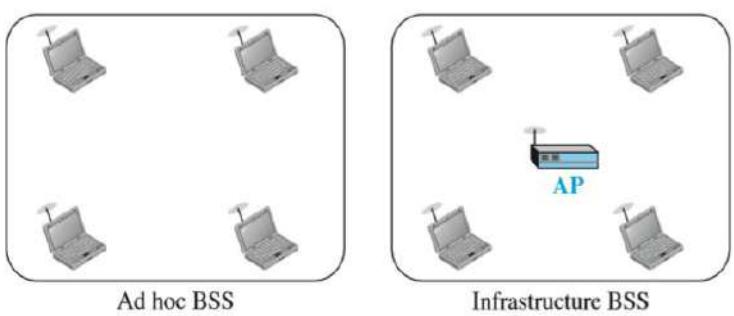
The need for an even higher data rate resulted in the design of the Gigabit Ethernet Protocol (1000 Mbps). The IEEE committee calls it the Standard 802.3z. The goals of the Gigabit Ethernet were to upgrade the data rate to 1 Gbps, but keep the address length, the frame format, and the maximum and minimum frame length the same. The goals of the Gigabit Ethernet design can be summarized as follows:

1. Upgrade the data rate to 1 Gbps.
2. Make it compatible with Standard or Fast Ethernet.
3. Use the same 48-bit address.
4. Use the same frame format.
5. Keep the same minimum and maximum frame lengths.
6. Support auto negotiation as defined in Fast Ethernet.

**4. 10 Gigabit Ethernet**

(2M)

The IEEE committee created 10 Gigabit Ethernet and called it Standard 802.3ae. The goals of the 10 Gigabit Ethernet design can be summarized as upgrading the data rate to 10 Gbps, keeping the same frame size and format, and allowing the interconnection of LANs, MANs, and WAN possible.

	<p>This data rate is possible only with fiber-optic technology at this time. The standard defines two types of physical layers: LAN PHY and WAN PHY.</p>
	<p><b>Briefly explain how Ethernet IEEE802.11 work in current Technologies.(15M) BTL2</b>  <b>Answer :Page- 439 Behrouz A. Forouzan</b>  <b>Definition (2M)</b>          IEEE has defined the specifications for a wireless LAN, called IEEE 802.11, which covers the physical and data-link layers. It is sometimes called wireless Ethernet. In some countries, including the United States, the public uses the term WiFi (short for wireless fidelity) as a synonym for wireless LAN.  <b>Basic Service Set.</b>          IEEE 802.11 defines the basic service set (BSS) as the building blocks of a wireless LAN. A basic service set is made of stationary or mobile wireless stations and an optional central base station, known as the access point (AP).</p> 
2	<p><b>Extended Service Set</b>          An extended service set (ESS) is made up of two or more BSSs with APs. In this case, the BSSs are connected through a distribution system, which is a wired or a wireless network. The distribution system connects the APs in the BSSs. IEEE 802.11 does not restrict the distribution system; it can be any IEEE LAN such as an Ethernet. Note that the extended service set uses two types of stations: mobile and stationary. The mobile stations are normal stations inside a BSS.</p> <p><b>Collision During Handshaking</b>          What happens if there is a collision during the time when RTS or CTS control frames are in transition, often called the handshaking period? Two or more stations may try to send RTS frames at the same time. These control frames may collide. However, because there is no mechanism for collision detection, the sender assumes there has been a collision if it has not received a CTS frame from the receiver. The backoff strategy is employed, and the sender tries again.</p> <p><b>Hidden-Station Problem</b>          The solution to the hidden station problem is the use of the handshake frames (RTS and CTS). The RTS message from B reaches A, but not C. However, because both B and C are within the range of A, the CTS message, which contains the duration of data transmission from B to A, reaches C. Station C knows that some hidden station is using the channel and refrains from transmitting until that duration is over.</p> <p><b>Write the Features of Bluetooth architecture with example.</b></p>

**Definition :**

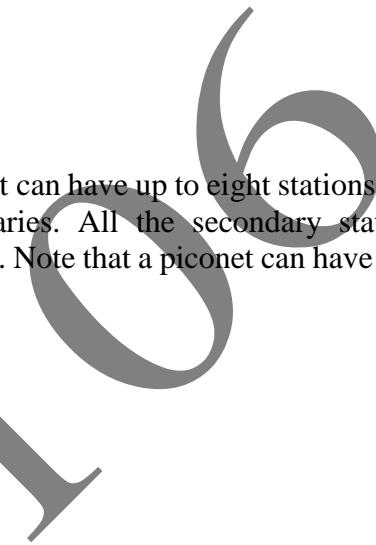
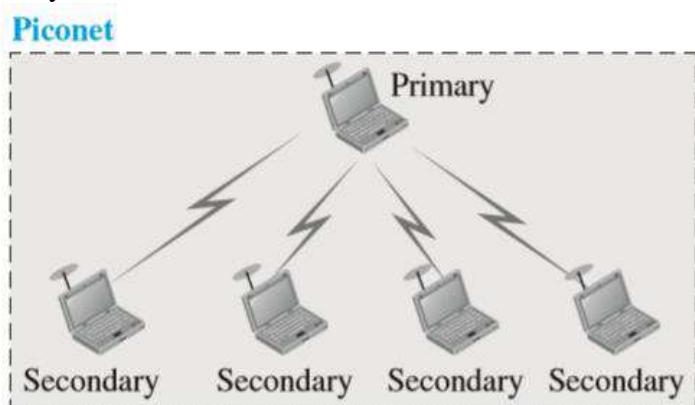
Bluetooth is a wireless LAN technology designed to connect devices of different functions such as telephones, notebooks, computers (desktop and laptop), cameras, printers, and even coffee makers when they are at a short distance from each other. A Bluetooth LAN is an ad hoc network, which means that the network is formed spontaneously; the devices, sometimes called gadgets, find each other and make a network called a piconet.

**Architecture**

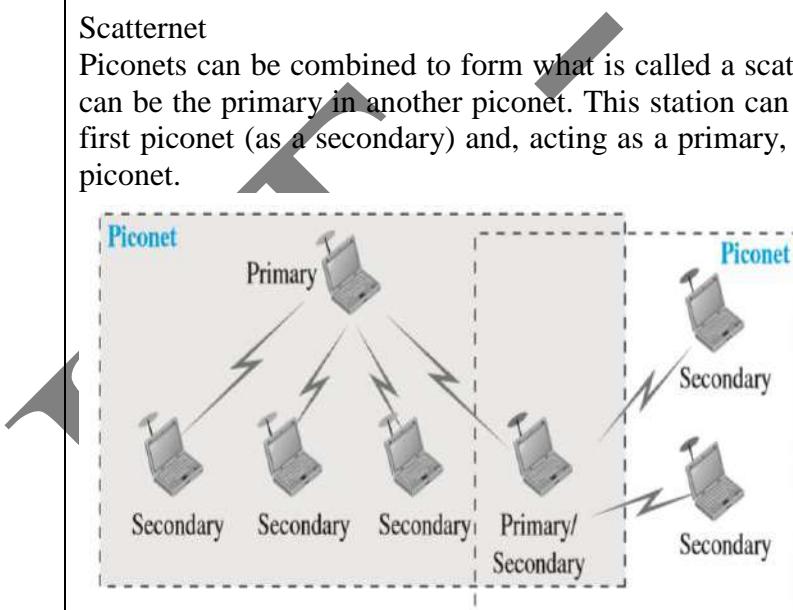
Bluetooth defines two types of networks: piconet and scatternet.

**Piconets**

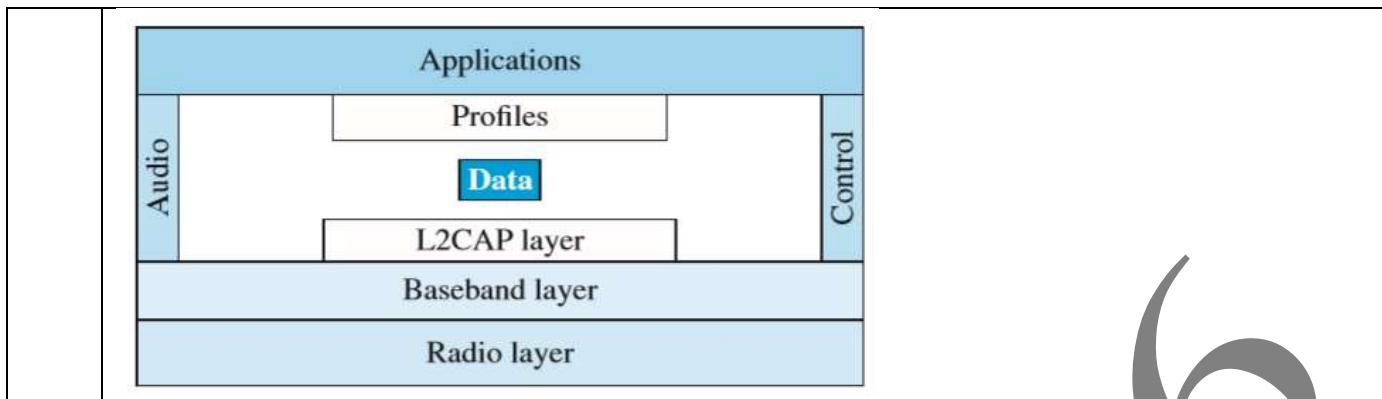
A Bluetooth network is called a piconet, or a small net. A piconet can have up to eight stations, one of which is called the primary; the rest are called secondaries. All the secondary stations synchronize their clocks and hopping sequence with the primary. Note that a piconet can have only one primary station.

**Scatternet**

Piconets can be combined to form what is called a scatternet. A secondary station in one piconet can be the primary in another piconet. This station can receive messages from the primary in the first piconet (as a secondary) and, acting as a primary, deliver them to secondaries in the second piconet.

**Bluetooth Layers**

**L2CAP** The Logical Link Control and Adaptation Protocol, or L2CAP (L2 here means LL), is roughly equivalent to the LLC sublayer in LANs. It is used for data exchange on an ACL link; SCO channels do not use L2CAP.



JIT - 2106

**UNIT III – NETWORK LAYER**

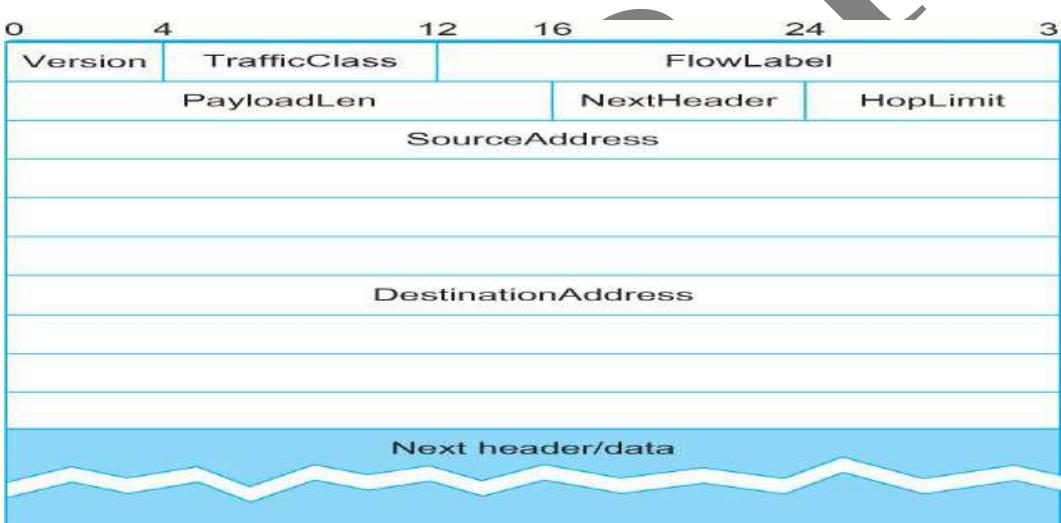
Network Layer Services – Packet switching – Performance – IPV4 Addresses – Forwarding of IP Packets - Network Layer Protocols: IP, ICMP v4 – Unicast Routing Algorithms – Protocols – Multicasting Basics – IPV6 Addressing – IPV6 Protocol.

**PART \* A**

<b>Q.No.</b>	<b>Questions</b>
1.	<b>Define Routing? BTL1</b> Routing is a process that takes place in the background so that, when a data packet turns up, we will have the right information in the forwarding table to be able to forward, or switch, the packet
2	<b>Write on the packet cost referred in distance vector and link state routing. (Apr/May 2012)</b> <b>BTL1</b> In distance vector routing, cost refer to hop count while in case of link state routing, cost is a weighted value based on a variety of factors such as security levels, traffic or the state of the link.
3	<b>What is source routing? (Nov/Dec 2013) BTL1</b> Source routing, also called path addressing, allows a sender of a packet to partially or completely specify the route the packet takes through the network
4	<b>What is subnetting? (Nov/Dec 2011) BTL1</b> Subnetting provides an elegantly simple way to reduce the total number of network numbers that are assigned. The idea is to take a single IP network number and allocate the IP address with that network to several physical networks, which are now referred to as subnets
5	<b>Explain IPV6 protocol. BTL1</b> IPv6 (Internet Protocol version 6) is a set of basics of IPv6 are similar to those of IPv4. The most obvious improvement in IPv6 over IPv4 is that IP addresses are lengthened from 32 bits to 128 bits. This extension anticipates considerable future growth of the Internet and provides relief for what was perceived as an impending shortage of network addresses. IPv6 also supports auto-configuration to help correct most of the shortcomings in version 4, and it has integrated security and mobility features
6	<b>Explain Multicast routing? BTL1</b> Multicast IP Routing protocols are used to distribute data (for example, audio/video streaming broadcasts) to multiple recipients. Using multicast, a source can send a single copy of data to a single multicast address, which is then distributed to an entire group of recipients
7	<b>What is PIM? BTL1</b> Protocol-Independent Multicast (PIM) is a family of multicast routing protocols for Internet Protocol (IP) networks that provide one-to-many and many-to-many distribution of data over a LAN, WAN or the Internet. It is termed <i>protocol-independent</i> because PIM does not include its own topology discovery mechanism, but instead uses routing information supplied by other routing protocols. There are four variants of PIM: <ul style="list-style-type: none"> <li>• PIM Source-Specific Multicast</li> <li>• Bidirectional PIM</li> </ul>

	<ul style="list-style-type: none"> <li>• PIM Dense Mode</li> <li>• PIM Sparse Mode</li> </ul>						
8	<p><b>What is DVMRP? BTL1</b></p> <p>The Distance Vector Multicast Routing Protocol (DVMRP), is a routing protocol used to share information between routers to facilitate the transportation of IP multicast packets among networks. The protocol is based on the RIP protocol. The router generates a routing table with the multicast group of which it has knowledge with corresponding distances. When a multicast packet is received by a router, it is forwarded by the router's interfaces specified in the routing table</p>						
9	<p><b>Explain IPV4 protocol. BTL1</b></p> <p>IPv4 (Internet Protocol Version 4) is the fourth revision of the Internet Protocol (IP) used to identify devices on a network through an addressing system. The Internet Protocol is designed for use in interconnected systems of packet-switched computer communication networks. IPv4 is the most widely deployed Internet protocol used to connect devices to the Internet. IPv4 uses a 32-bit address scheme</p>						
10	<p><b>What are the differences between IPV4 and IPV6? BTL1</b></p> <table border="1"> <thead> <tr> <th>IPV4</th> <th>IPV6</th> </tr> </thead> <tbody> <tr> <td>A 32-bit numeric address in IPv4 is written in decimal as four numbers separated by periods. Each number can be zero to 255.</td> <td>IPv6 addresses are 128-bit IP address written in hexadecimal and separated by colons.</td> </tr> <tr> <td>For example, 1.160.10.240 could be an IP address.</td> <td>An example IPv6 address could be written like this: 3ffe:1900:4545:3:200:f8ff:fe21:67cf</td> </tr> </tbody> </table>	IPV4	IPV6	A 32-bit numeric address in IPv4 is written in decimal as four numbers separated by periods. Each number can be zero to 255.	IPv6 addresses are 128-bit IP address written in hexadecimal and separated by colons.	For example, 1.160.10.240 could be an IP address.	An example IPv6 address could be written like this: 3ffe:1900:4545:3:200:f8ff:fe21:67cf
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For example, 1.160.10.240 could be an IP address.	An example IPv6 address could be written like this: 3ffe:1900:4545:3:200:f8ff:fe21:67cf						
11	<p><b>What is IP addressing? BTL1</b></p> <p>An IP address is a numerical label assigned to each device in a computer network that uses internet protocol for communication.</p> <p>Two important functions at IP address</p> <ul style="list-style-type: none"> <li>• Host identification</li> <li>• Location addressing</li> </ul>						
12	<p><b>Why is IPV4 to IPV6 transition required? Apr/May 17 BTL1</b></p> <p>Auto Configuration - Auto Configuration is now built in and helps make IP addressing more manageable. With IPv4, we relied on DHCP or manually configuring IP addresses.</p> <p>Direct Addressing - With Direct Addressing, the primary use of NAT (Network Area Translation) now becomes obsolete with IPv6. So, Direct Addressing is now possible.</p> <p>Mobility - Mobility is better integrated into IPv6 than it is with IPv4. It makes it easier for users to roam to different networks and keep their same IP address.</p> <p>Improved Integrated Security (IPSec) - IPSec is now integrated into IPv6, while with IPv4 it was more an add-on</p>						
13	<p><b>Differentiate between forwarding table and routing table. Nov/Dec 17 BTL1</b></p> <p>A routing table uses a packet's destination IP address to determine which IP address should next receive the packet, that is, the "next hop" IP address.</p>						

	A forwarding table uses the "next hop" IP address to determine which interface should deliver the packet to that next hop, and which layer 2 address (e.g., MAC address) should receive the packet on multipoint interfaces like Ethernet or Wi-Fi
14	<p><b>What is RIP? BTL1</b></p> <p>RIP (Routing Information Protocol) is a widely-used protocol for managing router information within a self-contained network such as a corporate local area network or an interconnected group of such LANs. Using RIP, a gateway host (with a router) sends its entire routing table (which lists all the other hosts it knows about) to its closest neighbor host every 30 seconds. The neighbor host in turn will pass the information on to its next neighbor and so on until all hosts within the network have the same knowledge of routing paths, a state known as network convergence</p>
15	<p><b>Explain about OSPF. BTL1</b></p> <p>OSPF (Open Shortest Path First) is a router protocol used within larger autonomous system networks in preference to the Routing Information Protocol (RIP), an older routing protocol that is installed in many of today's corporate networks. Using OSPF, a host that obtains a change to a routing table or detects a change in the network immediately multicasts the information to all other hosts in the network so that all will have the same routing table information</p>
16	<p><b>What are the responsibilities of network layer? BTL1</b></p> <p>The network layer is responsible for the source-to-destination delivery of packet across multiple network links. The specific responsibilities of network layer include the following: Logical addressing. Routing.</p>
17	<p><b>What is meant by hop count? BTL1</b></p> <p>The pathway requiring the smallest number of relays, it is called hop-count routing, in which every link is considered to be of equal length and given the value one.</p>
18	<p><b>What is time-to-live or packet lifetime? BTL1</b></p> <p>As the time-to-live field is generated, each packet is marked with a lifetime; usually the number of hops that are allowed before a packet is considered lost and accordingly, destroyed. The time-to-live determines the lifetime of a packet.</p>
19	<p><b>How the routers get the information about neighbor? BTL1</b></p> <p>A router gets its information about its neighbors by periodically sending them short greeting packets. If the neighborhood responds to the greeting as expected, it is assumed to be alive and functioning. If it does not, a change is assumed to have occurred and the sending router then alerts the rest of the network in its next LSP.</p>
20	<p><b>What is LSP? BTL1</b></p> <p>In link state routing, a small packet containing routing information sent by a router to all other router by a packet called link state packet.</p>
21	<p><b>What are the metrics used by routing protocols? (Apr/May 2015) BTL1</b></p> <p>Path length, bandwidth, load, hop count, path cost, delay, Maximum Transmission Unit (MTU), reliability and communications cost.</p>
22	<p><b>Identify and prove the class of the following IP Address: (Nov /Dec2015) BTL5</b></p> <p>(a) 110.34.56.45 (b) 212.208.63.23</p>

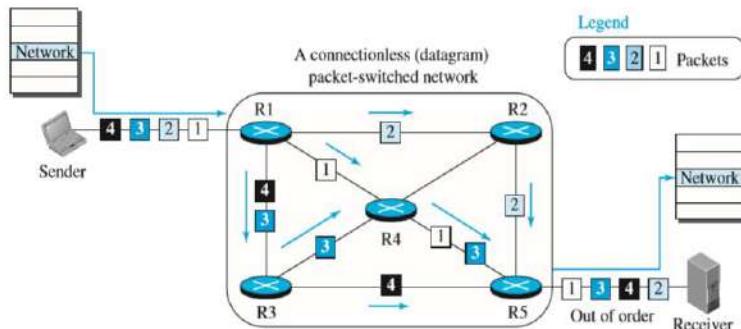
	<p>(a) 110.34.56.45 – Class A          (b) 212.208.63.23- Class C</p>						
	<p><b>PART – B</b></p> <p><b>Explain IPv6 packet format and how fragmentation is applied in datagram delivery. (13M)</b>          BTL2</p> <p><b>Answer Page:318- Larry L. Peterson</b></p> <p><b>Definitions</b> (3M)</p> <p>Internet Protocol Version 6 (IPv6) is an Internet Protocol (IP) used for carrying data in packets from a source to a destination over various networks. IPv6 is the enhanced version of IPv4 and can support very large numbers of nodes as compared to IPv4. It allows for 2<sup>128</sup> possible node, or address, combinations.</p> <p><b>Explanation</b> (5M)</p> <p><b>Packet Header Format</b> (5M)</p> <p>1</p> 						
2	<p><b>Discuss about Link-state routing and routers.(13M) BTL 2</b></p> <p><b>Answer Page:277- Larry L. Peterson</b></p> <p><b>Definition for OSPF</b> (3M)</p> <p>Link State (OSPF) reach its directly connected neighbors, and if we make sure that the totality of this knowledge is disseminated to every node, then every node will have enough knowledge Link-state routing is the second major class of intra domain routing protocol. The starting assumptions for link-state routing are rather similar to those for distance vector routing.</p> <p><b>Header Format</b> (5M)</p> <table border="1"> <thead> <tr> <th>VERSION</th> <th>TYPE</th> <th>MESSAGE LENGTH</th> </tr> </thead> <tbody> <tr> <td>SOURCE ADDRESS</td> <td></td> <td></td> </tr> </tbody> </table>	VERSION	TYPE	MESSAGE LENGTH	SOURCE ADDRESS		
VERSION	TYPE	MESSAGE LENGTH					
SOURCE ADDRESS							

	<table border="1"> <tr> <td colspan="2">Area Id</td></tr> <tr> <td colspan="2">Checksum</td></tr> <tr> <td colspan="2">Authentication type</td></tr> <tr> <td colspan="2">Authentication</td></tr> </table>	Area Id		Checksum		Authentication type		Authentication	
Area Id									
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	<b>Diagram (LSA):</b> (5M)								
	<b>Explain about the inter domain routing (BGP) routing algorithms. (13M) BTL2</b> <p><b>Answer Page:306- Larry L. Peterson</b></p> <p><b>Definition</b></p> <p>BGP used to exchange n/w reachability information among BGP routers and two routers are in same network or different AS may exchange information.</p> <p><b>Types of AS</b> (6M)</p> <ul style="list-style-type: none"> <li>■ <b>Stub AS(2M)</b>: an AS that has only a single connection to one other AS; such an AS will only carry local traffic with in that AS. The small corporation in figure is an eg., of a stub AS.</li> <li>■ <b>Multihomed AS(2M)</b>: an AS that has connections to more than one other AS but that refuses to carry transit traffic; for example, the large corporation at the top</li> <li>■ <b>Transit AS(2M)</b>: an AS that has connections to more than one other AS and that is designed to carry both transit and local traffic, such as the backbone providers.</li> </ul> <p><b>Diagram</b> (4M)</p>								
3	<p><b>Explain in detail about RIP. (13M) (Nov/Dec 2015) BTL2</b></p> <p><b>Answer Page:269- Larry L. Peterson</b></p> <p><b>Definition for RIP</b> (3M)</p> <p>A very important concept in IP addressing is the network address. When an organization is given a block of addresses, the organization is free to allocate the addresses to the devices that need to be connected to the Internet. The first address in the class, however, is normally (not always) treated as a special address.</p> <p><b>Packet Header Format</b> (5M)</p> <table border="1"> <thead> <tr> <th>COMMAND</th> <th>VERSION</th> <th>MUST BE ZERO</th> </tr> </thead> <tbody> <tr> <td>FAMILY OF NET 1</td> <td>ADDRESS OF NET 1</td> <td></td> </tr> </tbody> </table>	COMMAND	VERSION	MUST BE ZERO	FAMILY OF NET 1	ADDRESS OF NET 1			
COMMAND	VERSION	MUST BE ZERO							
FAMILY OF NET 1	ADDRESS OF NET 1								
4	JIT-JEPPIAAR/CSE/Mr.S.DEEPAN/II <sup>rd</sup> Yr/SEM 05/CS8591/COMPUTER NETWORKS/UNIT 1-5/QB+Keys/Ver1.0								

	<table border="1"> <tr><td colspan="2"><b>ADDRESS OF NET 1</b></td></tr> <tr><td colspan="2"><b>DISTANCE TO NET 1</b></td></tr> <tr> <td><b>FAMILY OF NET 2</b></td><td colspan="2"><b>ADDRESS OF NET 2</b></td></tr> <tr><td colspan="2"><b>ADDRESS OF NET 2</b></td></tr> <tr><td colspan="2"><b>DISTANCE TO NET 1</b></td></tr> </table>	<b>ADDRESS OF NET 1</b>		<b>DISTANCE TO NET 1</b>		<b>FAMILY OF NET 2</b>	<b>ADDRESS OF NET 2</b>		<b>ADDRESS OF NET 2</b>		<b>DISTANCE TO NET 1</b>		
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<b>ADDRESS OF NET 2</b>													
<b>DISTANCE TO NET 1</b>													
	<b>Explanation</b>	(5M)											
	<b>Explain in detail about PIM. (13M) BTL2</b>												
	<b>Answer Page:336- Larry L. Peterson</b>												
	<b>Definition</b>	(3M)											
	<p><i>Protocol Independent Multicast</i>, or PIM, was developed in response to the scaling problems of earlier multicast routing protocols. In particular, it was recognized that the existing protocols did not scale well in environments where a relatively small proportion of routers want to receive traffic for a certain group.</p>												
	<b>Diagram</b>	(5M)											
5	<p>RP = Rendezvous point Shared tree Source-specific tree for source R1</p>												
	<b>Explanation</b>	(5M)											
	<b>PART -C</b>												
1	<b>Explain multicast routing in detail. (15M) (Nov/Dec 2015) BTL2</b>												
	<b>Answer Page:332- Larry L. Peterson</b>												
	<b>Definition of Multicasting</b>	(3M)											
	<p>Definition Multicast routing is the process by which the multicast distribution trees are determined or, more concretely, the process by which the multicast forwarding tables are built. As with unicast routing, it is not enough that a multicast routing protocol “work”; it must also scale reasonably well as the network grows, and it must accommodate the autonomy of different routing domains</p>												
	<b>Definition of DVMRP</b>	(3M)											
	<p>Distance-vector routing, which we discussed in for unicast, can be extended to support multicast. The resulting protocol is called DVMRP Distance-vector routing, which we discussed in for unicast, can be extended to support multicast.</p>												
	<b>Diagram</b>	(4M)											

	<p><b>Explanation</b></p>	(5M)															
2	<p><b>Explain in detail about IP v4 addressing. (15M) BTL2</b></p> <p><b>Answer Page:250- Larry L. Peterson</b></p> <p><b>Definition</b></p> <p>A very important concept in IP addressing is the network address. When an organization is given a block of addresses, the organization is free to allocate the addresses to the devices that need to be connected to the Internet.</p> <p><b>Diagram</b></p> <p><b>Class A</b></p> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">0</td> <td style="padding: 2px;">Netid</td> <td style="padding: 2px;">Host ID</td> </tr> </table> <ul style="list-style-type: none"> <li>• <b>Class B</b></li> </ul> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">10</td> <td style="padding: 2px;">Net id</td> <td style="padding: 2px;">Host ID</td> </tr> </table> <ul style="list-style-type: none"> <li>• <b>Class C</b></li> </ul> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">110</td> <td style="padding: 2px;">net id</td> <td style="padding: 2px;">Host id</td> </tr> </table> <ul style="list-style-type: none"> <li>• <b>Class D</b></li> </ul> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">1110</td> <td colspan="2" style="padding: 2px;">Multicast address</td> </tr> </table> <ul style="list-style-type: none"> <li>• <b>Class E</b></li> </ul> <table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <td style="padding: 2px;">1111</td> <td colspan="2" style="padding: 2px;">reserved for future use</td> </tr> </table> <p><b>Applications</b></p>	0	Netid	Host ID	10	Net id	Host ID	110	net id	Host id	1110	Multicast address		1111	reserved for future use		(3M) (5M)
0	Netid	Host ID															
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3	<p><b>Discuss with a neat architecture of Packet Switching.(15M) BTL2</b></p> <p><b>Answer Page:516- Larry L. Peterson</b></p> <p>The source of the message sends the packets one by one; the destination of the message receives the packets one by one. The destination waits for all packets belonging to the same message to arrive before delivering the message to the upper layer. The connecting devices in a packet-switched network still need to decide how to route the packets to the final destination. Today, a packet-switched network can use two different approaches to route the packets: the datagram approach and the virtual circuit approach.</p> <p><b>Datagram Approach:</b></p>																

**Connectionless Service** When the Internet started, to make it simple, the network layer was designed to provide a connectionless service in which the network-layer protocol treats each packet independently, with each packet having no relationship to any other packet. The idea was that the network layer is only responsible for delivery of packets from the source to the destination. In this approach, the packets in a message may or may not travel the same path to their destination.



Each packet is routed based on the information contained in its header: source and destination addresses. The destination address defines where it should go; the source address defines where it comes from. The router in this case routes the packet based only on the destination address. The source address may be used to send an error message to the source if the packet is discarded.

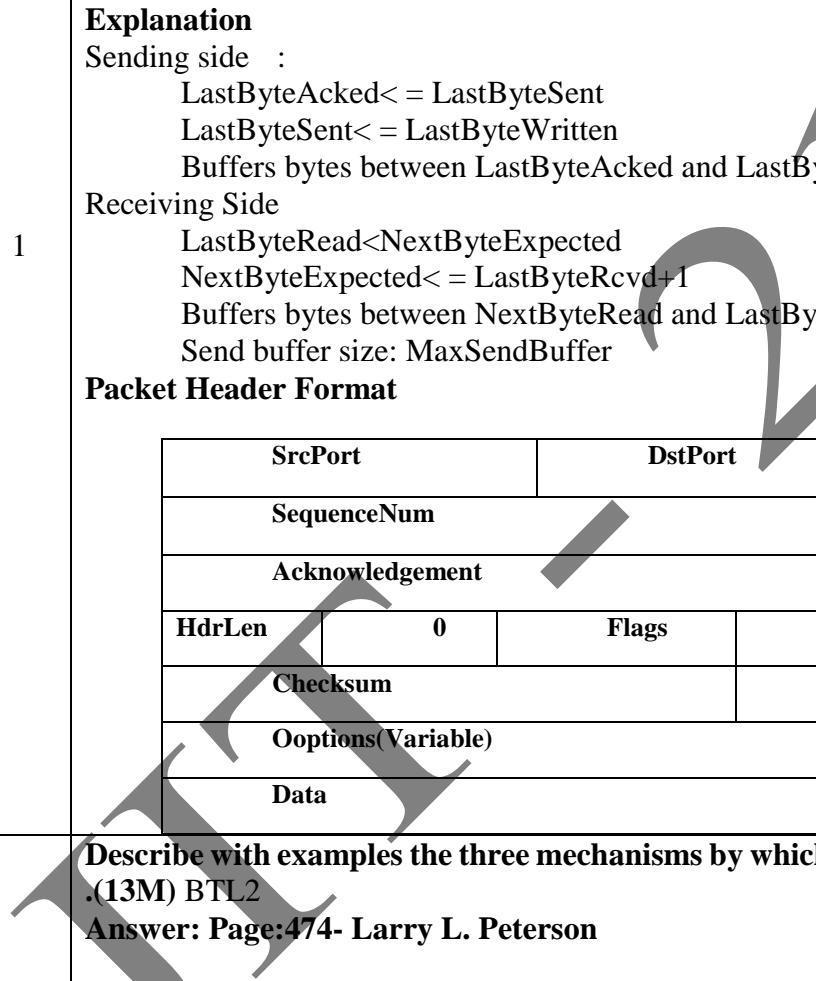
#### Virtual-Circuit Approach:

**Connection-Oriented Service** In a connection-oriented service (also called virtual-circuit approach), there is a relationship between all packets belonging to a message. Before all datagrams in a message can be sent, a virtual connection should be set up to define the path for the datagrams. After connection setup, the datagrams can all follow the same path. Each packet is forwarded based on the label in the packet. To follow the idea of connection-oriented design to be used in the Internet, we assume that the packet has a label when it reaches the router.

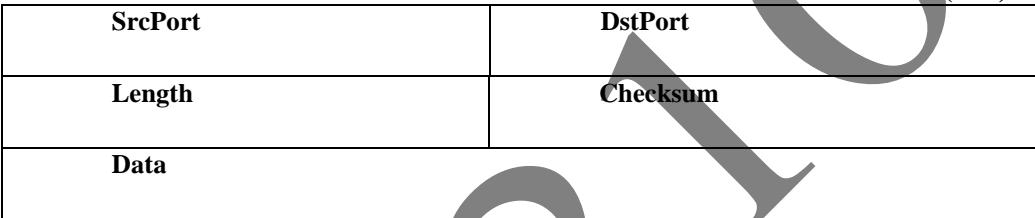
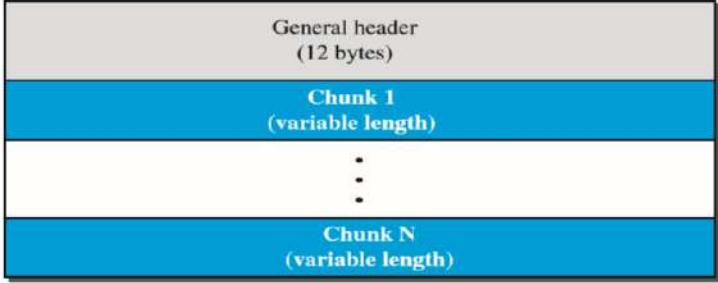
<b>UNIT IV – TRANSPORT LAYER</b>											
Introduction – Transport Layer Protocols – Services – Port Numbers – User Datagram Protocol – Transmission Control Protocol – SCTP.											
<b>PART * A</b>											
<b>Q.No.</b>	<b>Questions</b>										
1.	<p><b>Give any two Transport layer service. (Dec 2012) BLT1</b>  Transport layer performs multiplexing/demultiplexing function. Multiple applications employ same transport protocol, but use different port number. According to lower layer n/w protocol, it does upward multiplexing or downward multiplexing.  Reliability: Error Control and Flow Control</p>										
2	<p><b>Mention the various adaptive retransmission policy of TCP. BLT1</b></p> <ul style="list-style-type: none"> <li>• Simple average</li> <li>• Exponential / weighted average</li> <li>• Exponential RTT backoff</li> <li>• Jacobson's Algorithm</li> </ul>										
3	<p><b>Give the datagram format of UDP? BLT1</b>  The basic idea of UDP is for a source process to send a message to a port and for the destination process to receive the message from a port.</p> <table border="1"> <tr> <td>Source Port Address 16 bits</td><td>Destination Port Address 16 bits</td></tr> <tr> <td>Total Length 16 bits</td><td>Checksum 16 bits</td></tr> </table> <p>Source port address: It is the address of the application program that has created the message.  Destination port address: It is the address of the application program that will receive the message.  Total Length: It defines the total length of the user datagram in bytes.  Checksum: It is a 16 bit field used in error correction</p>	Source Port Address 16 bits	Destination Port Address 16 bits	Total Length 16 bits	Checksum 16 bits						
Source Port Address 16 bits	Destination Port Address 16 bits										
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4	<p><b>What is the main difference between TCP &amp; UDP?(Nov/Dec 2014) BLT1</b></p> <table border="1"> <tr> <th>TCP</th><th>UDP</th></tr> <tr> <td>It provides Connection oriented service</td><td>Provides connectionless service.</td></tr> <tr> <td>Connection Establishment delay will be there</td><td>No connection establishment delay</td></tr> <tr> <td>Provides reliable service</td><td>Provides unreliable, but fast service</td></tr> <tr> <td>It is used by FTP, SMTP</td><td>It is used by DNS,SNMP, audio, video and multimedia applications.</td></tr> </table>	TCP	UDP	It provides Connection oriented service	Provides connectionless service.	Connection Establishment delay will be there	No connection establishment delay	Provides reliable service	Provides unreliable, but fast service	It is used by FTP, SMTP	It is used by DNS,SNMP, audio, video and multimedia applications.
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5	<b>What are the advantages of using UDP over TCP? (Nov/Dec 2010) BLT1</b> UDP is very useful for audio or video delivery which does not need acknowledgement. It is useful in the transmission of multimedia data. Connection Establishment delay will occur in TCP						
6	<b>What is TCP? (Nov/Dec 2011) BLT1</b> Transmission Control Protocol provides Connection oriented and reliable services. TCP guarantees the reliable, in order delivery of a stream of bytes. It is a full-duplex protocol, meaning that each TCP connection supports a pair of byte streams, one flowing in each direction. It is used by FTP, SMTP. The different phases in TCP state machine are Connection Establishment, Data transfer and Connection Release. TCP services to provide reliable communication are Error control, Flow control, Connection control and Congestion control						
7	<b>What is the difference between service point address, logical address and physical address?</b> BLT1						
	<table border="1"> <thead> <tr> <th>Service point addressing</th> <th>Logical addressing</th> <th>Physical addressing</th> </tr> </thead> <tbody> <tr> <td>The transport layer header includes a type of address called a service point address or port address, which makes a data delivery from a specific process on one computer to a specific process on another computer.</td> <td>If a packet passes the network boundary we need another addressing to differentiate the source and destination systems. The network layer adds a header, which indicates the logical address of the sender and receiver.</td> <td>If the frames are to be distributed to different systems on the network, the data link layer adds the header, which defines the source machine's address and the destination Machine's address.</td> </tr> </tbody> </table>	Service point addressing	Logical addressing	Physical addressing	The transport layer header includes a type of address called a service point address or port address, which makes a data delivery from a specific process on one computer to a specific process on another computer.	If a packet passes the network boundary we need another addressing to differentiate the source and destination systems. The network layer adds a header, which indicates the logical address of the sender and receiver.	If the frames are to be distributed to different systems on the network, the data link layer adds the header, which defines the source machine's address and the destination Machine's address.
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8	<b>What is the use of UDP's Pseudo header? BLT1</b> The pseudo header consists of three field from the IP header protocol number ,source IP address and destination IP address plus the UDP length field (which is included twice in checksum calculation).The pseudo header is used to check whether the message is delivered between 2 endpoints						
9	<b>What are the four aspects related to the reliable delivery of data? (May/June 2012) BLT1</b> The four aspects are Error control, Sequence control, Loss control and Duplication control.						
10	<b>What is UDP? BLT1</b> It stands for User Datagram Protocol. It is part of the TCP/IP suite of protocols used for data transferring. UDP is known as a "stateless" protocol, meaning it doesn't acknowledge that the packets being sent have been received						
11	<b>List the flag used in TCP header? BLT1</b> TCP header contains six flags. They are URG,ACK,PSH,RST,SYN,FIN						
12	<b>What is a port? BLT1</b> Applications running on different hosts communicate with TCP with the help of a concept called as ports. A port is a 16 bit unique number allocated to a particular application						
13	<b>List the services of end to end services. BLT1</b> <ul style="list-style-type: none"> <li>• Guarantee message delivery.</li> </ul>						

	<ul style="list-style-type: none"> <li>• Delivery messages in the same order they are sent.</li> <li>• Deliver at most one copy of each message.</li> <li>• Support arbitrarily large message.</li> <li>• Support synchronization</li> </ul>
14	<p><b>List out the three types of addresses in TCP/IP? BLT1</b></p> <p>Three types of addresses are used by systems using the TCP/IP protocol: the physical address, the internetwork address (IP address), and the port address</p>
15	<p><b>List the advantages of connection oriented services over connectionless services. Apr/May 17</b></p> <p>BLT1</p> <p>Connection-oriented Requires a session connection (analogous to a phone call) be established before any data can be sent. This method is often called a "reliable" network service. It can guarantee that data will arrive in the same order.</p> <p>Connectionless: Does not require a session connection between sender and receiver. The sender simply starts sending packets (called datagrams) to the destination. This service does not have the reliability of the connection-oriented method.</p>
16	<p><b>How do fast retransmit mechanism of TCP works? Apr/May 17</b></p> <p>BLT1</p> <p>In TCP/IP, fast retransmit and recovery (FRR) is a congestion control algorithm that makes it possible to quickly recover lost data packets. Without FRR, the TCP uses a timer that requires a retransmission timeout if a packet is lost. No new or duplicate packets can be sent during the timeout period. With FRR, if a receiver receives a data segment that is out of order, it immediately sends a duplicate acknowledgement to the sender. If the sender receives three duplicate acknowledgements, it assumes that the data segment indicated by the acknowledgements is lost and immediately retransmits the lost segment</p>
17	<p><b>What are the types of port numbers used in transport layer? BLT1</b></p> <ul style="list-style-type: none"> <li>• Well-known port</li> <li>• Registered port</li> <li>• Dynamic port</li> </ul>
18	<p><b>What is function of transport layer? BLT1</b></p> <p>The protocol in the transport layer takes care in the delivery of data from one application program on one device to an application program on another device. They act as a link between the upper layer protocols and the services provided by the lower layer.</p>
19	<p><b>What are the duties of the transport layer? BLT1</b></p> <p>The services provided by the transport layer</p> <p>End-to- end delivery</p> <p>Addressing</p> <p>Reliable delivery Flow control Multiplexing</p>
20	<p><b>What is meant by Concatenation? BLT1</b></p> <p>The size of the data unit belonging to a single session are so small that several can fit together into a single datagram or frame, the transport protocol combines them into a single data unit. The combining process is called concatenation.</p>
21	<p><b>List the flag used in TCP header. BTL1</b></p> <p>TCP header contains six flags. They are</p>

	URG,ACK,PSH,RST,SYN,FIN																						
	<b>PART * B</b>																						
	<b>Explain TCP Reliable stream Protocol. (13M) BTL2</b>																						
	<b>Answer: Page:388- Larry L. Peterson</b>																						
	<b>Definitions</b> (3M)																						
1	<p>TCP (Transmission Control Protocol) is a standard that defines how to establish and maintain a network conversation via which application programs can exchange data. TCP works with the Internet Protocol (IP), which defines how computers send packets of data to each other.</p> <p>Relationship between TCP send buffer (a) and receive buffer (b).</p> <p><b>Explanation</b> (5M)</p> <p>Sending side :</p> <ul style="list-style-type: none"> <li>LastByteAcked &lt;= LastByteSent</li> <li>LastByteSent &lt;= LastByteWritten</li> <li>Buffers bytes between LastByteAcked and LastByteWritten</li> </ul> <p>Receiving Side</p> <ul style="list-style-type: none"> <li>LastByteRead &lt; NextByteExpected</li> <li>NextByteExpected &lt;= LastByteRcvd + 1</li> <li>Buffers bytes between NextByteRead and LastByteRcvd.</li> <li>Send buffer size: MaxSendBuffer</li> </ul> <p><b>Packet Header Format</b> (5M)</p>  <table border="1"> <thead> <tr> <th>SrcPort</th> <th>DstPort</th> </tr> </thead> <tbody> <tr> <td>SequenceNum</td> <td></td> </tr> <tr> <td>Acknowledgement</td> <td></td> </tr> <tr> <td>HdrLen</td> <td>0</td> <td>Flags</td> <td>Advertisedwindow</td> </tr> <tr> <td>Checksum</td> <td></td> <td>UrgPtr</td> <td></td> </tr> <tr> <td>Options(Variable)</td> <td></td> <td></td> <td></td> </tr> <tr> <td>Data</td> <td></td> <td></td> <td></td> </tr> </tbody> </table>	SrcPort	DstPort	SequenceNum		Acknowledgement		HdrLen	0	Flags	Advertisedwindow	Checksum		UrgPtr		Options(Variable)				Data			
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2	<p><b>Describe with examples the three mechanisms by which congestion control is achieved in TCP .(13M) BTL2</b></p> <p><b>Answer: Page:474- Larry L. Peterson</b></p> <p><b>Definition AIMD</b> (2M)</p> <p>The additive-increase/multiplicative-decrease (AIMD) algorithm is a feedback control algorithm best known for its use in TCP congestion control. AIMD combines linear growth of the congestion window with an exponential reduction when congestion takes place.</p> <p><b>Diagram</b> (3M)</p> <p><b>Definition Slow start</b> (2M)</p> <p>Slow-start is part of the congestion control strategy used by TCP, the data transmission protocol used by many Internet applications. Slow-start is used in conjunction with other algorithms to avoid</p>																						

	<p>sending more data than the network is capable of transmitting, that is, to avoid causing network congestion.</p> <p><b>Diagram</b> (3M)</p> <p><b>Definition Fast Retransmission &amp;Fast Recovery</b> (3M)</p> <p>Fast retransmit and recovery (FRR) Posted by: Margaret Rouse. In TCP/IP, fast retransmit and recovery (FRR) is a congestion control algorithm that makes it possible to quickly recover lost data packets.</p>										
	<p><b>Discuss TCP congestion avoidance algorithm in detail. (13M) BTL2</b></p> <p><b>Answer: Page:486- Larry L. Peterson</b></p> <p>1.DEC Bit Method</p> <p><b>Definition</b></p> <p>When converting decimal numbers to binary numbers it is important to remember which the least significant bit (LSB) is, and which is the most significant bit (MSB).</p> <p><b>Diagram</b> (2M)</p> <p>2.Random early detection (RED)</p> <p><b>Definition</b></p> <p>RED algorithm defines how to monitor the queue length and when to drop a pkt.</p> <p>RED computes an avg. queue length using a weighted running average.</p> <p><b>Diagram</b> (2M)</p> <p>3.Source Based Congestion Avoidance</p> <p><b>Definition</b></p> <p>In connectionless networks it can be done by explicit messages (choke packets) from the network to the sources or by implicit means such as timeout on a packet loss. ... Congestion control is a social (network-wide) law.</p> <p><b>Diagram</b> (2M)</p>										
3	<p><b>Why does TCP use adaptive retransmission and describe its mechanism (13M) BTL2</b></p> <p><b>Answer: Page:404- Larry L. Peterson</b></p> <p>1. Original Algorithm (3M)</p> <p>2.Karn/Partridge Algorithm (3M)</p> <p>3.Jacobson/Karels Algorithm (3M)</p> <p><b>Explanation</b> (4M)</p>										
4	<p><b>Explain in detail about TCP. (13M) BTL2</b></p> <p><b>Answer: Page:382- Larry L. Peterson</b></p> <p><b>Definition</b> (3M)</p> <p>Transmission Control Protocol provides Connection oriented and reliable services. TCP guarantees the reliable, in order delivery of a stream of bytes. It is a full-duplex protocol, meaning that each TCP connection supports a pair of byte streams, one flowing in each direction. It is used by FTP, SMTP. The different phases in TCP state machine are Connection Establishment, Data transfer and Connection Release. TCP services to provide reliable communication are Error control, Flow control, Connection control and Congestion control.</p> <p><b>Diagram</b> (5M)</p> <table border="1"> <tr> <td>SrcPort</td> <td>DstPort</td> </tr> <tr> <td>SequenceNum</td> <td></td> </tr> <tr> <td>Acknowledgement</td> <td></td> </tr> <tr> <td>HdrLen</td> <td>0</td> <td>Flags</td> <td>Advertisedwindow</td> </tr> </table>	SrcPort	DstPort	SequenceNum		Acknowledgement		HdrLen	0	Flags	Advertisedwindow
SrcPort	DstPort										
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5											

	<table border="1"> <tr><td>Checksum</td><td>UrgPtr</td></tr> <tr><td>Options(Variable)</td><td></td></tr> <tr><td>Data</td><td></td></tr> </table>	Checksum	UrgPtr	Options(Variable)		Data		
Checksum	UrgPtr							
Options(Variable)								
Data								
	<b>Explanation</b> (5M)							
<b>PART * C</b>								
<b>Explain UDP protocol operation in detail. (15M) BTL2</b> <b>Answer: Page:384- Larry L. Peterson</b> <b>Definition of UDP</b> It stands for User Datagram Protocol. It is part of the TCP/IP suite of protocols used for data transferring. UDP is known as a "stateless" protocol, meaning it doesn't acknowledge that the packets being sent have been received. <b>Diagram</b>		(3M)						
1	 <table border="1"> <tr><td>SrcPort</td><td>DstPort</td></tr> <tr><td>Length</td><td>Checksum</td></tr> <tr><td>Data</td><td></td></tr> </table>	SrcPort	DstPort	Length	Checksum	Data		(6M)
SrcPort	DstPort							
Length	Checksum							
Data								
<b>Explanation</b> (6M)								
<b>Explain the Features of SCTP with header format. (15M) BTL2</b> <b>Answer: Page:412- Larry L. Peterson</b> Stream Control Transmission Protocol (SCTP) is a new transport-layer protocol designed to combine some features of UDP and TCP in an effort to create a better protocol for multimedia communication. <b>SCTP Services</b> Process-to-Process Communication SCTP, like UDP or TCP, provides process-to-process communication. Multiple Streams We learned that TCP is a stream-oriented protocol. Each connection between a TCP client and a TCP server involves a single stream. The problem with this approach is that a loss at any point in the stream blocks the delivery of the rest of the data. This can be acceptable when we are transferring text; it is not when we are sending real-time data such as audio or video.								
2	 <table border="1"> <tr><td>General header (12 bytes)</td></tr> <tr><td>Chunk 1 (variable length)</td></tr> <tr><td>:</td></tr> <tr><td>Chunk N (variable length)</td></tr> </table>	General header (12 bytes)	Chunk 1 (variable length)	:	Chunk N (variable length)			
General header (12 bytes)								
Chunk 1 (variable length)								
:								
Chunk N (variable length)								

Source port address 16 bits	Destination port address 16 bits
Verification tag 32 bits	
Checksum 32 bits	

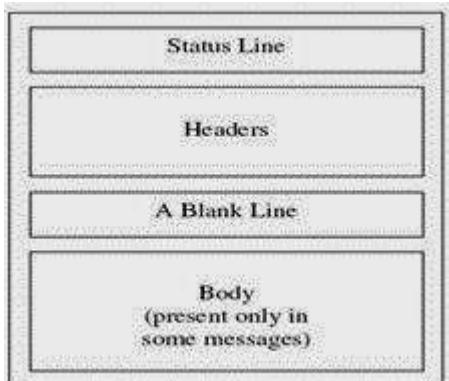
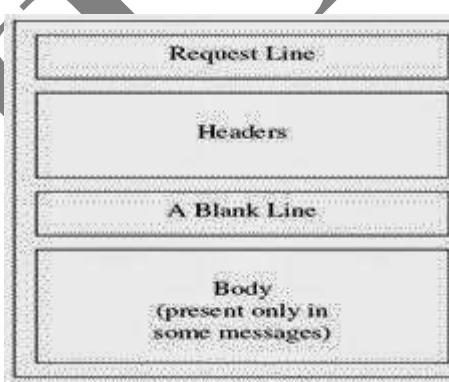
**Packet Format** An SCTP packet has a mandatory general header and a set of blocks called chunks. There are two types of chunks: control chunks and data chunks. A control chunk controls and maintains the association; a data chunk carries user data. In a packet, the control chunks come before the data chunks.

**General Header** The general header (packet header) defines the end points of each association to which the packet belongs, guarantees that the packet belongs to a particular association, and preserves the integrity of the contents of the packet including the header itself.

This prevents a packet from a previous association from being mistaken as a packet in this association. It serves as an identifier for the association; it is repeated in every packet during the association. The next field is a checksum. However, the size of the checksum is increased from 16 bits (in UDP, TCP, and IP) to 32 bits in SCTP to allow the use of the CRC-32 checksum.

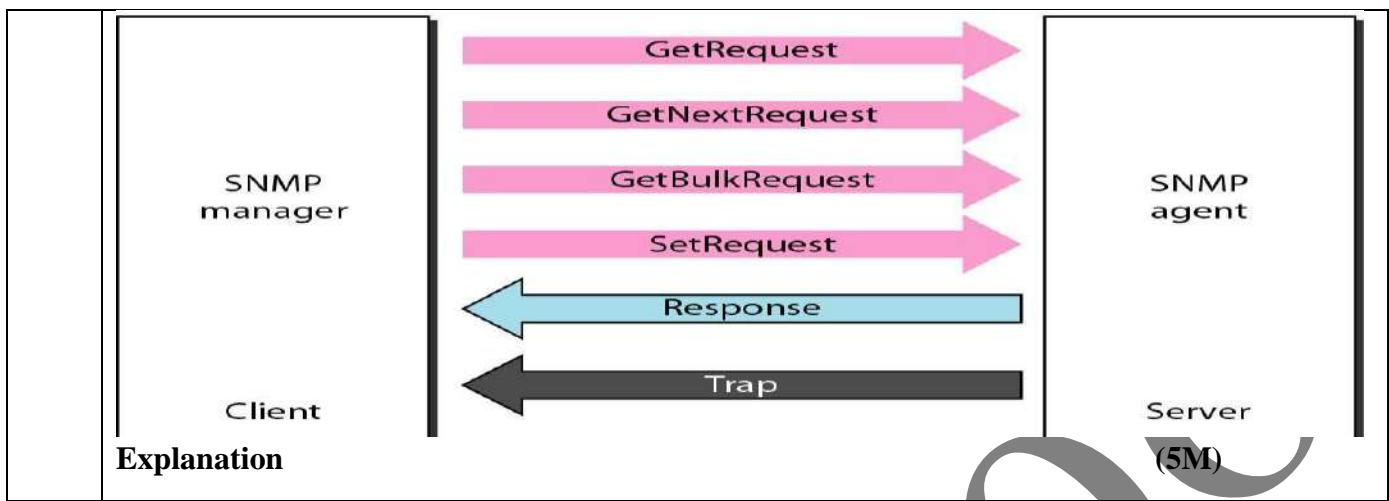
<b>UNIT V – APPLICATION LAYER</b>	
WWW and HTTP – FTP – Email –Telnet –SSH – DNS – SNMP.	
<b>PART * A</b>	
<b>Q.No.</b>	<b>Questions</b>
1.	<p><b>What are the four main properties of HTTP? BLT1</b></p> <ul style="list-style-type: none"> <li>• Global Uniform Resource Identifier.</li> <li>• Request-response exchange.</li> <li>• Statelessness.</li> <li>• Resource metadata</li> </ul>
2	<p><b>What are the four groups of HTTP Headers? What are the two methods of HTTP? BLT1</b></p> <p>The four groups of HTTP headers are</p> <ul style="list-style-type: none"> <li>• General headers</li> <li>• Entity Headers</li> <li>• Request Headers and Response Headers.</li> </ul> <p>Two metho ds</p> <ul style="list-style-type: none"> <li>• GetMethod( )</li> <li>• PostMethod( )</li> </ul>
3	<p><b>What is WWW? Nov/Dec 2010,May/June 2014 BLT1</b></p> <p>World Wide Web is an internet application that allows user to view pages and move from one web page to another. It helps to store and share data across varied distances</p>
4	<p><b>What is the function of SMTP? NOV/DEC 2012, APR/MAY 2015 BLT1</b></p> <p>The TCP/IP protocol supports electronic mail on the Internet is called Simple Mail Transfer (SMTP). It is a system for sending messages to other computer users based on e-mail addresses. SMTP provides mail exchange between users on the same or different computers</p>
5	<p><b>Why is an application such as POP needed for electronic messaging? Apr/May 2012 BLT1</b></p> <p>Workstations interact with the SMTP host, which receives the mail on behalf of every host in the organization, to retrieve messages by using a client-server protocol such as Post Office Protocol. Although POP3 is used to download messages from the server, the SMTP client still needed on the desktop to forward messages from the workstation user to its SMTP mail server</p>
6	<p><b>What is the purpose of Domain Name System? MAY/JUNE 2012 BLT1</b></p> <p>Domain Name System can map a name to an address and conversely an address to name.</p>
7	<p><b>Discuss the three main division of the domain name space. NOV/DEC 2008 BLT1</b></p> <p>Domain name space is divided into three different sections: generic domains, country domains &amp; inverse domain.</p> <p>Generic domain: Define registered hosts according to their generic behavior, uses generic suffixes.</p> <p>Country domain: Uses two characters to identify a country as the last suffix.</p> <p>Inverse domain: Finds the domain name given the IP address</p>

8	<b>What is a Web browser? BLT1</b> Web browser is a software program that interprets and displays the contents of HTML webpages.								
9	<b>What is URL? BLT1</b> URL is Uniform Resource Locator. URL is a string identifier that identifies a page on the World Wide Web (WWW)								
10	<b>What do you mean by TELNET? BLT1</b> TELNET is used to connect remote computers and issue commands on those computers								
11	<b>What are the responsibilities of Application Layer? BLT1</b> The Application Layer enables the user, whether human or software, to access the network. It provides user interfaces and support for services such as e-mail, shared database management and other types of distributed information services <ul style="list-style-type: none"> <li>• Network virtual Terminal</li> <li>• File transfer, access and Management (FTAM)</li> <li>• Mail services</li> <li>• Directory Services</li> </ul>								
12	<b>Write down the three types of WWW documents. BLT1</b> The documents in the WWW can be grouped into three broad categories: static, dynamic and active. <ul style="list-style-type: none"> <li>• <i>Static</i>: Fixed-content documents that are created and stored in a server.</li> <li>• <i>Dynamic</i>: Created by web server whenever a browser requests the document.</li> <li>• <i>Active</i>: A program to be run at the client side</li> </ul>								
13	<b>What are the two types of connections in FTP? BLT1</b> The two types of connections in FTP are <ul style="list-style-type: none"> <li>• Control connection</li> <li>• Open connection</li> </ul>								
14	<b>Define HTTP. BLT1</b> HTTP is Hypertext Transfer Protocol. It is used mainly to access data on the World Wide Web. The protocol transfer data in the form of plaintext, hypertext, audio, video and so on								
15	<b>Compare the HTTP and FTP. BLT1</b> <table border="1"> <thead> <tr> <th style="text-align: center;">FT P</th> <th style="text-align: center;">HTT P</th> </tr> </thead> <tbody> <tr> <td>FTP transfers the file from client to server and server to client.</td> <td>HTTP transfer the file from server to client.(i.e. web pages)</td> </tr> <tr> <td>It uses two different port connections. (i.e. port 20 and port 21)</td> <td>HTTP use only one port connection. (i.e. Port 80)</td> </tr> <tr> <td>FTP uses two parallel TCP connections to transfer a file. They are Control Connection and Data connection.</td> <td>It also uses TCP protocol.</td> </tr> </tbody> </table>	FT P	HTT P	FTP transfers the file from client to server and server to client.	HTTP transfer the file from server to client.(i.e. web pages)	It uses two different port connections. (i.e. port 20 and port 21)	HTTP use only one port connection. (i.e. Port 80)	FTP uses two parallel TCP connections to transfer a file. They are Control Connection and Data connection.	It also uses TCP protocol.
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FTP uses two parallel TCP connections to transfer a file. They are Control Connection and Data connection.	It also uses TCP protocol.								

	Out – of – band	In – band
16	<b>Define SNMP. (May/June 2012) BLT1</b> Simple Network Management Protocol (SNMP) is an "Internet-standard protocol for managing devices on IP networks". Devices that typically support SNMP include routers, switches, servers, workstations, printers, & modem. It is used mostly in network management systems to monitor network-attached devices for conditions that warrant administrative attention	
17	<b>State the usage of conditional get in HTTP. Apr/May 17 BLT1</b> The HTTP Protocol defines a caching mechanism, in which the proxy web-servers can cache pages, files, images etc. Since caching is in place, There is a method which the servers are asked to return the document, either the “cached” or “live” document. This request of asking the server for a document considering a specific parameter is called a Conditional GET Request	
18	<b>Give the format of HTTP response message. BLT1</b> 	
19	<b>Discuss the TCP connections needed in FTP. BLT1</b> FTP establishes two connections between the hosts. One connection is used for datatransfer, the other for control information. The control connection uses very simple rules of communication. The data connection needs more complex rules due to the variety of data types transferred.	
20	<b>Give the format of HTTP request message. BLT1</b> 	
21	<b>Define Name Resolution. BTL1</b> To improve reliability, some of the name servers can be located outside the zone. The process of looking up a name and finding an address is called name resolution.	

22	<p><b>What is Telnet and its three main ideas.</b> BTL1</p> <p>A Telnet is a Transmission Control Protocol (TCP). Connection used to transmit data with interspersed Telnet Control Information. The Telnet Protocol is built upon three main ideas:</p> <ol style="list-style-type: none"> <li>1. The concept of a network virtual terminal</li> <li>2. The principle of negotiated options</li> <li>3. A symmetric view of terminals and processes.</li> <li>4. Telnet is the standard TCP/IP protocol for virtual terminal service.</li> </ol>
23	<p><b>What is TFTP?</b> BTL1</p> <p>Trivial file transfer protocol is designed for transferring bootstrap and configuration files. It is so simple and can fit into ROM of a disc less memory. TFTP does reading and writing of files. Reading means copying files from server site to client site and writing in FTP means copying a file from client site to server site.</p>
24	<p><b>Describe why HTTP is defined as a stateless protocol?</b> BTL1</p> <p>Maintaining state across request – Response connections significantly increases the initial interactions in a connections since the identity of each party needs to be established and any saved state much be retrieved. HTTP is therefore stateless to ensure that internet is scalable since state is not contained in a HTTP request / response pairs by default.</p>
	<p><b>PART * B</b></p> <p><b>Discuss how the Simple Mail Transfer Protocol (SMTP) is used in electronic mail. (13M)</b></p> <p>BTL2</p> <p><b>Answer: Page:643- Larry L. Peterson</b></p> <p><b>Definition</b> (3M)</p> <p>SMTP (Simple Mail Transfer Protocol) is a TCP/IP protocol used in sending and receiving e-mail. On Unix-based systems, send mail is the most widely-used SMTP server for e-mail. ... Many mail servers now support Extended Simple Mail Transfer Protocol (ESMTP), which allows multimedia related files.</p> <p><b>Diagram</b> (5M)</p> <p>1</p> <p>UA Alice MTA client</p> <p>UA: user agent MTA: message transfer agent MAA: message access agent</p> <p>LAN or WAN</p> <p>MTA server</p> <p>MTA client</p> <p>Internet</p> <p>System</p> <p>MAA client Bob UA</p> <p>LAN or WAN</p> <p>MAA server</p> <p>MTA server</p> <p>System</p> <p><b>Explanation</b> (5M)</p>

	<b>Explain the role of a DNS on a computer network, including its involvement in the process of a user accessing a web page. (13M) BTL 2</b>	
	<b>Answer: Page:657- Larry L. Peterson</b>	
2	<p><b>Definition</b> (3M)</p> <p>Domain Name System can map a name to an address and conversely an address to name. The Domain Name System converts domain names into IP numbers. IP numbers uniquely identify hosts on the Internet; however they are difficult to remember. We therefore need a memorable way of identifying hosts.</p> <p><b>Diagram</b> (5M)</p> <pre> graph TD     User["User user@cs.princeton.edu"] --&gt; Mail[Mail program]     Mail --&gt; NameServer[Name server]     NameServer -- "2 cs.princeton.edu" --&gt; Mail     NameServer --&gt; IP[IP]     Mail -- "192.12.69.5" --&gt; TCP[TCP]     TCP -- "192.12.69.5" --&gt; IP     </pre>	
3	<p><b>Explanation</b> (5M)</p> <p><b>Answer in detail about FTP. (6M) BTL2</b></p> <p><b>Definition</b> (3M)</p> <p>File Transfer Protocol (FTP) is a standard Internet protocol for transmitting files between computers on the Internet over TCP/IP connections. Clients initiate conversations with servers by requesting to download a file. Using FTP, a client can upload, download, delete, rename, move and copy files on a server</p> <p><b>Diagram</b> (3M)</p>	
4	<p><b>Explain about SNMP and its group management. (13M) BTL2</b></p> <p><b>Answer: Page:666- Larry L. Peterson</b></p> <p><b>Definition</b> (3M)</p> <ul style="list-style-type: none"> <li>A network is a complex system, both in terms of the number of nodes that are involved and in terms of the suite of protocols that can be running on any one node.</li> <li>All the state that is maintained and manipulated on any one of these nodes—for example, address translation tables, routing tables, TCP connection state, and so on—then it becomes tedious to manage all of this information.</li> </ul> <p><b>SNMP Architecture</b> (5M)</p>	



Explain how HTTP involved in web services? (13M) BTL2

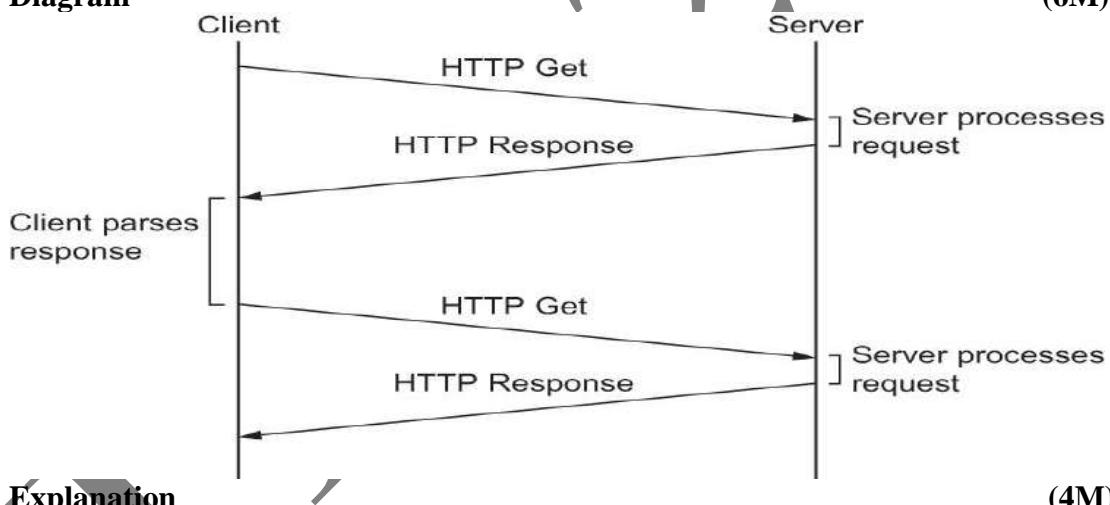
**Answer: Page:650- Larry L. Peterson**

**Definition**

The web contains a set of cooperating clients & servers, speaking the same language HTTP. Users are exposed to web thru a graphical client pgm / web browser.

All web browsers have a function, allowing the user to open a URL, which provides info about the location of objects on the web.

**Diagram**



### PART \*C

Write short notes on following protocol

a).MIME b).IMAP c). POP3. (15M) BTL 2

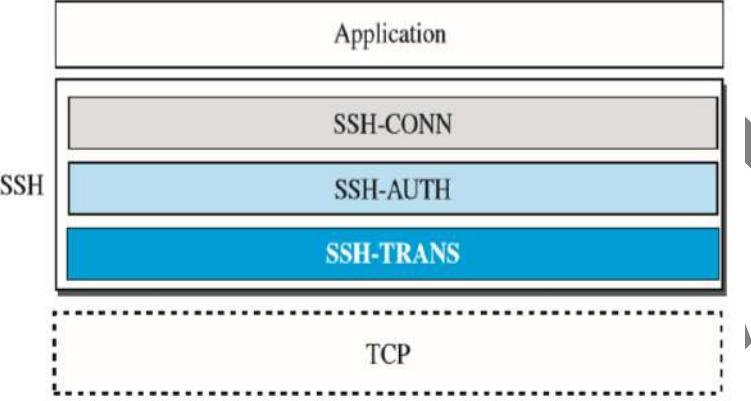
**Answer: Page:648- Larry L. Peterson**

**1 Definition of MIME**

(2M)

MIME (Multi-Purpose Internet Mail Extensions) is an extension of the original Internet e-mail protocol that lets people use the protocol to exchange different kinds of data files on the Internet: audio, video, images, application programs, and other kinds, as well as the ASCII text handled in the original protocol.

	<b>Explanation</b> (3M)
	<b>Definition of IMAP</b> (2M)
	IMAP (Internet Message Access Protocol) is a standard email protocol that stores email messages on a mail server, but allows the end user to view and manipulate the messages as though they were stored locally on the end user's computing device(s).
	<b>Explanation</b> (3M)
	<b>Definition of POP3</b> (2M)
	POP3 (Post Office Protocol 3) is the most recent version of a standard protocol for receiving e-mail. POP3 is a client/server protocol in which e-mail is received and held for you by your Internet server.
	<b>Explanation</b> (3M)
	<b>Explain TELNET with neat architecture.(15M) BTI2</b>
	<b>Answer: Page:668- Larry L. Peterson</b>
	<p>One of the original remote logging protocols is TELNET, which is an abbreviation for TErminal NETwork. Although TELNET requires a logging name and password, it is vulnerable to hacking because it sends all data including the password in plaintext (not encrypted). A hacker can eavesdrop and obtain the logging name and password. Because of this security issue, the use of TELNET has diminished in favor of another protocol, Secure Shell (SSH), which we describe in the next section. Although TELNET is almost replaced by SSH, we briefly discuss TELNET here for two reasons:</p> <ol style="list-style-type: none"> <li>1. The simple plaintext architecture of TELNET allows us to explain the issues and challenges related to the concept of remote logging, which is also used in SSH when it serves as a remote logging protocol.</li> <li>2. Network administrators often use TELNET for diagnostic and debugging purposes.</li> </ol>
2	<p><b>a. Local logging</b></p> <p><b>b. Remote logging</b></p>
	<p>When a user logs into a local system, it is called local logging. As a user types at a terminal or at a workstation running a terminal emulator, the keystrokes are accepted by the terminal driver. The terminal driver passes the characters to the operating system. The operating system, in turn, interprets the combination of characters and invokes the desired application program or utility.</p>

	<p>However, when a user wants to access an application program or utility located on a remote machine, she performs remote logging. Here the TELNET client and server programs come into use. The user sends the keystrokes to the terminal driver where the local operating system accepts the characters but does not interpret them. The characters are sent to the TELNET client, which transforms the characters into a universal character set called Network Virtual Terminal (NVT) characters (discussed below) and delivers them to the local TCP/IP stack.</p>
	<p><b>Write the features of SSH with header format. (15M) BTL2</b></p> <p><b>Answer: Page:907- Larry L. Peterson</b></p> <p>Secure Shell (SSH) is a secure application program that can be used today for several purposes such as remote logging and file transfer, it was originally designed to replace TELNET. There are two versions of SSH: SSH-1 and SSH-2, which are totally incompatible. The first version, SSH-1, is now deprecated because of security flaws in it.</p> 
3	<p>SSH Transport-Layer Protocol (SSH-TRANS) Since TCP is not a secured transport-layer protocol, SSH first uses a protocol that creates a secured channel on top of the TCP. This new layer is an independent protocol referred to as SSH-TRANS. When the procedure implementing this protocol is called, the client and server first use the TCP protocol to establish an insecure connection. Then they exchange several security parameters to establish a secure channel on top of the TCP. We discuss transport-layer security in Chapter 32, but here we briefly list the services provided by this protocol:</p> <ol style="list-style-type: none"> <li>1. Privacy or confidentiality of the message exchanged</li> <li>2. Data integrity, which means that it is guaranteed that the messages exchanged between the client and server are not changed by an intruder.</li> <li>3. Server authentication, which means that the client is now sure that the server is the one that it claims to be</li> <li>4. Compression of the messages, which improves the efficiency of the system and makes attack more difficult.</li> </ol> <p><b>SSH Connection Protocol (SSH-CONN)</b></p> <p>After the secured channel is established and both server and client are authenticated for each other, SSH can call a piece of software that implements the third protocol, SSHCONN. One of the services provided by the SSH-CONN protocol is multiplexing. SSH-CONN takes the secure channel established by the two previous protocols and lets the client create multiple logical channels over it.</p>

**EC8691 MICROPROCESSORS AND MICROCONTROLLERS****L T P C****3 0 0 3****OBJECTIVES:**

- To understand the Architecture of 8086 microprocessor.
- To learn the design aspects of I/O and Memory Interfacing circuits.
- To interface microprocessors with supporting chips.
- To study the Architecture of 8051 microcontroller.
- To design a microcontroller based system

**UNIT I THE 8086 MICROPROCESSOR****9**

Introduction to 8086 – Microprocessor architecture – Addressing modes - Instruction set and assembler directives – Assembly language programming – Modular Programming - Linking and Relocation - Stacks - Procedures – Macros – Interrupts and interrupt service routines – Byte and String Manipulation.

**UNIT II 8086 SYSTEM BUS STRUCTURE****9**

8086 signals – Basic configurations – System bus timing –System design using 8086 – I/O programming – Introduction to Multiprogramming – System Bus Structure – Multiprocessor configurations – Coprocessor, Closely coupled and loosely Coupled configurations – Introduction to advanced processors.

**UNIT III I/O INTERFACING****9**

Memory Interfacing and I/O interfacing - Parallel communication interface – Serial communication interface – D/A and A/D Interface - Timer – Keyboard /display controller – Interrupt controller – DMA controller – Programming and applications Case studies: Traffic Light control, LED display , LCD display, Keyboard display interface and Alarm Controller.

**UNIT IV MICROCONTROLLER****9**

Architecture of 8051 – Special Function Registers(SFRs) - I/O Pins Ports and Circuits - Instruction set - Addressing modes - Assembly language programming.

**UNIT V INTERFACING MICROCONTROLLER****9**

Programming 8051 Timers - Serial Port Programming - Interrupts Programming – LCD & Keyboard Interfacing - ADC, DAC & Sensor Interfacing - External Memory Interface- Stepper Motor and Waveform generation - Comparison of Microprocessor, Microcontroller, PIC and ARM processors

**TOTAL: 45 PERIODS****OUTCOMES:****At the end of the course, the students should be able to:**

- Understand and execute programs based on 8086 microprocessor.
- Design Memory Interfacing circuits.
- Design and interface I/O circuits.
- Design and implement 8051 microcontroller based systems.

**TEXT BOOKS:**

1. Yu-Cheng Liu, Glenn A.Gibson, —Microcomputer Systems: The 8086 / 8088 Family - Architecture, Programming and Design, Second Edition, Prentice Hall of India, 2007. (UNIT I- III)

2. Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, —The 8051 Microcontroller and Embedded Systems: Using Assembly and C, Second Edition, Pearson education, 2011. (UNIT IV,V)

**Subject Code: EC8691****Subject Name: MICROPROCESSORS  
AND MICROCONTROLLERS****Year/Semester: III /05****Subject Handler: Mrs.R.Ramakala****Unit 1 THE 8086 MICROPROCESSOR**

**Introduction to 8086 – Microprocessor architecture – Addressing modes - Instruction set and assembler directives – Assembly language programming – Modular Programming - Linking and Relocation - Stacks - Procedures – Macros – Interrupts and interrupt service routines – Byte and String Manipulation.**

Q. No.	Questions & Answers
1	<p><b>What are the types of instruction sets of 8086 microprocessor? BTL 1</b></p> <p>There are eight types of instructions. They are</p> <ul style="list-style-type: none"> <li>• Data copy/Transfer instructions</li> <li>• Arithmetic &amp; Logical instructions</li> <li>• Branch instructions</li> <li>• Loop instructions</li> <li>• Machine control instructions</li> <li>• Flag manipulation instructions</li> <li>• Shift &amp; rotate instructions</li> <li>• String instructions</li> </ul>
2	<p><b>What are flag manipulation instructions? BTL 1</b></p> <p>The instructions that directly modify the flags of 8086 are called as the flag manipulation instructions. E.g.: CLC --- clear carry flag, CMC --- complement carry flag, STC --- set carry flag , CLD --- clear direction flag</p>
3	<p><b>Explain the instructions LODS &amp; STOS. BTL 2</b></p> <p>a)LODS: Load String Byte or String Word</p> <ul style="list-style-type: none"> <li>• The LODS instruction loads the AL/AX register by the content of a string pointed to by DS: SI registers pair.</li> <li>• The SI is modified automatically depending on direction flag. If it is a byte transfer (LODSB), the SI is modified by one &amp; if it is a word transfer (LODSW), the SI is modified by two.</li> <li>• No other flags are affected by this instruction.</li> </ul> <p>b)STOS: Store String Byte or String Word</p> <ul style="list-style-type: none"> <li>• The STOS instruction stores the AL/AX register contents to a location in the string pointed by ES: DI register pair.</li> <li>• The DI is modified accordingly.</li> <li>• No flags are modified by this instruction.</li> </ul>
4	<p><b>Define control transfer instruction &amp; explain their types. BTL 1</b></p> <p>The instructions that transfer the flow of execution of the program to a new address specified in the instruction directly or indirectly are called the control transfer or branching instructions. They are of two types.</p> <p><b>Unconditional control transfer instructions:</b> In these types of instructions, the execution control is transferred to the specified location independent of any status or condition.</p> <p><b>Conditional control transfer instructions:</b> In these instructions, The control is transferred to the specified location provided the result of the previous operation satisfies a particular condition, otherwise, the execution continues in normal flow sequence.</p>
5	<p><b>What are assembler directives? Give example. BTL 1</b></p> <p>The assembler is a program used to convert an assembly language program into the equivalent</p>

	machine code modules that may be further converted to executable codes. Therefore the hints given to the assembler to complete all these tasks in some predefined alphabetical strings is called an assembler directive. E.g.: DB-----define byte, END----end of program, EQU-----equate
6	<b>What is the function of parity flag? (Nov 2013) BTL 1</b> The parity flag is set, if the result of the byte operation or lower byte of the word operation contains an even number of ones.
7	<b>Define a MACRO.</b> BTL 1 A number of instructions appearing again & again in the main program can be assigned as a macro definition (i.e.) a label is assigned to the repeatedly appearing string of instructions. The process of assigning a label or macro name to the string is called defining a macro. A macro within a macro is called a nested macro.
8	<b>Which interrupt has got the highest priority among all the external interrupts?</b> BTL 1 The Non-Maskable Interrupt pin of 8086 has got the highest priority among the external Interrupts.
9	<b>What are the segment registers present in 8086?</b> BTL 1 There are four segment registers in 8086. They are i. Code Segment register (CS) ii. Data Segment register (DS) iii. Extra Segment register (ES) iv. Stack Segment register (SS)
10	<b>What do you mean by instruction pipelining?</b> BTL 1 While the execution unit executes the previously decoded instruction, the Bus Interface Unit fetches the next instruction and places it in the pre fetched instruction byte queue. This forms a pipeline.
11	<b>What is the use of the Trap flag in the flag register of 8086?</b> BTL 1 When the Trap flag is set, the processor enters the single step execution mode. A trap interrupt is generated after execution of each instruction. The processor executes the current instruction and the control is transferred to the Trap interrupt service routine.
12	<b>List the instruction formats in 8086 instruction set.</b> BTL 1 There are six general formats of instruction in 8086. They are <ul style="list-style-type: none"> <li>• One byte instruction.</li> <li>• Register to Register.</li> <li>• Register to/from Memory with no Displacement.</li> <li>• Register to/from memory with Displacement.</li> <li>• Immediate operand to Register.</li> <li>• Immediate operand to Memory with 16-bit Displacement.</li> </ul>
13	<b>What are the addressing modes of sequence control transfer instructions in 8086? Give example.</b> BTL 1 <ul style="list-style-type: none"> <li>• Immediate eg: Mov AX,0005H.</li> <li>• Direct eg: Mov AX,[5000H].</li> <li>• Register eg: Mov BX,AX.</li> <li>• Register Indirect eg: Mov AX,[Bx].</li> <li>• Indexed eg: Mov AX,[SI].</li> <li>• Register Relative eg: Mov AX,50H[BX].</li> <li>• Based Indexed eg: Mov AX,[Bx] [SI].</li> <li>• Relative Based Indexed eg: Mov AX,50H [BX] [SI].</li> </ul>
14	<b>What are the differences between 8085 and 8086? (Nov 2013)</b> BTL1 8-bit microprocessor                    16-bit microprocessor

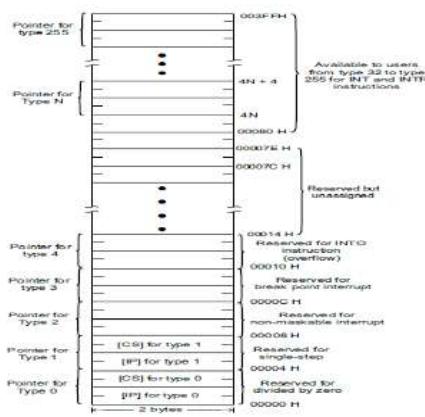
	<p>It is capable of addressing 28 memory locations</p> <p>Low speed</p> <p>It can be configured only in single processor mode</p>	<p>It is capable of addressing <math>2^{16}</math> memory locations</p> <p>High speed</p> <p>It can be configured in single processor mode and multiprocessor mode</p>																																																
15	<p><b>How is the physical address generated in 8086? (or) How 16 bit address is converted into 20 bit address in 8086? (Nov 2013) (Apr/May 2017) BTL 1</b></p> <p>The content of the segment register called as segment address is shifted Left bit-wise four times and to this result, content of an offset register also called as offset address is added, to produce a 20-bit physical address.</p> <table style="margin-left: 20px;"> <tr> <td>eg:</td> <td>segment address</td> <td>1005H</td> </tr> <tr> <td></td> <td>Offset address</td> <td>5555H</td> </tr> <tr> <td></td> <td>Segment address</td> <td>0001 0000 0000 0101</td> </tr> <tr> <td></td> <td>Shifted by 4 bit positions</td> <td>0001 0000 0000 0101 0000</td> </tr> <tr> <td></td> <td></td> <td style="text-align: center;">+</td> </tr> <tr> <td></td> <td>Offset address</td> <td>0101 0101 0101 0101</td> </tr> <tr> <td></td> <td>Physical address</td> <td>0001 0101 0101 1010 0101</td> </tr> <tr> <td></td> <td></td> <td style="text-align: center;">1    5    5    A    5</td> </tr> </table>	eg:	segment address	1005H		Offset address	5555H		Segment address	0001 0000 0000 0101		Shifted by 4 bit positions	0001 0000 0000 0101 0000			+		Offset address	0101 0101 0101 0101		Physical address	0001 0101 0101 1010 0101			1    5    5    A    5																									
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16	<p><b>Explain XLAT instruction.</b> BTL 2</p> <ul style="list-style-type: none"> <li>The XLAT (Translate) instruction replaces a byte in the AL register with a byte from a 256-byte, user coded translation table.</li> <li>XLAT is useful for translating characters from one code to another like ASCII to EBCDIC and ASCII to HEX etc.</li> </ul>																																																	
17	<p><b>Draw the PSW format for 8086.(May/June 2016) BTL 2</b></p> <table border="1" style="margin-left: 20px; width: fit-content;"> <tr> <td>B1</td><td>B1</td><td>B1</td><td>B1</td><td>B1</td><td>B1</td><td>B9</td><td>B8</td><td>B7</td><td>B6</td><td>B5</td><td>B4</td><td>B3</td><td>B2</td><td>B1</td><td>B0</td> </tr> <tr> <td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td><td></td> </tr> <tr> <td>U</td><td>U</td><td>U</td><td>U</td><td>OF</td><td>DF</td><td>IF</td><td>TF</td><td>SF</td><td>ZF</td><td>U</td><td>AF</td><td>U</td><td>PF</td><td>U</td><td>CF</td> </tr> </table> <p>U: Undefined; CF : Carry flag - Set by carry out of MSB      PF: Parity flag- set if result has even parity; AF : Auxiliary carry flag - used for BCD operation; ZF : Zero flag - set if result = 0; SF : Sign flag - set if result is -ve.      TF : Trap flag - set to enable single step execution mode. IF: Interrupt flag- set to enable interrupt ;DF : Direction flag - set to enable auto decrement mode for string operation ;OF: Overflow flag - used for signed arithmetic operation</p>	B1	B1	B1	B1	B1	B1	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0	5	4	3	2	1	0											U	U	U	U	OF	DF	IF	TF	SF	ZF	U	AF	U	PF	U	CF	
B1	B1	B1	B1	B1	B1	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0																																			
5	4	3	2	1	0																																													
U	U	U	U	OF	DF	IF	TF	SF	ZF	U	AF	U	PF	U	CF																																			
18	<p><b>Explain the function of TEST pin in 8086 BTL 2</b></p> <p>This input is examined by a “WAIT” instruction. When the processor executes WAIT instruction, it enters into wait state (Idle state). If the TEST pin goes low, the processor will come out from the idle state and continues the execution; otherwise it remains in an idle state.</p>																																																	
19	<p><b>Give the operation of CBW and TEST instructions of 8086? (Nov 2013) BTL 1</b></p> <p>CBW instruction converts the byte in AL to word value in AX by extending the sign of AL throughout the register AH. TEST instruction performs logical AND operation of the two operands updating the flag registers without saving the result</p>																																																	
20	<p><b>What do you mean by addressing modes? (May 2014) BTL 1</b></p> <p>The addressing modes clearly specify the location of the operand and also how its location may be determined.</p>																																																	
21	<p><b>What is meant by a vectored interrupt? (May 2014) BTL 1</b></p> <p>There is an interrupt vector table which stores the information regarding the location of interrupt service routine (ISR) of various interrupt. Whenever an interrupt occurs the memory location of ISR is determined using the vector table and the program control branches to ISR after saving the flags and the program location.</p>																																																	

22	<p><b>Write about the different types of interrupts supported in 8086. (May 2015) BTL1</b></p> <p>Interrupts in 8086 are classified into three. They are:</p> <ul style="list-style-type: none"> <li>i) Pre defined interrupt           <ul style="list-style-type: none"> <li>- Type 0 to Type 4 interrupts.</li> </ul> </li> <li>ii) Hardware interrupt           <ul style="list-style-type: none"> <li>- Mask able interrupt and Non Mask able interrupt</li> </ul> </li> <li>iii) Software interrupt(INT n)           <ul style="list-style-type: none"> <li>- 256 types of software interrupt.</li> </ul> </li> </ul>																
23	<p><b>Define Stack. (May/June 2016) (Apr/May 2017) BTL 1</b></p> <p>A <b>stack</b> pointer is a small register that stores the address of the last program request in a <b>stack</b>. A <b>stack</b> is a specialized buffer which stores data from the top down. As new requests come in, they "push down" the older ones.</p>																
24	<p><b>What are Macros? APRIL/ MAY 2019 BTL 1</b></p> <p>When procedure is called within the main program by an assembler, the program control will be transferred to the procedures starting address and starts execution of a group of instructions available in the procedure. In macros, whenever macro is called by its name, each time the assembler will insert the defined group of instructions in the main program itself i.e., program control is not transferred anywhere.</p>																
25	<p><b>Given that (BX=0158. (D I)=10A5 Displacement =1B57 (DS)=2100 .Determine the effective address and physical address for the following addressing modes. (a) Register Indirect (b).Relative based indexed. April/may 2019 BTL 1</b></p> <table style="width: 100%; border-collapse: collapse;"> <tbody> <tr> <td style="width: 40%;">segment address</td> <td style="width: 60%;">1005H</td> </tr> <tr> <td>Offset address</td> <td>5555H</td> </tr> <tr> <td>Segment address</td> <td>0001 0000 0000 0101</td> </tr> <tr> <td>Shifted by 4 bit positions</td> <td>0001 0000 0000 0101 0000</td> </tr> <tr> <td></td> <td style="text-align: center;">+</td> </tr> <tr> <td>Offset address</td> <td>0101 0101 0101 0101</td> </tr> <tr> <td>Physical address</td> <td>0001 0101 0101 1010 0101</td> </tr> <tr> <td></td> <td style="text-align: center;">1    5    5    A    5</td> </tr> </tbody> </table>	segment address	1005H	Offset address	5555H	Segment address	0001 0000 0000 0101	Shifted by 4 bit positions	0001 0000 0000 0101 0000		+	Offset address	0101 0101 0101 0101	Physical address	0001 0101 0101 1010 0101		1    5    5    A    5
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	+																
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	1    5    5    A    5																

### PART B

1	<p><b>Discuss in detail the three types of interrupt system of Intel 8086. (May 2014) (Apr/May 2016, 2017) (13M) APRIL/ MAY 2019 BTL 6</b></p> <p><b>Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, PG.NO:169-173</b></p> <ul style="list-style-type: none"> <li>• 8086 can implement seven different types of interrupts.</li> <li>• NMI and INTR are external interrupts implemented via <i>Hardware</i>.</li> <li>• INT n, INTO and INT3 (breakpoint instruction) are software interrupts implemented through <i>Program</i>.</li> <li>• The 'divide-by-0' and 'Single-step' are interrupts <i>initiated by CPU</i>.</li> </ul> <p style="text-align: right;"><b>(5M)</b></p>
---	--

Name	Initiated by:	Maskable?	Trigger	Priority	Acknowledge signal?	Vector table address-	Interrupt latency
NMI	External hardware	No	↑Edge, hold 2 T states min.	2	None	00008H–0000BH	Current instruction + 51 T states
INTR	External hardware	Yes via IF	High level until acknowledged	3	INTA	n * 4 <sup>b</sup>	Current instruction + 61 T states
INT n	Internal via software	No	None	1	None	n * 4	51 T states
INT 3 (break point)	Internal via software	No	None	1	None	0000CH–0000FH	52 T states
INTO	Internal via software	No	None	1	None	00010H–00013H	53 T states
Divide-by-0	Internal via CPU	Yes via OF	None	1	None	00000H–00003H	51 T states
Single-step	Internal via CPU	Yes via TF	None	4	None	00004H–00007H	51 T states

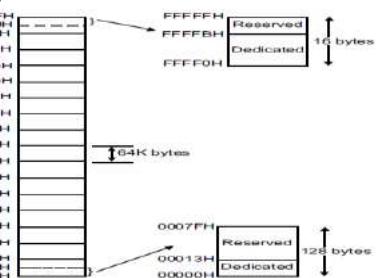


(8M)

- 2 Explain the memory concepts of Intel 8086 and explain how data transfer takes place. (13M) BTL 5

**Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, PG.NO:26-35**

8086, via its 20-bit address bus, can address  $2^{20} = 1,048,576$  or 1 MB of different memory locations. Thus the memory space of 8086 can be thought of as consisting of 1,048,576 bytes or 524,288 words. The memory map of 8086 is shown in Figure, where the whole memory space starting from 00000 H to FFFFF H is divided into 16 blocks—each one consisting of 64 KB. This division is arbitrary but at the same time a convenient one—because the most significant hex digit increases by 1 with each additional block. Thus, 30000 H memory location is 65,536 bytes higher in memory than the memory location 20000 H. (3M)



(2M)

The lower and upper ends of the memory map are shown separately—earmarking some spaces as reserved and some as ‘dedicated’. The reserved locations are meant for future hardware and software needs while the dedicated locations are used for processing of specific system interrupts and reset functions. (4M)

	<p>The different memory segmentations done in case of 8086 are</p> <ul style="list-style-type: none"> <li>• Continuous</li> <li>• partially overlapped</li> <li>• fully overlapped and</li> <li>• disjointed</li> </ul> <p>This is shown in Fig.12.2.</p> <p><b>Fig. 12.2: Depiction of different types of segments</b></p> <p>In the figure,</p> <table border="0"> <tr> <td>Segments-0 and 1</td> <td>→ Continuous</td> </tr> <tr> <td>Segments-1 and 2</td> <td>→ Partially overlapped</td> </tr> <tr> <td>Segments-2 and 3</td> <td>→ Fully overlapped</td> </tr> <tr> <td>and Segments-2 and 4</td> <td>→ Disjointed</td> </tr> </table> <p>(4M)</p> <p>The 20-bit physical (real) address is generated by combining the offset (residing in IP, BP, SP, BX, SI or DI) and the content of one of the segment registers CS, DS, ES or SS. The process of combination is as follows: The content of the segment register is internally appended with 0 H (0000 H) on its right most end to form a 20-bit memory address—this 20-bit address points to the start of the segment. The offset is then added to the above to get the physical address. (2M)</p>	Segments-0 and 1	→ Continuous	Segments-1 and 2	→ Partially overlapped	Segments-2 and 3	→ Fully overlapped	and Segments-2 and 4	→ Disjointed
Segments-0 and 1	→ Continuous								
Segments-1 and 2	→ Partially overlapped								
Segments-2 and 3	→ Fully overlapped								
and Segments-2 and 4	→ Disjointed								
3	<p><b>Describe the addressing modes 8086 with examples from instruction set of 8086.</b> (Apr/May 2016) (13M) BTL 6</p> <p><b>Ans:</b> Refer Yu-Cheng Liu, Glenn A.Gibson, PG.NO:35-39</p> <ul style="list-style-type: none"> <li>• Register operand addressing. (1M)</li> <li>• Immediate operand addressing. (1M)</li> <li>• Memory operand addressing. (1M)</li> <li>• Direct Addressing (1M)</li> <li>• Register Indirect Addressing (1M)</li> <li>• Based Addressing (2M)</li> <li>• Indexed Addressing (2M)</li> <li>• Based Indexed Addressing and (2M)</li> <li>• Based Indexed with displacement. (2M)</li> </ul>								
4	<p><b>What is a ‘REP’ instruction? Discuss. (3M)</b> <b>Write an 8086 ALP to find the sum of numbers in an array of 10 elements.(7M) (Apr/May 2016) BTL 3</b></p>								

'REP' stands for repeat and is used for repeating basic string operations—required for processing arrays of data.

There are a number of repeat instructions available and are used as a prefix in string instructions. The prefixes for use with the basic string instructions are shown in Fig. 14.19.

Prefix	Used with	Meaning
REP	MOVS STOS	Repeat while not end of string $CX \neq 0$
REPE/REPZ	CMPS SCAS	Repeat while not end of string and strings are equal $CX \neq 0$ and $ZF = 1$
REPNE/REPNZ	CMPS SCAS	Repeat while not end of string and strings are not equal $CX \neq 0$ and $ZF = 0$

(3M)

```

DATA SEGMENT
ARR DB 5,3,7,1,9,2,6,8,4,10
LEN DW $-ARR
SUM DW ?
DATA ENDS
CODE SEGMENT
ASSUME DS:DATA CS:CODE
START:
MOV AX,DATA
MOV DS,AX
LEA SI,ARR
MOV AX,0
MOV CX,LEN
REPEAT:
MOV BL,ARR[SI]
MOV BH,0
ADD AX,BX
INC SI
LOOP REPEAT
MOV SUM,AX
MOV AH,4CH
INT 21H
CODE ENDS
END START

```

(7M)

- 5 List the basic string instructions and the operations they perform. (3M) BTL 3  
 Write an 8086 ALP for Multiplication of two 8-bit numbers. BTL 3

Mnemonic	Meaning	Format	Operation
LOOP	Loop	LOOP Short-label	$(CX) \leftarrow (CX) - 1$ Jump is initiated to location defined by short-label if $(CX) \neq 0$ ; otherwise, execute next sequential instruction.
LOOPE/LOOPZ	Loop while equal/loop while zero	LOOPE/LOOPZ Short-label	$(CX) \leftarrow (CX) - 1$ Jump to the location by short-label if $(CX) \neq 0$ and $(ZF) = 1$ ; otherwise execute next sequential instruction.
LOOPNE/ LOOPNZ	Loop while not equal/ loop while not zero	LOOPNE/LOOPNZ Short-label	$(CX) \leftarrow (CX) - 1$ Jump to the location defined by short label if $(CX) \neq 0$ and $(ZF) = 0$ ; otherwise execute next sequential instruction

(3M)

DATA SEGMENT

VAR1 DB 0EDH

VAR2 DB 99H

RES DW?

DATA ENDS

ASSUME CS: CODE, DS:DATA

CODE SEGMENT

START: MOV AX, DATA

MOV DS, AX

MOV AL, VAR1

MOV BL, VAR2

MUL BL

MOV RES, AX

MOV AH, 4CH

INT 21H

CODE ENDS

END START

(7M)

6 Explain the different instruction used for input and output operation in I/O mapped I/O mode of 8086. (13M) BTL 5

**Ans:** Refer. Doughlas V.Hall, PG.NO:B3 &B5

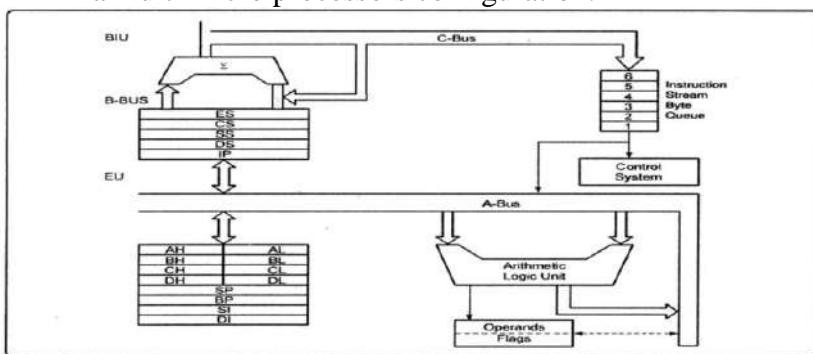
- In this scheme, there is only one address space. This address space is allocated to both memory and I/O devices. Some addresses are assigned to memories and some to I/O devices.
- The address for I/O devices is different from the addresses which have been assigned to memories. An I/O device is also treated as a memory location. In this scheme one address is assigned to each memory location and one address is assigned to each I/O device.
- In this scheme, all data transfer instructions of the microprocessor can be used for transferring data from and to either memory or I/O devices.
- For example, MOV D,M instruction would transfer one byte of data from a memory location or an input device to the register D, depending on whether the address in the H-L register pair is assigned to a memory location or to an input device.
- If H-L contains address of a memory location, data will be transferred from that memory location to register D, while if H-L pair contains the address of an input device, data will be transferred from that input device to register D.
- This scheme is suitable for small systems. In this scheme, IO/ M signal is not used to distinguish between memory and I/O devices. An I/O device is interfaced in the same

	manner as a memory device.	(10M)
		(3M)
9	i) Write an 8086 ALP to sort out any given ten numbers in ascending and descending order. (Nov 2013) (10M) ii) Give the functions of NMI, BHE and TEST pins of 8086. (3) (Nov 2013) BTL 3 Refer Yu-Cheng Liu, Glenn A.Gibson PG.NO:26	
	<b>Ascending Order</b> DATA SEGMENT STRING1 DB 99H,12H,56H,45H,36H DATA ENDS CODE SEGMENT ASSUME CS:CODE,DS:DATA START: MOV AX,DATA MOV DS,AX MOV CH,04H UP2: MOV CL,04H LEA SI,STRING1 UP1: MOV AL,[SI] MOV BL,[SI+1] CMP AL,BL JC DOWN MOV DL,[SI+1] XCHG [SI],DL MOV [SI+1],DL DOWN: INC SI DEC CL JNZ UP1 DEC CH JNZ UP2	DATA SEGMENT STRING1 DB 99H,12H,56H,45H,36H DATA ENDS CODE SEGMENT ASSUME CS:CODE,DS:DATA START: MOV AX,DATA MOV DS,AX MOV CH,04H UP2: MOV CL,04H LEA SI,STRING1 UP1:MOV AL,[SI] MOV BL,[SI+1] CMP AL,BL JNC DOWN MOV DL,[SI+1] XCHG [SI],DL MOV [SI+1],DL DOWN: INC SI DEC CL JNZ UP1 DEC CH JNZ UP2 INT 3
		(10M)
10	<b>Non Maskable Interrupt</b> Interrupt cannot be disabled by any software instruction. This interrupt is activated by low to high transition on 8086 NMI input pin. <b>BHE</b> : The bus high enable is used to indicate the transfer of data over the higher order ( D15-D8 ) data bus. It goes low for the data transfer over D15-D8 and is used to derive chip selects of odd address memory bank or peripherals. <b>TEST</b> : This input is examined by a ‘WAIT’ instruction. If the TEST pin goes low, execution will continue, else the processor remains in an idle state. The input is synchronized internally during each clock cycle on leading edge of clock.	(1M) (1M) (1M)
10	i) Explain briefly about internal hardware architecture of 8086 microprocessor with a	

**neat diagram.(10M) ii) Write a 8086 assembly language program to convert BCD data - Binary data.(3M) (May 2015) (Apr/May 2017). APRIL/MAY 2019. BTL 5**

**Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, PG.NO:26-33**

- It is a 16-bit Microprocessor ( $\mu$ p). Its ALU, internal registers works with 16bit binary word.
- 8086 has a 20 bit address bus can access up to  $2^{20} = 1$  MB memory locations.
- 8086 has a 16bit data bus. It can read or write data to a memory/port either 16bits or 8 bit at a time.
- It can support up to 64K I/O ports.
- It provides 14, 16 -bit registers.
- Frequency range of 8086 is 6-10 MHz
- It has multiplexed address and data bus AD0- AD15 and A16 – A19.
- It requires single phase clock with 33% duty cycle to provide internal timing.
- It can prefetch upto 6 instruction bytes from memory and queues them in order to speed up instruction execution.
- It requires +5V power supply.
- A 40 pin dual in line package.
- 8086 is designed to operate in two modes, Minimum mode and Maximum mode.
- The minimum mode is selected by applying logic 1 to the MN / MX# input pin. This is a single microprocessor configuration.
- The maximum mode is selected by applying logic 0 to the MN / MX# input pin. This is a multi micro processors configuration.



(10M)

**DATA SEGMENT**

BCD DW 27H

BIN DW ?

**DATA ENDS**

**CODE SEGMENT**

ASSUME CS:CODE,DS:DATA

START: MOV AX,DATA

MOV DS,AX

MOV AX,BCD

AND AX,07H

MOV BX,AX

MOV AX,BCD

AND AX,0F0H

MOV CX,0AH

MUL CX

ADD AX,BX

MOV BIN,AX

MOV AH,4CH

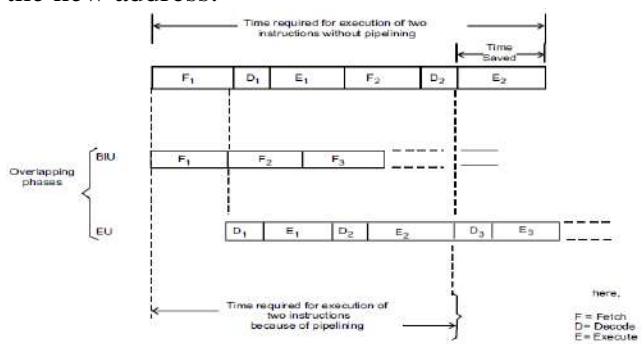
	INT 21H CODE ENDS END START	(3M)
11	<p>i) Explain about ASSUME, EQU, DD assembler directives.(6)  ii) Explain briefly about interrupt handling process in 8086.(7) (May 2015) BTL 5</p> <p><b>Ans:</b> Refer. Doughlas V.Hall, PG.NO:6.31-6.32</p> <p><b>ASSUME :</b> assume logical segment name</p> <p>It is used to assign the names of the logical segments used in the program.</p> <p><b>Syntax :</b> ASSUME segment register : name</p> <p>Eg) ASSUME CS : CODE  ASSUME DS : DATA</p> <p><b>DD : Define Double Word</b></p> <p>It is used to reserve four bytes</p> <p><b>Syntax :</b> Name of the variable DD Initial values</p> <p>Eg) number DD 12345678</p> <p><b>EQU : Equate</b></p> <p>It is used to assign a label with a value or a symbol. The use of this directive is to reduce the recurrence of the numerical values or constants in a program.</p> <p><b>Syntax :</b> name EQU expression/text</p> <p>Eg) label EQU 0500H</p> <p>Addition EQU ADD</p> <p>When an interrupt occurs (hardware or software), the following things happen: The contents of flags register, CS and IP are pushed on to the stack.TF and IF are cleared which disable single step and INTR interrupts respectively. Program jumps to the starting address of ISS. At the end of ISS, when IRET is executed in the last line, the contents of flag register, CS and IP are popped out of the stack and placed in the respective registers. When the flags are restored, IF and TF get back their previous values.</p>	(2M)
		(7M)
1	<p><b>PART * C</b></p> <p><b>1 Explain Complete arithmetic operation, (15M) BTL 5</b></p> <p><b>AAA: ASCII Adjust After Addition</b> The AAA instruction is executed after an ADD instruction that adds two ASCII coded operands to give a byte of result in AL. The AAA instruction converts the resulting contents of AL to unpacked decimal digits. After the addition, the AAA instruction examines the lower 4 bits of AL to check whether it contains a</p>	

valid BCD number in the range 0 to 9. If it is between 0 to 9 and AF is zero, AAA sets the 4 high order bits of AL to 0. The AH must be cleared before addition. If the lower digit of AL is between 0 to 9 and AF is set, 06 is added to AL. The upper 4 bits of AL are cleared and AH is incremented by one. If the value in the lower nibble of AL is greater than 9 than the AL is incremented by 06, AH is incremented by 1, the AF and CF flags are set to 1, and the higher 4 bits of AL are cleared to 0. The remaining flags are unaffected. The AH is modified as sum of previous contents (usually 00) and the carry from the adjustment. This instruction does not give exact ASCII codes of the sum, but they can be obtained by adding 3030H to AX. (5M)

**AAS: ASCII Adjust AL After Subtraction** AAS instruction corrects the result in AL register after subtracting two unpacked ASCII operands. The result is in unpacked decimal format. If the lower 4 bits of AL register are greater than 9 or if the AF flag is 1, the AL is decremented by 6 and AH register is decremented by 1, the CF and AF are set to 1. Otherwise, the CF and AF are set to 0, the result needs no correction. As a result, the upper nibble of AL is 00 and the lower nibble may be any number from 0 to 9. The procedure is similar to the AAA instruction. AH is modified as difference of the previous contents (usually zero) of AH and the borrow for adjustment. (10M)

2 Explain the operations of instructions queue residing in BIU (May 2017) (15M) BTL 6

- The instruction queue is 6-bytes in length, operates on FIFO basis, and receives the instruction codes from memory.
- BIU fetches the instructions meant for the queue ahead of time from memory.
- In case of JUMP and CALL instructions, the queue is dumped and newly formed from the new address.



(15M)

3 Explain the Programmers model of 8086 (May 2018) (15M) BTL 5

- Data group, pointers and index group, status and control flag group and segment group.
- The data group consists of AX (accumulator), BX (base), CX (count) and DX (data).
- Pointer and Index group consist of SP (Stack pointer), BP (Base pointer), SI (Source Index), DI (Destination index) and IP (Instruction pointer).
- Segment group consists of ES (Extra Segment), CS (Code Segment), DS (Data Segment) and SS (Stack Segment).

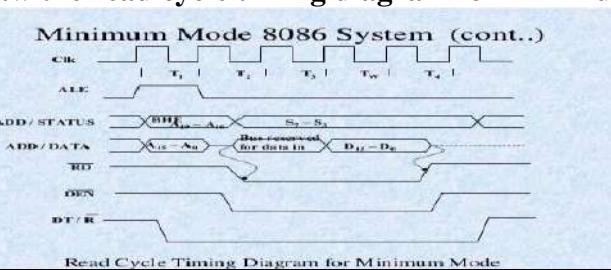


(15M)

## UNIT II

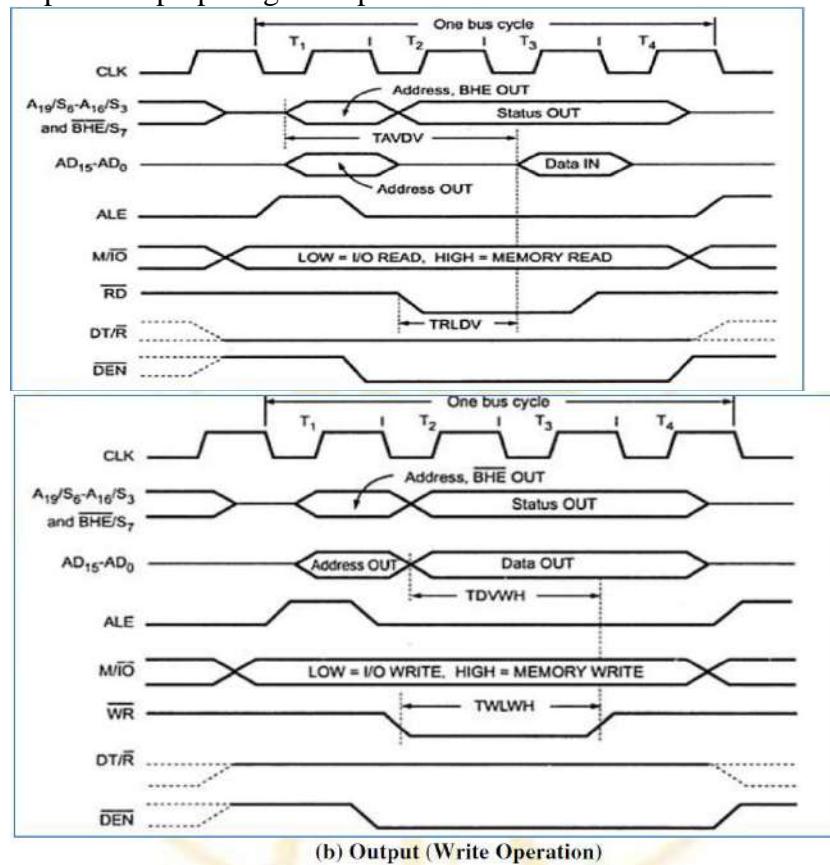
**8086 signals – Basic configurations – System bus timing – System design using 8086 – I/O programming – Introduction to Multiprogramming – System Bus Structure – Multiprocessor configurations – Coprocessor, Closely coupled and loosely Coupled configurations – Introduction to advanced processors.**

<b>Q. No.</b>	<b>Questions &amp; Answers</b>
1	<b>What is meant by multiprocessor system? BTL 1</b> If a microprocessor system contains two or more components that can execute instructions independently then the system is called as multiprocessor system.
2	<b>What is meant by multiprogramming? (Apr/May 2017) BTL 1</b> Multitasking has the same meaning of multiprogramming but in a more general sense, as it refers to having multiple (programs, processes, tasks, threads) running at the same time. This term is used in modern operating systems when multiple tasks share a common processing resource (e.g., CPU and Memory). Multiprogramming is a rudimentary form of parallel processing in which several programs are run at the same time on a uniprocessor. Since there is only one processor, there can be no true simultaneous execution of different programs.
3	<b>What is closely coupled configuration BTL 1</b> If the processor supporting processor, clock generator, bus control logic, memory and I/O System, communicate shared memory then it is called closely coupled system.
4	<b>What the advantages are of loosely coupled? BTL 1 APRIL/ MAY 2019 BTL 1</b> <ul style="list-style-type: none"> <li>• Better system throughput by having more than one processor.</li> <li>• A greater degree of parallel processing can be achieved.</li> <li>• System structure is more flexible.</li> <li>• A failure in one module does not cause any breakdown of the system.</li> </ul>
5	<b>What is meant by memory contention &amp; hot spot contention? BTL 1</b> <ul style="list-style-type: none"> <li>• A memory module can handle only one access request at a time. Hence when several processors request the same memory module it gives rise to memory contention.</li> <li>• When several processors repeatedly access the same memory location, it gives rise to hot spot contention.</li> </ul>
6	<b>What is meant by bus arbitration? BTL 1</b> The mechanism which decides the selection of current master to access bus is known as bus arbitration.
7	<b>What are the advantages of Daisy Chaining? BTL 1</b> <ul style="list-style-type: none"> <li>• It is simple and cheaper method</li> <li>• It requires the least number of lines and this number is independent of the number of masters in the system.</li> </ul>
8	<b>What is meant by bus arbitration? BTL 1</b> The mechanism which decides the selection of current master to access bus is called bus arbitration.
9	<b>What is meant by Numeric processor? BTL 1</b> The numeric processor 8087 is a coprocessor which has been specially designed to work under the control of the processor 8086 and to support additional numeric processing capabilities.
10	<b>On which data types can memory operands operate? BTL 1</b> 1. Word integer, 2. Short integer, 3. Long integer, 4. Packed BCD, 5. Short real, 6. Long Real 7. Temporary real
11	<b>What is the use of TC STOP Mode? BTL 1</b> If the TC Stop bit is set the channel is disabled after the TC output goes high, thus automatically preventing further DMA Operation on that channel.
12	<b>What are advantages of coprocessor? (May 2014) BTL 1</b> The co-processors & supplementary processors which can fetch operands & execute it. It can read CPU status & queue status, make bus and interrupt request, receive reset & ready signals, receive bus grants, maintain an instruction queue decode the external op code.
13	<b>What is co-processor? (Nov 2013) BTL 1</b>

	The 8086/8088 must be supplemented with co-processors that extends the instruction set to allow the necessary special computations to be accomplished more efficiently. Eg: 8087 Numeric Data Processor.
14	<b>What is a Floating point Coprocessor? (Nov 2013) BTL 1</b> The floating point coprocessor uses real data types or floating point types of the following format: Real data $X = \pm 2^{\text{exp}} \times \text{mantissa}$ , which may vary from extremely small to extremely large values.
15	<b>What is meant by loosely coupled configuration? (May 2014) (Apr/May 2016) BTL 1</b> In a loosely coupled multiprocessor system each CPU has its own bus control logic and bus arbitration is resolved by extending this logic and adding external logic that is common to all the modules.
16	<b>Differentiate external vs. internal bus. (Apr/May 2016) BTL 4</b> The internal data bus is the one responsible for transferring the data between the data registers and each other or between the data registers and the CPU. The external data bus transfers the data between the internal registers and the external memory or directly to the output.
17	<b>Define Bus. Why Bus request and cycle stealing are required? (May 2015) BTL 1</b> Bus is a group of parallel conductors which carries data, address and control signals from one unit to another unit. Bus request and Cycle stealing are required to access the RAM without interfering with the CPU. It is similar to DMA for allowing I/O controllers to read or write RAM without CPU intervention.
18	<b>Draw the read cycle timing diagram for minimum mode. (May 2015) BTL 2</b>  A detailed timing diagram for a 8086 system in minimum mode. It shows the following signals over time: Clk (clock), ALE (Address Latch Enable), ADD / STATUS (Address/Status bus), ADD / DATA (Address/Data bus), RD (Read), DEN (Data Enable), and DT/R (Data Transfer/Ram). The ADD / STATUS bus shows address lines A15-A10 and S2-S1. The ADD / DATA bus shows data lines D15-D8 and D15-D8. The RD signal is asserted during T1 and T2. The DEN signal is asserted during T3. The DT/R signal is asserted during T4. The diagram is labeled "Read Cycle Timing Diagram for Minimum Mode".
19	<b>Write some example for advanced processor. (Apr/May 2017) BTL 1</b> ARM Processor AMD Processor
20	<b>What is the function of BHE signal in 8086? BTL 1</b> BHE signal means Bus High Enable signal. The BHE signal is made low when there is some read or write operation is carried out. ie .When ever the data bus of the system is busy i.e. whenever there is some data transfer then the BHE signal is made low.
21	<b>State the significance of LOCK signal in 8086? BTL 1</b> If 8086 is working at maximum mode, there are multiprocessors are present. If the system bus is given to a processor then the LOCK signal is made low. That means the system bus is busy and it cannot be given of any other processors. After the use of the system bus again the LOCK signal is made high. That means it is ready to give the system bus to any processor.
22	<b>What are the functions of status pins in 8086? BTL 1</b> S2 S1 S0 0 0 0 ---- Interrupt acknowledge 0 0 1 ---- Read I/O 0 1 0 ---- Write I/O 0 1 1 ---- Halt 1 0 0 ---- Code access

	<p>1 0 1 ---- Read memory      1 1 0 ---- Write memory      1 1 1 ---- inactive      S4 S3      0 0 --I/O from extra segment      0 1 --I/O from Stack Segment      1 0 --I/O from Code segment      1 1 --I/O from Data segment      S5 --Status of interrupt enable flag      S6 --Hold acknowledge for system bus      S7 --Address transfer</p>
23	<p><b>Give the functions of coprocessor.</b> BTL 1</p> <p>Coprocessors cannot fetch instructions from memory, execute program flow control instructions, do input/output operations, manage memory, and so on. The coprocessor requires the host (main) processor to fetch the coprocessor instructions and handle all other operations aside from the coprocessor functions. In some architecture, the coprocessor is a more general-purpose computer, but carries out only a limited range of functions under the close control of a supervisory processor.</p>
24	<p><b>What is the need for multi processor system?</b> BTL 1</p> <p>Due to the limited data width and lack of floating point arithmetic instructions, 8086 requires many instructions for computing even single floating point operation. For this NDP (8087) is used. Some processor like DMA controllers can help 8086 with low level operations while the CPU can take care of high level operations.</p>
25	<p><b>What is Multiprocessing?</b> BTL 1</p> <p>Multiprocessing is the use of two or more central processing units (CPUs) within a single computer system. The term also refers to the ability of a system to support more than one processor and/or the ability to allocate tasks between them.</p>
30	<p><b>Define system bus timing.</b> BTL 1</p> <p>Timing diagram of 8086 bus cycles includes general bus operation, memory &amp; I/O read cycle and memory &amp; I/O write cycle in minimum mode operation. memory &amp; I/O read cycle and memory &amp; I/O write cycle in maximum mode operation. Interrupt acknowledgement, bus request, bus grant timing in minimum and maximum mode operation.</p>
31	<p><b>Draw the format of the Flag register. APRIL/ MAY 2019</b> BTL 1</p>
<b>Part B/Unit II</b>	
1.	<p><b>Explain system bus timings in 8086. (13M) (Apr/May 2016) (Apr/May 2017)</b> BTL 5</p> <p><b>Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, PG.NO:324-329</b></p> <p>When processor is ready to initiate the bus cycle, BHE, M/IO, DEN and DT/R must be stable i.e. DEN = high and DT/R = 0 for input or DT/R = 1 for output.</p>

2. At the trailing edge of ALE, ICs 74LS373 or 8282 latches the address.  
 3. During T2 the address signals are disabled and S3-S7 are available on AD16/S3-AD19/S6 and BHE/S7. In case of Input operation, is activated during T2 and AD0 to AD15 go in high impedance preparing for input. (6M)



(7M)

2. Explain in detail about IO programming. (May 2014) BTL 2

**Input port:**

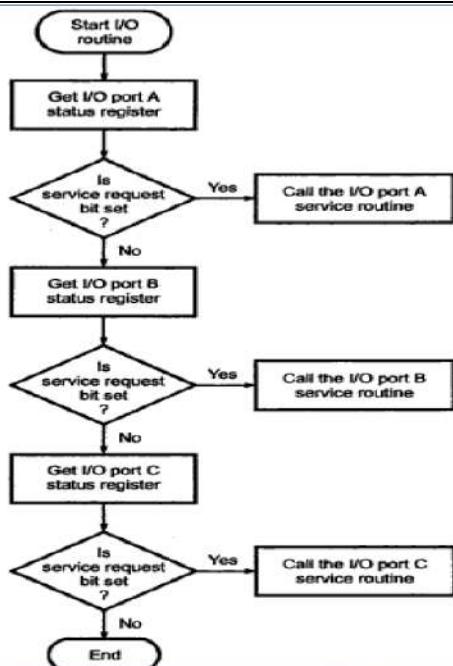
It is used to read data from the input device such as keyboard. The simplest form of input port is a buffer. The input device is connected to the microprocessor through buffer. This buffer is a tri-state buffer and its output is available only Enable when enable signal is active. When microprocessor wants to read data from the input device (keyboard), the control signals from the microprocessor activates the buffer by asserting enable Input of the buffer, once the buffer is enabled, data train the Input device is available on the data bus. Microprocessor reads this data by Initiating read command. (5M)

**Output port:**

It is used to send data to the output device such as display from the microprocessor. The simplest form of output port is a latch. The output device is connected to the microprocessor through latch. When microprocessor wants to send data to the output device, it puts the data on the data bus and activates the clock signal of the latch. (5M)

**Programmed I/O:**

I/O operations will mean a data transfer between an I/O device and memory or between an I/O device and the CPU. If any computer system I/O operations are completely controlled by the CPU, then that system is said to be using ‘programmed I/O’.



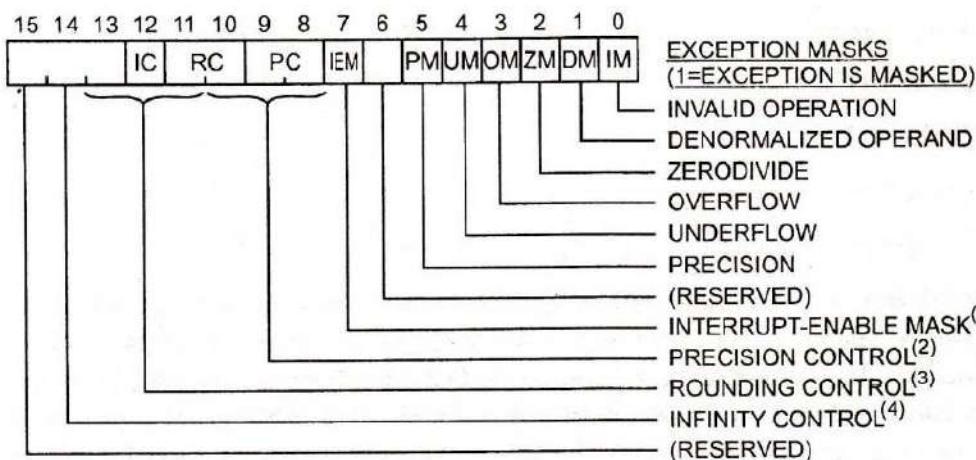
(3M)

3. Explain the execution steps of 8087 coprocessor. (8) (May 2014) (Apr/May 2016) BTL 4  
Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, PG.NO:456-460

#### Features of 8087:

1. It can operate on data of the integer, decimal, and real types, with lengths ranging from 2 to 10 bytes.
2. Its instruction set not only includes various forms of addition and subtraction, but also provides many useful functions such as square root, exponential, tangent, and so on.
3. It is high performance numeric data processor. It can multiply two 64-bit real numbers in about 27  $\mu$ s and calculate square root in about 36  $\mu$ s.
4. It follows IEEE floating point standard.
5. It is multibus compatible.

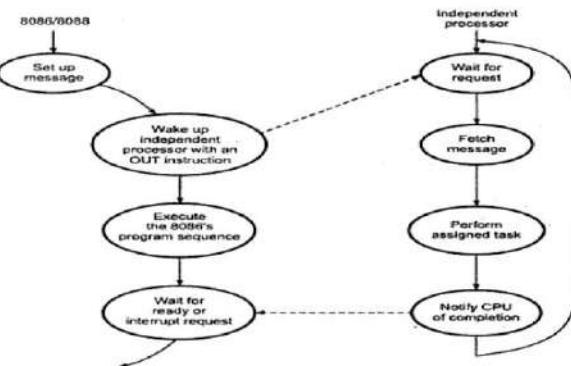
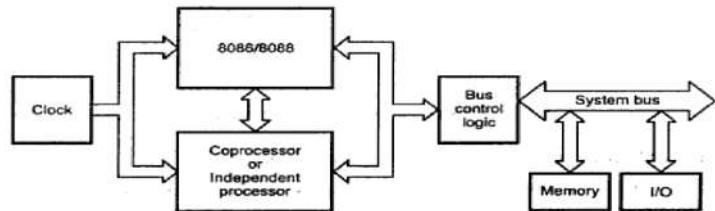
(8M)



(5M)

4. Explain the closely coupled configuration of multi-processor configuration with Suitable diagram. (May 2015) (Apr/May 2016) (Apr/May 2017) BTL 4  
Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, PG.NO:460-467

- It has P processors, M memory modules and C I/O channels.  
 They are connected through a set of 3 interconnection networks.
- PMIN (Processor Memory Interconnection Network)
  - IOPIN (I/O Processor Interconnection Network)
  - ISIN (Interrupt Signal Interconnection Network)
- (8M)



(5M)

5. Discuss the maximum mode configuration of 8086 with a neat diagram. Mention the functions of various signals. (16) (May 2015)APRIL/ MAY 2019BTL 6

**Ans:** Refer Yu-Cheng Liu, Glenn A.Gibson, PG.NO:314-324

#### Maximum Mode Configurations:

Fig. shows the typical maximum mode configuration. In the maximum mode additional circuitry is required to translate the control signals. The additional circuitry converts the status signals ( $\bar{S}_2 - \bar{S}_0$ ) into the I/O and memory transfer signals. It also generates the control signals required to direct the data flow and for controlling 8282 latches and 8286 transceivers. The Intel 8288 bus controller is used to implement this control circuitry.

Fig. shows that the 8288 is able to originate the address latch enable signal to the 8282's, the enable and direction signals to the 8286 transceivers, and the interrupt acknowledge signal to the interrupt controller. It also decodes the  $\bar{S}_2 - \bar{S}_0$  signals to generate MRDC, MWTC, IORC, IOWC, MCE/PDEN, AEN, IOB, CEN, AIOWC, and AMWC signals.

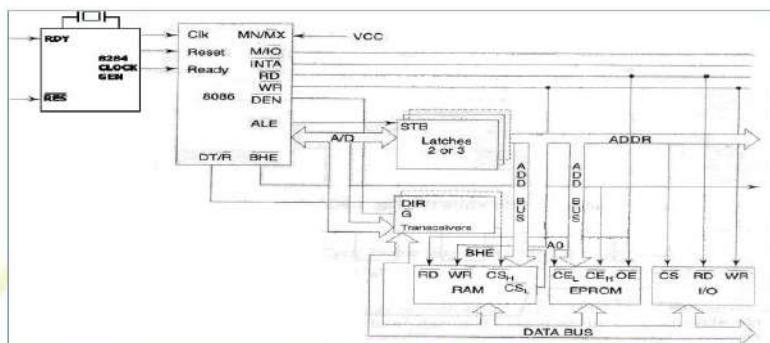
**MRDC (Memory Read Command)** : It instructs the memory to put the contents of the addressed location on the data bus.

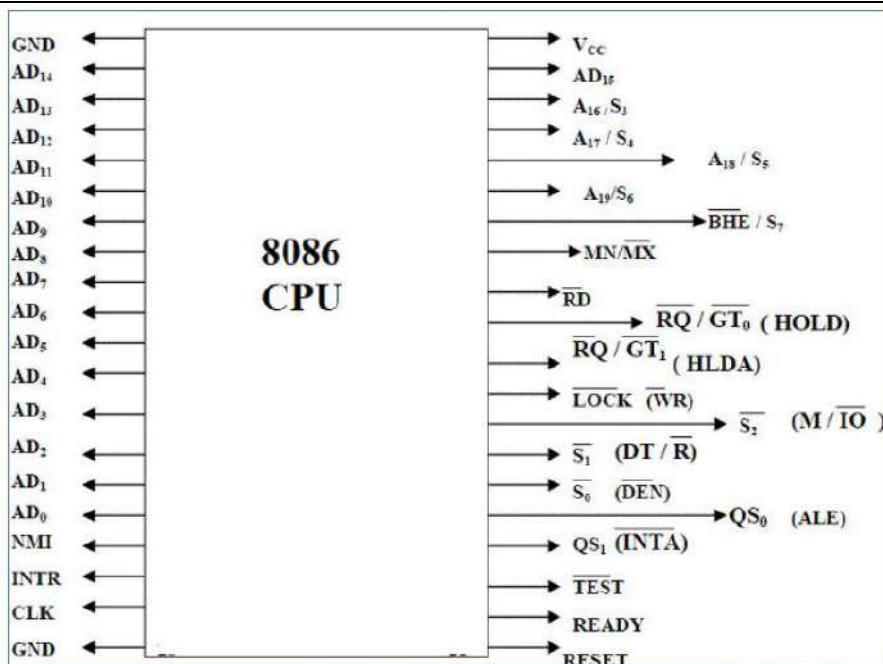
**MWTC (Memory Write Command)** : It instructs the memory to accept the data on the data bus and load the data into the addressed memory location.

(8M)

	<p style="text-align: right;">(5M)</p>
6.	<p><b>Write an 8086 assembly language program to check whether the given string is palindrome. BTL 3</b></p> <p><b>Ans: Refer Notes</b></p> <p>DATA SEGMENT</p> <p>BLOCK1 DB 'MALAYALAM'</p> <p>MSG1 DB "IT IS PALINDROME \$"</p> <p>MSG2 DB "IT IS NOT PALINDROME \$"</p> <p>PAL DB 00H</p> <p>DATA ENDS</p> <p>PRINT MACRO MSG</p> <p>MOV AH,09H</p> <p>LEA DX,MSG</p> <p>INT 21H</p> <p>INT 3H</p> <p>ENDM</p> <p>EXTRA SEGMENT</p> <p>BLOCK2 DB 9 DUP(?)</p> <p>EXTRA ENDS</p> <p>CODE SEGMENT</p> <p>ASSUME CS:CODE,DS:DATA,ES:EXTRA</p> <p>START: MOV AX,DATA</p> <p>MOV DS,AX</p> <p>MOV AX,EXTRA</p> <p>MOV ES,AX</p> <p>LEA SI,BLOCK1</p> <p>LEA DI,BLOCK2+8</p> <p>MOV CX,00009H</p> <p>BACK: CLD</p> <p>LODSB</p> <p>STD</p> <p>STOSB</p> <p>LOOP BACK</p> <p>LEA SI,BLOCK1</p> <p>LEA DI,BLOCK2</p> <p>MOV CX,0009H</p> <p>CLD</p> <p>REPZ CMPSB</p> <p>JNZ SKIP</p> <p>PRINT MSG1</p> <p>SKIP: PRINT MSG2</p>

	CODE ENDS END START	(13M)
7	<p><b>With neat block diagram explain the architecture of 8086 in minimum mode configuration. Also explain the bus timing diagram for input and output transfer on a maximum mode.</b> <u>APRIL/ MAY 2019</u> BTL 3</p> <p>1. A minimum mode of 8086 configuration depicts a standalone system of computer where no other processor is connected. This is similar to 8085 block diagram with the following difference.</p> <p>2. The Data transceiver block which helps the signals traveling a longer distance to get boosted up. Two control signals data transmit/ receive are connected to the direction input of transceiver (Transmitter/Receiver) and DEN* signal works as enable for this block.</p> <p><b>Steps:</b></p> <p>For interfacing memory module to 8086, it is necessary to have odd and even memory banks. This is implemented by using two EPROMs and two RAMs. Data lines D15-D8 are connected to odd bank of EPROM and RAM, and data lines D7 - D0 are connected to even bank of EPROM and RAM.</p> <p>Address lines are connected to EPROM and RAM as per their capacities.</p> <p>RD signal is connected to the output enable (OE) signals of EPROMs and RAMs.</p> <p>WR signal is connected to WR signal of RAMs.</p> <p>Two separate decoders are used to Generate chip select signals for memory and I/O devices. These chip select signals are logically ORed with either BHE or to generate final chip select signals.</p> <p>RD and WR signals are connected to the RD and WR signals of I/O device.</p> <p>Data lines D15-D0 are connected to the data lines of I/O device</p>	(8M)
8	<b>Explain the pin details of 8086</b> <u>APRIL/ MAY 2018</u> BTL 3 (13M)	(5M)



(3M)  
(10)**Functional Description****9. Explain in detail about IO programming. (13M) BTL 4**

The transfer of data between keyboard and microprocessor, and microprocessor and display device is called input /output data transfer or I/O data transfer. This data transfer is done by using I/O ports.

**Input port:**

It is used to read data from the input device such as keyboard. The simplest form of input port is a buffer. The input device is connected to the microprocessor through buffer. This buffer is a tri-state buffer and its output is available only Enable when enable signal is active. When microprocessor wants to read data from the input device (keyboard), the control signals from the microprocessor activates the buffer by asserting enable Input of the buffer, once the buffer is enabled, data train the Input device is available on the data bus. Microprocessor reads this data by Initiating read command. (4M)

**Output port:**

It is used to send data to the output device such as display from the microprocessor. The simplest form of output port is a latch. The output device is connected to the microprocessor through latch. When microprocessor wants to send data to the output device, it puts the data on the data bus and activates the clock signal of the latch. (3M)

**a. Programmed I/O:**

I/O operations will mean a data transfer between an I/O device and memory or between an I/O device and the CPU. If any computer system I/O operations are completely controlled by the CPU, then that system is said to be using ‘programmed I/O’. (3M)

**b. Interrupt Driven I/O**

The most common method of servicing such device is the polled approach. This is where the processor must test each device in sequence. It needs communication with the processor. It is easy to see that a large portion of the main program is looping through this continuous polling cycle. Allows the processor to execute its main program and only stop to service peripheral devices when it is told to do so by the device itself.

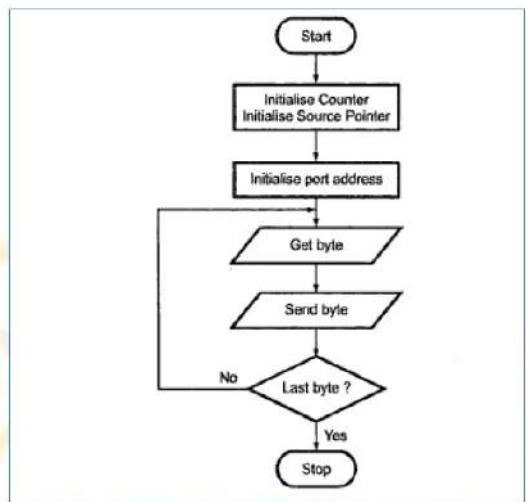
The method would provide an external asynchronous input to the processor. Instruction that is currently being executed and fetch a new routine that will service the requesting device. Once this servicing is completed, the processor would resume exactly where it

left off.

This method of servicing I/O request is called Interrupt driven I/O. When a processor is interrupted, It stops executing its current program and calls a special routine which services the Interrupt. Interruption is called Interrupt and the special routine executed to service the Interrupt is called Interrupt Service routine (ISR).

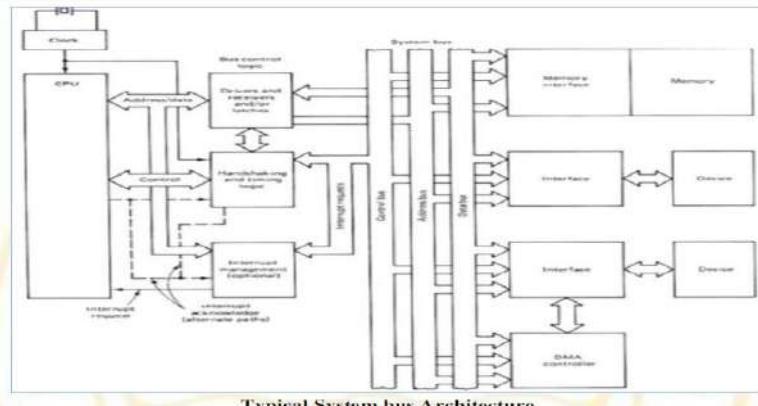
### c. Direct Memory Access (DMA) Transfer

In software control data transfer, processor executes a series of instructions to carry out data transfer. For each instruction execution fetch, decode arid execute phases are required. Fig. gives the flowchart to transfer data from memory to I/O device. So this method of data transfer is not suitable for large data transfers.



(3M)

- 10 Write short notes on System Bus Structure. (13M) BTL 3



(3M)

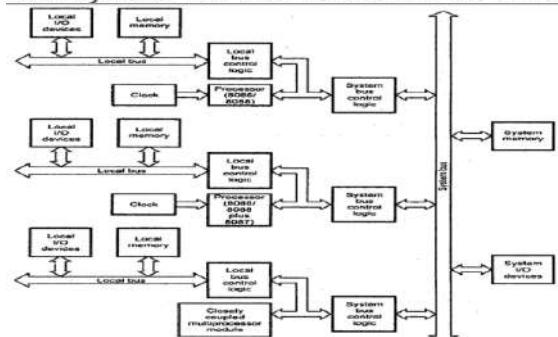
The complexity of the bus control logic depends in the amount of translation needed between the system bus and the pins on the CPU. All of the address and data lines and most of the control lines use are capable of being logically disconnected from the CPU or bus control logic. The timing of the signals within the CPU and bus control logic is controlled by a clock. The bus cycles and CPU activity are controlled by ground of clock pulses. The CPU on put is transaction would processed by outputting the address of the data during first clock cycle.

Read is to take place during the second clock cycle. Waiting an intermediate number of clock cycles for the addressed device to put the data on the data lines, inputting the data and signaling the device that the transfer is complete during the last clock cycle. (10M)

### Part C/ Unit II

- 1 Explain the loosely coupled architecture of 8086. (15M) (May 2016) BTL 3

The Fig. shows nonhierarchical loosely coupled multiprocessor system. In loosely coupled systems, each processor has a set of input-output devices and a large local memory where it accesses most of the instructions and data. The processor, its local memory and input-output interfaces are together called computer module. Processes which execute on different computer modules communicate by exchanging messages through a **Message Transfer System (MTS)**. The coupling in such a system is very loose. Hence, such systems are also referred to as a **distributed systems**.



(15M)

## 2 Discuss Multiprogramming concept in detail (15M) (May 2015) BTL 3

### Multiprogramming:

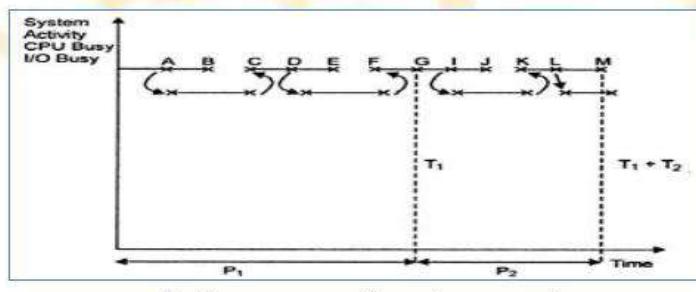
A process can be defined as a programming unit which performs an independent task. A processor that process (execute) serially, because it can process one task at a time that's why it is called **uniprogramming system**. In a **multiprogramming** environment, the codes for two 'or' more processes are in memory at the same time and are executed by time-multiplexing.

The performance of a system is generally measured in terms of the number of jobs completed in a time period (that is referred as **system throughput**).

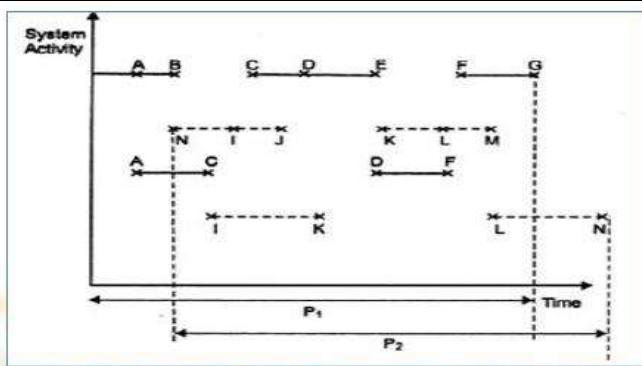
The following Figure presents completion of a task consisting two processes P1 and P2 by using uniprogramming.

1) The P1 starts and continue until F/O is required (Point A), then F/O is initialized and the processing continues in parallel with I/O until the processing requires the input data. At this time it should wait until I/O is finished (Point B).

The 110 in finished (Point C) the processing is resumed and the same description applies to point D, E and F. At the end of P1, P2 can start which has the same operation as that P1.



**Uniprogramming Approach**

**Multiprogramming Approach**

(15M)

**3 List the Features of advanced Microprocessor. (15M) BTL 3****Features (80286)**

- 1) The 80286 is a 16-bit processor. The 16-bit ALU allows to process 16-bit data.
- 2) It has 24-bit address bus. It can access up to 16 Mbytes (2<sup>24</sup>) of physical memory or 1 Gigabyte (2<sup>30</sup>) of virtual memory.
- 3) The 80286 can be operated at three different clock speeds. These are 4 MHz(80286-4), 6 MHz (80286-6), and 8 MHz (80286).
- 4) The 80286 includes special instructions to support operating systems.
- 5) The 80286 is housed in a 68-pin leadless flat package.
- 6) It contains four separate processing units. These are the Bus Unit (BU), the Instruction Unit (lii), the Address Unit (AU) and the Execution Unit (EU)
- 7) The 80286 microprocessor is compatible with their earlier 8086, 8088, 80186 and 80188 chips.
- 8) It has virtual memory-management circuitry and protection circuitry.

**80386 Features:**

- 1) The 80386 is a 32-bit processor. The 32-bit ALU allows to process 32-bit data.
- 2) It has 32-bit address bus.
- 3) The 80386 runs with speed up to 20 MHz instructions per second.
- 4) The pipelined architecture of the 80386, allows simultaneous instruction fetching, decoding, execution and memory management.
- 5) It allows programmers to switch between different operating systems
- 6) It can operate on 7 different data types:
  - a. Bit b. Byte c. Word d. Double word e. word f. Quad word g. Ten byte.
- 7) The 80386 can operate in real mode, protected mode or a variation of protected mode called virtual 8086 mode.

**8) The 80386 microprocessor is compatible with their earlier 8086, 8088.**

(15M)

**UNIT III I/O INTERFACING**

**Memory Interfacing and I/O interfacing - Parallel communication interface – Serial communication interface – D/A and A/D Interface - Timer – Keyboard /display controller – Interrupt controller – DMA controller – Programming and applications Case studies: Traffic Light control, LED display , LCD display, Keyboard display interface and Alarm Controller.**

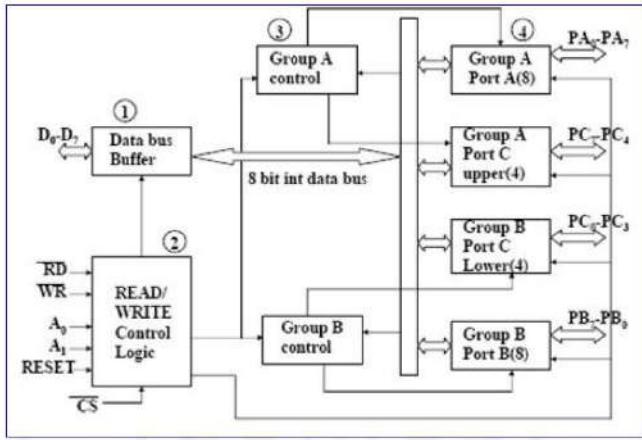
**Part A**

Q. No.	Questions & Answers								
1	<b>Name the Command word to set bit PC, using BSR mode. BTL 1</b> <table border="1" data-bbox="308 1899 1017 1944"> <tr> <td>0</td><td>D6</td><td>D5</td><td>D4</td><td>D3</td><td>D2</td><td>D1</td><td>D0</td></tr> </table> D6,D5,D4 – Don't Care	0	D6	D5	D4	D3	D2	D1	D0
0	D6	D5	D4	D3	D2	D1	D0		

	D3,D2,D1- Bit Select Do- Bit set. Reset
2	<b>Why the 8255A is designed so that only the bits in PORT C can be set/reset? BTL 1</b> Since the pins are designed to activate for selecting Port A and Port B.
3	<b>What is the use of BSR mode in 8255 BTL 1</b> It is used for setting and Reset the Bits
4	<b>List the advantages and disadvantages of parallel communication over serial communication. (Apr/May 2016) BTL 1</b> For transferring data between computers, laptops two methods are used, namely, Serial Transmission and Parallel Transmission. There are some similarities and dissimilarities between them. One of the primary differences is that; in Serial Transmission data is sent bit by bit whereas, in Parallel Transmission a byte (8 bits) or character is sent.
5	<b>What is key bouncing? (Apr/May 2016) BTL 1</b> When a key is pressed the contact bounce back and forth and settle down only after a small time delay (about 20ms). Even though a key is actuated once, it will appear to have been actuated several times. This problem is called Key Bouncing
6	<b>How does 8255 PPI discriminate between the memory section data and I/O section data BTL 1</b> The 8255 PPI discriminate between memory section data and I/O Section by use of the Address lines and by use of the decoder.
7	<b>What is the function of STB and OBF signal in the 8255 when programmed for mode –1 operation? BTL 1</b> The input device activates this signal to indicate CPU that the data to be read is already sent on the port lines of 8255 port.
8	<b>Name the major block of 8259 Programmable Interrupt Controller. BTL 1</b> There are three major blocks 1.Interrupt service register , 2.Priority resolver, 3.Interrrupt Request Register, 4.Interrupt Mask Register
9	<b>What are the modes of operation of 8259 Interrupt Controller? BTL 1</b> 1. Fully Nested Mode, 2.Special Fully Mode, 3.Rotating Priority Mode, 4.Special masked Mode, 5.Polled Mode.
10	<b>What is the maximum number of devices that can be connected to interrupt mode BTL 1</b> We can connect 8 Devices in the interrupt mode
11	<b>Mention the function of SP/EN signal in the 8259 PIC. BTL 1</b> With the help of SP/EN signal it can either be operated in Master mode and Slave Mode
12	<b>Why CAS2-CAS0 lines on 8259 PIC are bi-directional? BTL 1</b> CAS2-CAs0 is used for selecting one of the possible slaves that can be connected.
13	<b>What is the use of address enable (AEN) pin of 8257 DMA Controller? BTL 1</b> ALE is used to differentiate between the Address and Data Signals.
14	<b>What are the operating modes of 8255? (Nov/Dec 2013) BTL 1</b> Mode-0, Mode-1 and Mode-2.
15	<b>What is bus stealing? (Nov/Dec 2013) BTL 1</b> During DMA data transfer, the I/O component connected to the system bus is given control of the system bus for a bus cycle. This is called bus stealing or cycle stealing.
16	<b>What are the advantages of Programmable Interval Timer/Counter IC? (May/Jun 2014)</b> BTL 1 <ul style="list-style-type: none"> <li>• Interrupt a time sharing operating system at evenly spaced intervals.</li> </ul>

	<ul style="list-style-type: none"> <li>• Output precisely timed signals with programmed period to an I/O device.</li> <li>• Count the number of times an event occurs in an external experiment.</li> </ul> <p>Cause the processor to be interrupted after a programmable number of external events have occurred.</p>																																																																		
17	<p><b>List the features of Memory Mapped I/O. (May/Jun 2014) BTL 1</b></p> <ul style="list-style-type: none"> <li>• The device registers can be accessed and manipulated with any instruction or addressing mode.</li> </ul> <p>The maximum number of available memory locations is reduced.</p>																																																																		
18	<p><b>Give the Various modes and Applications of 8254. (May/Jun 2015) BTL 1</b></p> <ul style="list-style-type: none"> <li>• MODE 0 : Interrupt on terminal Count ( can be used as Interrupt).</li> <li>• MODE 1 : Hardware re trigger able One shot (For generating One shot Pulse)</li> <li>• MODE 2 : Rate Generator ( The mode is used to generate a pulse equal to given clock period at a given interval.)</li> <li>• MODE 3: Square wave generator ( For generating continuous square wave)</li> <li>• MODE 4: Software triggered strobe ( To trigger after a specific count)</li> </ul> <p>MODE 5: Hardware triggered strobe ( To Trigger by a hardware event)</p>																																																																		
19	<p><b>Draw the format of read back command register of 8254. (Apr/May 2017) BTL 1</b></p> <p>This register is accessed when lines A0 &amp; A1 are at logic 1. It is used to write a command word, which specifies the counter to be used, its mode, and either a read or write operation. Following table shows the result for various control inputs.</p> <table border="1"> <thead> <tr> <th>A1</th><th>A0</th><th>RD</th><th>WR</th><th>CS</th><th>Result</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write Counter 0</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Write Counter 1</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>Write Counter 2</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>Write Control Word</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Read Counter 0</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>Read Counter 1</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>Read Counter 2</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>No operation</td></tr> <tr> <td>X</td><td>X</td><td>1</td><td>1</td><td>0</td><td>No operation</td></tr> <tr> <td>X</td><td>X</td><td>X</td><td>X</td><td>1</td><td>No operation</td></tr> </tbody> </table>	A1	A0	RD	WR	CS	Result	0	0	1	0	0	Write Counter 0	0	1	1	0	0	Write Counter 1	1	0	1	0	0	Write Counter 2	1	1	1	0	0	Write Control Word	0	0	0	1	0	Read Counter 0	0	1	0	1	0	Read Counter 1	1	0	0	1	0	Read Counter 2	1	1	0	1	0	No operation	X	X	1	1	0	No operation	X	X	X	X	1	No operation
A1	A0	RD	WR	CS	Result																																																														
0	0	1	0	0	Write Counter 0																																																														
0	1	1	0	0	Write Counter 1																																																														
1	0	1	0	0	Write Counter 2																																																														
1	1	1	0	0	Write Control Word																																																														
0	0	0	1	0	Read Counter 0																																																														
0	1	0	1	0	Read Counter 1																																																														
1	0	0	1	0	Read Counter 2																																																														
1	1	0	1	0	No operation																																																														
X	X	1	1	0	No operation																																																														
X	X	X	X	1	No operation																																																														
20	<p><b>What is meant by Direct Memory Access? BTL 1</b></p> <p>Direct Memory Access (DMA) is a capability provided by some computer bus architectures that allows data to be sent directly from an attached device (such as a disk drive) to the memory on the allows data to be sent directly from an attached device (such as a disk drive) to the memory on the computer's motherboard. The microprocessor is freed from involvement with the data transfer, thus speeding up the overall computer.</p>																																																																		
21	<p><b>What is meant by control register? BTL 1</b></p> <p>A control register is a processor register which changes or controls the general behavior of a CPU or other digital device. Common tasks performed by control registers include interrupt control, switching the addressing mode, paging control, and coprocessor control.</p>																																																																		
22	<p><b>Write a 16 bit delay program in 8086 (Apr/May 2017) BTL 1</b></p> <p>LOOP1: MOV DI, 01ADH      LOOP: MOV BP, FFFFH      NOP      NOP      NOP</p>																																																																		

	DEC BP JNZ LOOP1 DEC DI JNZ LOOP
23	<b>Give the applications of I/O interface</b> BTL 1 1. Traffic Light Control 2. LED and LCD Display Alarm Controller
24	<b>List the applications of D/A interface.</b> BTL 1 The DAC find applications in areas like Digitally controlled gains Motor speed controls Programmable gain amplifiers etc.
25	<b>What is mode o operation of 8255? APRIL /MAY 2019.</b> BTL 1 Two 8-bit ports (port A and port B) and two 4-bit ports (port C upper and lower) are available. The two 4-bit ports can be combined used as a third 8-bit port. 2. Any port can be used as an input or output port. 3. Output ports are latched. Input ports are not latched. 4. A maximum of four ports are available so that overall 16 I/O configurations are possible.
26	<b>What are the operating modes in 8279? APRIL /MAY 2019.</b> BTL 1 8279 provides two output modes for selecting the display options. <b>1. Display Scan:</b> In this mode, 8279 provides 8 or 16 character-multiplexed displays those can be organized as dual 4-bit or single 8-bit display units. <b>2. Display Entry:</b> 8279 allows options for data entry on the displays. The display data is entered for display from the right side or from the left side.
<b>Part B/Unit III</b>	
1	<b>With a block diagram of internal structure of 8255 PPI and explain the functions of each block Illustrate the 8255 mode 1 output and input port timings. (Apr/May 2017)</b> BTL 5 (13M) <b>Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, PG.NO:369-377</b> The parallel input-output port chip 8255 is also called as programmable peripheral input-output port. The Intel's 8255 is designed for use with Intel's 8-bit, 16-bit and higher capability microprocessors. It has 24 input/output lines which may be individually programmed in two groups of twelve lines each, or three groups of eight lines. The two groups of I/O pins are named as Group A and Group B. Each of these two groups contain a subgroup of eight I/O lines called as 8-bit port and another subgroup of four lines or a 4-bit port. Thus group A contains an 8-bit port A along with a 4-bit port, C upper. The port A lines are identified by symbols PA0 – PA7 while the port C lines are identified as PC4 – PC7. Similarly, Group B contains an 8-bit port B, containing lines PB0 – PB7 and a port C with lower bits PC0 – PC3. The port C upper and port C lower can be used in combination as an port 8-bit port C. (8M)



(5M)

- 2 With a neat block diagram explain the function of each block of a programmable interrupt controller. (13M) BTL 5

**Ans:** Refer Yu-Cheng Liu, Glenn A.Gibson, PG.NO:361-369

**Interrupt Request Register (IRR):** The interrupts at IRQ input lines are handled by Interrupt Request Register internally. IRR stores all the interrupt requests in it in order to serve them one by one on the priority basis.

**IN-service Register (ISR):** This stores all the interrupt requests those are being served, i.e. ISR keeps track of the requests being served.

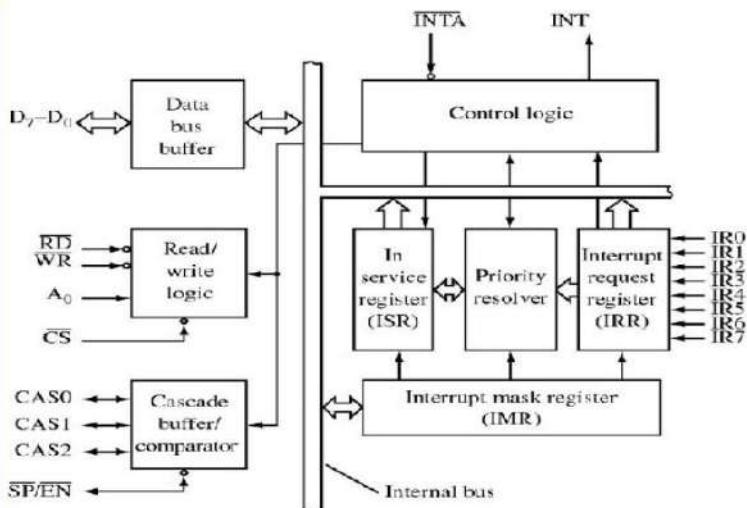
**Priority Resolver:** This unit determines the priorities of the interrupt requests appearing simultaneously. The highest priority is selected and stored into the corresponding bit of ISR during INTA pulse. The IR0 has the highest priority while the IR7 has the lowest priority, normally in fixed priority mode. The priorities however may be altered by programming the 8259A in rotating priority mode.

**Interrupt Mask Register (IMR):** This register stores the bits required to mask the interrupt inputs. IMR operates on IRR at the direction of the Priority resolver.

**Interrupt Control Logic:** This block manages the interrupt and interrupt acknowledge signals to be sent to the CPU for serving one of the eight interrupt requests. This also accepts the interrupt acknowledge (INTA) signal from CPU that causes the 8259A to release vector address on to the data bus.

**Data Bus Buffer:** This tristate bi-directional buffer interfaces internal 8259A bus to the microprocessor system data bus. Control words, status and vector information pass through data buffer during read/write operations.

(8M)



(5M)

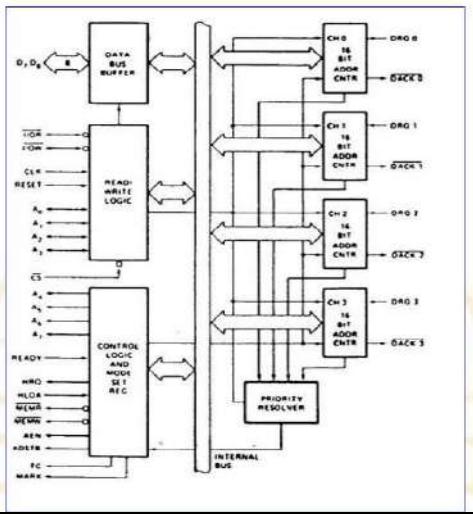
- 3 Draw the block diagram of DMA controller IC and explain the function of each block. (May 2015) & (May 2014) (Apr/May 2016) (Apr/May 2017) (13M) BTL 5

**Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, PG.NO:395-402**

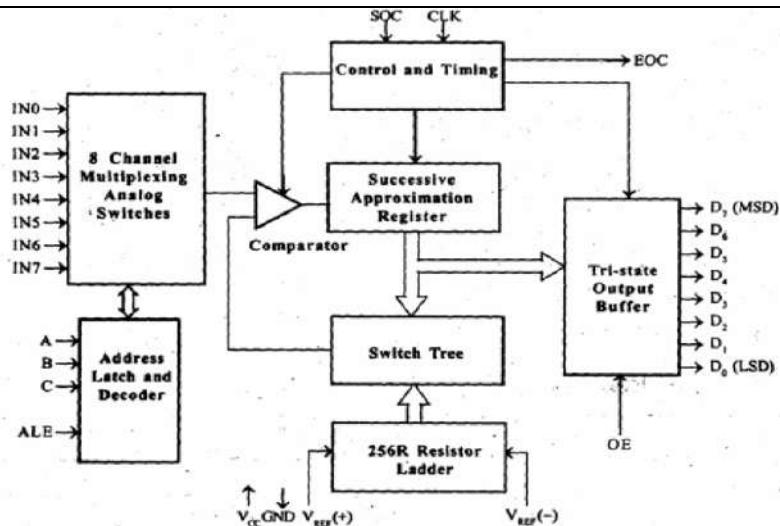
The direct memory access or DMA mode of data transfer is the fastest amongst all the modes of data transfer. In this mode, the device may transfer data directly to/from memory without any interference from the CPU. The device requests the CPU (through a DMA controller) to hold its data, address and control bus, so that the device may transfer data directly to/from the memory. Intel's 8257 is a four channel DMA controller designed to be interfaced with their family of microprocessors. The 8257, on behalf of the devices, requests the CPU for bus access using local bus request input i.e. HOLD in minimum mode. In maximum mode of the microprocessor RQ/GT pin is used as bus request input. On receiving the HLDA signal or RQ/GT signal from the CPU, the requesting device gets the access of the bus, and it completes the required number of DMA cycles for the data transfer and then hands over the control of the bus back to the CPU. The chip supports four DMA channels, i.e. four peripherals can be independently request for DMA data transfer through these channels at a time. The DMA controller has 8-bit internal data buffer, a read/write unit, a control unit, a priority resolving unit along with a set of registers.

**Register organization of 8257:** The 8257 performs the DMA operation over four independent DMA channels. Each of the four channels of 8257 has a pair of two 16-bit registers, namely, DMA address register and terminal count register. Also, there are two common registers for all the channels namely mode set register and status register. The CPU selects one of these registers using A<sub>0</sub> – A<sub>3</sub>.

(8M)



	(5M)
4	<p><b>With a block schematic explain how a (4x4) matrix hex keyboard can be interfaced to a CPU using 8279 keyboard display controller? (Nov 2013) (13M) BTL 5</b></p> <p><b>Ans:</b> Refer Yu-Cheng Liu, Glenn A.Gibson, PG.NO:383-395</p> <p>Intel's 8279 is a general purpose keyboard display controller that simultaneously drives the display of a system and interfaces a keyboard with the CPU leaving the CPU free for its routine task. The keyboard display interface scans the keyboard to identify if any key has been pressed and sends the code if the pressed key to the CPU. This also transmits the data received from the CPU to the display device. The controller performs both of these operations without involving the CPU. The 8279 is a 40 pin device with two major segments, Keyboard and Display. The keyboard can be connected to a max of 64 – contact key matrix. Keyboard entries are denounced and stored in the internal FIFO RAM and an interrupt signal is generated with each entry. The display segment can provide a 16 character (byte) scanned display. This segment contains 16 x 8 R/w memory (RAM), which can be used to read or write information for the display purposes. This 16-byte display RAM can be used either as an integrated block of 16 x 8 bits or 16 x 4 bits of 2 blocks. The internal architecture of 8279 (8M) is shown in the fig.</p>
5	<p><b>Interface a D/A converter and A/D convertor with a microprocessor. Explain with a Program, how to generate a sine wave using this. (May 2015) (13M) BTL 6</b></p> <p><b>Ans:</b> Refer Yu-Cheng Liu, Glenn A.Gibson.,PG.NO:374-377</p> <ul style="list-style-type: none"> <li>ADC0809 is an 8-bit successive approximation type ADC with inbuilt 8-channel multiplexer.</li> <li>The ADC0809 is suitable for interface with 8086 microprocessor.</li> <li>The ADC0809 is available as a 28 pin IC in DIP (Dual Inline Package).</li> <li>The ADC0809 has a total unadjusted error of <math>\pm 1</math> LSD (Least Significant Digit).</li> <li>The ADC0808 is also same as ADC0809 except the error. The total unadjusted error in ADC0808 is <math>\pm 1/2</math> LSD.</li> </ul>

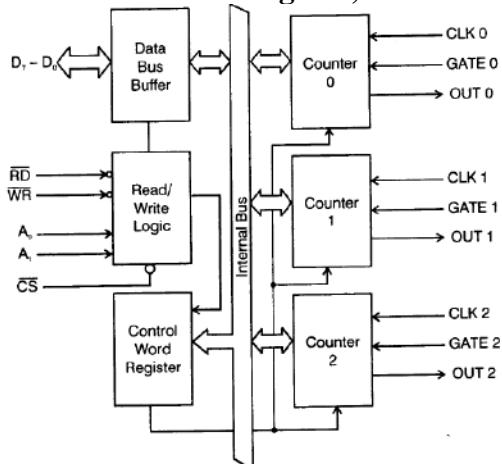


- To convert the digital signal to analog signal a Digital-to-Analog Converter (DAC) has to be employed.
  - The DAC will accept a digital (binary) input and convert to analog voltage or current.
  - Every DAC will have "n" input lines and an analog output.
  - The DAC require a reference analog voltage ( $V_{ref}$ ) or current ( $I_{ref}$ ) source.
  - The smallest possible analog value that can be represented by the n-bit binary code is called resolution.
  - The resolution of DAC with n-bit binary input is  $1/2^n$  of reference analog value.
  - Every analog output will be a multiple of the resolution.
- (13M)

**6 Describe with MODE 0 and MODE 3 configurations of 8254 timer in detail.(13M)**

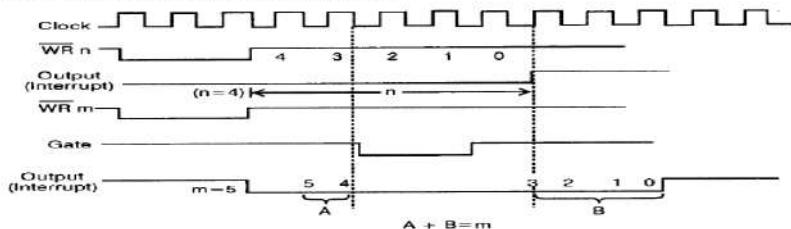
BTL 6

**Ans: Refer Yu-Cheng Liu, Glenn A.Gibson,PG.NO:380-382**



**Mode 0: Interrupt On Terminal Count**

- Mode 0 is typically used for event counting.
- After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.
- GATE = 1 enables counting;
- GATE = 0 disables counting. GATE has no effect on OUT.
- After the Control Word and initial count (say,  $n=4$ ,  $m=5$ ) are written to a Counter, the initial count will be loaded on the next CLK pulse.
- This mode can be used as an interrupt.

**Mode 3: Square Wave Mode**

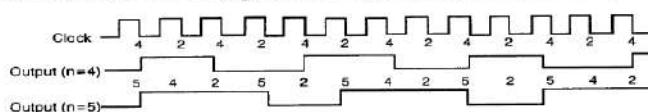
- Mode 3 is typically used for Baud rate generation.
- Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for the remainder of the count.
- Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.
- Mode 3 is implemented as follows:

**Even counts:**

OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.

**Odd counts:**

For odd counts, OUT will be high for  $(N+1)/2$  counts and low for  $(N-1)/2$  counts.



(13M)

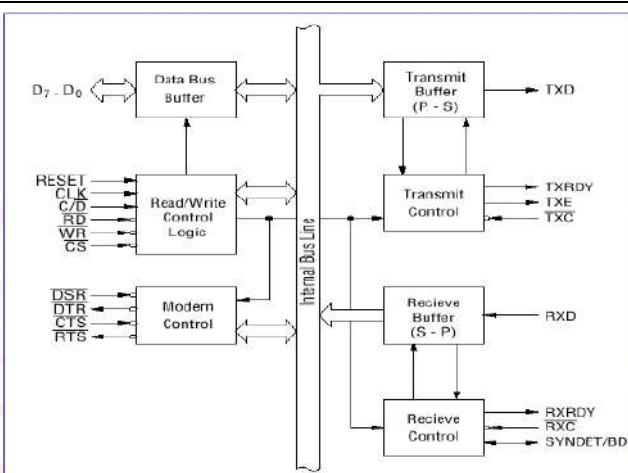
7

- Bring about the features of 8251. (6) (Nov 2013)
- Discuss how 8251 is used for serial data communication. (6). APRIL /MAY 2019.
- Explain the advantages of using the USART chips in microprocessor based systems. (7) (13M) BTL 6

**Ans: Refer Yu-Cheng Liu, Glenn A.Gibson, PG.NO:361-369**

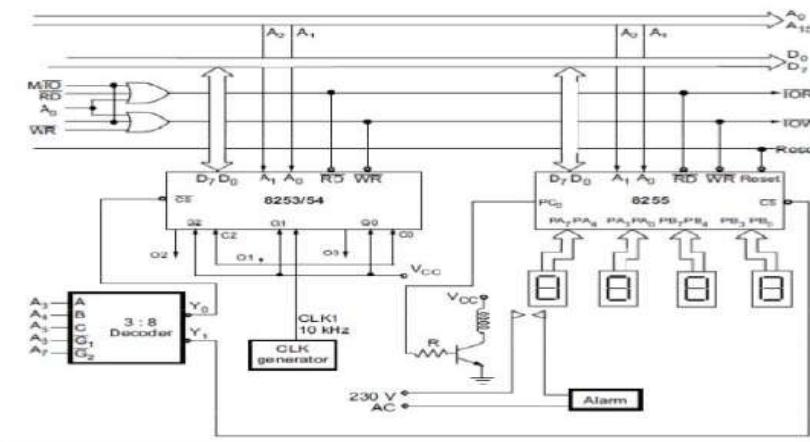
**Architecture of 8251:**

The data buffer interfaces the internal bus of the circuit with the system bus. The read write logic controls the operation of the peripheral depending upon the operations initiated by the CPU. This unit also selects one of the two internal addresses those are control address and data address at the behest of the c/d SIGNAL. The modem control unit handles the modem handshake signals to coordinate the communication between the modem and the USART. The transmit control unit transmits the data byte received by the data buffer from the CPU for further serial communication.

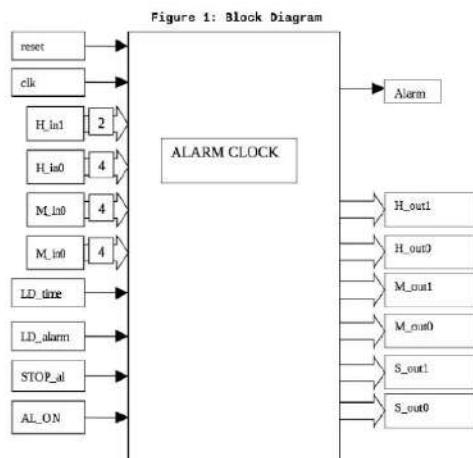


(13M)

- 8 Draw and explain the block diagram of alarm controller. (Apr/May 2016) (13M) BTL 6



(8M)

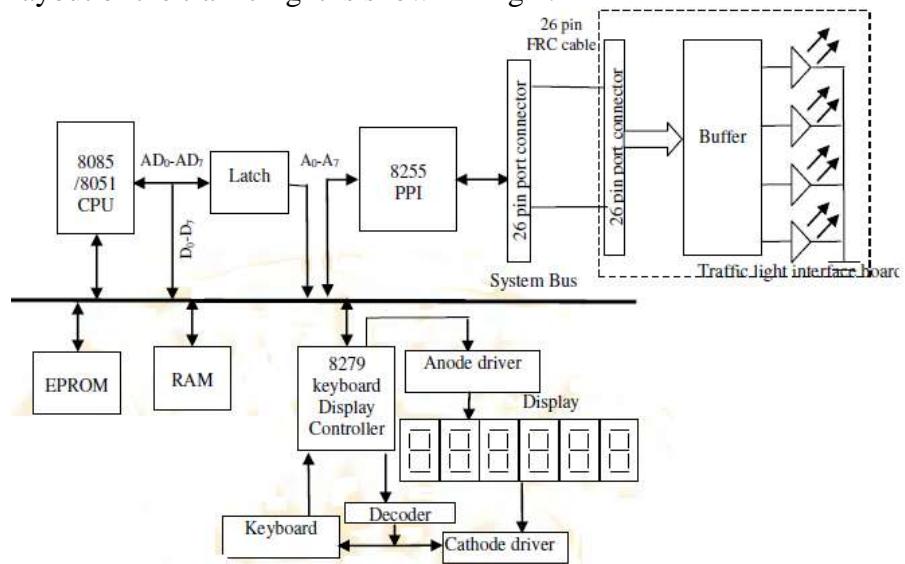


(5M)

- 9 Explain design of Traffic Light Controller using 8086 microprocessor in detail. (May 2015) (13M) BTL 5

The 8085/8051 Microprocessor/ Microcontroller is a popular Microprocessor/Microcontroller used in Industries for various applications. Such as traffic light control, temperature control, stepper motor control, etc. The traffic lights are interfaced to Microprocessor/ Microcontroller system through buffer and ports of programmable peripheral Interface 8255. So the traffic lights can be automatically switched ON/OFF in desired sequence. The Interface board has been designed to work with parallel port of

Microprocessor/ Microcontroller system. The hardware of the system consists of two parts. The first part is Microprocessor / Microcontroller based system. Microprocessor/ Microcontroller as CPU and the peripheral devices like EPROM, RAM, Keyboard & Display Controller 8279, Programmable as Peripheral Interface 8255, 26 pin parallel port connector, 21 keys Hexa key pad and six number of seven segment LED's. The second part is the traffic light controller interface board, which consist of 36 LED's in which 20 LED's are used for vehicle traffic and they are connected to 20 port lines of 8255 through Buffer. Remaining LED's are used for pedestrian traffic. The traffic light interface board is connected to Main board using 26 core flat cables to 26-pin Port connector. The LED's can be switched ON/OFF in the specified sequence by the Microprocessor/ Microcontroller. The block diagram of the system is shown in fig.1. The layout of the traffic light is shown in fig 2. (8M)



(5M)

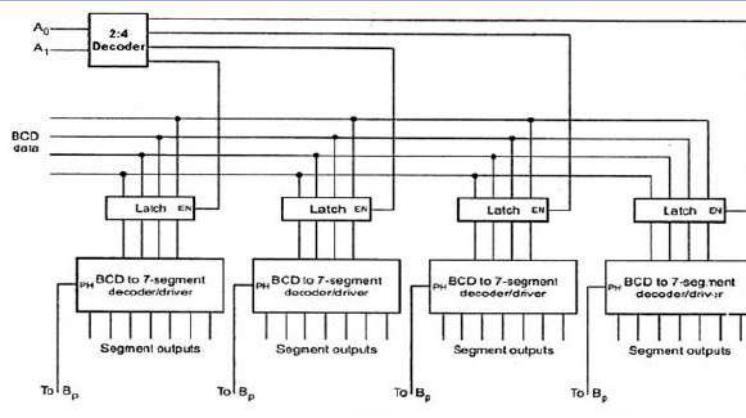
- 10 Explain in detail about interfacing of four LCD digits to 8086. APRIL /MAY 2019 (13M)  
BTL 5

LED displays are available in two very common formats.

1. 7 segment displays
2. 5 by 7 dot-matrix displays.

#### Seven-Segment display

Seven segment displays are generally used as numerical indicators. Any number between 0 and 9 can be indicated by lighting the Segments. (8M)



(5M)

#### Part C

- 1 With block diagram explain the serial communication interface. **Dec 03,04,07,11, May**

**07,08,10,11,13. (15M) BTL 5****Classification**

Serial data transmission can be classified on the basis of how transmission occurs.

1. Simplex
2. Half duplex
3. Full duplex

**Simplex**

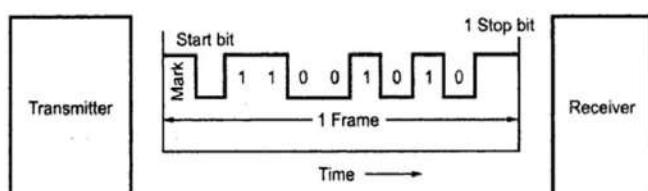
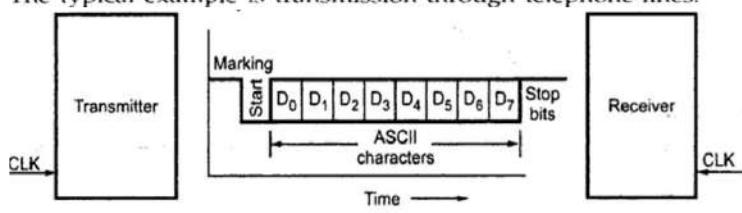
In simplex, the hardware exists such that data transfer takes place only in one direction. There is no possibility of data transfer in the other direction. A typical example is transmission from a computer to the printer.

**Half Duplex**

The half duplex transmission allows the data transfer in both directions, but not simultaneously. A typical example is a walkie-talkie.

**Full Duplex**

The full duplex transmission allows the data transfer in both direction simultaneously. The typical example is transmission through telephone lines.



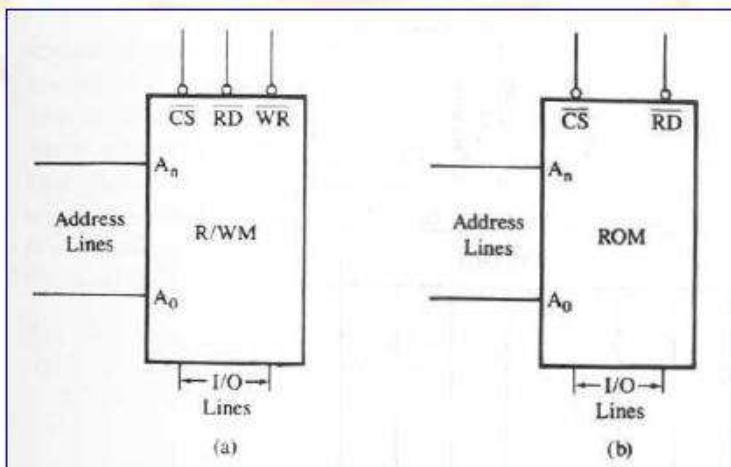
(15M)

**2 Explain the Memory Interfacing in detail. (15M) BTL 5**

**Interfacing:** An interface is a shared boundary between the devices which involves sharing information. Interfacing is the process of making two different systems communicate with each other. Memory is an essential component of microcomputer system; it stores binary instructions and data for the microprocessor. They can be classified in two groups: prime (or main) memory and storage memory. The R/W memory is made up of registers, and each register can use this memory to hold programs and store data. On the other hand, the ROM stores information permanently in the form of diodes. **Memory mapping:** The assignment of memory addresses to various registers in a memory chip is called as memory mapping.

**The requirements of a memory chip.**

1. A memory chip requires address lines to identify a memory register, a chip select CS signal.
2. The number of address lines required is determined by the number of registers in a chip ( $2^n$ )
3. If additional address lines are available in a system, chip select signal is used.
4. The control signal Read (RD) enables the output buffer. The control signal Write (WR) enables the input buffer.

**Memory Map and Address**

(15M)

- 3 Explain the mode of operation of 8255 (15M) May 15 BTL 5  
**MODES OF OPERATION OF 8255**

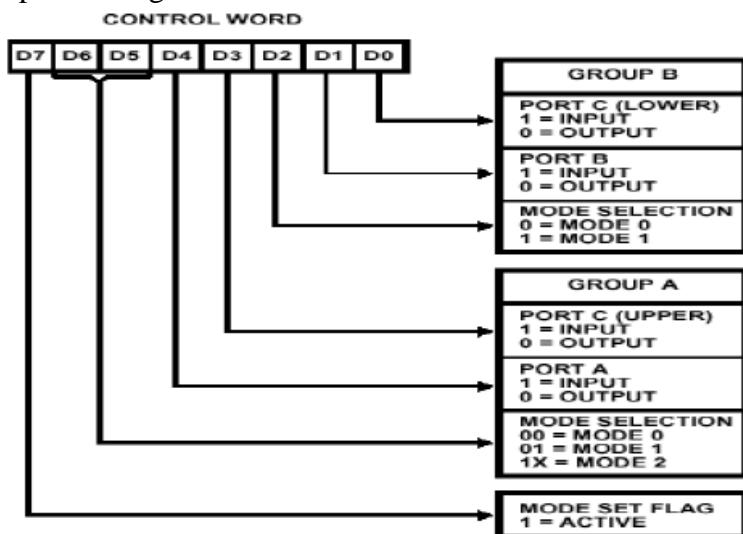
There are two basic modes of operation of 8255 viz. I/O mode and Bit Set-Reset mode (BSR). In I/O mode, the 8255 ports work as programmable I/O ports, while in the BSR mode only port C (PC0 – PC7) can be used to set or reset its individual port bits.

If D7=1, bits D6-D0 determines i/o functions in various mode.

If bit D7=0, port C operates in the bit Set , Reset mode. BSR control word does not affect the functions of port A and B.

To communicate with peripherals through the 8255A, three steps are necessary:

- Determine the address of port A,B and C and of the control register according to the chip select logic and address lines A0 and A1.



(15M)

**UNIT IV MICROCONTROLLER**

**Architecture of 8051 – Special Function Registers(SFRs) - I/O Pins Ports and Circuits - Instruction set - Addressing modes - Assembly language programming.**

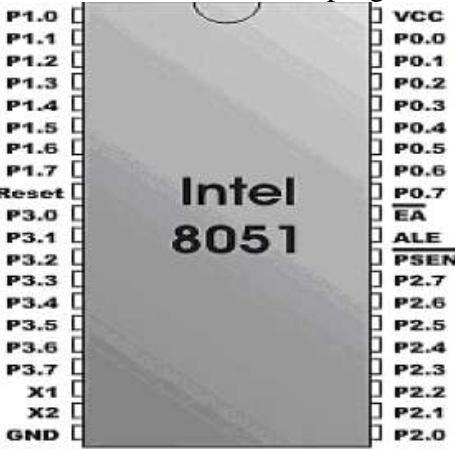
**PART A**

Q. No.	Questions & Answers
1	<b>Discuss the salient features of 8051 family of controllers?</b> BTL 6 Eight-bit CPU with registers A (the accumulator) and B.

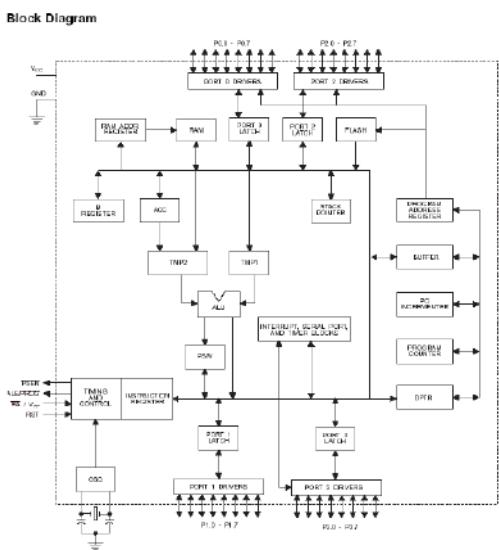
	<p>Sixteen-bit program counter (PC)      Data pointer (DPTR).      Eight-bit program status word (PSW)      Eight-bit stack pointer (SP).      Internal ROM or EPROM (4 KB)      Internal RAM (128 bytes)</p> <ol style="list-style-type: none"> <li>1. Four register banks (each 8 registers)</li> <li>2. 16 bytes, which may be addressed at bit level</li> <li>3. Eighty bits of general purpose data memory</li> </ol> <p>Two 16-bit timer / counters: T0 &amp; T1      Full duplex serial data receivers / transmitter (SBUF)      Control registers: TCON, TMOD, SCON, PCON, IP and IE.</p>								
2	<p><b>What is the size of RAM in 8051? BTL 1</b>      The size of the RAM is <b>128 bytes</b></p> <ol style="list-style-type: none"> <li>1. Four register banks (each 8 registers)</li> <li>2. 16 bytes, which may be addressed at bit level</li> </ol> <p>Eighty bits of general purpose data memory</p>								
3	<p><b>How many ports are available in 8051 micro controller? BTL 1</b>      There are mainly four ports available in this 8051 micro controller. They are</p> <p><b>Port0:</b> serve as inputs, outputs, or, when used together, as a bi-directional low order address and as data bus for external memory.</p> <p><b>Port1:</b> has got no dual functions.</p> <p><b>Port2:</b> may be used as an input / output port similar in operation to port 1. The alternate use of port2 is to supply a high-order address byte in conjunction with the Port0 low-order byte to address external memory.</p> <p><b>Port3:</b> is an input / output pin similar to the Port 1. In this case each and every pin has an additional function.</p>								
4	<p><b>How to select the register bank of Intel 8051. (May 2015) BTL 1</b>      RSO and RS1 are the D3 and D4 bits present in the 8-bit register of the PSW</p> <table border="0"> <tr> <td>0</td><td>BANK 0 is selected from Internal ROM</td></tr> <tr> <td>1</td><td>BANK 1 is selected from Internal ROM</td></tr> <tr> <td>2</td><td>BANK 2 is selected from Internal ROM</td></tr> <tr> <td>3</td><td>BANK 3 is selected from Internal ROM</td></tr> </table>	0	BANK 0 is selected from Internal ROM	1	BANK 1 is selected from Internal ROM	2	BANK 2 is selected from Internal ROM	3	BANK 3 is selected from Internal ROM
0	BANK 0 is selected from Internal ROM								
1	BANK 1 is selected from Internal ROM								
2	BANK 2 is selected from Internal ROM								
3	BANK 3 is selected from Internal ROM								
5	<p><b>List the flags of 8051 and give their usage. BTL 1</b></p> <p><u>Status flags:</u> These flags are modified according to the result of arithmetic and logical operations.      1. Carry flag, 2. Auxiliary carry flag, 3. Overflow flag, 4. Parity flag and <u>General purpose user flags:</u> These flags can be set or cleared by the programmer as desired 1. Flag 0, 2. GF0, 3. GF1</p>								
6	<p><b>What is the difference between microprocessor and microcontroller? (May 2014) BTL 1</b></p> <table border="1"> <tr> <td>It has only CPU</td> <td>It has CPU, memory, I/O, Timer, AD converter</td> </tr> <tr> <td>It has more number of instructions for transferring data from external memory.</td> <td>It has less number of instructions for transferring data from external memory.</td> </tr> <tr> <td>No special function registers are available</td> <td>special function registers are available</td> </tr> </table>	It has only CPU	It has CPU, memory, I/O, Timer, AD converter	It has more number of instructions for transferring data from external memory.	It has less number of instructions for transferring data from external memory.	No special function registers are available	special function registers are available		
It has only CPU	It has CPU, memory, I/O, Timer, AD converter								
It has more number of instructions for transferring data from external memory.	It has less number of instructions for transferring data from external memory.								
No special function registers are available	special function registers are available								
7	<p><b>What is the function of DPTR register? BTL 1</b>      The data pointer (DPTR) is the 16-bit address register that can be used to fetch any 8 bit data from the data memory space. When it is not being used for this purpose, it can be used as two</p>								

	eight bit registers, DPH and DPL
8	<b>What is the significance of EA line of 8051 microcontroller? (May/Jun 2014)</b> BTL 1 When there is no on-chip ROM in microcontroller and EA pin is connected to GND, it indicates that the code is stored in external ROM.
9	<b>What is the difference between MOVX and MOV ? (Nov/Dec 2013)</b> BTL 1 The MOV instruction is used to access code space of on-chip ROM and MOVX instruction is used to access data space or external memory.
10	<b>What are the different ways of operand addressing in 8051? (Apr/May 2016)</b> BTL 1 Different ways of addressing modes are <b>1) Immediate addressing mode 2) Direct addressing mode 3) Register direct addressing mode 4) Register indirect addressing mode 5) Indexed addressing mode.</b>
11	<b>Write an 8051 ALP to toggle P1 a total of 200 times. Use RAM location 32H to hold your counter value instead of registers R0-R7. (Apr/May 2016)</b> BTL 1 MOV P1,#55H ;P1=55H MOV 32H,#200 ;load counter value into RAM loc 32H LOP1: CPL P1 ;toggle P1 ACALL DELAY DJNZ 32H,LOP1 ;repeat 200 times
12	<b>Mention some of the 8051 special function register.</b> BTL 1 ACC: Accumulator, B: B-Register, PSW: Program Status Word, SP: Stack Pointer, DPTR: Data Pointer, IE: Interrupt Enable, SCON: Serial Control, PCON: Power Control.
13	<b>What is the function of XTAL 1 and XTAL 2 pins?</b> BTL 1 8051 internal clock circuit. In this crystal of proper frequency can be connected to these two pins. XTAL 1 is connected to GND and oscillator signal is connected to XTAL 2.
14	<b>Write an ALP to add the values ABH and 47H. Store the result in R1.</b> BTL 1 MOV A, #AB H ADD A, #47 H MOV R1, A L1: SJMP L1
15	<b>How is RAM memory space allocated in 8051?</b> BTL 1 1. 32 bytes from 00 to 1FH is for register bank and stack. 2. 16 bytes from 20H to 2FH is for bit addressable read/write memory 80 byte 30H to 7FH is for scratch pad
16	<b>What is the purpose of overflow flag?</b> BTL 1 The overflow flag is usually a single bit in a system status register used to indicate when an arithmetic overflow has occurred in an operation, indicating that the signed two's-complement result would not fit in the number of bits used for the operation (the ALU width).
17	<b>What is the difference between LCALL and ACALL instructions?</b> BTL 1 The ACALL instruction calls a subroutine located at the specified address. The PC is incremented twice to obtain the address of the following instruction. The 16-bit PC is then stored on the stack (low-order byte first) and the stack pointer is incremented twice. No flags are affected. The LCALL instruction calls a subroutine located at the specified address. This instruction first adds 3 to the PC to generate the address of the next instruction. This result is pushed onto the stack low-byte first and the stack pointer is incremented by 2. The high-order and low-order bytes of the PC are loaded from the second and third bytes of the instruction respectively. Program execution is transferred to the subroutine at this address. No flags are affected by this instruction.
18	<b>What is the operation of the given 8051 microcontroller instruction XRL A?</b> BTL 1 The XRL instruction performs a logical exclusive OR operation between the specified operands. The result is stored in the destination operand.
19	<b>Write a program to perform multiplication of 2 numbers using 8051?</b> BTL 1

	<pre> MOV A, #data1 MOV B, #data2 MUL AB MOV DPTR, # 4500H MOVX @ DPTR, A INC DPTR MOV A,B MOVX @ DPTR, A STOP : SJMP STOP </pre>														
20	<p><b>Write a program to perform 2's complement of a given number using 8051? BTL 1</b></p> <pre> MOV DPTR, # 4500H MOVX A, @ DPTR CPL A ADD A,#01H INC DPTR STOP : SJMP STOP </pre>														
21	<p><b>Which port used as multifunction port? List the signals. (Apr/May 2017) BTL 1</b></p> <p>Port 3 has multifunction port. Each pin of port 3 has i/o or as of one of the alternate function.</p> <p>Signals are:</p> <ul style="list-style-type: none"> <li>P3.0– RXD</li> <li>P3.1– TXD</li> <li>P3.4– T0</li> <li>P3.5- T1</li> </ul>														
22	<p><b>Illustrate the CJNE instruction (Apr/May 2017) BTL 1</b></p> <p><b>CJNE-</b> Compare and jump if not equal. This instruction compares the magnitudes of the source byte and the destination byte.</p>														
23	<p><b>If a 12 Mhz crystal is connected with 8051, how much is the time taken for the count in timer 0 to get incremented by one? BTL 1</b></p> <p>Baud rate = oscillator frequency/12 = <math>(12 \times 10^6) / 12 = 10^6</math> Hz  <math>T = 1/f = 1/(1 \times 10^6) = 1 \mu\text{sec}</math>.</p>														
24.	<p><b>Which bits of the PSW are responsible for selection of the register banks? APRIL/MAY 2019 BTL 1</b></p> <p><b>Processor Status Word</b></p>														
25	<p><b>For an 8051 system of 11.0592 Mhz find the time delay for the following subroutine: APRIL/MAY 2019 BTL 1</b></p> <table style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th colspan="2"><b>MACHINE CYCLE</b></th> </tr> </thead> <tbody> <tr> <td><b>DELAY MOV R3 # 250</b></td> <td><b>1</b></td> </tr> <tr> <td><b>NOP</b></td> <td><b>1</b></td> </tr> <tr> <td><b>NOP</b></td> <td><b>1</b></td> </tr> <tr> <td><b>NOP</b></td> <td><b>1</b></td> </tr> <tr> <td><b>NOP</b></td> <td><b>1</b></td> </tr> <tr> <td><b>DJNZ R3 ;HERE</b></td> <td><b>2</b></td> </tr> </tbody> </table>	<b>MACHINE CYCLE</b>		<b>DELAY MOV R3 # 250</b>	<b>1</b>	<b>NOP</b>	<b>1</b>	<b>NOP</b>	<b>1</b>	<b>NOP</b>	<b>1</b>	<b>NOP</b>	<b>1</b>	<b>DJNZ R3 ;HERE</b>	<b>2</b>
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	RET	1
	Part B/Unit IV	
1	<p><b>Draw &amp; explain the pin configuration of 8051 in detail(May 2014) (13M) BTL 5</b></p> <p><b>Ans: Refer:</b> Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:75-79</p> <p>8051 is available in a 40 pin plastic and ceramic DIP packages. The pin diagram of 8051 is shown in the following figure.</p> <p><b>VCC:</b> This is a +5V supply voltage pin.</p> <p><b>VSS:</b> This is a return pin for the supply.</p> <p><b>RESET:</b> The reset input resets the 8051, only when it goes high for two or more machine cycles. For a proper initialization after reset, the clock must be running.</p> <p><b>ALE/PROG:</b> The latch enable output pulse indicates that the valid address bits are available on their respective pins. This ALE signal is valid only for external memory accesses. Normally, the ALE pulses are emitted at a rate of one-sixth of the oscillator frequency. This pin acts as program pulse input during on-chip EPROM programming. ALE may be used for external timing or clocking purpose. One ALE pulse is skipped during each access to external data memory.</p> <p><b>EA/VPP:</b> External access enable pin, if tied low, indicates that the 8051 can address external program memory. In other words, the 8051 can execute a program in external memory, only if EA is tied low. For execution of programs in internal memory, the EA must be tied high. This pin also receives 21 volts for programming of the on-chip EPROM. (8M)</p> 	(5M)
2	<p><b>Explain in detail the different addressing modes supported by 8051.APRIL/MAY 2019. (13M) BTL 5</b></p> <p><b>Ans: Refer:</b> Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, .PG.NO:90-96</p> <p>8051 supports six addressing modes as listed below.</p> <ol style="list-style-type: none"> <li>1. Direct Addressing (2M)</li> <li>2. Indirect Addressing (2M)</li> <li>3. Register Indirect (2M)</li> <li>4. Register specific (Register Implicit) (2M)</li> <li>5. Immediate mode (2M)</li> <li>6. Indexed Addressing (3M)</li> </ol>	
3	<p><b>Draw the architecture of 8051 and explain.(16) (May 2015)(Apr/May 2016) (13M) BTL 5</b></p> <p><b>Ans: Refer:</b> Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:22-23</p> <p><b>Accumulator (ACC):</b> The accumulator register (ACC or A) acts as an operand register. This may either be implicit or specified in the instruction. The ACC register is allotted an address in the on-chip special function register bank.</p> <p><b>B Register:</b> This register is used to store one of the operands for multiply and divide instructions. In other instructions, it may just be used as a scratch pad. This register is considered as a special function register.</p>	

**Program Status Word (PSW):** This set of flags contains the status information and is considered as one of the special function registers. This bit-addressable register has the following format: (8M)



(5M)

4 Write an 8051ALP to create a square wave of 66% duty cycle on bit 3 of port1. (Apr/May 2016) (13M) BTL 1

```

MOV TMOD, #01           ;Timer 0, mode 1(16-bit mode)
HERE:    MOV TL0, #0F2H      ;TL0 = F2H, the Low byte
        MOV TH0, #0FFH      ;TH0 = FFH, the High byte
        CPL P1.5            ;toggle P1.5
        ACALL DELAY         ;load TH, TL again
        SJMP HERE           ;delay using Timer 0
DELAY:   SETB TR0            ;start Timer 0
AGAIN:  JNB TFO, AGAIN      ;monitor Timer 0 flag until
        ;it rolls over
        CLR TR0             ;stop Timer 0
        CLR TFO              ;clear Timer 0 flag
        RET
    
```

(13M)

5 Explain the instruction set of 8051? (May 2015) (13M) BTL 5

**Ans:** Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:533-536  
These instructions perform arithmetic operations such as addition, subtraction, increment and decrement.

**Addition** — Any 8-bit number, or the contents of a register, or the contents of a memory location can be added to the contents of the accumulator and the result is stored in the accumulator

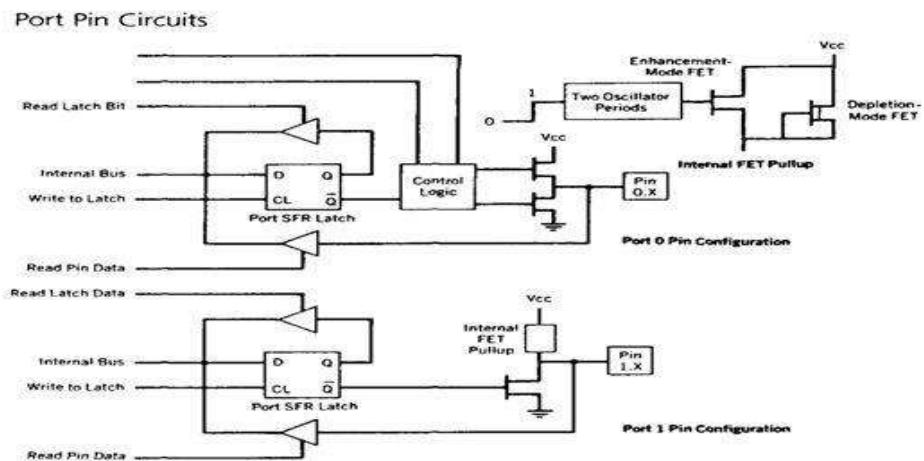
**Subtraction** — Any 8-bit number, or the contents of a register, or the contents of a memory location can be subtracted from the contents of the accumulator and the result is stored in the accumulator.

**Increment / Decrement** — The 8-bit contents of a register or a memory location can be incremented or decremented by one. Similarly, the 16-bit contents of a register pair can be incremented or decremented by 1. These increment and decrement operation differ from the addition and subtraction in an important way; i.e., they can be performed in one of the registers or in a memory location. (13M)

6 Explain the I/O structure of 8051 (8) (Nov 2013) (May 2014) (13M) BTL 5

**Ans:** Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:76-85

**Port 0 to 3 Latches and Drivers:** These four latches and driver pairs are allotted to each of the no-chip I/O ports. These latches have been allotted addresses in the special function register bank. Using the allotted addresses, the user can communicate with these ports. These are identified as P0, P1, P2 and P3. (8M)



(5M)

7 List the special function registers of 8051 TMOD, SMOD and explain their functions. (2015) (13M) BTL 5

Ans: Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:92-93.

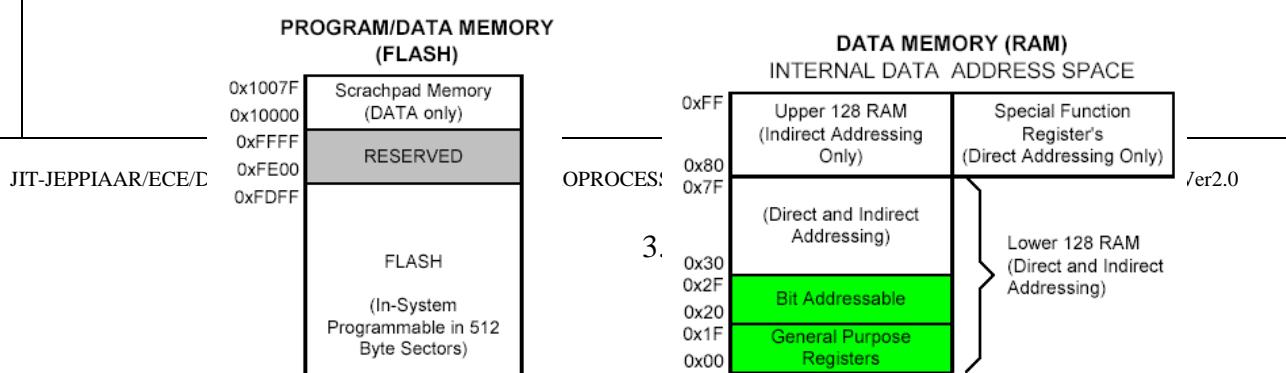
NAME	FUNCTION	INTERNAL RAM ADDRESS (HEX)
A	Accumulator	0E0
B	Arithmetic	0F0
DPH	Addressing external memory	83
DPL	Addressing external memory	82
IE	Interrupt enable control	0A8
IP	Interrupt priority	0B8
PO	Input/output port latch	80
P1	Input/output port latch	90
P2	Input/output port latch	A0
P3	Input/output port latch	0B0
PC ON	Power control	87
PSW	Program status word	0D0
SCON	Serial port control	98
SBUF	Serial port data buffer	99
SP	Stack pointer	81
TMOD	Timer / counter mode control	89
TCON	Timer / counter control	88
TLO	Timer 0 low byte	8A
THO	Timer 0 low byte	8C
TL1	Timer 0 low byte	8B
TH1	Timer 1 high byte	8D

#### Special Function Registers

(13M)

8 Explain the internal and external data memory organization of 8051. (10) (Nov2013) Explain in detail about the 8051 register bank and stack. APRIL/M 2019 (13M) BTL 5

Ans: Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, ‘PG.NO:367-374



		(13M)
9	<p><b>Describe how to program and interface an LCD to an 8051 using Assembly language programming. APRIL/MAY2019 (13M) BTL 5</b></p> <p>MOV A,#38H // Use 2 lines and 5x7 matrix      ACALL CMND      MOV A,#0FH // LCD ON, cursor ON, cursor blinking ON      ACALL CMND      MOV A,#01H //Clear screen      ACALL CMND      MOV A,#06H //Increment cursor      ACALL CMND      MOV A,#82H //Cursor line one , position 2      ACALL CMND      MOV A,#3CH //Activate second line      ACALL CMND      MOV A,#49D      ACALL DISP      MOV A,#54D      ACALL DISP      MOV A,#88D      ACALL DISP      MOV A,#50D      ACALL DISP      MOV A,#32D      ACALL DISP      MOV A,#76D      ACALL DISP      MOV A,#67D      ACALL DISP      MOV A,#68D      ACALL DISP      MOV A,#0C1H //Jump to second line, position 1      ACALL CMND      MOV A,#67D      ACALL DISP      MOV A,#73D      ACALL DISP      MOV A,#82D      ACALL DISP      MOV A,#67D      ACALL DISP      MOV A,#85D</p>	

	<pre> ACALL DISP MOV A,#73D ACALL DISP MOV A,#84D ACALL DISP MOV A,#83D ACALL DISP MOV A,#84D ACALL DISP MOV A,#79D ACALL DISP MOV A,#68D ACALL DISP MOV A,#65D ACALL DISP MOV A,#89D ACALL DISP HERE: SJMP HERE CMND: MOV P1,A CLR P3.5 CLR P3.4 SETB P3.3 CLR P3.3 ACALL DELY RET DISP:MOV P1,A SETB P3.5 CLR P3.4 SETB P3.3 CLR P3.3 ACALL DELY RET DELY: CLR P3.3 CLR P3.5 SETB P3.4 MOV P1,#0FFh SETB P3.3 MOV A,P1 JB ACC.7,DELY CLR P3.3 CLR P3.4 RET END </pre> <p style="text-align: right;">(13M)</p>
10	<p><b>Briefly explain about the interfacing of 8051 with external data ROM. <u>APRIL/MAY2019</u></b></p> <p><b>(13M) BTL 5</b></p> <p>When EA = 0, the EA pin is strapped to GND, and all program fetches are directed to external memory regardless of whether or not the 8751 has some on-chip ROM for program code. This external ROM can be as high as 64K bytes with address space of 0000 – FFFFH. With the 8751 (89C5.1) system where EA = V<sub>cc</sub>, the microcontroller fetches the program code of addresses 0000 – OFFFH from on-chip ROM since it has 4K bytes of on-chip program ROM and any</p>

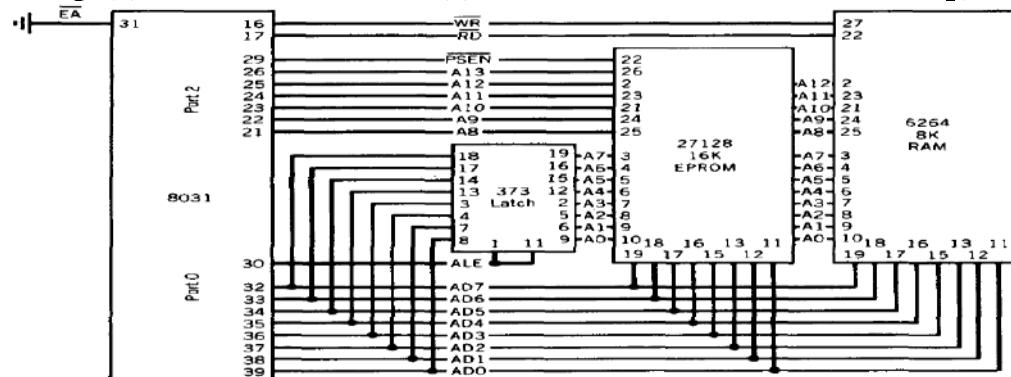
fetches from addresses 1000H – FFFFH are direct ed to external ROM. With the 8752 (89C52) system where EA = V<sub>cc</sub>, the microcontroller fetches the program code of addresses 0000 – 1FFFH from on-chip ROM since it has 8K bytes of on-chip program ROM and any fetches from addresses 2000H – FFFFH are direct ed to external ROM. (8M)



(5M)

**PART C**

- 1 Discuss the number of pin sets aside for addresses in each of the following memory chips(1) 16 K \* 4 DRAM and (2)16K \* 4 SRAM .APRIL/MAY2019\_(15M) BTL 5



(15M)

- 2 With necessary diagrams explain how to interface LM 35 temperature sensor and then discuss the issues of signal condoning. APRIL/MAY2019\_(15M) BTL 5

Important components in digital temperature measurement system are:

1. A sensor, sensor is nothing but a component or device whose physical parameters will change according to changes in atmospheric parameters or factors. For eg: Temperature Sensor, it might change its resistance, output voltage or dimension as there is some change in surrounding temperature. In this project we are using LM35, its output voltage increases by +10mV as there is 1° C rise in temperature.
2. A digital converter, as we all know the output of the sensor will be in form of analog voltage. This analog voltage can't be distinguished by the micro-controller or any other digital device. In order to understand changes in the output of sensor we need to convert it into digital form ie. Binary Data

(15M)

- 3 Write an ALP for Multibyte addition (15M) BTL 2

Mnemonic	Operation
MOV A,#42h	A = 42BCD
ADD A,#13h	A = 55h; C = 0
DA A	A = 55h; C = 0
ADD A,#17h	A = 6Ch; C = 0
DA A	A = 72BCD; C = 0
ADDC A,#34h	A = A6h; C = 0
DA A	A = 06BCD; C = 1
ADDC A,#11h	A = 18BCD; C = 0
DA A	A = 18BCD; C = 0

(15M)

<b>UNIT V INTERFACING MICROCONTROLLER</b>	
<b>Programming 8051 Timers - Serial Port Programming - Interrupts Programming – LCD &amp; Keyboard Interfacing - ADC, DAC &amp; Sensor Interfacing - External Memory Interface- Stepper Motor and Waveform generation - Comparison of Microprocessor, Microcontroller, PIC and ARM processors</b>	
<b>PART A</b>	
<b>Q. No.</b>	<b>Questions &amp; Answers</b>
1	<b>What is the relation between RPM and steps per second in stepper motor interfacing?</b> BTL 1 Steps per second= $(\text{rpm} \times \text{steps per revolution})/60$
2	<b>Write short notes on interrupts in 8051?</b> BTL 1 Interrupts may be generated by internal chip operations or provided by external interrupts sources. Five interrupts are provided in 8051. Three of these interrupts are generated automatically by internal operations: <b>Timer flag 0, Timer flag 1, and the serial port interrupts (RI or TI)</b> . Two interrupts are triggered by external signals provided by the circuitry that is connected to the pins INT0 and INT1 (port pins P3.2 and P3.3).
3	<b>What is the purpose of Interrupt priority (IP) Control register in 8051?</b> BTL 1 Register IP bits determine if any interrupt is to have a high or low priority. Bits set to 1 give the accompanying interrupt a high priority; a 0 assigns a low priority. If two interrupts with the same priority occur at the same time, then they have the following ranking: 1.IE0, 2.TF0, 3.IE1, 4.TF1,5.Serial = RI or TI.
4	<b>What is the purpose of counters in 8051 micro controller?</b> BTL 1 The counters have been included on the chip to relieve the processor of timing and control chores. When the program wishes to count a certain number of internal pulses or external events, a number is placed in one of the counters. The number represents the following: <b>(Maximum count)-(Desired count) + 1</b> . The counter increments from the initial number to the maximum and then rolls over to zero on the final pulse.
5	<b>What is the basic difference between a timer and a counter?</b> (May 2015) BTL 1 The only difference between a timer and a counter is the source of clock pulses to the counters. When used as a timer, the clock pulses are sourced from the oscillator through the divide-by-12d circuit. When used as a counter, pin T0 (P3.4) supplies pulses to counter 0, and pin T1(P3.5) to counter 1.
6	<b>Explain the operating mode 0 of 8051 serial port?</b> BTL 2 <ul style="list-style-type: none"> <li>Mode 0 of 8051 serial port is shift register mode.</li> <li>Serial data enters and exits through RXD pin.</li> <li>Pin TXD is connected to the internal shift frequency pulse source.</li> <li>8-bits are transmitted and received.</li> </ul> The baud rate is fixed at 1/12 of the crystal frequency.
7	<b>Define watch dog timer.</b> BTL 1 <ul style="list-style-type: none"> <li>Watch dog timer is a dedicated timer to take care of system malfunction. It can be used to reset the controller during software malfunction, which is referred to as “Hanging”. A watchdog timer contains a timer that expires after a certain interval unless it is restarted. It resets the microcontroller and starts the software over from the beginning if the software does not restart it periodically.</li> </ul>
8	<b>What is the function of the TMOD register?</b> BTL 1 TMOD (Timer mode) register is used to set the various timer operation modes. TMOD is dedicated solely to the two timers (T0 & T1) and can be considered to be two duplicate 4-bit

	registers, each of which controls the action of the timers.																
9	<b>What is the difference between watch dog timer and ordinary timer? (Nov 2013) BTL 1</b> The watch dog timer is provided for the system to check itself and reset if it is not functioning properly. It is a 16 bit-counter which is incremented every state time.																
10	<b>List out the advantages of LCD over LED. BTL 1</b> <ul style="list-style-type: none"> <li>• Declining prices of LED,</li> <li>• Ability to display numbers, characters and graphics</li> <li>• Incorporating a refreshing controller.</li> </ul> Ease of programming for characters and graphics.																
11	<b>What is the significance of BUSY flag in LCD interfacing? BTL 1</b> When D7 pin=1 and RS pin=0 the BUSY flag is set which means that LCD is busy taking care of internal operations and will not accept any new information. Therefore we have to check BUSY flag before writing data to LCD.																
12	<b>How a pressed key is detected in keyboard interfacing? BTL 1</b> The keyboards are organized in a matrix of rows and columns. The microcontroller grounds all rows by providing zero to the output latch then reads the columns.																
13	<b>What is the significance of WR and INTR pin in ADC chip? BTL 1</b> WR is an active low input and when it undergoes low to high transition the Start of conversion signal is given. INTR is an active low output pin. It is normally high when the A to D conversion is finished. It goes low to signal EOC.																
14	<b>Write an ALP to generate a saw tooth waveform. BTL 1</b> <pre>MOV A.#00H MOV P1,A BACK: INC A SJMP BACK</pre>																
15	<b>What is the significance of PSEN in memory interfacing? BTL 1</b> PSEN (Program Store Enable) is an output signal for the 8051 microcontroller, which is connected to the OE pin of external ROM containing the program code. This is used when external ROM has to be accessed.																
16	<b>What is SBUF? BTL 1</b> SBUF stands for SERIAL BUFFER. SBUF is physically two registers. One is write only and is used to hold the data to be transmitted out of the 8051 via TXD. The other one is read only and holds the received data from external sources via RXD.																
17	<b>What are the serial communication modes available in 8051? BTL 1</b> Mode 0, Mode 1, Mode 2, Mode 3 is the serial communication modes available in 8051.																
18	<b>What are the contents of SCON register? (May 2015) BTL 1</b> <b>SM0</b> - Serial port mode bit 0, <b>SM1</b> - Serial port mode bit 1, <b>SM2</b> - Serial port mode 2 bit multiprocessor communication enable bit; <b>REN</b> - Reception Enable bit. <b>TB8</b> - Transmitter bit 8. <b>RB8</b> - Receiver bit 8 or the 9th bit received in modes 2 and 3, <b>TI</b> - Transmit Interrupt flag & <b>RI</b> - Receive Interrupt flag. <table border="1" style="margin-top: 10px;"> <tr> <td>7</td><td>6</td><td>5</td><td>4</td><td>3</td><td>2</td><td>1</td><td>0</td></tr> <tr> <td>SM0</td><td>SM1</td><td>SM2</td><td>REN</td><td>TB8</td><td>R</td><td>TI</td><td>RI</td></tr> </table>	7	6	5	4	3	2	1	0	SM0	SM1	SM2	REN	TB8	R	TI	RI
7	6	5	4	3	2	1	0										
SM0	SM1	SM2	REN	TB8	R	TI	RI										
19	<b>What are the various baud rates possible in 8051 and how are they set? BTL 1</b> <table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Baud rate</th> <th>TH1 (Dec)</th> <th>TH1 (Hex)</th> <th rowspan="4"></th> </tr> </thead> <tbody> <tr> <td>9600</td> <td>-3</td> <td>FD</td> </tr> <tr> <td>4800</td> <td>-6</td> <td>FA</td> </tr> <tr> <td>2400</td> <td>-12</td> <td>F4</td> </tr> </tbody> </table>	Baud rate	TH1 (Dec)	TH1 (Hex)		9600	-3	FD	4800	-6	FA	2400	-12	F4			
Baud rate	TH1 (Dec)	TH1 (Hex)															
9600	-3	FD															
4800	-6	FA															
2400	-12	F4															

	1200	-24	E8															
20	<b>What are the various types of sensors that can be interfaced with 8051? (Apr/ May 2017)</b> BTL 1 1. Temperature Sensor, 2. IR Sensor, 3. Ultrasonic Sensor, 4. Touch Sensor, 5. Proximity Sensors, 6. Pressure Sensor, 7. Level Sensors, 8. Smoke and Gas Sensors.																	
21	<b>Define Baud rate of 8051. (Apr/May 2016)</b> BTL 1 In serial communication the data is rate known as the baud rate, which simply means the number of bits transmitted per second. In the serial port modes that allow variable baud rates, this baud rate is set by timer 1. The 8051 serial port is full duplex.																	
22	<b>What are the applications of stepper motor?</b> BTL 1 <b>Industrial Machines</b> – Stepper motors are used in automotive gauges and machine tooling automated production equipments. <b>Security</b> – new surveillance products for the security industry. <b>Medical</b> – Stepper motors are used inside medical scanners, samplers, and also found inside digital dental photography, fluid pumps, respirators and blood analysis machinery. <b>Consumer Electronics</b> Stepper motors in cameras for digital camera focus and zooming																	
23	<b>Compare polling and interrupt. (Apr/May 2016)</b> BTL 1 Interrupt is a signal to the microprocessor from a device that requires attention. The microprocessor will respond by setting aside execution of its current task and deal with the interrupting device. When the interrupting device has been dealt with, the microprocessor continues with its original task as if it had never been interrupted. In Polling the processor continuously polls or tests every device in turn as to whether it requires attention (e.g. has data to be transferred). The polling is carried out by a polling program that shares processing time with the currently running task.																	
24	<b>What is the significance of TCON register?</b> BTL 1 The Timer Control SFR is to configure, modify the way in which the 8051's two timers operate. This SFR controls whether each of the two timers is running or stopped and contains a flag to indicate that each timer has overflowed. Some non-timer related bits are located in the TCON SFR. These bits are used to configure the way in which the external interrupts are activated.																	
25	<b>List the 8051 interrupts with its priority (Apr/May 2017)</b> BTL 1 Types of Interrupts in 8051 Microcontroller The 8051 microcontroller can recognize five different events that cause the main program to interrupt from the normal execution. These five sources of interrupts in 8051 are: 1. Timer 0 overflow interrupt- TF0 2. Timer 1 overflow interrupt- TF1 3. External hardware interrupt- INT0 4. External hardware interrupt- INT1 Serial communication interrupt- RI/TI																	
26	<b>What are the different modes in which timer 2 can operate? APRIL/MAY 2019.</b> BTL 1 <table border="1"> <thead> <tr> <th>M1 / MO</th> <th>Mode</th> <th>Operating Mode</th> </tr> </thead> <tbody> <tr> <td>0 0</td> <td>0</td> <td>13-bit timer mode 8-bit timer/counter THx with TLx as 5-bit prescaler</td> </tr> <tr> <td>0 1</td> <td>1</td> <td>16-bit timer mode 16-bit timer/counter THx and TLx are cascaded; there is no prescaler</td> </tr> <tr> <td>1 0</td> <td>2</td> <td>8-bit auto reload 8-bit auto reload timer/counter; THx holds a value which is to be reloaded TLx each time it overflows</td> </tr> <tr> <td>1 1</td> <td>3</td> <td>Split timer mode</td> </tr> </tbody> </table>	M1 / MO	Mode	Operating Mode	0 0	0	13-bit timer mode 8-bit timer/counter THx with TLx as 5-bit prescaler	0 1	1	16-bit timer mode 16-bit timer/counter THx and TLx are cascaded; there is no prescaler	1 0	2	8-bit auto reload 8-bit auto reload timer/counter; THx holds a value which is to be reloaded TLx each time it overflows	1 1	3	Split timer mode		
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1 1	3	Split timer mode																
32	<b>When is an external memory access generated in 8051?APRIL/MAY 2019.</b> BTL 1																	

**EA/VPP:** External access enable pin, if tied low, indicates that the 8051 can address external program memory. In other words, the 8051 can execute a program in external memory, only if EA is tied low. For execution of programs in internal memory, the EA must be tied high. This pin also receives 21 volts for programming of the on-chip EPROM.

### PART-B

- 1 Draw the block diagram of Intel 8051 timer/counter and explain its different modes of operations. (May 2015) (13M) BTL 5

**Ans:** Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:202-221

#### Timer Modes of Operation

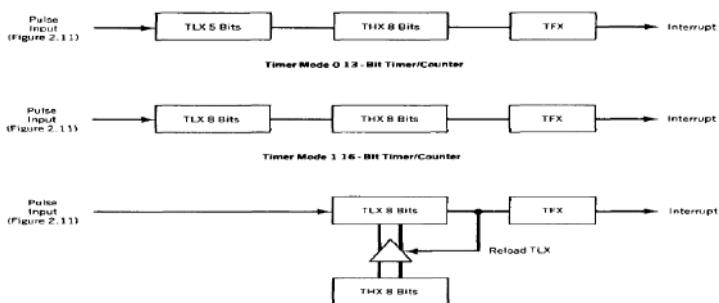
The timers may operate in any one of four modes that are determined by the mode bits, M1 and M0, in the TMOD register. Figure 2.12 shows the four timer modes.

#### Timer Mode 0

Setting timer X mode bits to 00b in the TMOD register results in using the THX register as an 8-bit counter and TLX as a 5-bit counter; the pulse input is divided by 32d in TL so that TH counts the original oscillator frequency reduced by a total 384d. As an example, the 6 megahertz oscillator frequency would result in a final frequency to TH of 15625 hertz. The timer flag is set whenever THX goes from FFh to 00h, or in .0164 seconds for a 6 megahertz crystal if THX starts at 00h.

#### Timer Mode 1

Mode 1 is similar to mode 0 except TLX is configured as a full 8-bit counter when the mode bits are set to 01b in TMOD. The timer flag would be set in .1311 seconds using a 6 megahertz crystal.



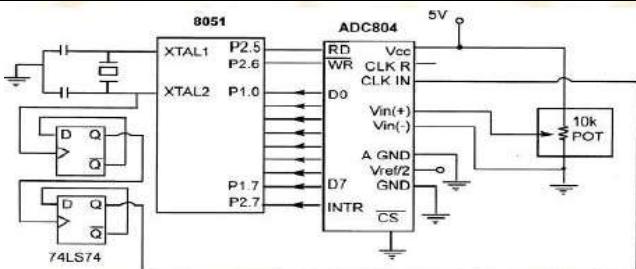
(13M)

- 2 Explain how to interface ADC in detail. (16) (Dec 2013) (13M) BTL 5

**Ans:** Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:322-327

**Analog-to-digital converter (ADC) interfacing:** ADCs (analog-to-digital converters) are among the most widely used devices for data acquisition. A physical quantity, like temperature, pressure, humidity, and velocity, etc., is converted to electrical (voltage, current) signals using a device called a transducer, or sensor. We need an analog-to-digital converter to translate the analog signals to digital numbers, so microcontroller can read them.

**ADC804 chip:** ADC804 IC is an analog-to-digital converter. It works with +5 volts and has a resolution of 8 bits. Conversion time is another major factor in judging an ADC. Conversion time is defined as the time it takes the ADC to convert the analog input to a digital (binary) number. In ADC804 conversion time varies depending on the clocking signals applied to CLK R and CLK IN pins, but it cannot be faster than 110 $\mu$ s.



(13M)

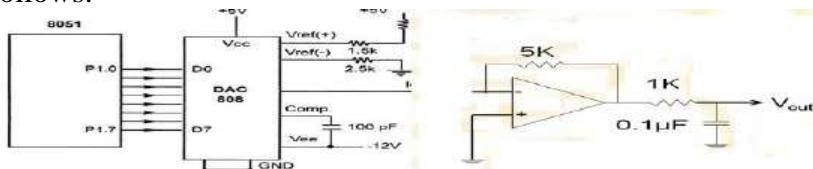
**4 Explain how to interface DAC in detail.(13)APRIL/MAY 2019 (13M) BTL 5**

**Ans:** Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:344-348

**Digital-to-Analog (DAC) converter:** The DAC is a device widely used to convert digital pulses to analog signals. In this section we will discuss the basics of interfacing a DAC to 8051. The two method of creating a DAC is binary weighted and R/2R ladder. The Binary Weighted DAC, which contains one resistor or current source for each bit of the DAC connected to a summing point. These precise voltages or currents sum to the correct output value. This is one of the fastest conversion methods but suffers from poor accuracy because of the high precision required for each individual voltage or current. Such high-precision resistors and current sources are expensive, so this type of converter is usually limited to 8-bit resolution or less. The R-2R ladder DAC, which is a binary weighted DAC that uses a repeating cascaded structure of resistor values R and 2R. This improves the precision due to the relative ease of producing equal valued matched resistors (or current sources). However, wide converters perform slowly due to increasingly large RC-constants for each added R-2R link. The first criterion for judging a DAC is its resolution, which is a function of the number of binary inputs.

#### **DAC0808:**

The digital inputs are converter to current  $I_{out}$ , and by connecting a resistor to the  $I_{out}$  pin, we can convert the result to voltage. The total current  $I_{out}$  is a function of the binary numbers at the D0-D7 inputs of the DAC0808 and the reference current  $I_{ref}$ , and is as follows:



(13M)

**6 With necessary hardware & software details explain how to interface LCD'S with 8051(16) (May 2015) (13M) BTL 5**

**Ans:** Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:300-306

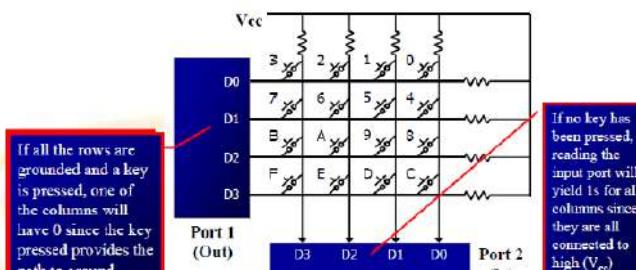
LCD is finding widespread use replacing LEDs for the following reasons:

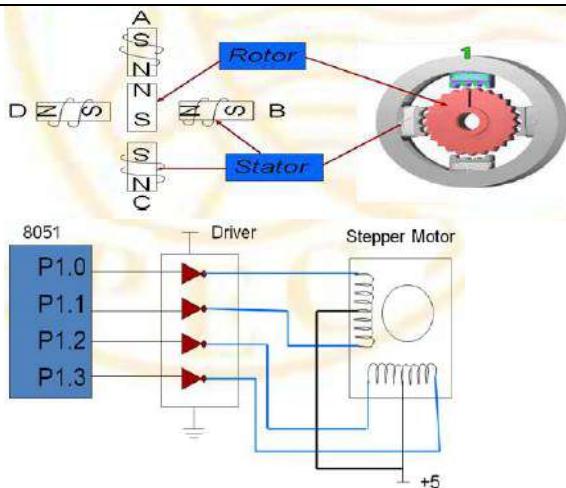
1. The declining prices of LCD
2. The ability to display numbers, characters, and graphics
3. Incorporation of a refreshing controller into the LCD, thereby relieving the CPU of the task of refreshing the LCD
4. Ease of programming for characters and graphics

#### **Sending Data/ Commands to LCDs with Time Delay:**

To send any of the commands to the LCD, make pin RS=0. For data, make RS=1. Then send a high-to-low pulse to the E pin to enable the internal latch of the LCD. This is shown in the code below. The interfacing diagram of LCD to 8051 is as shown in the figure.

	<table border="1"> <thead> <tr> <th><b>Pin</b></th><th><b>Symbol</b></th><th><b>I/O</b></th><th><b>Description</b></th></tr> </thead> <tbody> <tr> <td>1</td><td>V<sub>SS</sub></td><td>--</td><td>Ground</td></tr> <tr> <td>2</td><td>V<sub>CC</sub></td><td>--</td><td>+5V power supply</td></tr> <tr> <td>3</td><td>V<sub>EE</sub></td><td>--</td><td>Power supply to control contrast</td></tr> <tr> <td>4</td><td>RS</td><td>I</td><td>RS=0 to select command register, RS=1 to select data register</td></tr> <tr> <td>5</td><td>R/W</td><td>I</td><td>R/W=0 for write, R/W=1 for read</td></tr> <tr> <td>6</td><td>E</td><td>I/O</td><td>Enable</td></tr> <tr> <td>7</td><td>DB0</td><td>I/O</td><td>The 8-bit data bus</td></tr> <tr> <td>8</td><td>DB1</td><td>I/O</td><td>The 8-bit data bus</td></tr> <tr> <td>9</td><td>DB2</td><td>I/O</td><td>The 8-bit data bus</td></tr> <tr> <td>10</td><td>DB3</td><td>I/O</td><td>The 8-bit data bus</td></tr> <tr> <td>11</td><td>DB4</td><td>I/O</td><td>The 8-bit data bus</td></tr> <tr> <td>12</td><td>DB5</td><td>I/O</td><td>The 8-bit data bus</td></tr> <tr> <td>13</td><td>DB6</td><td>I/O</td><td>The 8-bit data bus</td></tr> <tr> <td>14</td><td>DB7</td><td>I/O</td><td>The 8-bit data bus</td></tr> </tbody> </table>	<b>Pin</b>	<b>Symbol</b>	<b>I/O</b>	<b>Description</b>	1	V <sub>SS</sub>	--	Ground	2	V <sub>CC</sub>	--	+5V power supply	3	V <sub>EE</sub>	--	Power supply to control contrast	4	RS	I	RS=0 to select command register, RS=1 to select data register	5	R/W	I	R/W=0 for write, R/W=1 for read	6	E	I/O	Enable	7	DB0	I/O	The 8-bit data bus	8	DB1	I/O	The 8-bit data bus	9	DB2	I/O	The 8-bit data bus	10	DB3	I/O	The 8-bit data bus	11	DB4	I/O	The 8-bit data bus	12	DB5	I/O	The 8-bit data bus	13	DB6	I/O	The 8-bit data bus	14	DB7	I/O	The 8-bit data bus	(13M)
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7	<p><b>Explain the different modes of operation of serial port in 8051, indicating various registers associated with it. (16) (Apr/May 2016) (13M) BTL 5</b></p> <p><b>Ans:</b> Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:244-231</p> <p><b>Serial Port</b></p> <p>The serial buffer consists of two separate registers:</p> <ol style="list-style-type: none"> <li>1. Transmit buffer</li> <li>2. Receive buffer.</li> </ol> <p>Writing data to the SFR sbuf sets this data in the serial output buffer and starts the transmission.</p> <p>Reading from the sbuf register reads data from the serial receive buffer.</p> <p>The serial port can simultaneously transmit and receive data.</p> <p>It can also buffer one byte at receive, which prevents the receive data from being lost</p> <p>The serial port can operate in one of four modes.</p> <p><b>a) Mode 0</b></p> <p>In this mode, the rxd0i pin receives serial data and the rxd0o pin transmits serial data. The txd0 pin outputs the shift clock.</p> <p>Eight bits are transmitted with LSB first.</p> <p>The baud rate is fixed at 1/12 of the crystal (clk input) frequency.</p> <p><b>b) Mode 1</b></p> <p>In this mode, the rxd0i pin receives serial data and the txd0 pin transmits serial data. No external shift clock is used, and the following 10 bits are transmitted:</p> <ol style="list-style-type: none"> <li>1. One Start Bit (always 0)</li> <li>2. Eight Data Bits (LSB first)</li> <li>3. One Stop Bit (always 1)</li> <li>4. On receive,</li> </ol> <p><b>c) Mode 2</b></p> <p>The baud rate is fixed at 1/32 or 1/64 of the oscillator (clk input) frequency, and the following 11 bits are transmitted or received:</p> <ol style="list-style-type: none"> <li>1. One Start Bit (0)</li> <li>2. Eight Data Bits (LSB first)</li> <li>3. One Programmable Ninth Bit</li> <li>4. One Stop Bit (1)</li> </ol> <p>The ninth bit can be used to control the parity of the serial interface.</p> <p><b>d) Mode 3</b></p> <p>The only difference between Mode 2 and Mode 3 is that the baud rate is variable in Mode 3.</p>	(13M)																																																												
8	<b>How do you interface 8051 microcontroller with keyboard? Explain in detail. (13M)</b>																																																													

	<p><b>BTL 6</b></p> <p><b>Ans: Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:311-314</b></p> <p>Keyboards are organized in a matrix of rows and columns. The CPU accesses both rows and columns through ports. Therefore, with two 8-bit ports, an 8 x 8 matrix of keys can be connected to a microprocessor. When a key is pressed, a row and a column make a contact. Otherwise, there is no connection between rows and columns. A 4x4 matrix connected to two ports. The rows are connected to an output port and the columns are connected to an input port.</p> 
	(13M)
	<b>PART C</b>
1	<p><b>Write an ALP to generate a triangular waveform and sine waveform (15M) BTL 6</b></p> <p><b>Ans: Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:331,344-346</b></p> <p>MOV A, #00H      INCR: MOV P1, A      INC A      CJNE A, #255, INCR      DECR: MOV P1, A      DEC A      CJNE A, #00, DECR      SJMP INCR      END</p> <p style="text-align: right;">(8M)</p> <p>ORG 0000H      AGAIN: MOV DPTR, #SINETABLE      MOV R3, #COUNT      UP: CLR A      MOVC A, @A+DPTR      MOV P1, A      INC DPTR      DJNZ R3, UP      SJMP AGAIN      ORG 0300H      SINETABLE DB 128, 192, 238, 255, 238, 192, 128, 64, 17, 0, 17, 64, 128</p> <p style="text-align: right;">(7M)</p> <p>END</p>
2	<p><b>Explain in detail the procedure to interface stepper motor with 8051. (May 2015) BTL 5</b></p> <p><b>Ans: Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:432-438</b></p> <p>Stepper motor is a widely used device that translates electrical pulses into mechanical movement. Stepper motor is used in applications such as; disk drives, dot matrix printer, robotics etc., The construction of the motor is as shown in figure 1 below.</p>



(8M)

Program:

```

MOV A,#66H
BACK: MOV P1,A
RR A
ACALL DELAY
SJMP BACK
DELAY: MOV R1,#100
UP1: MOV R2,#50
UP: DJNZ R2,UP
DJNZ R1,UP1
RET

```

Program:

```

ORG 0000H
MOV A, #66H
MOV R0, #45
BACK: RR A
MOV P1, A
ACALL DELAY
DJNZ R0, BACK
END

```

(5M)

- 3 Write a program for generation of unipolar square waveform of 1KHZ frequency using Timer 0 of 8051 in mode 0. Consider the system frequency as 12 MHZ. (Apr/May 2017) BTL 5

**Ans:** Refer: Mohamed Ali Mazidi, Janice Gillispie Mazidi, Rolin McKinlay, PG.NO:203

**Mode-1 baud rate generation:**

Timer-1 is used to generate baud rate for mode-1 serial communication.

Timer-1 is used in timer mode-2 as an auto-reload 8-bit timer.

The data rate is generated by timer-1 using the following formula

Where, SMOD is the 7th bit of PCON register fosc is the crystal oscillator frequency  
 $f_{baud} = \frac{f_{osc}}{12 \times [256 - (TH1)]}$  is the timer overflow frequency in timer mode-2, which is the auto-reload mode. (8M)

If timer-1 is not run in mode-2, then the baud rate is,

$$f_{baud} = \frac{2^{SMOD}}{32} \times \frac{f_{osc}}{12 \times [256 - (TH1)]}$$

(5M)

CS8501      THEORY OF COMPUTATION

L T P C

3 0 0 3

**OBJECTIVES:**

- To understand the language hierarchy
- To construct automata for any given pattern and find its equivalent regular expressions
- To design a context free grammar for any given language
- To understand Turing machines and their capability
- To understand undecidable problems and NP class problems

**UNIT I            AUTOMATA FUNDAMENTALS**

9

Introduction to formal proof – Additional forms of Proof – Inductive Proofs –Finite Automata  
 – Deterministic Finite Automata – Non-deterministic Finite Automata – Finite Automata  
 with Epsilon Transitions

**UNIT II            REGULAR EXPRESSIONS AND LANGUAGES**

9

Regular Expressions – FA and Regular Expressions – Proving Languages not to be regular –  
 Closure Properties of Regular Languages – Equivalence and Minimization of Automata.

**UNIT III            CONTEXT FREE GRAMMAR AND LANGUAGES**

9

CFG – Parse Trees – Ambiguity in Grammars and Languages – Definition of the Pushdown  
 Automata – Languages of a Pushdown Automata – Equivalence of Pushdown Automata  
 and CFG, Deterministic Pushdown Automata.

**UNIT IV            PROPERTIES OF CONTEXT FREE LANGUAGES**

9

Normal Forms for CFG – Pumping Lemma for CFL – Closure Properties of CFL – Turing Machines  
 – Programming Techniques for TM.

**UNIT V            UNDECIDABILITY**

9

Non Recursive Enumerable (RE) Language – Undecidable Problem with RE – Undecidable  
 Problems about TM – Post's Correspondence Problem, The Class P and NP.

**TOTAL :45PERIODS****OUTCOMES:**

**Upon completion of the course, the students will be able to:**

- Construct automata, regular expression for any pattern.
- Write Context free grammar for any construct.
- Design Turing machines for any language.
- Propose computation solutions using Turing machines.
- Derive whether a problem is decidable or not.

**TEXT BOOK:**

1. J.E.Hopcroft, R.Motwani and J.D Ullman, -Introduction to Automata Theory, Languages and Computations, Second Edition, Pearson Education, 2003.

**REFERENCES**

2. H.R.Lewis and C.H.Papadimitriou, -Elements of the theory of Computation, Second Edition, PHI, 2003.

<b>UNIT I AUTOMATA FUNDAMENTALS</b>	
<b>PART A</b>	
<b>Q.No</b>	<b>Questions</b>
<b>1</b>	<b>List out the four ways of theorem proving. (Nov/Dec 2010) (BTL 1)</b> The four ways of theorem proving are: 1. Deductive 2. If and only if 3. Induction 4. Proof by contradiction
<b>2</b>	<b>What is deductive proof? (BTL 1)</b> A deductive proof consists of a sequence of statements, which starts from a hypothesis, or a given statement to a conclusion. Each step is satisfying some logical principle.
<b>3</b>	<b>Differentiate NFA from DFA. (Nov/Dec 2011, May/June 2013, Nov/Dec 2015) (BTL 2)</b> Non Deterministic Finite Automaton is the one in which there exists many paths for a specific input from current state to next state. NFA can be used in theory of computation because they are more flexible and easier to use than DFA. Deterministic Finite Automaton is a FA in which there is only one path for a specific input from current state to next state. There is a unique transition on each input symbol.
<b>4</b>	<b>What is a Non Deterministic Finite Automaton? (BTL 1)</b> Non Deterministic Finite Automaton is the one in which there exists many paths for a specific input from current state to next state. NFA can be used in theory of computation because they are more flexible and easier to use than DFA.
<b>5</b>	<b>Write a short note on minimization of DFA. (BTL 1)</b> Minimization of DFA reduces the number of states from given FA. First find out which two states are equivalent and then those two states are to be replaced by one representative state. For finding the equivalent states, the rule applied is that “The two states S1 & S2 are equivalent if and only if both the states are final or non-final states”.
<b>6</b>	<b>Prove <math>1+2+3+\dots+n = n(n + 1)/2</math> using induction method. (Nov/Dec 2012) (BTL 5)</b> Consider the two step approach for a proof by method of induction 1. Basis of induction: Let $n = 1$ then $LHS = 1$ and $RHS = 1 + 1/2 = 1$ Hence, $LHS = RHS$ . 2. Induction hypothesis: To prove $1 + 2 + 3 + \dots + n = n(n + 1)/2$ Consider $n = n + 1$ then, $\begin{aligned} 1 + 2 + 3 + \dots + n + (n + 1) &= n(n + 1)/2 + (n + 1) \\ &= n^2 + 3n + 2/2 \\ &= (n + 1)(n + 2)/2 \end{aligned}$ Thus it is proved that $1 + 2 + 3 + \dots + n = n(n + 1)/2$ .
<b>7</b>	<b>Define – Finite Automaton (Nov/Dec 2016) (BTL 1)</b>

	FA consists of a finite set of states and a set of transitions from state to state that occur on input symbols chosen from an alphabet $\Sigma$ . Finite Automaton is denoted by a 5-tuple $(Q, \Sigma, \delta, q_0, F)$ , where $Q$ is the finite set of states, $\Sigma$ is a finite input alphabet, $q_0$ in $Q$ is the initial state, $F$ is the set of final states and $\delta$ is the transition mapping function $Q * \Sigma$ to $Q$ .
8	<b>Define – Transition Diagram</b> (BTL 2) Transition diagram is a directed graph in which the vertices of the graph correspond to the states of FA. If there is a transition from state $q$ to state $p$ on input $a$ , then there is an arc labelled ‘ $a$ ’ from $q$ to $p$ in the transition diagram.
9	<b>What are the applications of automata theory?</b> (BTL 3) The applications of automata theory are as follows: 1. In compiler construction 2. In switching theory and design of digital circuits 3. To verify the correctness of a program 4. Design and analysis of complex software and hardware systems 5. To design finite state machines such as Moore and Mealy machines
10	<b>What is a string?</b> (BTL 1) A string $x$ is accepted by a Finite Automaton $M = (Q, \Sigma, \delta, q_0, F)$ if $\delta(q_0, x) = p$ , for some $p$ in $F$ . FA accepts a string $x$ if the sequence of transitions corresponding to the symbols of $x$ leads from the start state to accepting state.
11	<b>List out the operations on strings.</b> (BTL 1) The various operations performed on strings are: 1. Length of a string 2. Empty string 3. Concatenation of string 4. Reverse of a string 5. Power of an alphabet 6. Kleene closure 7. Substring 8. Palindrome
12	<b>What are the components of finite automaton model?</b> (BTL 1) The components of FA model are input tape, read control and finite control. 1. The input tape is divided into number of cells. Each cell can hold one i/p symbol. 2. The read head reads one symbol at a time and moves ahead. 3. Finite control acts like a CPU. Depending on the current state and input symbol read from the input tape it changes state.
13	<b>List out the applications for finite automaton.</b> (BTL 4) Text editors and lexical analyzers are designed as finite state systems. A lexical analyzer scans the symbols of a program to locate strings corresponding to identifiers, constants etc, and it has to remember limited amount of information.
14	<b>Define TOC</b> (BTL 1) Theory of Computation is the branch that deals with how efficiently problems can be solved on a model of computation, using an algorithm. The field is divided into three major branches: automata theory, computability theory, and computational complexity theory.
15	<b>Why switching circuits are called as finite state systems?</b> (BTL 4) A switching circuit consists of a finite number of gates, each of which can be in any one of the two conditions 0 or 1. Although the voltages assume infinite set of values, the electronic circuitry is designed so that the voltages corresponding to 0 or 1 are stable and all others adjust to these values. Thus control unit of a computer is a finite state system.

<b>16</b>	<b>What is Moore machine and Mealy machine? (May/June 2008)</b> (BTL 1) A special case of FA is Moore machine in which the output depends on the state of the machine. An automaton in which the output depends on the transition and current input is called Mealy machine.
<b>17</b>	<b>What is meant by DFA? (Nov/Dec 2014)</b> (BTL 1) Deterministic Finite Automaton (DFA) also known as deterministic finite state machine is a finite state machine that accepts/rejects finite strings of symbols and only produces a unique computation (or run) of the automaton for each input string. 'Deterministic' refers to the uniqueness of the computation.
<b>18</b>	<b>What is regular language? (Nov/Dec 2018)</b> (BTL1) The language accepted by M is L(M) is the set $\{x \mid \delta(q_0, x) \text{ is in } F\}$ . A language is regular if it is accepted by some finite automaton.
<b>19</b>	<b>What is <math>\epsilon</math>-closure of state <math>q_0</math>?</b> (BTL 2) $\epsilon$ -closure ( $q_0$ ) denotes a set of all vertices p such that there is a path from $q_0$ to p labeled $\epsilon$ . Example: closure ( $q_0$ ) = $\{q_0, q_1\}$ .
<b>20</b>	<b>List out the operations on Languages.</b> (BTL 2) The operations permitted on languages are: 1. Product 2. Reversal 3. Power 4. Kleene star 5. Kleene plus 6. Union 7. Intersection
<b>21</b>	<b>Consider the string <math>x=011</math> and <math>y=110</math>. Find <math>xy</math> and <math>yx</math>. Are they equal? (Nov/Dec 2006)</b> (BTL 4) No, the two strings $xy$ and $yx$ are unequal. Because, $xy=011110$ and $yx=110011$ . Hence they are unequal. In general $xy \neq yx$ .
<b>22</b>	<b>What is meant by equivalent states in DFA?</b> (BTL 2) The two states are said to be equivalent if there are same inputs coming to the state and same output going out from the states.
<b>23</b>	<b>When do you say any two states are unequal in DFA?</b> (BTL 2) The two states are said to be unequal if there are same inputs coming to the state and not the same output going out from the states.
<b>24</b>	<b>NFSA is efficient than DFSA. Justify this. (May/June 2008)</b> (BTL 4) No. Both NFSA and DFSA are equivalent in terms of efficiency because, language accepted by NFSA is equal to that of language accepted by DFSA.
<b>25</b>	<b>How do you differentiate initial and final state in a FSA?</b> (BTL 2) In a FSA, the initial state or start state is represented by an arrow without origin. The final or accepting states are represented through double circles.
<b>PART- B</b>	
<b>1</b>	<b>(i) Explain if L is accepted by an NFA with <math>\epsilon</math>-transition then show that L is accepted by an NFA without <math>\epsilon</math>-transition. (6) (Nov/Dec 2009)</b> (BTL 3) Answer: Page No. 2-33 in A.A. Puntambekar book
	<b>Key Points:</b> 1. Theorem statement (2)

2. Procedure with derivation (2)  
 3. Example with diagram (1)  
 4. Result (1)

**(ii) Construct a DFA equivalent to the NFA.  $M=(\{p,q,r\}, \{0,1\}, \delta, p, \{q,s\})$  Where  $\delta$  is defined in the following table.** (7) (BTL 3)

	0	1
p	{q,s}	{q}
q	{r}	{q,r}
r	{s}	{p}
s	-	{p}

**(May/June 2011)**

Answer: Page No. 2-52 in A.A. Puntambekar book

Key Points:

- $\delta$  mapping for all states (4)
- Transition table of DFA (2)
- Transition Diagram of DFA (1)

**2 (i). Demonstrate how the set  $L = \{a^n b^n / n \geq 1\}$  is not a regular.** (7)

**(Nov/Dec 2011, May/June 2009)**

(BTL 4)

Answer: Page No. 3-59 in A.A. Puntambekar book

Key Points:

- Proof with derivation (7)

**(ii). Construct a DFA equivalent to the NFA given below.** (6) (BTL 3)

	0	1
P	{P,Q}	{P}
Q	{R}	{R}
R	{S}	-
S	{S}	{S}

**(Nov/Dec 2013)**

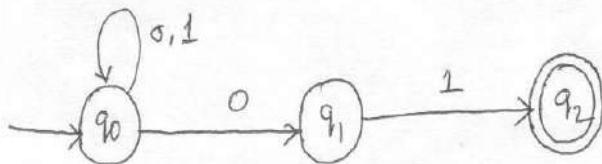
Answer: Page No. 2-53 in A.A. Puntambekar book

Key Points:

- $\delta$  mapping for all states (4)
- Transition table of DFA (1)
- Transition Diagram of DFA (1)

**3 (i). Examine whether the language  $L = (0^n 1^{n+1} / n \geq 1)$  is regular or not? Justify your answer.** (7) (May/June 2007) (BTL 5)

	<p>Answer: Page No. 3-58 in A.A. Puntambekar book</p> <p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. Proof with derivation (7)</li> </ol> <p><b>(ii). Let L be a set accepted by a NFA then show that there exists a DFA that accepts L.</b> (6) <b>(BTL 3)</b></p> <p>Answer: Page No. 2-48 in A.A. Puntambekar book</p> <p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. Proof using induction (6)</li> </ol>
4	<p><b>(i)Summarize a construction of NDFA accepting all string in {a, b}with either two consecutive a"s or two consecutive b"s. (6)</b> <b>(BTL 3)</b></p> <p>Answer: Page No. 2-27 in A.A. Puntambekar book</p> <p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. Transition Diagram of NFA (5)</li> <li>2. Transition table of NFA (1)</li> </ol> <p><b>(ii)Give the DFA accepting the following language. Set of all strings beginning with a 1 that when interpreted as a binary integer is a Multiple of 5. (7)</b> <b>(BTL 4)</b></p> <p>Answer: Page No. 2-15 in A.A. Puntambekar book</p> <p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. Transition table of DFA (5)</li> <li>2. Transition Diagram of DFA (2)</li> </ol>
5	<p><b>(i)Describe the following: Let L be a set accepted by an NFA. Then prove that there exists a deterministic finite automaton that accepts L.Is the converse true? Justify your answer.(7)</b> <b>(May/June 2014, Nov/Dec 2016)</b> <b>(BTL 5)</b></p> <p>Answer: Page No. 2-48 in A.A. Puntambekar book</p> <p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. Theorem statement (2)</li> <li>2. Procedure with derivation (3)</li> <li>3. Example with diagram (1)</li> <li>4. Result (1)</li> </ol> <p><b>(ii)Construct DFA equivalent to the NFA given below: (6)</b> <b>(BTL 4)</b></p>



Answer: Page No. 2-67 in A.A. Puntambekar book

Key Points:

1.  $\delta$  mapping for all states (4)
2. Transition table of DFA (1)
3. Transition Diagram of DFA(1)

**6** Compose that a language L is accepted by some  $\epsilon$ -NFA if and only if L is accepted by some DFA. (13) (Nov/Dec 2018) (BTL 3)

Answer: Page No. 2-33 in A.A. Puntambekar book

Key Points:

1. Theorem statement (2)
2. Procedure with derivation (8)
3. Example with diagram (2)
4. Result (1)

**7** (i). Show how a language L is accepted by some DFA if L is accepted by some NFA. (7) (May/June 2014, Nov/Dec 2016) (BTL 3)

Answer: Page No. 2-48 in A.A. Puntambekar book

Key Points:

1. Theorem statement (2)
2. Procedure with derivation (3)
3. Example with diagram (1)
4. Result (1)

(ii). Convert the following NFA to its equivalent DFA.(6)

	a	b
P	{P,Q}	{P}
Q	{R}	{R}
R	{S}	-
S	{S}	{S}

(May/June 2007)

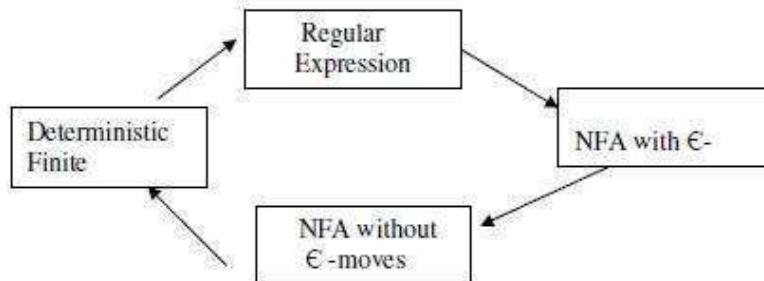
(BTL 4)

Answer: Page No. 2-53 in A.A. Puntambekar book

	<p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. <math>\delta</math> mapping for all states (4)</li> <li>2. Transition table of DFA (1)</li> <li>3. Transition Diagram of DFA (1)</li> </ol>												
<b>8</b>	<p><b>(i) Describe that “A language L is accepted by some DFA if and only if L is accepted by some NFA.(6) (May/June 2014, Nov /Dec 2016) (BTL 2)</b></p> <p>Answer: Page No. 2-48 in A.A. Puntambekar book</p> <p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. Theorem statement (2)</li> <li>2. Procedure with derivation (3)</li> <li>3. Example with diagram (1)</li> </ol> <p><b>(ii) Construct Finite Automate equivalent to the regular expression <math>(ab+a)^*</math> (7) (BTL 4)</b></p> <p>Answer: Page No. 3-11 in A.A. Puntambekar book</p> <p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. RE conversion for ab (2)</li> <li>2. RE conversion for a (2)</li> <li>3. RE conversion for <math>(ab + a)^*</math> (3)</li> </ol>												
<b>9</b>	<p><b>(i). Point out the steps in conversion of NFA to DFA and for the following convert NFA to a DFA. (7) (BTL 5)</b></p> <table style="margin-left: auto; margin-right: auto;"> <tr> <td><math>\delta</math></td> <td>a</td> <td>b</td> </tr> <tr> <td>p</td> <td><math>\{p\}</math></td> <td><math>\{p,q\}</math></td> </tr> <tr> <td>q</td> <td><math>\{r\}</math></td> <td><math>\{r\}</math></td> </tr> <tr> <td>r</td> <td><math>\{\phi\}</math></td> <td><math>\{\phi\}</math></td> </tr> </table> <p><b>(May/June 2009)</b></p> <p>Answer: Page No. 2-59 in A.A. Puntambekar book</p> <p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. <math>\delta</math> mapping for all states (4)</li> <li>2. Transition table of DFA (2)</li> <li>3. Transition Diagram of DFA(1)</li> </ol> <p><b>(ii). Discuss on the relation between DFA and minimal DFA. (6) (BTL 2)</b></p> <p>Answer: Page No. 2-87 in A.A. Puntambekar book</p> <p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. Difference between normal DFA and minimized DFA (3)</li> <li>2. Construction of equivalent states. (3)</li> </ol>	$\delta$	a	b	p	$\{p\}$	$\{p,q\}$	q	$\{r\}$	$\{r\}$	r	$\{\phi\}$	$\{\phi\}$
$\delta$	a	b											
p	$\{p\}$	$\{p,q\}$											
q	$\{r\}$	$\{r\}$											
r	$\{\phi\}$	$\{\phi\}$											
<b>10</b>	<b>Tabulate the difference between the NFA and DFA .Convert the following <math>\epsilon</math>-NFA to</b>												

	<b>DFA. (13)</b>																				
	<table border="1"> <thead> <tr> <th></th><th><math>\epsilon</math></th><th>a</th><th>b</th><th>c</th></tr> </thead> <tbody> <tr> <td>P</td><td>-</td><td>{P}</td><td>{Q}</td><td>{R}</td></tr> <tr> <td>Q</td><td>{P}</td><td>{Q}</td><td>{R}</td><td>-</td></tr> <tr> <td>*R</td><td>{Q}</td><td>{R}</td><td>-</td><td>{P}</td></tr> </tbody> </table>		$\epsilon$	a	b	c	P	-	{P}	{Q}	{R}	Q	{P}	{Q}	{R}	-	*R	{Q}	{R}	-	{P}
	$\epsilon$	a	b	c																	
P	-	{P}	{Q}	{R}																	
Q	{P}	{Q}	{R}	-																	
*R	{Q}	{R}	-	{P}																	
	(May/June 2011, Nov/Dec 2013) (BTL 5)																				
	Answer: Page No. 2-79 in A.A. Puntambekar book																				
	Key Points:																				
	<ol style="list-style-type: none"> <li>1. <math>\delta</math> mapping for all states (8)</li> <li>2. Transition table of DFA (3)</li> <li>3. Transition Diagram of DFA (2)</li> </ol>																				
	<b>PART – C</b>																				
1	<p><b>(i). Convert the regular expression ”a(a+b)*a” into <math>\epsilon</math>-NFA (8) (Nov/Dec 2011) (BTL 4)</b></p> <p>Answer: Page No. 3-19 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. <math>\delta</math> mapping for all states (5)</li> <li>2. Transition table of <math>\epsilon</math>-NFA (2)</li> <li>3. Transition Diagram of <math>\epsilon</math>- NFA (1)</li> </ol> <p><b>(ii). Find the minimal state DFA for the above <math>\epsilon</math>-NFA.(7) (BTL 3)</b></p> <p>Answer: Page No. 3-19 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Equivalent states construction (5)</li> <li>2. Resultant minimized DFSA (2)</li> </ol>																				
2	<p><b>(i) Draw the transition diagram for recognizing the set of all Operators in c Language.(15) (BTL 4)</b></p> <p>Answer: Page No. 2-18 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Language set of Operators (3)</li> <li>2. Transition diagram (12)</li> </ol>																				
3	<p><b>Give DFA's accepting the following language over the alphabet{0,1}. The set of all the strings beginning with a1 that when interrupted as a binary integer , is multiple of 5, For example strings 101,1010 and 1111 are in the language 0,100 and 111 are not. (15) (BTL 5)</b></p> <p>Answer: Page No. 2-25 in A.A. Puntambekar book</p> <p>Key Points</p>																				

	<ol style="list-style-type: none"> <li>1. <math>\delta</math> mapping for all states (12)</li> <li>2. Transition table of DFA(2)</li> <li>3. Transition Diagram of DFA (1)</li> </ol>
<b>UNIT II REGULAR EXPRESSIONS AND LANGUAGES</b>	
<b>Regular Expressions – FA and Regular Expressions – Proving Languages not to be regular – Closure Properties of Regular Languages – Equivalence and Minimization of Automata</b>	
<b>PART – A</b>	
<b>1</b>	<b>Write the regular expression for “set of all strings with even length”.</b> (BTL 4) The regular expression for “set of all strings with even length” is $R = (11)^*$ .
<b>2</b>	<b>What is a regular expression? (May/June 2010)</b> (BTL 1) A regular expression is a string that describes the whole set of strings according to certain syntax rules. These expressions are used by many text editors and utilities to search bodies of text for certain patterns etc. Definition: Let $\Sigma$ be an alphabet. The regular expression over $\Sigma$ and the sets they denote are: 1. $\Phi$ is a r.e and denotes empty set 2. $\epsilon$ is a r.e and denotes the set $\{ \epsilon \}$ 3. For each ‘a’ in $\Sigma$ , $a^+$ is a r.e and denotes the set $\{a\}$ 4. If ‘r’ and ‘s’ are r.e denoting the languages R and S respectively the $(r+s)$ , $(rs)$ and $(r^*)$ are r.e that denote the sets $RUS$ , $RS$ and $R^*$ respectively
<b>3</b>	<b>If <math>L = \{The\ language\ starting\ and\ ending\ with\ ‘a’\ and\ having\ any\ combinations\ of\ ‘b’\ in\ between\},</math> then what will be the regular expression?</b> (BTL 4) The regular expression is written as $r = a b^* a$ .
<b>4</b>	<b>Write the regular expression for the language that accepts all strings in which ‘a’ appears tripled over the set <math>\Sigma = \{a\}</math>.</b> (BTL 4) The regular expression is written as $r = (aaa)^*$ .
<b>5</b>	<b>Write the regular expression for the language in which every string will have at least one ‘a’ followed by at least one ‘b’.</b> (BTL 4) The regular expression for the language in which every string will have at least one ‘a’ followed by atleast one ‘b’ is given as: $R=a^+b^+$
<b>6</b>	<b>Construct a regular expression for the language over the set <math>\Sigma = \{a, b\}</math> in which total numbers of ‘a’ are divisible by 3.</b> (BTL 4) The regular expression is $(b^* a b^* a b^* a b^*)^*$ .
<b>7</b>	<b>Write the regular expression to denote language L which accepts all the strings that begins or ends with either 00 or 11. (May/June 2014)</b> (BTL 4) The regular expression consists of two parts: $L1 = (00+11) (\text{any no of } 0's \text{ and } 1's) = (00+11)(0+1)^*$ $L2 = (\text{any no of } 0's \text{ and } 1's)(00+11) = (0+1)^*(00+11)$ Hence, regular expression $R=L1+L2 = [(00+11)(0+1)^*] + [(0+1)^* (00+11)]$ .
<b>8</b>	<b>Define – Context Free Grammar (Nov/Dec 2018)</b> (BTL 1) A Context Free Grammar (CFG) is denoted as $G = (V, T, P, S)$ where V and T are finite set of variables and terminals respectively. V and T are disjoint. P is a finite set of productions each is of the form $A \rightarrow \alpha$ where A is a variable and $\alpha$ is a string of symbols from $(V \cup T)^*$
<b>9</b>	<b>What is the relationship between FA and regular expression?</b> (BTL 4)



10	<p><b>List out the ways to simplify the context free grammar.</b> (Nov/Dec 2009) <span style="float: right;">(BTL 2)</span></p> <p>The three ways of simplifying a context free grammar are:</p> <ol style="list-style-type: none"> <li>1. Removing the useless symbols from the set of productions</li> <li>2. By eliminating the empty productions</li> <li>3. By eliminating the unit productions</li> </ol>
11	<p><b>List out the methods that are used for converting DFA to RE.</b> <span style="float: right;">(BTL 2)</span></p> <p>The three methods are:</p> <ol style="list-style-type: none"> <li>1. Regular Expression Equation Method</li> <li>2. Arden's Theorem</li> <li>3. State Elimination Technique</li> </ol>
12	<p><b>State Arden's theorem.</b> (May/june 2010) <span style="float: right;">(BTL 1)</span></p> <p>Arden's theorem helps in checking the equivalence of two regular expressions. Let P and Q be the two regular expressions over the input alphabet <math>\Sigma</math>. The regular expression R is given as:  <math>R = Q + RP</math> which has a unique solution as <math>R = QP^*</math>.</p>
13	<p><b>What is dead state?</b> <span style="float: right;">(BTL 2)</span></p> <p>All the non-final states which transmit to itself for all input symbols in <math>\Sigma</math> are called dead state.</p>
14	<p><b>Let R be any set of regular languages. Is U R regular? Prove it.</b> <span style="float: right;">(BTL 4)</span></p> <p>Yes, <math>UR</math> is regular. Let P, Q be any two regular languages. As per theorem <math>L(R) = L(P \cup Q) = L(P+Q)</math>    Since '+' is a operator for regular expressions <math>L(R)</math> is also regular.</p>
15	<p><b>What is pumping lemma?</b> (Nov/Dec 2012, May/june 2014, Nov/Dec 2015) <span style="float: right;">(BTL 1)</span></p> <p>Let L be a regular language. Then there exists a constant n such that for every string w in L such that <math> w  \geq n</math>, <math>w = xyz</math> such that:</p> <ol style="list-style-type: none"> <li>1. <math>y \neq \epsilon</math></li> <li>2. <math> xy  \leq n</math></li> <li>3. For all <math>i \geq 0</math>, <math>xy^i z \in L</math></li> </ol>
16	<p><b>What is sentential form?</b> <span style="float: right;">(BTL 1)</span></p> <p>A string of terminals and variables <math>\alpha</math> is called a sentential form if: <math>S \Rightarrow \alpha</math>, where S is the start symbol of the grammar.</p>
17	<p><b>List the closure properties of regular language.</b> (May/June 2016) <span style="float: right;">(BTL 2)</span></p> <p>The regular languages are closed under the following properties:</p> <ol style="list-style-type: none"> <li>1. Union</li> <li>2. Intersection</li> <li>3. Complement</li> <li>4. Difference</li> <li>5. Reversal</li> <li>6. Closure</li> <li>7. Concatenation</li> </ol>

	8. Homomorphism 9. Inverse Homomorphism	
18	<b>Prove that <math>(0 * 1^*)^* = (0 + 1)^*</math>. (Nov/Dec 2010, May/June 2013)</b> (BTL 5) LHS: $(0 * 1^*)^* = \{ \epsilon, 0, 1, 00, 11, 0011, 011, 0011110\dots \}$ RHS: $(0+1)^* = \{ \epsilon, 0, 1, 00, 11, 0011, 011, 0011110\dots \}$ Hence LHS = RHS is proved	
19	<b>What is an ambiguous grammar? (Nov/Dec 2010, May/June 2012, Nov/Dec 2015) (BTL 2)</b> A grammar is said to be ambiguous if it has more than one derivation tree for a sentence or in other words if it has more than one leftmost derivation or more than one rightmost derivation.	
20	<b>If <math>S \rightarrow aSb \mid aAb, A \rightarrow bAa, A \rightarrow ba</math> then determine CFL.</b> (BTL 5) Solution: $S \rightarrow aAb \Rightarrow abab$ $S \rightarrow aSb \Rightarrow a aAb b \Rightarrow a a ba b b$ (sub $S \rightarrow aAb$ ) $S \rightarrow aSb \Rightarrow a aSb b \Rightarrow a a aAb b b \Rightarrow a a a ba b b$ Thus $L = \{a^n b^m a^m b^n, \text{ where } n, m \geq 1\}$	
21	<b>When do you say a language is inherently ambiguous?</b> (BTL 2) A CFL 'L' is said to be inherently ambiguous, if all the grammars G1, G2, G3, ..., Gn of CFL are giving two or more derivation tree for the strings.	
22	<b>What is the use of pumping lemma?</b> (BTL 1) It is used to check whether the given language is regular or not.	
23	<b>Find the CFG for the RE <math>(0+1)^2</math></b> (BTL 5) $S \rightarrow AB$ $A \rightarrow 0 \mid 1$ $B \rightarrow 0 \mid 1$	
24	<b>What is the closure property of regular sets? (Nov/Dec 2017)</b> (BTL 1) If certain languages are regular and language L is formed by them by operations (such as union, concatenation and so on) and if we find L as regular, then this property is called closure property of regular sets.	
25	<b>Construct RE for the language over the set {a,b} in which total length is divisible by 3. (BTL 5)</b> The corresponding Regular expression is $[(0+1)(0+1)(0+1)]^*$	
<b>PART-B</b>		
1	<p><b>(i) Explain and draw the parse tree for the string <math>1+2*3</math> given the grammar <math>G=(V, \Sigma, R, E)</math> where</b>  <math>V=\{E, D, 1, 2, 3, 4, 5, 6, 7, 9, 0, +, -, *, /, (), *\}</math>  <math>\Sigma=\{1, 2, 3, 4, 5, 6, 7, 8, 9, 0, +, -, *, /, (), *\}</math> where R contains the following rules :</p> <p><math>E \rightarrow D \mid (E) \mid E+E \mid E-E \mid E/E</math>  <math>D \rightarrow 0 \mid 1 \mid 2 \mid \dots \mid 9</math></p>	(6) (BTL 2)
	Answer: Page No. 4-33 in A.A. Puntambekar book	
	Key Points:	
	<ol style="list-style-type: none"> <li>1. Definition of Parse tree (2)</li> <li>2. Parse tree diagram for <math>1+2*3</math> (4)</li> </ol>	
	<b>(ii). Let <math>G=(V, T, P, S)</math> be a Context Free Grammar then prove that if the recursive</b>	

	<p><b>inference procedure calls tells us that terminal string W is in the language of variable A ,then there is a parse tree with a root A and yield w.</b> (7) (May/June 2007) (BTL 4)</p> <p>Answer: Page No. 4-30 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Theorem statement (2)</li> <li>2. Induction proof (5)</li> </ol>
2	<p><b>Let G be the grammar s-&gt;0B 1A, A-&gt;0 0S 1AA, B-&gt;1 1S 0BB .For the string 00110101, find its leftmost derivation and derivation tree.</b> (8+5) (Nov/Dec 2018) (BTL 3)</p> <p>Answer: Page No. 4-56 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Left Most Derivation (LMD) (8)</li> <li>2. Derivation tree for 00110101 (5)</li> </ol>
3	<p><b>Examine the grammar</b>  <math>S \rightarrow 0A0/1B1/BB</math>  <math>B \rightarrow C</math>  <math>B \rightarrow S/A</math>  <math>C \rightarrow S/ \epsilon</math></p> <p><b>and Simplify using the safe order</b></p> <p>(i) Eliminate <math>\epsilon</math>- productions(3)  (ii) Eliminate unit production(3)  (iii) Eliminate useless symbols(3)  (iv) Put ( resultant) the grammar in Chomsky normal form(4) (May/June 2015)  (BTL 1)</p> <p>Answer: Page No. 4-60 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Resultant grammar after removal of <math>\epsilon</math>- productions (3)</li> <li>2. Resultant grammar after removal of unit productions (3)</li> <li>3. Resultant grammar after removal of useless productions (3)</li> <li>4. CNF (4)</li> </ol>
4	<p><b>(i) Develop an equivalent grammar G in CNF for the grammar G1 where</b></p> $G1 = (\{S, A, B\}, \{a, b\}, \{S \rightarrow ASB   \epsilon, A \rightarrow aAS   a, B \rightarrow SbS   A   bb\}, S) \quad (7)$ <p>(BTL 3)</p> <p>Answer: Page No. 5-7 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Optimized Grammar (4)</li> <li>2. CNF definition and rules (2)</li> </ol>

	<p>3. Resultant CNF (1)</p> <p>(ii) <b>What is an ambiguous grammar ? Explain with an example. (6) (May/June 2008) (BTL 3)</b></p> <p>Answer: Page No. 4-34 in A.A. Puntambekar book.</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Definition of ambiguous Grammar (2)</li> <li>2. Example grammar with two parse trees. (4)</li> </ol>
5	<p><b>i). Convert the following grammar into GNF (13) (Nov/Dec 2010) (BTL 4)</b></p> <p><b>S→XY1/0</b></p> <p><b>x→00X/Y</b></p> <p><b>Y→1X1</b></p> <p>Answer: Page No. 5-37 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. GNF definition (2)</li> <li>2. GNF step (11)</li> </ol>
6	<p><b>(i)If S-&gt;aSb aAb, A-&gt;bSa, A-&gt;ba is the context free grammar. Analyze the context free language. (5) (BTL 4)</b></p> <p>Answer: Page No. 4-20 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Language set (1)</li> <li>2. Derivation example(4)</li> </ol> <p><b>(ii)Consider the grammar</b>  <b>E-&gt;E + E   E*E   (E)   I</b>  <b>I -&gt;a+b</b>  <b>Show that the grammar is ambiguous (8) (May/June 2006, Nov/Dec 2009, Nov/Dec 2013) (BTL 4)</b></p> <p>Answer: Page No. 4-34 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Introduction to Ambiguity (3)</li> <li>2. Proof with two derivation trees.(5)</li> </ol>
7	<p><b>(i)Let G=(V,T,P,S)be a context free grammar (CFG).Then S <math>\alpha</math> if and only if there is a derivation tree for G which yields <math>\alpha</math>.Illustrate the relationship between Derivation and Derivation Trees. (8) (BTL 2)</b></p> <p>Answer: Page No. 4-30 in A.A. Puntambekar book</p>

	<p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Theorem Statement (2)</li> <li>2. Induction Proof (6)</li> </ol> <p><b>(ii) Consider the productions:</b></p> $S \rightarrow aB bA$ $A \rightarrow aS bAA a$ $B \rightarrow bS aBB b$ <p><b>For the string aaabbabbba ,find the leftmost derivation.(5) (BTL 3)</b></p> <p>Answer: Page No. 4-20 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. List the individual Production (1)</li> <li>2. Draw the LMD steps. (4)</li> </ol>
8	<p><b>(i). Brief about GNF. Compare GNF and CNF. (6) (BTL 2)</b></p> <p>Answer: Page No. 5-15 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. GNF Introduction (2)</li> <li>2. Comparison in tabular column (any 4 points) (4)</li> </ol> <p><b>(ii). Construct a grammar in GNF equivalent to</b></p> <p><b>P={S-&gt;aSa, S -&gt;bSb, S-&gt;aa, S-&gt;bb} (7) (May/June 2013) (BTL 4)</b></p> <p>Answer: Page No. 5-16 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. GNF Introduction (2)</li> <li>2. GNF steps (4)</li> <li>3. Resultant GNF (1)</li> </ol>
<b>PART – C</b>	
1	<p><b>Consider the grammar S-&gt; bSaS aSbS  ε.</b></p> <p><b>This grammar is ambiguous . show in particular that the string aab has two:</b></p> <p><b>(i) Parse tree. (5)</b></p>

	<p>(ii) LMD.(5)          (iii) RMD.(5)</p> <p>(Nov /Dec 2009) (BTL 4)</p> <p><b>Answer: Page No. 4-37 in A.A. Puntambekar book</b></p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagram of two parse trees for a string (5)</li> <li>2. Diagram for LMD (5)</li> <li>3. Diagram for RMD (5)</li> </ol>
2	<p><b>Set the algorithm for minimization of a DFA. Construct a minimized DFA for the RE <math>(a+b)(a+b)^*</math> and trace for the string baaaab.</b> (15) (BTL 5)</p> <p>Answer: Page No. 2-87 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Minimized DFA equivalent state construction algorithm. (10)</li> <li>2. Resultant minimized DFA (2)</li> <li>3. Tracing the string baaaab (3)</li> </ol>
3	<p><b>Convert given CFG to CNF where <math>V=\{S,A\}</math>, <math>T=\{0,1\}</math> and <math>P</math> is</b></p> $S \rightarrow AA \mid 0$ $A \rightarrow SS \mid 1$ <p>(Nov/Dec 2006, Nov/Dec 2007, May/June 2012, Nov/Dec 2016) (15) (BTL 5)</p> <p>Answer: Page No. 5-18 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. GNF Introduction (2)</li> <li>2. GNF steps (11)</li> <li>3. Resultant GNF (2)</li> </ol>
<p><b>UNIT III CONTEXT FREE GRAMMAR AND LANGUAGES</b></p> <p><b>CFG – Parse Trees – Ambiguity in Grammars and Languages – Definition of the Pushdown Automata – Languages of a Pushdown Automata – Equivalence of Pushdown Automata and CFG, Deterministic Pushdown Automata.</b></p>	
1	<p><b>What are the different ways of languages accepted by PDA? (Nov/Dec 2009) (BTL 2)</b></p> <p>The two different ways of language acceptance by PDA are:</p> <ol style="list-style-type: none"> <li>1. Acceptance by Empty Stack.</li> <li>2. Acceptance by Final State</li> </ol>
2	<p><b>Define – Pushdown Automata (Nov/Dec 2008, May/June 2009, Nov/Dec 2018) (BTL1)</b></p> <p>A pushdown Automata M is a system <math>(Q, \Sigma, \Gamma, \delta, q_0, Z_0, F)</math></p> <p><math>Q</math> is a finite set of states.</p>

	<p><math>\Sigma</math> is an alphabet called the input alphabet.  <math>\Gamma</math> is an alphabet called stack alphabet.  <math>q_0</math> in <math>Q</math> is called initial state.  <math>Z_0</math> in <math>\Gamma</math> is start symbol in stack.  <math>F</math> is the set of final states.  is a mapping from <math>Q \times (\Sigma \cup \{\epsilon\}) \times \Gamma</math> to finite subsets of <math>Q \times \Gamma^*</math>.</p>
3	<p><b>Define – Instantaneous Description (ID) in PDA (Nov/Dec 2013)</b> <span style="float: right;">(BTL 1)</span></p> <p>ID describe the configuration of a PDA at a given instant. ID is a triple such as <math>(q, w, \gamma)</math>, where <math>q</math> is a state, <math>w</math> is a string of input symbols and <math>\gamma</math> is a string of stack symbols.</p> <p>If <math>M = (Q, \Sigma, \Gamma, \delta, q_0, Z_0, F)</math> is a PDA we say that <math>(q, aw, Za) \mid \dots (p, , \beta a)</math> if <math>\delta(q, a, Z)</math> contains <math>(p, \beta)</math>.</p> <p>In <math>M</math> ‘<math>a</math>’ may be <math>\epsilon</math> or an input symbol. Example: <math>(q_1, BG)</math> is in <math>\delta(q_1, 0)</math> else that <math>(q_1, 011, GGR) \mid \dots (q_1, 11, BGGR)</math>.</p>
4	<p><b>What is the significance of PDA?</b> <span style="float: right;">(BTL 2)</span></p> <p>PDA is used to model the context of the language and where the Finite Automata is used to model regular expression.</p>
5	<p><b>When is a string accepted by a PDA? (Nov/Dec 2014)</b> <span style="float: right;">(BTL 1)</span></p> <p>The input string is accepted by the PDA if:</p> <ol style="list-style-type: none"> <li>1. The final state is reached</li> <li>2. The stack is empty</li> </ol>
6	<p><b>Is NPDA (Nondeterministic PDA) and DPDA (Deterministic PDA equivalent)? (May/June 2008)</b> <span style="float: right;">(BTL 3)</span></p> <p>The languages accepted by NPDA and DPDA are not equivalent. For example, <math>wwR</math> is accepted by NPDA and not by any DPDA.</p>
7	<p><b>Define – Deterministic PDA (Nov/Dec 2009)</b> <span style="float: right;">(BTL 1)</span></p> <p>A PDA <math>M = (Q, \Sigma, \Gamma, \delta, q_0, Z_0, F)</math> is deterministic if:</p> <ol style="list-style-type: none"> <li>1. For each <math>q</math> in <math>Q</math> and <math>Z</math> in <math>\Gamma</math>, whenever <math>\delta(q, \epsilon, Z)</math> is nonempty then <math>\delta(q, a, Z)</math> is empty for all <math>a</math> in <math>\Sigma</math></li> <li>2. For no <math>q</math> in <math>Q</math>, <math>Z</math> in <math>\Gamma</math>, and <math>a</math> in <math>\Sigma \cup \{\epsilon\}</math> does <math>\delta(q, a, Z)</math> contains more than one element.</li> </ol> <p>(Eg): The PDA accepting <math>\{wcwR \mid w \text{ in } (0+1)^*\}</math></p>
8	<p><b>Write the equivalence of acceptance by final state and empty stack.</b> <span style="float: right;">(BTL 3)</span></p> <p>The equivalence of acceptance by final state and empty stack is as follows:</p> <ol style="list-style-type: none"> <li>1. If <math>L = L(M_2)</math> for some PDA <math>M_2</math>, then <math>L = N(M_1)</math> for some PDA <math>M_1</math></li> <li>2. If <math>L = N(M_1)</math> for some PDA <math>M_1</math>, then <math>L = L(M_2)</math> for some PDA <math>M_2</math></li> </ol> <p>Where <math>L(M)</math> = language accepted by PDA by reaching a final state  <math>N(M)</math> = language accepted by PDA by empty stack</p>
9	<p><b>Prove that the NDPA is more powerful than that of DPDA? (May/June 2012)</b> <span style="float: right;">(BTL 4)</span></p> <p>No, NPDA is not powerful than DPDA. Because NPDA may produce ambiguous grammar by reaching its final state or by emptying its stack. But DPDA produces only unambiguous grammar.</p>
10	<p><b>What is the language generated by the grammar <math>G = (V, T, P, S)</math> where <math>P = \{S \rightarrow aSb, S \rightarrow ab\}</math>? (Nov/Dec 2011)</b> <span style="float: right;">(BTL 5)</span></p> <p><math>L(G) = \{a^n b^n \mid n \geq 1\}</math></p>
11	<p><b>What is the language generated by CFG or G?</b> <span style="float: right;">(BTL 2)</span></p> <p>The language generated from CFG is called Context Free language (CFL) which is accepted by PDA.</p>

12	<b>Define – Parse Tree</b> A data structure that represents the source program in a compiler is called parse tree. Parse tree can have nodes and edges.	(BTL 1)
13	<b>Draw the derivation tree for the grammar <math>G = (\{S, A, B\}, \{a, b\}, P, S)</math> Where P is given by <math>S \rightarrow Aa / bB, A \rightarrow ab, B \rightarrow aBb / a</math></b>	(BTL 5)
	<pre> graph TD     S --&gt; b     S --&gt; B     B --&gt; a   </pre>	
14	<b>Differentiate sentences from sentential forms.</b> A sentence is a string of terminal symbols. A sentential form is a string containing a mix of variables and terminal symbols or all variables. This is an intermediate form in doing a derivation.	(BTL 2)
15	<b>Define Pumping lemma for CFL. (May/June 2010, Nov/Dec 2013, May/June 2014)</b> <b>(BTL 1)</b> Let L be a regular language. Then there exists a constant n such that for every string w in L such that $ w  \geq n$ , $w = uvwxy$ such that: 1. $y \neq \epsilon$ 2. $ xy  \leq n$ 3. For all $i \geq 0$ , $uv^i wx^i y \in L$	(BTL 1)
16	<b>What are the uses of context free grammar?</b> The uses of context free grammar are as follows: 1. Construction of compilers 2. Simplified the definition of programming languages 3. Describes the arithmetic expressions with arbitrary nesting of balanced parenthesis {(),} 4. Describes block structure in programming languages 5. Model neural nets	(BTL 2)
17	<b>What are the properties of the CFL generated by CFG?</b> The properties are: 1. Each variable and each terminal of G appears in the derivation of some word in L 2. Here are no productions of the form $A \rightarrow B$ where A and B are variables	(BTL 4)
18	<b>List out the ways to simplify the context free grammar.</b> The three ways of simplifying a context free grammar are: 1. Removing the useless symbols from the set of productions 2. By eliminating the empty productions 3. By eliminating the unit productions	(BTL 2)
19	<b>List out the ways available to formally express PDA.</b> 1. Transition Diagram 2. Transition Table 3. Transition Function	(BTL 2)
20	<b>Analyze the relationship between NPDA and DPDA.</b> The NPDA is the superset of all DPDA. DPDA is the subset of NPDA. So all DPDA are NPDA's	(BTL 4)
21	<b>Can you say the language generated by a CFG in CNF is finite or infinite? If so, how? If not, why?</b>	(BTL 2)

	The language generated by CFG in CNF is finite because any rule in CFG is written in a finite form for CNF. For instance, Non-Terminal → Non-Terminal . Non-Terminal Non-Terminal → terminal. Thus we get any rule in this specific form. Hence language written in CNF is of finite form.
22	<b>What is the height of the parse tree to represent a string of length ‘n’ using Chomsky normal form? (Nov/Dec 2012, May/June 2015)</b> (BTL 3) Let ‘n’ be the length of the string, then the height of derivation tree in CNF is : $2 n -1$
23	<b>What is the height of the parse tree to represent a string of length ‘n’ using Grieback normal form?</b> (BTL 3) Let ‘n’ be the length of the string, then the height of derivation tree in GNF is : n
24	<b>Is the language of DPDA and NPDA are same? (May/June 2016)</b> (BTL 4) No. The language accepted by NPDA is not same as the language accepted by DPDA. Eg: $L=\{wwR \mid w \text{ belongs to } \{a,b\}\}$ is accepted only by NPDA, not DPDA.
25	<b>What is the additional feature of PDA when compared to FSA.</b> (BTL 2) The FSA consists of finite input tape and finite control with limited memory. But in PDA, along with input tape and finite control, it has extra component called Stack. So PDA is powerful than FSA.

**PART-B**

1	<b>(i). Describe the different types of acceptance of a PDA. Are they equivalent in sense of language acceptance? Justify your answer. (7)</b> (Nov/Dec 2009, May/June 2013) (BTL 4)
	Answer: Page No. 6-22 in A.A. Puntambekar book  Key Points: 1. Acceptance by Empty stack (1) 2. Acceptance by final state(1) 3. Proof of equivalence using induction method.(5)
2	<b>(ii). Design a PDA to accept <math>\{0^n 1^n \mid n &gt; 1\}</math> Draw the transition diagram for the PDA. Show by instantaneous description that the PDA accepts the string ‘0011’ (6)</b> (Nov/Dec 2010) (BTL 4) Answer: Page No. 6-6 in A.A. Puntambekar book  Key Points: 1. Diagram using stack.(3) 2. Transition mapping (2) 3. Resultant ID (1)
	<b>(i). Define deterministic PDA’s? Give example for Non –deterministic and Deterministic PDA. (7)</b> (BTL 1)  Answer: Page No. 6-25 in A.A. Puntambekar book.  Key Points: 1. Definition of DPDA and NPDA (2)

	<p>2. Relationship between them. (2) 3. Example language set for NPDA with steps. (3)</p> <p><b>(ii). Construct a PDA accepting <math>\{a^n b^m a^n / m, n \geq 1\}</math> by empty stack. Also construct the corresponding context-free grammar accepting the same set. (6) (May/June 2009) (BTL 3)</b></p> <p>Answer: Page No. 6-19 in A.A. Puntambekar book</p> <p>Key points:</p> <ol style="list-style-type: none"> <li>1. Diagram using stack. (2)</li> <li>2. Transition mapping (3)</li> <li>3. Resultant ID (1)</li> </ol>	
3	<p><b>(i) Define Non Deterministic Push Down Automata. Is it true that DPDA and NDPDA are equivalent in the sense of language acceptance is concern? Justify Your answer. (5) (BTL 3)</b></p> <p>Answer: Page No. 6-22 in A.A. Puntambekar book.</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Theorem statement (2)</li> <li>2. Proof using induction step. (3)</li> </ol> <p><b>(ii) Convert PDA to CFG. PDA is given by</b></p> <p><math>P = \{P, Q, \{0, 1\}, \{X, Y\}, \delta, q_0, Z\}</math>, <math>\delta</math> is defined by <math>\delta(p, 1, z) = \{(p, XZ)\}</math>,  <math>\delta(p, \epsilon, Z) = \{p, \epsilon\}</math>,  <math>\delta(p, 1, X) = \{(p, XX)\}</math>,  <math>\delta(q, 1, X) = \{(q, \epsilon)\}</math>,  <math>\delta(p, 0, X) = \{(q, X0)\}</math>,  <math>\delta(q, 0, Z) = \{(p, Z)\}</math></p> <p style="text-align: center;">(8)                      (May/June 2009)                      (BTL 4)</p>	
	<p>Answer: Page No. 6-42 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Steps for conversion (true symbols and <math>\epsilon</math> symbol) (5)</li> <li>2. ID for a string (2)</li> <li>3. Resultant CFG (1)</li> </ol>	
4	<p><b>What Construct a PDA that recognizes the language <math>\{a^i b^j c^k   i, j, k &gt; 0 \text{ and } i=j \text{ or } i=k\}</math>.</b></p> <p><b>Discuss about PDA acceptance</b></p> <ol style="list-style-type: none"> <li>i) From empty Stack to final state. (6)</li> <li>ii) From Final state to Empty Stack. (7)</li> </ol> <p><b>(Nov /Dec 2018)</b></p> <p>Answer: Page No. 6-15 in A.A. Puntambekar book</p>	<b>(BTL 4)</b>

	<p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagram using stack. (1)</li> <li>2. Transition mapping (8)</li> <li>3. Resultant ID (2)</li> <li>4. Transition diagram for final state and empty store. (2)</li> </ol>
	<p><b>(i). Give PDA to accept the language <math>L = \{a^n b^n   n \geq 1\}</math> by empty stack and by final stack.</b> (7) (Nov/Dec 2012) (BTL 3)</p> <p>Answer: Page No. 6-6 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagram using stack. (1)</li> <li>2. Transition mapping (3)</li> <li>3. Resultant ID (2)</li> <li>4. Transition diagram for final state and empty store (1)</li> </ol> <p><b>(ii) Construct PDA accepting <math>L = \{a^n b^{2n}   n \geq 1\}</math> by empty store.</b> (6) (May/June 2004) (BTL 4)</p> <p>Answer: Page No. 6-11 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagram using stack. (1)</li> <li>2. Transition mapping (4)</li> <li>3. Resultant ID (1)</li> </ol>
<b>PART-C</b>	
1	<p><b>(i) Design a PDA to accept each of the following language <math>\{a^m b^m c^n   m, n \geq 1\}</math></b> (15) (Nov / Dec 2013) (BTL 5)</p> <p>Answer: Page No. 6-19 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagram using stack.(2)</li> <li>2. Transition mapping (11)</li> <li>3. Resultant ID (2)</li> </ol>
2	<p><b>(i) If L is a CFL then prove that there exists PDA M, such that <math>L = N(M)</math>, language accepted by empty stack .</b> (7) (May/June 2006) (BTL 4)</p> <p>Answer: Page No. 6-22 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Theorem statement (2)</li> </ol>

	<p>2. Proof using induction (5)</p> <p><b>(ii) Construct PDA empty store , L= {a<sup>m</sup> b<sup>n</sup> n&lt;m}.</b> (8) (Nov/Dec 2011) (BTL 4)</p> <p>Answer: Page No. 6-15 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagram using stack. (2)</li> <li>2. Transition mapping (3)</li> <li>3. Resultant ID (3)</li> </ol>
3	<p><b>Design PDA that accepts a string of well-formed parenthesis. (15)</b> (BTL 4)</p> <p>Answer: Page No. 6-23 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagram using stack. (2)</li> <li>2. Transition mapping (11)</li> <li>3. Resultant ID (2)</li> </ol>

#### UNIT IV PROPERTIES OF CONTEXT FREE LANGUAGES

**Normal Forms for CFG – Pumping Lemma for CFL – Closure Properties of CFL – Turing Machines – Programming Techniques for TM.**

#### PART-A

1	<p><b>What is CNF?</b> (BTL 1)</p> <p>In formal language theory, a CFG is said to be in Chomsky Normal Form if all of its production rules are of the form:</p> <p style="text-align: center;"><math>A \rightarrow BC</math> or <math>A \rightarrow \alpha</math> or</p> <p style="text-align: center;"><math>S \rightarrow \epsilon</math> where A, B and C are non terminal symbol, <math>\alpha</math> is a terminal symbol, S is the start symbol, <math>\epsilon</math> is the empty string.</p>
2	<p><b>What is multiple tracks Turing machine? (Nov/Dec 2015)</b> (BTL 1)</p> <p>A Turing Machine in which the input tape is divided into multiple tracks where each track is having different inputs is called multiple tracks Turing machine.</p>
3	<p><b>What is a multidimensional Turing machine? (May/June 2008)</b> (BTL 1)</p> <p>The Turing Machine which has the useful finite control consists of a k-dimensional array of cells in all <math>2K</math> directions for some fixed K in a tape cell. Depending on the state and symbol scanned, the device changes state, prints a new symbol and moves its tape head in one of <math>2K</math> directions, along one of the K axes.</p>
4	<p><b>How is context-free grammar simplified?</b> (BTL 2)</p> <p>The steps for simplifying the context free grammar are as follows:</p> <ol style="list-style-type: none"> <li>1. First eliminate useless symbols, where the variable or terminals that do not appear in any derivation of a terminal string from the start symbol</li> <li>2. Next eliminate <math>\epsilon</math>- productions which are of the form <math>A \rightarrow \epsilon</math> for some variable A</li> <li>3. Eliminate unit productions, which are of the form <math>A \rightarrow B</math> for variables A, B</li> <li>4. Finally use any of the normal forms to get the simplified CFG</li> </ol>
5	<p><b>What is useless symbol?</b> (BTL 2)</p>

	A symbol x is useful if there is a derivation $S \Rightarrow^* \alpha x \beta \Rightarrow^* w$ for some $\alpha, \beta, w \in T^*$ or else, it is said to be useless symbol.	
6	<b>Define – Nullable Variable</b> Nullable variable in a CFG $G = (V, T, P, S)$ can be defined as follows: 1. Any variable A for which P contains the production $A \rightarrow A$ , is nullable 2. If P contains the production $A \rightarrow B_1, B_2, \dots, B_n$ and $B_1, B_2, \dots, B_n$ are nullable variables, then A is nullable 3. No other variables in V are nullable	(BTL1)
7	<b>What is a generating symbol?</b> Let $G = (V, T, P, S)$ is generating, if $X \Rightarrow^* w$ for some terminal string w. For example, $A \rightarrow aAB / \epsilon$ and $B \rightarrow b$ Then A is a generating symbol since $A \Rightarrow^* ab$	(BTL1)
8	<b>What is GNF?</b> A CFG is in GNF if the right hand sides of all productions rules start with a terminal symbol, optionally followed by some variables. Context-Free Grammar is in Greibach Normal Form, if all production rules are of the form: $A \rightarrow \alpha A_1 A_2 \dots A_n$ where A is a non-terminal symbol, is a terminal symbol, $A_1 A_2 \dots A_n$ is a sequence of non-terminal symbols not including the start symbol, S is the start symbol, and $\epsilon$ is the empty word.	(BTL 1)
9	<b>What is off-line Turing machine? (May/June 2011)</b> An Off-line Turing Machine is a multitape TM whose input tape is read only. The Turing Machine is not allowed to move the input tape head off the region between left and right end markers.	(BTL 2)
10	<b>What are the closure properties of CFL?</b> 1. CFL are closed under union, concatenation and Kleene closure. 2. CFL are closed under substitution and homomorphism. 3. CFL are not closed under intersection and complementation. 4. Closure properties of CFL's are used to prove that certain languages are not context free.	(BTL 2)
11	<b>What is substitution rule?</b> A production $A \rightarrow x_1 B x_2$ can be eliminated from a grammar if B is replaced by all strings derived by B in one step, provided A and B are variables.	(BTL 2)
12	<b>What is total recursive function?</b> If $f(i_1, i_2, \dots, i_k)$ is defined for all $i_1, \dots, i_k$ then we say f is a total recursive function. They are similar to recursive languages as they are computed by TM that always halts.	(BTL 1)
13	<b>What is partial recursive function?</b> A function $f(i_1, \dots, i_k)$ computed by a Turing machine is called a partial recursive function. They are similar to regular expression languages as they are computed by TM that may or may not halt on a given input.	(BTL 1)
14	<b>Define – Turing Machine (Nov/Dec 2010, May/June 2013, Nov/Dec 2018)</b> A Turing machine is denoted as $M = (Q, \Sigma, \Gamma, \delta, q_0, B, F)$ Q is a finite set of states. $\Sigma$ is set of i/p symbols, not including B. $\Gamma$ is the finite set of tape symbols. $q_0$ in Q is called start state. B in $\Gamma$ is blank symbol. F is the set of final states. $\delta$ is a mapping from $Q \times \Gamma$ to $Q \times \Gamma \times \{L, R\}$ .	(BTL 1)
15	<b>What is a Turning Machine?</b>	(BTL 1)

	A finite state machine with storage is called as Turing Machine. Turing machine is a simple mathematical model of a computer. TM has unlimited and unrestricted memory and is a much more accurate model of a general purpose computer. The Turing machine is a FA with an R/W Head. It has an infinite tape divided into cells, each cell holding one symbol.
16	<b>What are the special features of TM?</b> (BTL 4) In one move, TM depending upon the symbol scanned by the tape head and state of the finite control listed as below: 1. Changes state 2. Prints a symbol on the scanned tape cell 3. Moves the R/w head left or right
17	<b>Differentiate 2-way FA from TM.</b> (BTL 4) Turing machine can change symbols on its tape, whereas the FA cannot change symbols on tape. Also TM has a tape head that moves both left and right side, whereas the FA doesn't have such a tape head.
18	<b>Define – Instantaneous Description of TM (Nov/Dec 2015)</b> (BTL 2) The ID of a Turing Machine M is denoted as $\alpha_1 q \alpha_2$ . Here q is the current state of M s in Q; $\alpha_1 \alpha_2$ is the string in $I^*$ that is the contents of the tape up to the rightmost nonblank symbol or the symbol to the left of the head, whichever is the rightmost.
19	<b>What are the applications of TM?</b> (BTL 4) TM can be used as: 1. Recognizers of languages 2. Computers of functions on non negative integers 3. Generating devices
20	<b>When is a function f said to be Turing computable? (May/June 2011)</b> (BTL 4) A Turing Machine defines a function $y = f(x)$ for strings $x, y \in I^*$ , if $q_0 x \rightarrow^* q_f y$ . A function f is 'Turing Computable' if there exists a Turing Machine that performs a specific function.
21	<b>Is it possible that a turing machine could be considered as computer of functions from integers to integers? If yes, justify your answer.</b> (BTL 4) Yes, turing machines simulate computer of functions from integers to integers. That means it is the device for computing integer valued functions. In this scheme integers were represented in unary as blocks of a single character and machine computed by changing the lengths of blocks or by constructing new blocks on the input tape. Thus, it acts as a computing device.
22	<b>What are the features of universal turing machine?</b> (BTL 1) 1. Universal Turing machine is a kind of turing machine used to compute any computable sequence. 2. Another interesting feature of UTM is that it has an ability to manipulate an unbounded amount of data in finite amount of time.
23	<b>What is meant by multi-tape turing machine. (Nov/Dec 2012)</b> (BTL 2) The multitape turing machine is a type of turing machine in which there are more than one input tapes. Each tape is divided into cells and each cell can hold any symbol of finite tape alphabet.
24	<b>Differentiate multi-tape and multi-track turing machines. (May/june 2009)</b> (BTL 2) A multi-track turing machine is an extension of turing machine having n-tracks. The n symbols are at a time under the read/write head. There is only one read / write head in multi-track turing machine.  The multi tape turing machine is a generalization of multi-track turing machine. It consists of n-tapes with independently mobile read/write head. That means in multi track TM only

	single read/write head is present but in multi tape TM each tape has its own read / write head.
25	<b>Justify the power of NTM and DTM</b> (BTL 2) The power of Non deterministic TM and Deterministic TM are equivalent in nature. Because, all languages accepted by NTM is same as that of DTM.
<b>PART-B</b>	
1	<p><b>(i).State and describe the Halting Problem for Turing machine(6)</b>  <b>(May/June 2008, Nov/Dec 2010, Nov/Dec 2013, May/June 2014, Nov/Dec 2017) (BTL 3)</b></p> <p>Answer: Page No. 8-11 in A.A. Puntambekar book</p> <p>Key Points:</p> <ul style="list-style-type: none"> <li>1. Theorem statement (2)</li> <li>2. Proof using Contradiction (2)</li> <li>3. Diagram for M and M'(2)</li> </ul> <p><b>(ii).Design a Turing Machine to accept the language</b></p> <p><math>L=\{0^n 1^n / n \geq 1\}</math></p> <p><b>Draw the transition diagram (also specify the instantaneous description to trace the string 0011. (7) (May/June 2009, Nov/Dec 2011) (BTL 4)</b></p> <p>Answer: Page No. 7-17 in A.A. Puntambekar book</p> <p>Key Points:</p> <ul style="list-style-type: none"> <li>1. Diagrammatic representation of infinite tape (1)</li> <li>2. Transition mapping (4)</li> <li>3. Instantaneous Description (1)</li> <li>4. Transition Diagram(1)</li> </ul>
2	<p><b>(i). Describe the Chomsky hierarchy of languages (7) (May/June 2015) (BTL 1)</b></p> <p>Answer: Page No. 7-49 in A.A. Puntambekar book</p> <p>Key Points:</p> <ul style="list-style-type: none"> <li>1. Tabular representation of Grammar and Automata (2)</li> <li>2. Venn Diagram representation of 4 types of grammar. (2)</li> <li>3. Description about 4 different types of languages.(3)</li> </ul> <p><b>(ii). Explain the programming techniques for the TM construction. (6) (May/june 2009, Nov/Dec 2016) (BTL 1)</b></p> <p>Answer: Page No. 7-17 in A.A. Puntambekar book</p> <p>Key Points:</p>

	<ol style="list-style-type: none"> <li>1. Storage in finite control (2)</li> <li>2. Multiple tracks (2)</li> <li>3. Checking off Symbols (2)</li> </ol>	
3	<p><b>(i). Discuss a TM to accept the language <math>LE=\{1^n 2^n 3^n \mid n \geq 1\}</math> (6)</b>          (May/June 2008, May/June 2011, Nov/Dec 2018) <span style="float: right;">(BTL 4)</span></p> <p>Answer: Page No. 7-19 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagrammatic representation of infinite tape (1)</li> <li>2. Transition mapping (4)</li> <li>3. Instantaneous Description (1)</li> <li>4. Transition Diagram (1)</li> </ol> <p><b>(ii). Compare FSA, PDA with TM</b> <span style="float: right;">(7) <span style="margin-left: 20px;">(BTL 2)</span></span></p> <p>Answer: Page No. 7-51 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Tabular representation (1)</li> <li>2. Differences in terms of efficiency, language acceptance, inter-compatibility, etc. (4)</li> <li>3. Similarities among them. (2)</li> </ol>	
4	<p><b>(i)Illustrate the Turing machine for computing <math>f(m, n)=m-n</math> ( proper subtraction). (7)</b>          (Nov/Dec 2003, Nov/Dec 2005, May/June 2011, Nov/Dec 2012) <span style="float: right;">(BTL 5)</span></p> <p>Answer: Page No. 7-27 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagrammatic representation of infinite tape (1)</li> <li>2. Transition mapping (4)</li> <li>3. Instantaneous Description (1)</li> <li>4. Transition Diagram (1)</li> </ol> <p><b>(ii)Design a Turing Machine to compute <math>f(m+n)=m+n</math>, <math>\forall m,n \geq 0</math> and simulate their action on the input 0100. (6)</b> <span style="float: right;">(May/June 2009, Nov/Dec 2012) <span style="margin-left: 20px;">(BTL 5)</span></span></p> <p>Answer: Page No. 7-24 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagrammatic representation of infinite tape (1)</li> <li>2. Transition mapping (2)</li> <li>3. Instantaneous Description for 0100 (1)</li> <li>4. Transition Diagram (1)</li> </ol>	

5	<p><b>(i).Explain the TM as computer of integer function with an example. (7) (BTL 3)</b></p> <p>Answer: Page No. 7-26 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagrammatic representation of infinite tape (1)</li> <li>2. Transition mapping (3)</li> <li>3. Instantaneous Description(2)</li> <li>4. Transition Diagram (1)</li> </ol> <p><b>(ii)Design a TM to implement the function <math>f(x)= x+1</math>. (6) (BTL 3)</b></p> <p>Answer: Page No. 7-25 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagrammatic representation of infinite tape (1)</li> <li>2. Transition mapping (3)</li> <li>3. Instantaneous Description (1)</li> <li>4. Transition Diagram(1)</li> </ol>
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**PART- C**

1	<p><b>Define Turing machine for computing <math>f(m, n)=m*n</math> (15) (Nov/Dec 2007, May/June 2011, May/june 2014) (BTL 5)</b></p> <p>Answer: Page No. 7-29 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagrammatic representation of infinite tape (1)</li> <li>2. Transition mapping (12)</li> <li>3. Instantaneous Description (1)</li> <li>4. Transition Diagram (1)</li> </ol>
2	<p><b>Design a TM which reverses the given string {abb} (15) (BTL 4)</b></p> <p>Answer: Page No. 7-39 in A.A. Puntambekar book.</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Diagrammatic representation of infinite tape (1)</li> <li>2. Transition mapping (12)</li> <li>3. Instantaneous Description (1)</li> <li>4. Transition Diagram (1)</li> </ol>
3	<p><b>Construct a TM for a function <math>f(x)= x+3</math> (15) (BTL 5)</b></p>

	<p>Answer: Page No. 7-45 in A.A. Puntambekar book</p> <p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. Diagrammatic representation of infinite tape (1)</li> <li>2. Transition mapping (12)</li> <li>3. Instantaneous Description (1)</li> <li>4. Transition Diagram (1)</li> </ol>
<b>UNIT V UNDECIDABILITY</b>	
<b>Non Recursive Enumerable (RE) Language – Undecidable Problem with RE – Undecidable Problems about TM – Post's Correspondence Problem, The Class P and NP.</b>	
<b>PART - A</b>	
1	<p><b>When is recursively enumerable language said to be recursive? Is it true that the language accepted by non-deterministic Turing machine different from recursively enumerable language?</b> <span style="float: right;">(BTL 4)</span></p> <p>A language L is recursively enumerable if there is a TM that accepts L and recursive if there is a TM that recognizes L. Thus regular expression language is Turing acceptable and recursive language is Turing decidable languages.</p> <p>No, the language accepted by non-deterministic Turing machine is same as recursively enumerable language.</p>
2	<p><b>What is recursively enumerable language?</b> <span style="float: right;">(BTL 1)</span></p> <p>A language is recursively enumerable if there exists a Turing Machine that accepts every string of the language and does not accept strings that are not in the language.</p>
3	<p><b>Define – Decidability (Or) What is decidable problem?</b> <span style="float: right;">(BTL 2)</span></p> <p>A problem is said to be decidable if there exists a Turing machine which gives one 'yes' or 'no' answer for every input in the language.</p>
4	<p><b>Define Problem Solvable in Polynomial Time</b> <span style="float: right;">(BTL 2)</span></p> <p>A Turing Machine M is said to be of time complexity T(n) if whenever m given an input w of length n, m halts after making at most T(n) moves, regardless of whether or not m accepts.</p>
5	<p><b>Define – MPCP or Modified PCP. (Nov/Dec 2015)</b> <span style="float: right;">(BTL 1)</span></p> <p>The MPCP is: Given lists A and B of K strings from <math>\Sigma^*</math>, say A = w<sub>1</sub>, w<sub>2</sub>, ... w<sub>k</sub> and B = x<sub>1</sub>, x<sub>2</sub>, ..., x<sub>k</sub> does there exist a sequence of integers i<sub>1</sub>, i<sub>2</sub>, ..., i<sub>r</sub> such that w<sub>i1</sub>w<sub>i2</sub>...w<sub>ir</sub> = x<sub>i1</sub>x<sub>i2</sub>...x<sub>ir</sub>.</p>
6	<p><b>When a problem is said to be undecidable?</b> <span style="float: right;">(BTL 4)</span></p> <p>If a problem is not a recursive language, then it is said to be undecidable problem.</p>
7	<p><b>When a language is said to be recursive?</b> <span style="float: right;">(BTL 4)</span></p> <p>A language L is said to be recursive if there exists a Turing machine M that accepts L, and goes to halt state or else M rejects L.</p>
8	<p><b>Write examples of recursive languages?</b> <span style="float: right;">(BTL 3)</span></p> <p>The examples of recursive languages are given below:</p> <ol style="list-style-type: none"> <li>1. The language L defined as L = { "M", "w" : M is a DFSM that accepts w} is Recursive</li> <li>2. L defined as {"M1" U "M2" : DFSMs M1 and M2 and L(M1) = L(M2)} is Recursive</li> </ol>
9	<p><b>What is diagonalization language? (Nov/Dec 2014)</b> <span style="float: right;">(BTL 2)</span></p> <p>The language Ld Which consists of all those strings w such that the Turing machine represented by w does not accept the input w.</p>

	$L_d = \{ w_i \mid w_i \in L(M_i) \}$	
10	<b>What are the properties of recursive enumerable sets which are undecidable? (BTL 1)</b> The properties of recursive enumerable sets are: 1. Emptiness 2. Finiteness 3. Regularity 4. Context – freedom	
11	<b>What is Church's hypothesis? (May/June 2006) (BTL 1)</b> The notion of computable function can be identified with the class of partial recursive functions is known as Church-hypothesis or Church-Turing thesis. The Turing machine is equivalent in computing power to the digital computer.	
12	<b>What are the different types of grammar/languages? (BTL 1)</b> The different types of grammar/languages are: 1. Unrestricted or Phrase structure grammar.(Type 0 grammar).(for TMs) 2. Context sensitive grammar or context dependent grammar (Type1)(for Linear Bounded Automata ) 3. Context free grammar (Type 2) (for PDA) 4. Regular grammar (Type 3) (or Finite Automata). This hierarchy is called as Chomsky Hierarchy.	
13	<b>Prove that AMBIGUITY problem is un-decidable. (BTL 1)</b> Consider the ambiguity problem for CFGs. Use the “yes-no” version of AMB. An algorithm for FIND is used to solve AMB. FIND requires producing a word with two or more parses if one exists and answers “no” otherwise. By the reduction of AMB to FIND we conclude there is no algorithm for FIND and hence no algorithm for AMB.	
14	<b>Define – Universal Language (Nov/Dec 2018) (BTL 1)</b> A Universal Turing Machine Mu is an automaton, that given as input the description of any Turing Machine M and a string w, can simulate the computation of M on w.	
15	<b>Define – Rice Theorem (May/June 2009) (BTL 1)</b> The Rice theorem states that “Every nontrivial property of RE languages is undecidable.”	
16	<b>List out the various representation of TM. (BTL 2)</b> We can describe TM using: 1. Instantaneous description 2. Transition table 3. Transition diagram	
17	<b>List out the techniques for Turing machine construction. (Nov/Dec 2011) (BTL 2)</b> The various techniques used for Turing Machine construction are as follows: 1. Storage in finite control 2. Multiple tracks 3. Checking off symbols 4. Shifting over 5. Subroutines	
18	<b>What are UTM's or Universal Turing machines? (May/June 2015) (BTL 2)</b> Universal TMs are TMs that can be programmed to solve any problem that can be solved by any Turing machine. A specific Universal Turing machine U is Input to U: The encoding “M “of a Tm M and encoding “w” of a string w. Behavior: U halts on input “M” “w” if and only if M halts on input w.	
19	<b>What is the crucial assumption for encoding a TM? (BTL 2)</b>	

	The crucial assumption is that there are no transitions from any of the halt states of any given TM. Apart from the halt state, a given TM is total.
<b>20</b>	<b>State the halting problem of Turing Machine. (May/june 2011) (BTL 1)</b> The halting problem for TMs is: Given any Turing Machine M and an input string w, does M halt on w? This problem is undecidable as there is no algorithm to solve this problem.
<b>21</b>	<b>Define class P problem. (BTL 1)</b> The class of languages accepted by Deterministic Turing machine in polynomial time is called class P problems.
<b>22</b>	<b>Define class NP problem (BTL 1)</b> The class of languages accepted by Non-Deterministic Turing machine in polynomial time is called class NP problems.
<b>23</b>	<b>What do you mean by NP hard? (BTL 1)</b> A problem 'A' is said to be NP-hard if it satisfies the following condition. (i). The problem 'A' in NP should be converted to another problem 'B'. (ii).This conversion should happen in polynomial time.
<b>24</b>	<b>What do you mean by NP-Completeness? (Nov/Dec 2012) (BTL 1)</b> A problem which is both NP as well as NP-hard is said to be class of NP-Completeness problem.
<b>25</b>	<b>Give any 4 examples of NP completeness problem. (Nov/Dec 2014) (BTL 1)</b> 1. Hamiltonian cycle problem 2. 3-SAT problem 3. Longest path problem 4. Clique problem

**PART - B**

<b>1</b>	<b>(i). Describe about the tractable and intractable problems.(7) (BTL 2)</b>  Answer: Page No. 8-39 in A.A. Puntambekar book  Key Points: 1. Class P (1) 2. Class NP (2) 3. Class NP-hard (2) 4. Class NP-Complete(2)  <b>(ii). Explain PCP with an example.(6) (Nov/Dec 2007, May/June 2009, Nov/Dec 2015, Nov/Dec 2016) (BTL 1)</b>  Answer: Page No. 8-15 in A.A. Puntambekar book  Key Points: 1. Definition (2) 2. Tabular representation of two lists (3) 3. Solution for lists (1)
<b>2</b>	<b>(i)Describe about Recursive and Recursive Enumerable languages with example.(7) (BTL 1)</b>  Answer: Page No. 8-29 in A.A. Puntambekar book Key Points:

	<p>1. Definition of Recursive and RE set (2)      2. Diagrammatic explanation (3)      3. Differences between them (2)</p> <p><b>(ii) State and explain RICE theorem.(6) (May/June 2010) (BTL 1)</b></p> <p>Answer: Page No. 8-14 in A.A. Puntambekar book</p> <p>Key Points:      1. Theorem statement (2)      2. Proof with diagram (4)</p>															
3	<p><b>(i) Summarize diagonalization language.(6) (BTL 2)</b></p> <p>Answer: Page No. 8-4 in A.A. Puntambekar book</p> <p>Key Points:      1. Introduction to <math>L_d</math> (2)      2. Properties of <math>L_d</math> (3)      3. Diagram representation of string of TM (1)</p> <p><b>(ii) Show that the language <math>L_d</math> is not recursive enumerable language. (May/June 2006, May/June 2009) (BTL 4) (7)</b></p> <p>Answer: Page No. 8-5 in A.A. Puntambekar book</p> <p>Key Points:      1. Theorem statement (2)      2. Proof with diagram (5)</p>															
4	<p><b>Discuss post correspondence problem .Let <math>\Sigma=\{0,1\}</math>.Let A and B be the lists of three strings each ,defined as</b></p> <table border="1" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th></th> <th>List A</th> <th>List B</th> </tr> </thead> <tbody> <tr> <td><b>I</b></td> <td><b><math>W_i</math></b></td> <td><b><math>X_i</math></b></td> </tr> <tr> <td><b>1</b></td> <td><b>1</b></td> <td><b>11</b></td> </tr> <tr> <td><b>2</b></td> <td><b>10111</b></td> <td><b>10</b></td> </tr> <tr> <td><b>3</b></td> <td><b>10</b></td> <td><b>0</b></td> </tr> </tbody> </table> <p><b>(i). Does the PCP have a solution?(7) (May/ June 2007) (BTL 5)</b></p> <p>Answer: Page No. 8-37 in A.A. Puntambekar book</p> <p>Key Points:      1. Derivation steps (5)      2. Solution with list of integers. (2)</p> <p><b>(ii) Prove that the universal language is recursively enumerable.(6) (BTL 4)</b></p> <p>Answer: Page No. 8-10 in A.A. Puntambekar book</p> <p>Key Points:      1. Theorem statement      2. Proof with diagram</p>		List A	List B	<b>I</b>	<b><math>W_i</math></b>	<b><math>X_i</math></b>	<b>1</b>	<b>1</b>	<b>11</b>	<b>2</b>	<b>10111</b>	<b>10</b>	<b>3</b>	<b>10</b>	<b>0</b>
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<b>1</b>	<b>1</b>	<b>11</b>														
<b>2</b>	<b>10111</b>	<b>10</b>														
<b>3</b>	<b>10</b>	<b>0</b>														

5	<p><b>Show that the language L and its complement L' are both recursively enumerable then L is recursive.</b></p> <p>(Nov/Dec 2003, May/june 2005, May/june 2010)</p> <p>Answer: Page No. 8-8 in A.A. Puntambekar book</p> <p>Key Points:</p> <ol style="list-style-type: none"> <li>1. Theorem statement (2)</li> <li>2. Proof with diagram (13)</li> </ol>	<p>(13) (BTL 4)</p>
<b>PART-C</b>		
1.	<p><b>Write short notes on PCP and find the instances for the following lists x and y.</b></p> <p><math>x=(b, bab^3, ba)</math> and <math>y=(b^3, ba, a)</math> (15) (May/June 2007)</p>	<p>(BTL 5)</p>
Answer: Page No. 8-17 in A.A. Puntambekar book		
2.	<p><b>(i) Explain in detail Polynomial Time reduction and NPcompleteness. (8)</b></p> <p>(Nov/ Dec 2018)</p>	<p>(BTL 2)</p>
Answer: Page No. 8-17 in A.A. Puntambekar book		
3.	<p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. Description about tractable and intractable problems. (4)</li> <li>2. NP problems (20)</li> <li>3. NP hard an NP Completeness (2)</li> </ol> <p><b>(ii) Write short notes on NP-Hard Problems.(7)</b></p>	<p>(BTL 1)</p>
Answer: Page No. 8-18 in A.A. Puntambekar book		
3.	<p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. Description about tractable and intractable problems. (3)</li> <li>2. NP problems (2)</li> <li>3. NP hard (2)</li> </ol> <p><b>Find the languages obtained from the following operations: (15)</b></p> <p><b>(i). Union of two recursive languages</b></p> <p><b>(ii). Union of two two recursively enumerable languages.</b></p> <p><b>(iii). L if L and complement of L are recursively enumerable.</b></p> <p>(Nov/Dec 2008, May/June 2012, Nov/Dec 2014)</p>	<p>(BTL 4)</p>
Answer: Page No. 8-37 to 8-38 in A.A. Puntambekar book		
3.	<p><b>Key Points:</b></p> <ol style="list-style-type: none"> <li>1. Theorem statement (2)</li> </ol>	

- |  |   |
|--|---|
|  | 2. Proof deduction with suitable diagrams. (13) |
|--|---|

## Objective Questions

### CS6503- Theory of Computation

**1: Correct hierarchical relationship among context-free, right-linear, and context-sensitive language is**

- A. context-free  $\subset$  right-linear  $\subset$  context-sensitive
- B. context-free  $\subset$  context-sensitive  $\subset$  right-linear
- C. context-sensitive  $\subset$  right-linear  $\subset$  context-free
- D. right-linear  $\subset$  context-free  $\subset$  context-sensitive

Answer D

**2: In the following grammar :**

$x ::= x \oplus y \mid 4$

$y ::= z^* y \mid 2$

$z ::= id$

which of the following is true ?

- A.  $\oplus$  is left associative while  $*$  is right associative
- B. Both  $\oplus$  and  $*$  are left associative
- C.  $\oplus$  is right associative while  $*$  is left associative
- D. None of these

Answer A

**3. Which of the following CFG's can't be simulated by an FSM ?**

- A.  $S \rightarrow Sa \mid b$
- B.  $S \rightarrow aSb \mid ab$
- C.  $S \rightarrow abX, X \rightarrow cY, Y \rightarrow d \mid aX$
- D. None of these

Answer B

**4: ADG is said to be in Chomsky Form (CNF), if all the productions are of the form A --> BC or A --> a. Let G be a CFG in CNF. To**

**derive a string of terminals of length x , the number of productions to be used is**

- A.  $2x - 1$
- B.  $2x$
- C.  $2x + 1$
- D. None of these

Answer A

**5: Which of the following statements is correct?**

- A.  $A = \{ \text{ If } a^n b^n \mid n = 0, 1, 2, 3 \dots \}$  is regular language
- B. Set B of all strings of equal number of a's and b's defines a regular language
- C.  $L(A^* B^*) \cap B$  gives the set A
- D. None of these

Answer C

**6: P, Q, R are three languages, if P and R are regular and if  $PQ = R$ , then**

- A. Q has to be regular
- B. Q cannot be regular
- C. Q need not be regular
- D. Q cannot be a CFL

Answer C

**7: A class of language that is closed under**

- A. union and complementation has to be closed under intersection
- B. intersection and complement has to be closed under union
- C. union and intersection has to be closed under complementation

- D. both (A) and (B)

Answer D

**8: The productions**

- E --> E+E
- E --> E-E
- E --> E\*E
- E --> E / E
- E --> id

- A. generate an inherently ambiguous language
- B. generate an ambiguous language but not inherently so
- C. are unambiguous
- can generate all possible fixed length valid computation for carrying out addition, subtraction, multiplication and division, which can be expressed in one expression

Answer B

**9: Which of the following definitions below generates the same language as L, where**

$$L = \{x^n y^n \text{ such that } n \geq 1\} ?$$

- I. E --> xEy | xy
- II. xy | (x+x y y+)
- III .x+y+
- A. I only
- B. I and II
- C. II and III
- D. II only

Answer A

**10: Following context free grammar**

- S --> aB | bA
- A --> b | aS | bAA
- B --> b | bS | aBB

**generates strings of terminals that have**

- A. equal number of a's and b's
- B. odd number of a's and odd number b's
- C. even number of a's and even number of b's
- D. odd number of a's and even number of a's

**11: Define for the context free language**  
 $L = \{0;1\}$  init ( $L$ ) = {  $u | u v \in L$  for some  $v$  in  $\{0, 1\}$ }

If  $L = \{w | w$  is nonempty and has an equal number of 0's and 1's}, then init ( $L$ ) is set of all binary strings

- A. with unequal numbers of 0's and 1's.
- B. including the null string.
- C. Both (a) and (b)
- D. None of these

Answer: B

**12: Which of the following CFG's can't be simulated by an FSM ?**

- A.  $s \rightarrow sa | a$
- B.  $s \rightarrow abX, X \rightarrow cY, Y \rightarrow a | axY$
- C.  $s \rightarrow a sb | ab$
- D. none of these

Answer: C

**13: Basic limitation of FSM is that it**

- A. cannot remember arbitrary large amount of information
- B. sometimes fails to recognize grammars that are regular
- C. sometimes recognizes grammars are not regular
- D. None of these

Answer: A

**14: Which of the following is not possible algorithmically ?**

- A. Regular grammar to context free grammar
- B. Non-deterministic FSA to deterministic FSA
- C. Non-deterministic PDA to deterministic PDA
- D. None of these

Answer: C

**15: The set  $\{anbn | n = 1, 2, 3 \dots\}$  can be generated by the CFG**

- A.  $S \rightarrow ab | aSb$
- B.  $S \rightarrow aaSbb + abS$
- C.  $S \rightarrow ab | aSb | E$
- D.  $S \rightarrow aaSbb | ab | aabb$

Answer: D

**16: The CFG  
 $s \rightarrow as | bs | a | b$   
is equivalent to regular expression**

- A.  $(a + b)$
- B.  $(a + b)(a + b)^*$
- C.  $(a + b)(a + b)$
- D. None of these

Answer B

**17: Consider the grammar :**

**$S \rightarrow ABCc | Abc$**

**$BA \rightarrow AB$**

**$Bb \rightarrow bb$**

**$Ab \rightarrow ab$**

**$Aa \rightarrow aa$**

**Which of the following sentences can be derived by this grammar?**

- A. abc
- B. aab
- C. abcc
- D. abbb

Answer A

**18: Pumping lemma is generally used for proving that**

- A. given grammar is regular
- B. given grammar is not regular
- C. whether two given regular expressions are equivalent or not
- D. None of these

**19: The language of all words with at least 2 a's can be described by the regular expression**

- A.  $(ab)^*a$  and  $a(ba)^*$
- B.  $(a+b)^* ab^* a (a+b)^*$
- C.  $b^* ab^* a (a+b)^*$
- D. all of these

Answer D

**20: Any string of terminals that can be generated by the following CFG is**

$$\begin{aligned} S &\rightarrow XY \\ X &\rightarrow aX \mid bX \mid a \\ Y &\rightarrow Ya \mid Yb \mid a \end{aligned}$$

- A. has atleast one 'b'
- B. should end in a 'a'
- C. has no consecutive a's or b's
- D. has atleast two a's

Answer D

**21:  $L = (an bn an \mid n = 1,2,3)$  is an example of a language that is**

- A. context free
- B. not context free
- C. not context free but whose complement is CF
- D. both (b) and (c)

Answer: D

**22: If  $\Sigma = \{0, 1\}$ ,  $L = \Sigma^*$  and  $R = (0^n 1^n \text{ such that } n > 0)$**

**then languages  $L \cup R$  and  $R$  respectively are**

- A. Regular, Regular
- B. Regular, Not regular
- C. Not regular, Not regular
- D. None of these

Answer: B

**23: FSM can recognize**

- A. any grammar
- B. only CG
- C. Both (a) and (b)
- D. only regular grammar

Answer: D

**24: Set of regular languages over a given alphabet set is not closed under**

- A. union
- B. complementation
- C. intersection
- D. All of these

Answer: B

**25: Which of the following statement is correct?**

- A. All languages can not be generated by CFG
- B. Any regular language has an equivalent CFG
- C. Some non regular languages can't be generated by CFG
- D. both (b) and (c)

Answer: D

**26: Given  $A = \{0,1\}$  and  $L = A^*$ . If  $R = (0^n 1^n, n > 0)$ , then language  $L \cup R$  and  $R$  are respectively**

- A. regular, regular
- B. not regular, regular
- C. regular, not regular
- D. context free, not regular

Answer D

**27: Define for a context free language**

$L \leq \{0 ; 1\}$  init (L) = {u|uv  $\in L$  for some v in {0,1}}

(in other words, init (L) is the set of prefixes of L)

**Let L {w/w is nonempty and has an equal**

**REGULATION: 2017**  
**number of 0's and 1's)**

**Then init (L) is**

- A. set of all binary strings with unequal number of 0's and 1's
- B. set of all binary strings including the null string
- C. set of all binary strings with exactly one more 0's than the number of 1's or 1 more than the number of 0's
- D. none of these

Answer B

**28: If L1 and L2 are context free language and R a regular set, then which one of the languages below is not necessarily a context free language?**

- A. L1 L2
- B. L1  $\cap$  L2
- C. L1  $\cap$  R
- D. L1  $\cup$  L2

Answer B

**29: Consider a grammar with the following productions**

$$\begin{aligned}S &\rightarrow aab \mid bac \mid aB \\S &\rightarrow a S \mid b \\S &\rightarrow a b b \mid ab \\Sa &\rightarrow bdb \mid b\end{aligned}$$

**The above grammar is**

- A. Context free
- B. regular
- C. context sensitive
- D. LR ( k )

Answer C

**30: What can be said about a regular language L over {a} whose minimal finite state automation has two states?**

**ACADEMIC YEAR: 2019-2020**

- A. L must be { an | n is odd }
- B. L must be { an | n is even }
- C. L must be { an | n > 0 }
- D. Either L must be { an | n is odd }, or L must be { an | n is even }

Answer B

**31: In a context-sensitive grammar, number of grammar symbols on the left hand side of a production can't be greater than the number of**

- A. grammar symbols on the right hand side
- B. terminals on the right hand side
- C. non-terminals on the right hand side
- D. all of these

Answer C

**32: In a context-free grammar**

- A.  $\epsilon$  can't be the right hand side of any production
- B. terminal symbols can't be present in the left hand side of any production
- C. number of grammar symbols in the left hand side is not greater than the number of grammar symbols in the right hand side
- D. all of these

Answer D

**33: CFG can be recognized by a**

- A. push-down automata
- B. 2-way linear bounded automata
- C. both (a) and (b)
- D. none of these

Answer C

**34: Which of the following statements are true?**

- I. The set of all odd integers is a monoid under multiplication.

**REGULATION: 2017**

- II. The set of all complex number is a group under multiplication**
- III. The set of all integers under the operation \* given by  $a * b = a+b-ab$  is a monoid**
- IV.  $Z_s$  under symmetric difference  $\bar{Z}$  defined by  $A \bar{Z} B = (A-B) \cup (B-A)$  is an abelian group**
- A. I and II  
B. I, III and IV  
C. I, II and III  
D. I, II and IV

Answer B

**35: A given grammar is called ambiguous if**

- A. two or more productions have the same non-terminal on the left hand side  
B. a derivation tree has more than one associated sentence  
C. there is a sentence with more than one derivation tree corresponding to it  
D. brackets are not present in the grammar

Answer C

**36: Let L be a language recognizable by a finite automaton. The language**

$REVERSE(L) = \{ w \text{ such that } w \text{ is the reverse of } v \text{ where } v \in L \}$  is a

- A. regular language  
B. context-free language  
C. context-sensitive language  
D. recursively enumerable language

Answer A

**37: The grammars  $G = (\{s\}, \{0, 1\}, p, s)$  where  $p = (s \rightarrow 0S1, S \rightarrow 0S, S \rightarrow S1, S \rightarrow 0)$  is a**

- A. recursively enumerable language  
B. regular language  
C. context-sensitive language

**ACADEMIC YEAR: 2019-2020**

- D. context-free language

Answer B

**38: The logic of pumping lemma is a good example of**

- A. pigeon-hole principle  
B. divide-and-conquer technique  
C. recursion  
D. iteration

Answer A

**39: The intersection of CFL and regular language**

- A. is always regular  
B. is always context free  
C. both (a) and (b)  
D. need not be regular

Answer B

**40: For two regular languages**

$L1 = (a + b)^* a$  and  $L2 = b (a + b)^*$   
**the intersection of  $L1$  and  $L2$  is given by**

- A.  $(a + b)^* ab$   
B.  $ab (a + b)^*$   
C.  $a (a + b)^* b$   
D.  $b (a + b)^* a$

Answer D

**41: Context free grammar is not closed under**

- A. product  
B. union  
C. complementation  
D. kleen star

Answer C

**42: If L be a language recognizable by a finite automaton, then language front**

$\{L\} = \{ w \text{ such that } w \text{ is prefix of } v \text{ where } v \in L \}$ , is a

- A. regular language
- B. context-free language
- C. context-sensitive language
- D. recursive enumeration language

Answer A

**43: For which of the following application, regular expressions can not be used ?**

- A. Designing computers
- B. Designing compilers
- C. Both (a) and (b)
- D. Developing computers

Answer C

**44: Consider the following grammar**

$$\begin{aligned} S &\rightarrow Ax / By \\ A &\rightarrow By/Cw \\ B &\rightarrow x / Bw \\ C &\rightarrow y \end{aligned}$$

**Which of the regular expressions describe the same set of strings as the grammar ?**

- A.  $xw^*y + xw^*yx + ywx$
- B.  $xwy + xw^*xy + ywx$
- C.  $xw^*y + xw x yx + ywx$
- D.  $xw xy + xww^*y + ywx$

Answer A

**45: Which of the following statements is (are) correct ?**

- A. Recursive languages are closed under complementation.
- B. If a language and its complement are both regular, the language is recursive
- C. Set of recursively enumerable language is closed under union
- D. All of these

Answer D

**46: Which of the following statement is wrong ?**

- A. Any regular language has an equivalent context-free grammar.
- B. Some non-regular languages can't be generated by any context-free grammar
- C. Intersection of context free language and a regular language is always context-free
- D. All languages can be generated by context-free grammar

Answer D

**47: Consider a grammar :**

$G = (\{x, y\}, \{s, x, y\}, p, s)$   
where elements of parse :

$$\begin{aligned} S &\rightarrow x y, S \rightarrow y x, x \rightarrow x z, x \rightarrow x, \\ y &\rightarrow y, z \rightarrow z \end{aligned}$$

**The language L generated by G most accurately is called**

- A. Chomsky type 0
- B. Chomsky type 1
- C. Chomsky type 2
- D. Chomsky type 3

Answer D

**48: Consider a grammar :**

$G = (\{S\}, \{0, 1\}, p, s)$   
where elements of p are:  
 $S \rightarrow SS, S \rightarrow 0S1, S \rightarrow 1S0, S \rightarrow \text{empty}$

**The grammar will generate**

- A. regular language
- B. context-free language
- C. context-sensitive language
- D. recursive enumerable language

Answer A

**REGULATION: 2017**

**49: A grammar that produces more than one parse tree for some sentence is called**

- A. ambiguous**
- B. unambiguous**
- C. regular**
- D. none of these**

Answer A

**50: Given a grammar G a production of G with a dot at some position of the right side is called**

**ACADEMIC YEAR: 2019-2020**

- A. LR (0) item of G**
- B. LR (1) item of G**
- C. both (a) and (b)**
- D. none of these**

Answer A

<b>CS8592</b>	<b>OBJECT ORIENTED ANALYSIS AND DESIGN</b>	<b>L T P C</b>
		<b>3 0 0 3</b>

**OBJECTIVES:**

- To understand the fundamentals of object modeling
- To understand and differentiate Unified Process from other approaches.
- To design with static UML diagrams.
- To design with the UML dynamic and implementation diagrams.
- To improve the software design with design patterns.
- To test the software against its requirements specification

**UNIT I UNIFIED PROCESS AND USE CASE DIAGRAMS****9**

Introduction to OOAD with OO Basics – Unified Process – UML diagrams – Use Case –Case study – the Next Gen POS system, Inception -Use case Modelling – Relating Use cases – include, extend and generalization – When to use Use-cases

**UNIT II STATIC UML DIAGRAMS****9**

Class Diagram— Elaboration – Domain Model – Finding conceptual classes and description classes – Associations – Attributes – Domain model refinement – Finding conceptual class Hierarchies – Aggregation and Composition – Relationship between sequence diagrams and use cases – When to use Class Diagrams

**UNIT III DYNAMIC AND IMPLEMENTATION UML DIAGRAMS****9**

Dynamic Diagrams – UML interaction diagrams – System sequence diagram – Collaboration diagram – When to use Communication Diagrams – State machine diagram and Modelling –When to use State Diagrams – Activity diagram – When to use activity diagrams Implementation Diagrams – UML package diagram – When to use package diagrams – Component and Deployment Diagrams – When to use Component and Deployment diagrams

**UNIT IV DESIGN PATTERNS****9**

GRASP: Designing objects with responsibilities – Creator – Information expert – Low Coupling – High Cohesion – Controller Design Patterns – creational – factory method – structural – Bridge – Adapter – behavioural – Strategy – observer –Applying GoF design patterns – Mapping design to code

**UNIT V TESTING****9**

Object Oriented Methodologies – Software Quality Assurance – Impact of object orientation on Testing – Develop Test Cases and Test Plans

**TOTAL: 45 PERIODS****OUTCOMES:**

At the end of the course, the students will be able to:

- Express software design with UML diagrams
- Design software applications using OO concepts.
- Identify various scenarios based on software requirements
- Transform UML based software design into pattern based design using design patterns
- Understand the various testing methodologies for OO software

**TEXT BOOKS:**

1.Craig Larman, —Applying UML and Patterns: An Introduction to Object-Oriented Analysis and Design and Iterative Development, Third Edition, Pearson Education, 2005.

2.Ali Bahrami – Object Oriented Systems Development – McGraw Hill International Edition – 1999

**Subject Code : CS8592****Subject Name:** Object Oriented Analysis and Design**Year/Sem :III/05****Subject Handler:** Ms.Revathy

<b>UNIT -1- UNIFIED PROCESS AND USE CASE DIAGRAMS</b>	
<b>PART A</b>	
<b>Q.No</b>	<b>QUESTIONS</b>
1.	<p><b>What is Object Oriented analysis &amp; Design? (April/May 2017) BTL1</b></p> <p><b>Object-oriented analysis and design (OOAD)</b> is a popular technical approach for analyzing and designing an application, system, or business by applying object-oriented programming, as well as using visual modeling throughout the development life cycles</p>
2.	<p><b>List the 4 phases in UP. BTL1</b></p> <p>The Unified Process is an iterative and incremental development process. The four phases are</p> <ul style="list-style-type: none"> <li>• Inception</li> <li>• Elaboration</li> <li>• Construction</li> <li>• Transition</li> </ul>
3.	<p><b>Compose your views on iterative Development and write it benefits. BTL6</b></p> <p>Iterative development is a way of breaking down the software development of a large application into smaller chunks. In iterative development, feature code is designed, developed and tested in repeated cycles</p> <ul style="list-style-type: none"> <li>• Risks are mitigated earlier, because elements are integrated progressively.</li> <li>• Changing requirements and tactics are accommodated.</li> <li>• Improving and refining the product is facilitated, resulting in a more robust product.</li> <li>• Organizations can learn from this approach and improve their process.</li> </ul>
4.	<p><b>Define UML. BTL1</b></p> <p><b>Unified Modeling language (UML)</b> is a standardized modeling language enabling developers to specify, visualize, construct and document artifacts of a software system</p>
5.	<p><b>What is a POS system? List the components of POS system. BTL1</b></p> <p>A POS system is a computerized application used (in part) to record sales and handle payments; it is typically used in a retail store</p> <p>It includes hardware components such as a computer and bar code scanner, and software to run the system</p>
6.	<p><b>Define Use Case. Point out what test can help find useful use cases? (April/May 2017) BTL4</b></p> <ul style="list-style-type: none"> <li>• A use case is a list of actions or event steps typically defining the interactions between a role and a system to achieve a goal. The actor can be a human or other external system</li> <li>• It is used widely in developing tests at system or acceptance level</li> </ul>
7.	<p><b>Illustrate the relationship used in Use case. BTL3</b></p> <p>There can be 5 relationship types in a use case diagram.</p>

	<ul style="list-style-type: none"> <li>• Association between actor and use case</li> <li>• Generalization of an actor</li> <li>• Extend between two use cases</li> <li>• Include between two use cases</li> <li>• Generalization of a use case</li> </ul>
8.	<p><b>List out the advantages of Use case Modeling. BTL1</b></p> <ul style="list-style-type: none"> <li>• The use case diagram provides a comprehensive summary of the whole software system</li> <li>• feedback can be obtained at a very early stage of the development from the customers and the end users.</li> <li>• it requires the identification of exceptional scenarios for the use cases.</li> <li>• The use case model can be utilized in several other aspect of software development</li> </ul>
9.	<p><b>Classify the 3 kinds of actors in use case. BTL4</b></p> <ul style="list-style-type: none"> <li>• Actors can be:</li> <ol style="list-style-type: none"> <li>1. Human</li> <li>2. Systems/Software</li> <li>3.Hardware</li> <li>4.Timer/Clock</li> </ol> </ul>
10.	<p><b>Show the important deals in Inception of the POS system? Mention the requirements of Inception phase BTL3</b></p> <p>The POS system.</p> <ul style="list-style-type: none"> <li>• Project scope, project vision, and the business case</li> <li>• Reach stakeholder agreement on the project vision and business case</li> </ul>
11.	<p><b>Interpret the meaning of Generalization and specialization. BTL2</b></p> <p><b>Generalization</b> is the process of extracting shared characteristics from two or more classes, and combining them into a generalized superclass</p> <p><b>Specialization</b> means creating new subclasses from an existing class.</p>

12.	<p><b>Difference between Include and Extend use case relationships. (April/May 2017) BTL4</b></p> <p><b>Extend</b> is used when a use case conditionally adds steps to another first class use case</p> <p><b>Include</b> is used to extract use case fragments that are duplicated in multiple use cases</p>
13.	<p><b>Distinguish between method and message in object. (Nov/Dec 2015) BTL2</b></p> <p><b>The core difference between a method call and a message is this:</b></p> <ul style="list-style-type: none"> <li>• a method call only happens in your code: in ASM it's translated by a PUSH of the passed arguments.</li> <li>• a kernel message is mostly something sent to the kernel which is tracked and send back to a certain processes</li> </ul>
16.	<p><b>Discuss the Strength and Weakness of the Use case Diagram. BTL2</b></p> <p><b>Advantages:</b></p> <ul style="list-style-type: none"> <li>• Use case modeling is that it requires the identification of exceptional scenarios for the use cases</li> <li>• The use case model can be utilized in several other aspect of software development as well, e.g. Cost Estimation, Project Planning, Test Case Preparation and User Documentation</li> </ul> <p><b>Disadvantages:</b></p> <ul style="list-style-type: none"> <li>• They do not capture the non-functional requirements easily.</li> <li>• There might be a learning curve for the developer and/or specially, the client in using these use cases.</li> </ul>
17.	<p><b>Interpret the meaning of event, state. BTL2</b></p> <p><b>Event:</b> It is the occurrence that is relevant to an object or application.</p> <p><b>State:</b> state of an object is determined by the value of some of its attributes and the presence or absences of links with other objects.</p> <p><b>Transition:</b> It is the movement from one state to another, triggered by an event.</p>
21	<p><b>What is object oriented system development methodology? BTL1</b></p> <p>Object oriented system development methodology is a way to develop software by building self contained modules or objects that can be easily replaced, modified and reused.</p>
22	<p><b>What is iterative evolutionary development? BTL1</b></p> <ul style="list-style-type: none"> <li>• The iterative lifecycle is based on the successive enlargement and refinement of a system through multiple iterations, with cyclic feedback and adaptation as core drivers to converge upon a suitable system.</li> <li>• The system grows incrementally over time, iteration by iteration and thus this approach is also known as iterative and incremental development.</li> </ul>
23	<p><b>Define use case generalization? BTL1</b></p> <p>Use case generalization is used when you have one or more use cases that are rally specializations of more general case.</p>
24	<p><b>Explain object? (Nov/Dec 2018) BTL1</b></p> <p>An object is a combination of data and logic; the representation of some real-world entity.</p>
25	<p><b>Describe the Primary goals in the Design of UML. (Nov/Dec 2016) BTL2</b></p> <p>It provide users with a ready-to-use, expressive visual modeling language so they can develop and exchange meaningful models. It provide extensibility and specialization mechanisms to extend the core concepts.</p>

26	<p><b>Discuss the main advantages of object oriented development? BTL2</b></p> <ul style="list-style-type: none"> <li>• High level of abstraction</li> <li>• Seamless transition among different phases of software development</li> <li>• Encouragement of good programming techniques</li> <li>• Promotion of reusability</li> </ul>
<b>PART B</b>	
1	<p><b>i) Explain in detail about the Unified process in object oriented Analysis and Design? Explain the phases with neat diagrams. (7m) (April/May 2017, May/June 2016, April/May 2011) BTL4</b></p> <p><b>Answer:</b> pg.no:18 in Craig Larman book</p> <p><b>Definition(2m)</b></p> <p>The Unified Process is an iterative and incremental development process</p> <p><b>Diagram(1m)</b></p> <p><b>Explanation(4m)</b></p> <ul style="list-style-type: none"> <li>• Iterative Development</li> <li>• UP Practices and Concepts</li> <li>• The UP Phases and Schedule</li> <li>• The UP Disciplines (was Workflows)</li> <li>• The Agile UP</li> <li>• The Sequential "Waterfall"</li> </ul> <p><b>ii) What is UML activity Diagram? Using an example explain the features of basic UML activity diagram notation. (April/May 2017, May/June 2016) BTL4 (6m)</b></p> <p><b>Answer:</b> pg.no:477-478 in Craig Larman book</p> <p><b>Definition(2m)</b></p> <ul style="list-style-type: none"> <li>• A UML activity diagram shows sequential and parallel activities in a process.</li> </ul> <p><b>Diagram(1m)</b></p> <p><b>Explanation(3m)</b></p> <ul style="list-style-type: none"> <li>• A UML activity diagram shows sequential and parallel activities in a process.</li> <li>• They are useful for modeling business processes, workflows, data flows, and complex algorithms.</li> <li>• Basic UML activity diagram notation illustrates an action, partition, fork, join, and object node.</li> </ul>
2	<p><b>Write a problem statement for Library Management System. Design the UML Use Case diagram, Activity diagram, Class diagram, Sequence diagram, State chart diagram, Package diagram, and Component and Deployment diagram. (13m) (May/June 2016) BTL6</b></p> <p><b>Answer:</b> pg.no:7, Refer notes</p> <p><b>Explanation(8m)</b></p> <p><b>Diagram(5m)</b></p> <p><b>End-Users:</b></p> <ul style="list-style-type: none"> <li>• Librarian: To maintain and update the records and also to cater the needs of the users. Reader: Need books to read and also places various requests to the librarian.</li> <li>• Vendor: To provide and meet the requirement of the prescribed books.</li> </ul>
3	<p><b>Define use case Diagram? Model a use case diagram for a Banking System. Explain the business rules you are considering. b) Consider the following use Cases that play a role in the Banking System you have modeled: 1. Deposit 2. Withdraw Model sequence diagrams for the above two use cases. (13m) (Nov/Dec 2018) BTL1</b></p> <p><b>Answer:</b> pg.no:61-63 in Craig Larman book</p>

	<p><b>Definition (2m)</b></p> <ul style="list-style-type: none"> <li>A use case diagram is an excellent picture of the system context; it makes a good context diagram that is, showing the boundary of a system, what lies outside of it, and how it gets used.</li> </ul> <p><b>Explanation(8m)</b></p> <ul style="list-style-type: none"> <li>It serves as a communication tool that summarizes the behavior of a system and its actors.</li> <li>Background</li> <li>Use Cases and Adding Value</li> <li>Use Cases and Functional Requirements</li> <li>Use Case Types and Formats</li> <li>Fully Dressed Example: Process Sale</li> <li>Relating use cases- Include, Exclude, Generalize</li> <li>Example with diagram-ATM, Library Management System etc</li> </ul> <p><b>Diagram(3m)</b></p>
4	<p><b>(i).What is a POS system? Briefly explain about Inception Phase. (8m) BTL4</b></p> <p><b>Answer:</b> pg.no:33,47 in Craig Larman book</p> <p><b>Explanation(4m)</b></p> <ul style="list-style-type: none"> <li>The Next Gen POS System</li> <li>Architectural Layers and Case Study Emphasis</li> <li>Iterative Development and Iterative Learning</li> <li>Inception is the initial short step to establish a common vision and basic scope for the Project.</li> <li>It will include analysis of perhaps 10% of the use cases, analysis of the critical non-Functional requirement, creation of a business case, and preparation of the development Environment so that programming can start in the elaboration phase.</li> <li>Inception in one Sentence: Envision the product scope, vision, and business case.</li> </ul> <p><b>Diagram(4m)</b></p> <p><b>(ii). Comparison between Association and attributes. (5m) BTL4</b></p> <p><b>Answer:</b> pg.no:150,158 in Craig Larman book</p> <p><b>Explanation(5m)</b></p> <ul style="list-style-type: none"> <li>Association is a group of links having common structure and common behavior.</li> <li>Association depicts the relationship between objects of one or more classes.</li> <li>A link can be defined as an instance of an association</li> <li>A set of attributes for the objects that are to be instantiated from the class.</li> <li>Generally, different objects of a class have some difference in the values of the attributes.</li> <li>Attributes are often referred as class data</li> </ul>
5	<p><b>(i).Explain the purpose of usecase model? Identify the actors, scenarios, and usecases for a library Management system. (8m) (Nov/Dec 2016) BTL5</b></p> <p><b>Answer:</b> pg.no:58,64, refer notes in Craig Larman book</p> <p><b>Categories(8m)</b></p> <p><b>Actors of the Library Management System(4m)</b></p> <ul style="list-style-type: none"> <li>Member</li> <li>Administrator</li> <li>Librarian</li> <li>Guest</li> </ul> <p><b>Use cases of Library Management System(4m)</b></p> <ul style="list-style-type: none"> <li>Login</li> <li>View User Details</li> <li>View Books</li> <li>View Members</li> <li>Reserve Books</li> <li>Search Books</li> <li>Issue Books</li> <li>Return Books</li> </ul>

	<ul style="list-style-type: none"> <li>• Add/Remove Books</li> </ul> <p>Add/Remove Members</p> <p><b>(ii). Rank the 3 kinds of actors and explain the 3 common Use Case formats. BTL5 (5m)</b></p> <p><b>Answer:</b> pg.no:63,80 in Craig Larman book</p> <p><b>Use case(5m)</b></p> <ul style="list-style-type: none"> <li>• Primary actor has user goals fulfilled through using services of the SuD. For example, the cashier</li> <li>• Supporting actor provides a service (for example, information) to the SuD. The automated payment authorization service is an example</li> <li>• Offstage actor has an interest in the behavior of the use case, but is not primary or supporting; for example, a government tax agency</li> </ul>
6	<p><b>List the various UML diagram and examine the purpose of each diagram. (13m) BTL1</b></p> <p><b>Answer:</b> pg.no:133,249-250, refer notes in Craig Larman book</p> <p><b>Explanation(8m)</b></p> <p><b>Diagram(5m)</b></p> <ul style="list-style-type: none"> <li>• Class Diagram. Class diagrams are the most common diagrams used in UML</li> <li>• Object Diagram. Object diagrams can be described as an instance of class diagram.</li> <li>• Component Diagram.</li> <li>• Deployment Diagram.</li> <li>• Use Case Diagram.</li> <li>• Sequence Diagram.</li> <li>• Collaboration Diagram.</li> <li>• Statechart Diagram.</li> </ul>

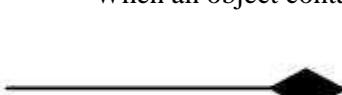
## PART C

1	<p><b>For the NextGen POS system design the following Conceptual class hierarchies. (15m) BTL2</b></p> <p><b>(i). Conceptual super class</b></p> <p><b>(ii). Conceptual subclass</b></p> <p><b>(iii). Authorization Transaction classes.</b></p> <p><b>(iv). Abstract Conceptual classes.</b></p> <p><b>Answer:</b> pg.no:535-540 in Craig Larman book</p> <p><b>Definition(2m)</b></p> <p>A conceptual superclass definition is more general or encompassing than a subclass definition.</p> <p><b>Explanation(10m)</b></p> <p><b>For example,</b> consider the superclass <i>Payment</i> and its subclasses (<i>CashPayment</i>, and so on). Assume the definition of <i>Payment</i> is that it represents the transaction of transferring money (not necessarily cash) for a purchase from one party to another, and that all payments have an amount of money transferred.</p> <p><b>Diagram(3m)</b></p>
2	<p><b>Explain the benefits and concepts of use case and use case model and analyze the relating use cases have in Library management system. (15m) BTL4</b></p> <p><b>Answer:</b> pg.no: 11, refer notes in Craig Larman book</p> <p><b>Explanation(10m)</b></p> <p><b>Actors of the Library Management System</b></p> <ul style="list-style-type: none"> <li>• Member</li> <li>• Administrator</li> <li>• Librarian</li> <li>• Guest</li> </ul>

	<p><b>Use cases of Library Management System</b></p> <ul style="list-style-type: none"> <li>• Login</li> <li>• View User Details</li> <li>• View Books</li> <li>• View Members</li> <li>• Reserve Books</li> <li>• Search Books</li> <li>• Issue Books</li> <li>• Return Books</li> <li>• Add/Remove Books</li> </ul> <p>Add/Remove Members</p> <p><b>Diagram(5m)</b></p> <p>3 Explain with example, how use case modeling is used to describe functional requirements. Identify the actors, scenario and use cases for the example. (15m) BTL5</p> <p>Answer: pg.no:58,64 in Craig Larman book</p> <p><b>Diagram(3m)</b></p> <p><b>Definition(2m)</b></p> <p>A use case is a collection of related success and failure scenarios that describe an actor using a system to support a goal. Use cases are text documents, not diagrams, and use-case modeling is primarily an act of writing text, not drawing diagrams.</p> <p><b>Explanation(8m)</b></p> <p>A use case diagram is an excellent picture of the system context; it makes a good context diagram that is, showing the boundary of a system, what lies outside of it, and how it gets used. It serves as a communication tool that summarizes the behavior of a system and its actors.</p> <ul style="list-style-type: none"> <li>• Background</li> <li>• Use Cases and Adding Value</li> <li>• Use Cases and Functional Requirements</li> <li>• Use Case Types and Formats</li> <li>• Fully Dressed Example: Process Sale</li> <li>• Relating use cases- Include, Exclude, Generalize</li> <li>• Example with diagram-ATM, Library Management System etc</li> </ul>
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4	<p><b>By considering your own application, perform and analyze the object oriented system Development and give the use case model for the same (use include, extend and generalization). (15m) BTL4</b></p> <p><b>Answer:</b> pg.no:494,497,260 in Craig Larman book</p> <p><b>Explanation(10m)</b></p> <p><b>Diagram(5m)</b></p> <p>To draw a use case diagram, we should have the following items identified.</p> <ul style="list-style-type: none"> <li>• Functionalities to be represented as use case</li> <li>• Actors</li> <li>• Relationships among the use cases and actors.</li> <li>• The name of a use case is very important. The name should be chosen in such a way so that it can identify the functionalities performed.</li> <li>• Give a suitable name for actors.</li> <li>• Show relationships and dependencies clearly in the diagram.</li> <li>• Do not try to include all types of relationships, as the main purpose of the diagram is to identify the requirements.</li> <li>• Use notes whenever required to clarify some important points.</li> </ul>
5	<p><b>A University conducts examinations and the results are announced. Prepare a report for the following:</b></p> <p>(i)Print the marks in the register number order semester wise for each department</p> <p>(ii)Print the Arrear list semester wise.</p> <p>(iii)Prepare a Rank list for each department.</p> <p>(iv)Prepare the final aggregate mark list for final year students.</p> <p><b>Identify the problem statement and Design and Explain the classes for each sequence. Draw a detailed flow chart using state chart diagrams. Design this system using Rational Rose. Design all the UML diagrams for designing this system. (15m) BTL6</b></p> <p><b>Answer:</b> Pg.no:489,11,refer notes in Craig Larman book</p> <p><b>Explanation(10m)</b></p> <ul style="list-style-type: none"> <li>• Print the marks in the register number order semester wise for each department</li> <li>• Print the Arrear list semester wise.Prepare a Rank list for each department</li> <li>• Prepare the final aggregate mark list for final year students.</li> </ul> <p><b>Diagram(5m)</b></p>

<b>UNIT 2- STATIC UML DIAGRAMS</b>	
<b>Class Diagram— Elaboration – Domain Model – Finding conceptual classes and description classes – Associations – Attributes – Domain model refinement – Finding conceptual class Hierarchies – Aggregation and Composition - Relationship between sequence diagrams and use cases – When to use Class Diagrams</b>	
<b>PART A</b>	
1	<p><b>Define design Class Diagram? When to use Class Diagrams? (May/June 2016) BTL1</b></p> <p>A class diagram in the Unified Modeling Language (UML) is a type of static structure diagram that describes the structure of a system by showing the system's classes, their attributes, operations (or methods), and the relationships among objects</p> <p>The class diagrams are widely used in the modeling of object oriented systems because they are the only UML diagrams, which can be mapped directly with object-oriented languages</p>
2	<p><b>Define Aggregation. BTL1</b></p> <p><b>Aggregation</b> is defined as a “part-of” or “has-a” relationship, with the ability to navigate from the whole to its parts. An aggregate object is an object that is composed of one or more other objects</p>
3	<p><b>List out the Components of Domain model? BTL1</b></p> <p>A domain model contains:</p> <ul style="list-style-type: none"> <li>• conceptual classes</li> <li>• associations between conceptual classes</li> <li>• attributes of a conceptual class</li> </ul>
4	<p><b>Distinguish abstract use case and concrete Use Case. BTL4</b></p> <p>A <b>concrete</b> use case is initiated by an actor and constitutes a complete flow of events. "Complete" means that an instance of the use case performs the entire operation called for by the actor.</p> <p>An <b>abstract</b> use case is never instantiated in itself</p>
5	<p><b>Express the meaning of Elaboration and What are the tasks performed in elaboration? (Nov/Dec 2015) BTL2</b></p> <p><b>Elaboration</b> is the second of the four phases in the RUP approach. It is to define and baseline the architecture of the system in order to provide a stable basis for the bulk of the design and implementation effort in the Construction phase</p> <p><b>Task Performed:</b></p> <ul style="list-style-type: none"> <li>• Elaboration are to address known risk factors and to establish and validate the system architecture.</li> <li>• During the Elaboration phase the project team is expected to capture a healthy majority of the system requirements</li> </ul>
6	<p><b>Compare and Contrast of Sequence and Collaboration diagram. BTL5</b></p> <p><b>Sequence diagrams</b> shows object interaction in timely manner(so no need of numbering the messages).</p> <p><b>Collaboration diagram</b> doesn't show object interaction in timely manner.</p>
7	<p><b>Define Domain Model. BTL1</b></p> <p>The <b>domain model</b> is a representation of meaningful real-world concepts pertinent to the domain that need to be modelled in software</p>
8	<p><b>Demonstrate how to create a Domain model. (Nov/Dec 2015,2016) BTL3</b></p> <ul style="list-style-type: none"> <li>• Identify Candidate Conceptual classes</li> <li>• Draw them in a Domain Model and Add associations necessary to record the responsibility and collaboration.</li> </ul>

	<ul style="list-style-type: none"> <li>• Add attributes necessary for information to be preserved</li> </ul>
9	<b>Express why we call a domain model a “Visual Dictionary”. (Nov/Dec 2016) BTL2</b> <p>It's easy to understand the terms of domain model and especially their relationships in a visual language, so domain model is called as Visual Dictionary</p>
10	<b>Define Conceptual class. (May/June 2016) BTL1</b> <ul style="list-style-type: none"> <li>• A domain model contains conceptual classes</li> <li>• A conceptual class is an idea, thing, or object</li> </ul>
11	<b>Compare Aggregation and Composition. BTL5</b> <ul style="list-style-type: none"> <li>• A directional association between objects.</li> <li>• Aggregation is also called a “Has-a” relationship.</li> </ul>  <ul style="list-style-type: none"> <li>• A restricted aggregation is called composition</li> <li>• When an object contains the other object it is called composition.</li> </ul> 
12	<b>Illustrate the usage of Description or specification class. BTL3</b> <p>There needs to be a description about an item or service,</p> <ol style="list-style-type: none"> <li>1. Independent of the current existence of any examples of those items or services.</li> <li>2. Deleting instances of things they describe (for example, Item) results in a loss of information that needs to be maintained, due to the incorrect association of information with the deleted thing.</li> <li>3. It reduces redundant or duplicated information.</li> </ol>
13	<b>Generalize the purpose of association relationship. BTL6</b> <p><b>Association</b> is a relationship between classifiers which is used to show that instances of classifiers could be either linked to each other or combined logically or physically into some aggregation</p>
14	<b>Define attribute? List out the types of attributes. (Nov/Dec 2018) BTL1</b> <p>An attribute is a specification that defines a property of an object, element, or file</p> <p>Types:</p> <ul style="list-style-type: none"> <li>• Single valued attributes</li> <li>• Multi valued attributes</li> <li>• Compound /Composite attributes</li> <li>• Simple / Atomic attributes</li> <li>• Stored attributes</li> <li>• Derived attributes</li> <li>• Complex attributes</li> <li>• Key attributes</li> <li>• Non key attributes</li> <li>• Required attributes</li> <li>• Optional/ null value attributes</li> </ul>
15	<b>Give the meaning of abstract conceptual class. BTL2</b> <p>It is useful to identify abstract classes in the domain model because they constrain what classes it is possible to have concrete instances of, thus clarifying the rules of the problem domain.</p>

16	<b>How to create Domain model? BTL6</b> <ul style="list-style-type: none"> <li>• Identify Candidate Conceptual classes</li> <li>• Draw them in a Domain Model and Add associations necessary to record the responsibility and collaboration.</li> <li>• Add attributes necessary for information to be preserved</li> </ul>
17	<b>Compare qualified association and reflexive association. BTL5</b> <ul style="list-style-type: none"> <li>• The reflexive association is used when objects in the same class can be associated</li> <li>• Qualified associations provide the same functionality as indexes</li> </ul>
18	<b>Point out the main goals of Establishing conceptual class Hierarchies. BTL4</b> <p>A conceptual model is the first step before drawing a UML diagram. It helps to understand the entities in the real world and how they interact with each other</p>
19	<b>What Artifacts May Start in Inception? BTL2</b> <p>Some sample artifacts are Vision and Business Case, Use-Case Model, Supplementary Specification, Glossary, Risk List &amp; Risk Management Plan, Prototypes and proof-of-concepts etc.</p>
20	<b>Illustrate what Tests Can Help Find Useful Use Cases? BTL2</b> <ol style="list-style-type: none"> <li>1. The Boss Test</li> <li>2. The EBP Test</li> <li>3. The Size Test</li> </ol>
21	<b>List the key ideas for Planning the Next Iteration? BTL1</b> <p>Organize requirements and iterations by risk, coverage, and criticality.</p>
22	<b>How to Create a Domain Model? BTL6</b> <p>The current iteration requirements under design:</p> <ol style="list-style-type: none"> <li>1. Find the conceptual classes (see a following guideline).</li> <li>2. Draw them as classes in a UML class diagram.</li> <li>3. Add associations and attributes.</li> </ol>
23	<b>Define Requirements and mention its types. BTL1</b> <p>Requirements are capabilities and conditions to which the system and more broadly, the project must conform.</p> <ol style="list-style-type: none"> <li>1. Functional</li> <li>2. Reliability</li> <li>3. Performance</li> <li>4. Supportability</li> </ol>

**PART B**

1	<p><b>(i)Distinguish between the Concepts of Component and Deployment Diagram with an example of Book bank system. BTL2 (13m)</b></p> <p><b>Answer:</b> pg.no:651-653 in Craig Larman book</p> <p><b>Definition(2m)</b></p> <ul style="list-style-type: none"> <li>• A component is a code module. Component diagrams are physical analogs of class diagram.</li> </ul> <p><b>Explanation(8m)</b></p> <p>Deployment diagrams show the physical configurations of software and hardware</p> <p><b>Diagram(3m)</b></p>
2	<p><b>Constructs the design for Library information system which comprises and following notations. (13m) (i). Aggregation and Composition (ii).Generalization and Specialization. (iii). Association (Nov/Dec 2015) BTL6</b></p> <p><b>Explanation(8m)</b></p>

	<p><b>Diagram(5m)</b>  <b>Answer:</b> pg.no:264, refer notes in Craig Larman book</p> <p><b>Aggregation (2m)</b> is a vague kind of association in the UML that loosely suggests whole-part relationships (as do many ordinary associations). It has no meaningful distinct semantics in the UML versus a plain association, but the term is defined in the UML.</p> <p><b>Composition(2m)</b>, also known as composite aggregation, is a strong kind of whole-part aggregation and is useful to show in some models. A composition relationship implies that</p> <p><b>Generalization(2m)</b> is the process of extracting shared characteristics from two or more classes, and combining them into a generalized superclass.</p> <p><b>Specialization(2)</b> means creating new subclasses from an existing class</p> <p>An <b>Attribute</b> is a logical data value of an object.  An <b>Association</b> is a relationship between classes</p>
3	<p><b>i) Summarize the Elaboration phase. Discuss the differences between elaboration and inception with suitable diagram for university domain. (Nov/Dec 2015, April/May 2017)</b></p> <p><b>BTL2 (8m) Answer:</b> pg.no:33,123,127 in Craig Larman book</p> <p><b>Definition(2m)</b></p> <ul style="list-style-type: none"> <li>Elaboration is the initial series of iterations during which the team does serious investigation, implements (programs and tests) the core architecture, clarifies most requirements, and tackles the high-risk issues.</li> </ul> <p><b>Explanation(6m)</b></p> <ul style="list-style-type: none"> <li>In the UP, "risk" includes business value.</li> <li>Therefore, early work may include implementing scenarios that are deemed important, but are not especially technically risky.</li> <li>Inception is the initial short step to establish a common vision and basic scope for the Project.</li> </ul> <p><b>ii) Describe a suitable example showing the various relationships used in Use Case and also give a short note on each relationship. BTL2 (5m)</b></p> <p><b>Answer:</b> pg.no:61-63 in Craig Larman book   <b>Relationship(5m)</b></p> <p>To draw a use case diagram, we should have the following items identified.</p> <ul style="list-style-type: none"> <li>Functionalities to be represented as use case</li> <li>Actors</li> <li>Relationships among the use cases and actors.</li> <li>The name of a use case is very important. The name should be chosen in such a way so that it can identify the functionalities performed.</li> <li>Give a suitable name for actors.</li> <li>Show relationships and dependencies clearly in the diagram.</li> <li>Do not try to include all types of relationships, as the main purpose of the diagram is to identify the requirements.</li> <li>Use notes whenever required to clarify some important points.</li> </ul>
4	<p><b>(i). Describe the strategies used to identify the conceptual classes. (5m) (Nov/Dec 2018) (April/May 2017) BTL2</b></p> <p><b>Answer:</b> pg.no:14,136 in Craig Larman book</p> <p><b>Conceptual Class(5m)</b></p> <ul style="list-style-type: none"> <li>The domain model illustrates conceptual classes or vocabulary in the domain.</li> </ul>

	<p>Informally, a conceptual class is an idea, thing, or object.</p> <ul style="list-style-type: none"> <li>More formally, a conceptual class may be considered in terms of its symbol, intension, and extension</li> <li>Symbol words or images representing a conceptual class.</li> <li>Intension the definition of a conceptual class.</li> <li>Extension the set of examples to which the conceptual class applies</li> </ul> <p><b>(ii).Describe the steps to create a domain model used for representing the conceptual classes. (8m) (May/June 2016) BTL2</b></p> <p><b>Answer:</b> pg.no:134 in Craig Larman book</p> <p><b>Explanation(5m)</b></p> <p>The current iteration requirements under design:</p> <ol style="list-style-type: none"> <li>Find the conceptual classes (see a following guideline).</li> <li>Draw them as classes in a UML class diagram.</li> <li>Add associations and attributes.</li> </ol> <p><b>Diagram(3m)</b></p>
5	<p><b>(i).Illustrate the concepts of Domain model with example. (7m)</b></p> <p><b>Answer:</b> pg.no:134 in Craig Larman book</p> <p><b>Domain Model(5m)</b></p> <ul style="list-style-type: none"> <li>Applying UML notation, a domain model is illustrated with a set of class diagrams in which no operations (method signatures) are defined.</li> <li>It provides a conceptual perspective. It may show: <ul style="list-style-type: none"> <li>domain objects or conceptual classes</li> <li>associations between conceptual classes</li> <li>attributes of conceptual classes</li> </ul> </li> </ul> <p><b>Diagram(2m)</b></p> <p><b>(ii).Show when to model with Description classes with example. (6m) BTL3</b></p> <p><b>Answer:</b> pg.no:147 in Craig Larman book</p> <p><b>Explanation (6m)</b></p> <ul style="list-style-type: none"> <li>A class represents a collection of objects having same characteristic properties that exhibit common behavior.</li> <li>It gives the blueprint or description of the objects that can be created from it.</li> <li>Creation of an object as a member of a class is called instantiation</li> </ul>
6	<p><b>Describe in detail about the Class Diagram. (13m) (Nov/Dec 2018) (May/June 2016) BTL1</b></p> <p><b>Answer:</b> pg.no:249-250 in Craig Larman book</p> <p><b>Definition (2m)</b></p> <p>A static view of the class definitions is usefully shown with a design class diagram.</p> <p><b>Explanation(8m)</b></p> <p>This illustrates the attributes and methods of the classes.</p> <ul style="list-style-type: none"> <li>relationships used in class diagram</li> <li>Generalization(class to class)</li> <li>Association (object to object)</li> <li>Aggregation (object to object)</li> <li>Composition (object to object)</li> </ul> <p><b>Diagram(3m)</b></p>

<b>PART C</b>	
1	<p><b>With a suitable example explain how to design a class. Give all possible representation in a class (such as: name, attribute, visibility, methods, and responsibilities). BTL6 (15m)</b></p> <p><b>Answer:</b> pg.no:333 in Craig Larman book</p> <p><b>Explanation(10m)</b></p> <ul style="list-style-type: none"> <li>• <b>Name:</b> The first row in a class shape.</li> <li>• <b>Attributes:</b> The second row in a class shape. Each attribute of the class is displayed on a separate line.</li> <li>• <b>Methods:</b> The third row in a class shape. Also known as operations, methods are displayed in list format with each operation on its own line.</li> <li>• <b>Interfaces:</b> A collection of operation signatures and/or attribute definitions that define a cohesive set of behaviors.</li> <li>• <b>Inheritance:</b> The process of a child or sub-class taking on the functionality of a parent or superclass, also known as generalization.</li> <li>• <b>Bidirectional association:</b> The default relationship between two classes.</li> </ul> <p><b>Diagram(5m)</b></p>
2	<p><b>Explain the concepts of Finding Description classes with the example of Airline and mobile phone company. BTL5 (15m)</b></p> <p><b>Answer:</b> pg.no:147 in Craig Larman book</p> <p><b>Explanation(10m)</b></p> <p>The class diagram is one of the most commonly used diagrams in UML, as explained in depth in our guide on class diagrams. Software engineers and business professionals often choose class diagrams to map the structure of particular systems because they clearly display the various classes, attributes, operations, and relationships between objects.</p> <p><b>Diagram(5m)</b></p>

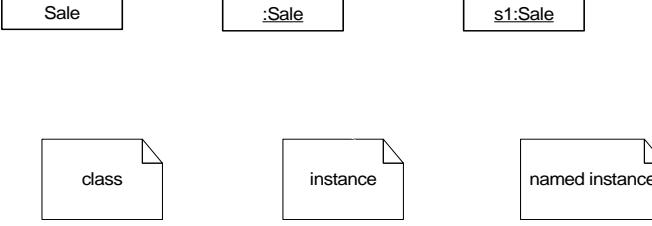
### UNIT-3 DYNAMIC AND IMPLEMENTATION UML DIAGRAMS

**Dynamic Diagrams – UML interaction diagrams - System sequence diagram – Collaboration diagram – When to use Communication Diagrams - State machine diagram and Modelling –When to use State Diagrams - Activity diagram – When to use activity diagrams**

**Implementation Diagrams - UML package diagram - When to use package diagrams - Component and Deployment Diagrams – When to use Component and Deployment diagrams**

#### PART A

1	<b>Express the use of Sequence Diagram. BTL2</b> <ul style="list-style-type: none"> <li>• A <b>sequence diagram</b> shows object interactions arranged in time sequence.</li> <li>• It depicts the objects and classes involved in the scenario and the sequence of messages exchanged between the objects needed to carry out the functionality of the scenario</li> <li>• Sequence diagrams are sometimes called event diagrams or event scenarios</li> </ul>
2	<b>Distinguish sequence diagram and communication diagram. BTL2</b> <ul style="list-style-type: none"> <li>• A sequence diagram shows time sequence as a geometric dimension, but the relationships among roles are implicit</li> <li>• A collaboration diagram shows the relationships among roles geometrically and relates messages to the relationships, but time sequences are less clear because they are implied by the sequence numbers</li> </ul>
3	<b>Demonstrate what do you mean by sequence diagram in UML? Where and for what it is used? BTL3</b> <p>A sequence diagram is a type of interaction diagram because it describes how and in what order a group of objects works together.</p> <p>These diagrams are used by software developers and business professionals to understand requirements for a new system or to document an existing process. Represent the details of a UML use case.</p> <ul style="list-style-type: none"> <li>• Model the logic of a sophisticated procedure, function, or operation.</li> <li>• See how objects and components interact with each other to complete a process.</li> <li>• Plan and understand the detailed functionality of an existing or future scenario.</li> </ul>
4	<b>What is meant by System Behavior? Nov/Dec 2015 BTL1</b> <ul style="list-style-type: none"> <li>• It is useful to understand what the external events are that our system must respond to, and to examine the details regarding what our system is supposed to do in response to those external events.</li> <li>• This is useful because we design and program primarily to service these events.</li> <li>• They are the driving force that define our software. The results of this investigation are referred to as the System Behavior model.</li> </ul>
5	<b>Define Package. Draw UML notation for Package. BTL1</b> <p><b>Package</b> is a namespace used to group together elements that are semantically related and might change together.</p>
6	<b>Analyze the use of UML Package Diagram BTL4</b> <ul style="list-style-type: none"> <li>• A package diagram is a UML diagram composed only of packages and the dependencies between them.</li> <li>• A package is a UML construct that enables you to organize model elements, such as use cases or classes, into groups.</li> </ul>

7	<b>Define Logical architecture. (Nov/Dec 2018) BTL1</b>
	The logical architecture, describes the system in terms of its conceptual organization in layers, packages, classes, interfaces and subsystems.
8	<b>Formulate the guideline to be followed when designing with layers. BTL6</b>
	The essential ideas of using layers:
	Organize the large - scale logical structure of a system into discrete layers of distinct, related responsibilities, with a clean, cohesive separation of concerns such that the "lower" layers are low - level and general services, and the higher layers are more application specific.
	Collaboration and coupling is from higher to lower layers; lower - to - higher layer coupling is avoided.
9	<b>List the layers of architectural layers. (April/May 2017) BTL1</b>
	The layers include:
	<ul style="list-style-type: none"> <li>• User Interface</li> <li>• Application Logic and Domain Objects</li> <li>• Technical Services</li> </ul>
	<b>Layers are:</b>
	<ul style="list-style-type: none"> <li>• strict layered architecture</li> <li>• relaxed layered architecture</li> </ul>
10	<b>Differentiate strict layered and relaxed layered architecture. BTL2</b>
	<b>Strict layered architecture:</b> a layer only calls upon the services of the layer directly below it. This design is common in network protocol stacks
	<b>Relaxed layered architecture:</b> a higher layer calls upon several lower layers
11	<b>Summarize the Model View separation principle. BTL5</b>
	The <b>Model - View Separation principle</b> states that model (domain) objects should not have direct knowledge of view (UI) objects, at least as view objects.
	<b>Example:</b> a Register or Sale object should not directly send a message to a GUI window object ProcessSaleFrame, asking it to display something, change color, close, and so forth.
12	<b>List the common UML Interaction diagram notation. BTL1</b>
	<ul style="list-style-type: none"> <li>• Patterns, principles, and idioms can be applied to improve the quality of the Interaction Diagrams</li> </ul>
	 <p>The diagram illustrates six UML interaction diagram notations arranged in two rows. The top row contains three boxes: 'Sale' (a simple rectangle), ':Sale' (a rectangle with a colon and a hyphen), and 's1:Sale' (a rectangle with a label 's1:' preceding the name). The bottom row contains three boxes: 'class' (a rectangle with a small document icon), 'instance' (a rectangle with a small document icon), and 'named instance' (a rectangle with a small document icon).</p>
13	<b>Name the layers in the 3 tier architecture. BTL1</b>
	<b>Three-tier architecture</b> (Model View Controller - MVC), in software engineering, is a client-server architecture in which presentation, application processing, and data management functions are physically separated
14	<b>Show the relationship between Interaction and Class diagram . (Nov/Dec 2015) BTL3</b>
	<b>Interaction diagrams</b> are models that describe how group of objects collaborate to realize some behavior.
	A <b>class diagram</b> describes the static structure of a system. It shows how a system is structured rather than how it behaves.

15	<b>Express the meaning of Facade. BTL2</b> Facade pattern hides the complexities of the system and provides an interface to the client using which the client can access the system
16	<b>Differentiate Class diagram and Interaction diagram. BTL4</b> <b>Interaction diagrams</b> are models that describe how group of objects collaborate to realize some behavior. A <b>class diagram</b> describes the static structure of a system. It shows how a system is structured rather than how it behaves.
17	<b>Illustrate the term Classifier. May/June 2016 BTL3</b> A <b>classifier</b> is an abstract metaclass classification concept that serves as a mechanism to show interfaces, classes, datatypes and components. A <b>classifier</b> describes a set of instances that have common behavioral and structural features
18	<b>Summarize SSD. BTL2</b> An SSD shows system events for one scenario of a use case, therefore it is generated from inspection of a use case
19	<b>Summarize the benefits of using layers. BTL5</b> <ul style="list-style-type: none"> <li>Source code changes are rippling throughout the system - many parts of the systems are highly coupled.</li> <li>Application logic is intertwined with the user interface, so it cannot be reused with a different interface or distributed to another processing node.</li> </ul>
20	<b>Compare and Contrast asynchronous and synchronous message. BTL4</b> In UML, filled arrowheads show a synchronous message, while stick arrowheads show an asynchronous message. <ul style="list-style-type: none"> <li>If a caller sends asynchronous message, it must wait until the message is done, such as invoking a subroutine. asynchronous calls in multithreaded applications and in message-oriented middleware</li> </ul>
21	<b>What is meant by link? BTL1</b> <ul style="list-style-type: none"> <li>A link is a connection path between two objects; it indicates some form of navigation and visibility between the objects is possible .</li> <li>More formally, a link is an instance of an association.</li> </ul> <b>For example</b> , there is a link or path of navigation from a Register to a Sale, along which messages may flow, such as the make 2 Payment message.
22	<b>List the approaches for identifying classes. BTL1</b> The four alternative approaches for identifying classes: <ul style="list-style-type: none"> <li>The noun phrase approach.</li> <li>The common class patterns approach.</li> <li>The use-case driven, sequence/collaboration modeling approach.</li> <li>The classes, responsibilities and collaborators (CRC) approach.</li> </ul>
23	<b>Evaluate How to create an instance? BTL5</b> <ul style="list-style-type: none"> <li>Any message can be used to create an instance, but there is a convention in the UML to use a message named create for this purpose.</li> <li>If another (perhaps less obvious) message name is used, the message may be annotated with a special feature called a UML stereotype, like so: «create».</li> <li>The create message may include parameters, indicating the passing of initial values. This indicates, for example, a constructor call with parameters in Java.</li> </ul>
24	<b>Give the guidelines for naming a class. BTL1</b> The guidelines for naming classes: <ul style="list-style-type: none"> <li>The class name should be singular.</li> <li>One general rule for naming classes is that you should use names with which the users or clients</li> </ul>

	<p>are comfortable.</p> <ul style="list-style-type: none"> <li>• The name of a class should reflect its intrinsic nature Use readable name.</li> <li>• Capitalize class names.</li> </ul>
25	<p><b>What is meant by Pure Fabrication? BTL1</b></p> <ul style="list-style-type: none"> <li>• This is another GRASP pattern.</li> <li>• A Pure Fabrication is an arbitrary creation of the designer, not a software class whose name is inspired by the Domain Model. A use-case controller is a kind of Pure Fabrication.</li> </ul>
26	<p><b>Discover the major Difference between Component and Deployment Diagram. BTL3</b></p> <p><b>Component diagram</b> have different elements of the system that have been grouped together and contains the link between these components.</p> <p>A <b>Deployment diagram</b> describes on which hardware elements do these components reside</p>
27	<p><b>Define State Chart Diagram. BTL1</b></p> <p><b>Statechart diagram</b> is one of the five UML diagrams used to model the dynamic nature of a system.</p>
28	<p><b>What is package diagram? BTL4</b></p> <p><b>Package diagram:</b> It is a kind of structural diagram, shows the arrangement and organization of model elements in middle to large scale project.</p>
29	<p><b>Compare Activity and state chart diagram BTL5</b></p> <p>Mention the Elements of an Activity Diagram.</p> <p><b>Activity diagrams</b> are similar to the procedural flow charts. <b>Activity diagrams</b> support description of parallel activities and synchronization aspects involved in different activities</p>
30	<p><b>Formulate the purpose of Interaction Diagram. BTL6</b></p> <p><b>Interaction diagrams</b> are models that describe how a group of objects collaborate in some behavior - typically a single use-case.</p>
	<b>PART B</b>
1	<p><b>(i).Illustrate the relationship between sequence diagram (Nov/Dec 2018) and Use Case with example. (8m) (Nov/Dec2016) BTL3</b></p> <p>Answer: pg.no:176,222 in Craig Larman book</p> <p><b>Relationship(8m)</b></p> <p>Sequence Diagram models the collaboration of objects based on a time sequence. It shows how the objects interact with others, in a particular, scenario of a use case.</p> <p>For example: Visual Paradigm can automate this process by generating a flow of events of a use case to a sequence diagram</p> <p><b>(ii).Demonstrate the Interaction Diagram notations and explain it? (5m)</b></p> <p>Answer: pg.no:221 in Craig Larman book</p> <p><b>Diagram(5m)</b></p> <p>Patterns, principles, and idioms can be applied to improve the quality of the Interaction Diagrams</p> <div style="text-align: center; margin-top: 20px;"> </div>
2	<p><b>(i).Describe briefly about the logical architecture (Nov/Dec 2018) and UML package diagram. (7m) BTL1</b></p>

	<p><b>Answer:</b> pg.no: 197-199 in Craig Larman book</p> <p><b>Explanation(5m)</b></p> <ul style="list-style-type: none"> <li>• Layer is a coarse-grained grouping of classes, packages, or subsystems that has cohesive (strongly related) responsibilities for a major aspect of the system</li> <li>• Application layer is the focus of Use Cases</li> <li>• Higher layers (such as UI layer) call upon services of lower layers, but not normally vice versa.</li> </ul> <p><b>Diagram(2m)</b></p> <p><b>(ii).Identify the relationship between Domain layer and Domain model. (6m) BTL1</b></p> <p><b>Answer:</b> pg.no:134-136 in Craig Larman book</p> <p><b>Domain Layer(6m)</b></p> <ul style="list-style-type: none"> <li>• A Conceptual model in the field of computer science is also known as a domain model.</li> <li>• A conceptual model represents 'concepts' (entities) and relationships between them.</li> <li>• A domain model in problem solving and software engineering is a conceptual model of all the topics related to a specific problem. It describes the various entities, their attributes, roles, and relationships, plus the constraints that govern the problem domain</li> </ul>
3	<p><b>What is Model View separation principle? Examine the motivation for Model View separation. (13m) (April/May 2017, May/June 2016) BTL1</b></p> <p><b>Answer:</b> pg.no:209,331 in Craig Larman book</p> <p><b>Diagram(2m)</b></p> <p><b>Definition(2m)</b></p> <p>The <b>Model - View Separation principle</b> states that model (domain) objects should not have direct knowledge of view (UI) objects, at least as view objects.</p> <p><b>Explanation(7m)</b></p> <p><b>Example:</b> a Register or Sale object should not directly send a message to a GUI window object ProcessSaleFrame, asking it to display something, change color, close, and so forth.</p>
4	<p><b>(i).What are the benefits of using layers? Provide the relationship between Domain layer and Domain model. (7m) BTL1</b></p> <p><b>Answer:</b> pg.no:134-136 in Craig Larman book</p> <p><b>Benefits(5m)</b></p> <ul style="list-style-type: none"> <li>• A Conceptual model in the field of computer science is also known as a domain model.</li> <li>• A conceptual model represents 'concepts' (entities) and relationships between them.</li> <li>• A domain model in problem solving and software engineering is a conceptual model of all the topics related to a specific problem. It describes the various entities, their attributes, roles, and relationships, plus the constraints that govern the problem domain</li> </ul> <p><b>Diagram (2m)</b></p> <p><b>(ii).Describe the concepts of Relaxed layer coupling. (6m) BTL1</b></p> <p><b>Answer:</b> pg.no:199 in Craig Larman book</p> <p><b>Concept coupling(4m)</b></p> <ul style="list-style-type: none"> <li>• There are two general approaches to layering: strict layering and relaxed layering.</li> <li>• A relaxed layered application loosens the constraints such that a component can interact with components from any lower layer.</li> <li>• Using relaxed layering can improve efficiency because the system does not have to forward simple calls from one layer to the next.</li> </ul> <p><b>Diagram(2m)</b></p>
5	<p><b>Draw a neat sketch of logical layered architecture of Next Gen application and Discuss the components in detail. (13m) (Nov/Dec 2016) BTL2</b></p> <p><b>Answer:</b> pg.no:199 in Craig Larman book</p> <p><b>Definition(2m)</b></p> <p><b>Explanation(8m)</b></p>

	<p><b>Diagram(3m)</b></p> <ul style="list-style-type: none"> <li>• In a strictly layered model, each layer only calls the services of the layer below it</li> <li>• For information services, the layered model is usually considered relaxed</li> <li>• For example, the GUI may utilize logging, or a form may directly access a database for a query</li> <li>• We will primarily concentrate on the middle layer, the Domain or Application Logic layer</li> <li>• For UI, we will primarily be concerned with how it interacts with the middle layer</li> </ul>
6	<p><b>What are the system sequence diagram? Differentiate the relationship between SSDs and use cases? Explain with an Example. (13m) (Nov/Dec 2016) BTL2</b></p> <p>Answer: pg.no:176,222 in Craig Larman book</p> <p><b>Definition(2m)</b></p> <p>Sequence Diagram models the collaboration of objects based on a time sequence. It shows how the objects interact with others, in a particular, scenario of a use case.</p> <p><b>Explanation(8m)</b></p> <p>For example: Visual Paradigm can automate this process by generating a flow of events of a use case to a sequence diagram</p> <p><b>Diagram(3m)</b></p>
7	<p><b>Describe the UML notation for class diagram with an example. Explain the concept of Link, Association and Inheritance. (13m) (May/June 2016) BTL2</b></p> <p>Answer: pg.no:133,249 in Craig Larman book</p> <p><b>Explanation(8m)</b></p> <p><b>Link (2m)</b></p> <p>A link represents a connection through which an object collaborates with other objects. Rumbaugh has defined it as “a physical or conceptual connection between objects”. Through a link, one object may invoke the methods or navigate through another object. A link depicts the relationship between two or more objects.</p> <p><b>Association (3m)</b></p> <p>Association is a group of links having common structure and common behavior. Association depicts the relationship between objects of one or more classes. A link can be defined as an instance of an association.</p> <p><b>Inheritance(3m)</b></p> <p>Inheritance is the mechanism that permits new classes to be created out of existing classes by extending and refining its capabilities. The existing classes are called the base classes/parent classes/super-classes, and the new classes are called the derived classes/child classes/subclasses.</p> <p><b>Diagram(5m)</b></p>
8	<p><b>Apply Interactive modeling for a Payroll system in UML. (13m) (Nov/Dec 2016) BTL3</b></p> <p>Answer: pg.no:221-226 in Craig Larman book</p> <p><b>Definition (2m)</b></p> <p>The term interaction diagram, is a generalization of two more specialized UML diagram types both can be used to express similar message interactions:</p> <p><b>Explanation(6m)</b></p> <ul style="list-style-type: none"> <li>• collaboration diagrams <ul style="list-style-type: none"> <li>- illustrate object interactions in a graph or network format, in which objects can be placed anywhere on the diagram</li> </ul> </li> <li>• sequence diagrams</li> </ul> <p><b>Diagram(5m)</b></p>

<b>PART C</b>	
1.	<p><b>For the Course Registration system design the following UML diagrams. (15m)</b> (i).Conceptual Class Diagram (Over all system). (ii).Sequence and collaboration diagram (Login process, maintaining the course details.) <b>BTL6</b></p> <p><b>Conceptual Diagram(7m)</b>  <b>Sequence Diagram(8m)</b>  <b>Answer:</b> pg.no:15,Refer notes</p>
2.	<p><b>Design the logical layer architecture for Next Generation application. (15m) (Nov/Dec 2016)</b>  <b>BTL6</b></p> <p><b>Diagram(5m)</b>  <b>Answer:</b> pg.no: 144, refer notes  <b>Explanation(10m)</b></p> <ul style="list-style-type: none"> <li>• To achieve a layered architecture:</li> <li>• Organize the large-scale logical structure of a system into discrete layers of distinct, related responsibilities, with a clean, cohesive separation of concerns such that the "lower" layers are low-level and general services, and the higher layers are more application specific.</li> <li>• Collaboration and coupling is from higher to lower layers; lower-to-higher layer coupling must be avoided.</li> </ul>
3.	<p><b>Explain in detail about the relationship between interaction diagram and class Diagram. (15m) BTL5</b></p> <p><b>Answer:</b> pg.no:133,221 in Craig Larman book  <b>Definition(2m)</b> Interaction diagrams are models that describe how group of objects collaborate to realize some behavior.  <b>Explanation(8m)</b>  A <b>class diagram</b> describes the static structure of a system. It shows how a system is structured rather than how it behaves.<b>Diagram(3m)</b></p>
4	<p><b>Write a problem statement for Quiz System. Design the UML Use Case diagram, Activity diagram, Class diagram, Sequence diagram, State chart diagram, Package diagram, and Component and Deployment diagram (15m) BTL6</b></p> <p><b>Answer:</b> pg.no:11,477,478,133,249-250 in Craig Larman book  <b>Explanation(10m)</b>  <b>Diagram(5m)</b>  <b>PROBLEM STATEMENT:</b>  Developing a quiz system which includes both the user and the administrator wherein the administrator is privileged to prepare the quiz questions for the users based on the selected category. The competency of the user is evaluated at the end by displaying the score obtained by the user in the quiz that he undertook. The quiz system can be used to evaluate the competency of the person taking the quiz</p>
4.	<p><b>Comparison of sequence and communication diagram by using the Ticket Reservation system. (15m) BTL4</b></p> <p><b>Answer:</b> pg.no:223,refer notes  <b>Definition(2m) sequence diagram</b>  Participants are mostly arranged along the top of page, unless the drop-box participant creation notation is used. It is easy to gather the participants involved in particular interactions  <b>Explanation(8m)</b>  <b>Communication diagram</b> Participants as well as links are the focus, so they are shown clearly as rectangles  <b>Diagram(3m)</b></p>

<b>UNIT 4- DESIGN PATTERNS</b>	
<b>GRASP: Designing objects with responsibilities – Creator – Information expert – Low Coupling –High Cohesion – Controller Design Patterns – creational – factory method – structural – Bridge – Adapter – behavioural –Strategy – observer –Applying GoF design patterns – Mapping design to code</b>	
<b>PART A</b>	
1	<b>Define DesignPatterns. (Nov/Dec 2016) BTL1</b> <ul style="list-style-type: none"> <li>Pattern (or design pattern) is a written document that describes a general solution to a design problem that recurs repeatedly in many projects.</li> <li>Software designers adapt the pattern solution to their specific project</li> </ul>
2	<b>What is Elaboration? BTL1</b> <p>Elaboration is the initial series of iterations during which the team does serious investigation, implements (programs and tests) the core architecture, clarifies most requirements, and tackles the high-risk issues. In the UP, "risk" includes business value. Therefore, early work may include implementing scenarios that are deemed important, but are not especially technically risky.</p>
3	<b>Define responsibility. What are the various types of responsibilities? BTL1</b> <p><b>Responsibility-driven design</b> is essentially assigning responsibilities to collaborating objects. It is an iterative approach.</p> <p><b>Two basic types of responsibility:</b> <i>Doing</i> and <i>Knowing</i></p> <p><b>Doing:</b> doing something, creating an object, doing a calculation, initiate some action in another object, control activity between objects. Generate some activity</p> <p><b>Knowing:</b> knowing about private encapsulated data, related objects, or things that can be derived or calculated</p>
4	<b>What are the steps for mapping design to code? (Nov/Dec 2015,April/May 2017) BTL1</b> <p>The design model can be more or less close to the implementation model depending on how you map its classes to classes or similar constructs in the implementation language</p>
5	<b>List out the categories of Design patterns. State the use of design pattern. BTL1</b> <p>Design patterns are divided into three fundamental groups:</p> <ul style="list-style-type: none"> <li>Behavioral,</li> <li>Creational, and</li> <li>Structural</li> </ul> <p><b>USES</b></p> <p>A design pattern provides a general reusable solution to a common design problem</p> <p>They are used for solving common software design problems that occur again and again.</p>
6	<b>Define GRASP. BTL1</b> <p><b>GRASP :</b> General responsibility assignment software patterns (or principles), which consist of guidelines for assigning responsibility to classes and objects in object-oriented design</p>
7	<b>When a pattern is said to be a good pattern? BTL1</b> <p>There is a set of properties that a pattern must fulfill in order to be a good one. A pattern encapsulating: a solution (but not obvious), a proven concept, relationships, and human component</p>
8	<b>Define modular design. (May/June 2016, April/May 2017) BTL2</b> <p>Modular design is a design approach that creates things out of independent parts with standard interfaces</p>
9	<b>Interpret the need of Information Expert. BTL2</b> <ul style="list-style-type: none"> <li>To fulfill the responsibility of knowing and answering the sale's total, three responsibilities were</li> </ul>

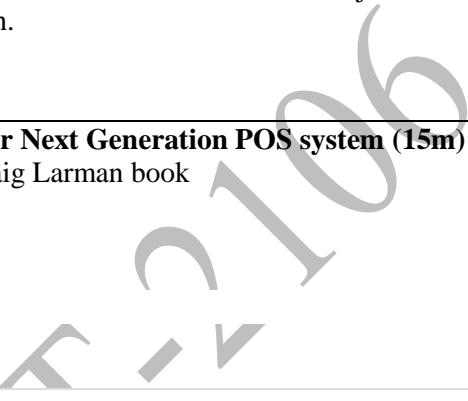
	<p>assigned to three design classes.</p> <ul style="list-style-type: none"> <li>The fulfillment of a responsibility often requires information that is spread across different classes of objects. This implies that there are many “partial experts” who will collaborate in the task</li> </ul>
10	<p><b>Distinguish between coupling and cohesion. (Nov/Dec 2015,2016,April/May 2017) BTL2</b></p> <p><b>Coupling</b> is the indication of the relationships between modules.</p> <p><b>Coupling</b> shows the relative independence among the modules.</p> <p><b>Cohesion</b> is the indication of the relationship within module <b>Cohesion</b> is a degree (quality) to which a component / module focuses on the single thing</p>
11	<p><b>Express the benefits of low coupling. BTL4</b></p> <p>Benefits of low coupling are</p> <ul style="list-style-type: none"> <li>maintainability – changes are confined in a single module</li> <li>testability – modules involved in unit testing can be limited to a minimum</li> <li>readability – classes that need to be analyzed are kept at a minimum</li> </ul>
12	<p><b>Analyze the meaning of coupling and also analyze its types. BTL5</b></p> <p>Coupling is basically a connectivity between various modules. There are two modules, one is the 'calling' module that sends some data to the module connected to it i.e. the 'called' module. Coupling is the interaction of various modules to each other</p> <ul style="list-style-type: none"> <li>Highly Coupled</li> <li>Loosely Coupled</li> <li>No Direct Coupling</li> <li>Data Coupling</li> <li>Stamp Coupling</li> <li>Content Coupling</li> <li>Common Coupling</li> </ul>
13	<p><b>“A system must be loosely coupled and highly cohesive”-Justify. BTL6</b></p> <p>High cohesion within modules and low coupling between modules are often regarded as related to high quality in OO programming languages.</p>
14	<p><b>Compose your views on High Cohesion. BTL3</b></p> <p>It is a measure of the strength of relationship between the methods and data of a class and some unifying purpose or concept served by that class</p>
15	<p><b>Examine the benefits of controller. BTL2</b></p> <p>The controller pattern assigns the responsibility of dealing with system events to a non-UI class that represents the overall system or a use case scenario</p>
16	<p><b>Summarize the list of structural patterns used during design phase of software development. BTL5</b></p> <p>Adapter Pattern. Adapting an interface into another according to client expectation.</p> <p>Bridge Pattern. Separating abstraction (interface) from implementation.</p> <p>Composite Pattern</p> <p>Decorator Pattern</p> <p>Facade Pattern</p> <p>Flyweight Pattern</p> <p>proxy Pattern</p>
17	<p><b>Analyze the situation to use Factory method pattern and its advantages. BTL4</b></p>

	<ul style="list-style-type: none"> <li>The Intent to use Factory method is to define an interface for creating an object, but let subclasses decide which class to instantiate.</li> <li>Factory Method lets a class defer instantiation to subclasses.</li> </ul> <p><b>Advantages:</b></p> <ul style="list-style-type: none"> <li>It hides implementation of an application seam (the core interfaces that make up the application)</li> <li>It easily test the seam of an application (that is to mock/stub) certain parts of your application so you can build and test the other parts</li> <li>Allows to change the design of your application more readily, this is known as loose coupling</li> </ul>
18	<p><b>Discover the Limitations of Factory Pattern BTL3</b></p> <ul style="list-style-type: none"> <li>Makes code more difficult to read as all of your code is behind an abstraction that may in turn hide abstractions.</li> <li>Can be classed as an anti-pattern when it is incorrectly used,</li> <li>Example some people use it to wire up a whole application when using an IOC container, instead use Dependency Injection.</li> </ul>
19	<p><b>Illustrate the benefits of bridge pattern. BTL3</b></p> <ul style="list-style-type: none"> <li>Decoupling of the interface and implementation</li> <li>Improved extensibility</li> <li>Hiding of the implementation details from clients</li> </ul>
20	<p><b>Generalize your view on creator. BTL6</b></p> <ul style="list-style-type: none"> <li>Creational design patterns are design patterns that deal with object creation mechanisms.</li> <li>The basic form of object creation could result in design problems or in added complexity to the design.</li> <li>Creational design patterns solve this problem by somehow controlling this object creation.</li> </ul>
21	<p><b>Point out the interface and domain layer responsibilities. (May/June 2016) BTL4</b></p> <ul style="list-style-type: none"> <li>A UI object retrieves the domain object from a well-known source, such as a factory object that is responsible for creating domain objects.</li> <li>The UI layer should not have any domain logic responsibilities.</li> <li>It should only be responsible for userinterface tasks, such as updating widgets</li> </ul>
22	<p><b>Analyse: How to Choose the Initial Domain Object? BTL4</b></p> <ul style="list-style-type: none"> <li>Choose as an initial domain object a class at or near the root of the containment or aggregation hierarchy of domain objects.</li> <li>This may be a facade controller, such as Register, or some other object considered to contain all or most other objects, such as a Store.</li> </ul>
23	<p><b>Define Responsibilities and Methods. BTL1</b></p> <ul style="list-style-type: none"> <li>The UML defines a responsibility as "a contract or obligation of a classifier".</li> <li>Responsibilities are related to the obligations of an object in terms of its behavior.</li> <li>Basically, these responsibilities are of the following two types: - knowing –doing</li> </ul>
24	<p><b>List out some scenarios that illustrate varying degrees of functional cohesion. BTL1</b></p> <ul style="list-style-type: none"> <li>Very low cohesion</li> <li>low cohesion</li> <li>High cohesion</li> <li>Moderate cohesion</li> </ul>
25	<p><b>Discuss on Fine-Grained Classes? BTL2</b></p> <ul style="list-style-type: none"> <li>Consider the creation of the Credit Card, Drivers License, and Check software objects.</li> <li>Our first impulse might be to record the data they hold simply in their related payment classes, and eliminate such fine grained classes.</li> <li>However, it is usually a more profitable strategy to use them they often end up providing useful</li> </ul>

	<p>behavior and being reusable.</p> <ul style="list-style-type: none"> <li>• <b>For example</b>, the Credit Card is a natural Expert on telling you its credit company type (Visa, MasterCard, and so on). This behavior will turn out to be necessary for our application.</li> </ul>
26	<p><b>What is a Metaphor? BTL1</b> It is an analogy that relates two unrelated things by using one to denote the other.</p>
<b>PART B</b>	
1	<p><b>Explain the design principles in object modeling. Explain in detail the GRASP method for designing objects with example. (13m) (Nov/Dec 2016) BTL4</b></p> <p><b>Answer:</b> pg.no: 271,277,321 in Craig Larman book</p> <p><b>Definition(2m)</b></p> <p>The GRASP patterns are a learning aid to help one understand essential object design, and apply design reasoning in a methodical, rational, explainable way. This approach to understanding and using design principles is based on patterns of assigning responsibilities.</p> <p><b>Explanation(8m)</b></p> <ul style="list-style-type: none"> <li>• The UML defines a responsibility as "a contract or obligation of a classifier"</li> <li>• Basically, these responsibilities are of the following two types: <ul style="list-style-type: none"> <li>• knowing</li> <li>• i doing</li> </ul> </li> </ul> <p>Example: SalesLineItem</p> <p><b>Diagram(3m)</b></p>
2	<p><b>Explain in detail about mapping design to code concepts in detail. (13m) (Nov/Dec 2015) BTL4</b></p> <p><b>Answer:</b> pg.no:371 in Craig Larman book</p> <p><b>Definition(2m)</b></p> <p>The design model can be more or less close to the implementation model depending on how you map its classes to classes or similar constructs in the implementation language</p> <p><b>Explanation(8m)</b></p> <ul style="list-style-type: none"> <li>• Programming and the Development Process</li> <li>• Mapping Designs to Code</li> <li>• Creating Class Definitions from DCDs</li> <li>• Creating Methods from Interaction Diagrams</li> <li>• Container/Collection Classes in Code</li> <li>• Exceptions and Error Handling</li> <li>• Defining the SalemakeLineItem Method</li> </ul> <p><b>Diagram(3m)</b></p>
3	<p><b>What is GRASP? Describe the design patterns and principles used in it. (13m) BTL1</b></p> <p><b>Answer:</b> pg.no: 271 in Craig Larman book</p> <p><b>Explanation(8m)</b></p> <p><b>Diagram(5m)</b></p> <ul style="list-style-type: none"> <li>• General responsibility assignment software patterns (or principles), abbreviated GRASP, consist of guidelines for assigning responsibility to classes and objects in object-oriented design</li> <li>• The different patterns and principles used in GRASP are controller, creator, indirection, information expert, high cohesion, low coupling, polymorphism, protected variations, and pure fabrication.</li> </ul>

4	<p><b>Examine the following GRASP patterns: (i)Creator,(ii).Information Expert, (iii)Low coupling, (iv).High cohesion. (13m) (April/May 2017,May/June 2016) BTL1</b></p> <p><b>Answer:</b> pg.no:281,290,285,283 in Craig Larman book</p> <p><b>Explanation(8m)</b></p> <p><b>Solution</b> Assign class B the responsibility to create an instance of class A</p> <p>if one or more of the following is true:</p> <p>B aggregates an object. .</p> <p>B contains an object. .</p> <p>B records instances of objects. .</p> <p>B closely uses objects. .</p> <p>B has the initializing data that will be passed to A when it is created (thus B is an Expert with respect to creating A).</p> <p>B is a creator of an object.</p> <p>If more than one option applies, prefer a class B which aggregates or contains class A</p> <p><b>Diagram(5m)</b></p>
5	<p><b>(i).Explain about Creator and controller design patterns with example. (13m) (Nov/Dec 2016) BTL4</b></p> <p><b>Answer:</b> pg.no:281,302 in Craig Larman book</p> <p><b>Explanation(8m)</b></p> <p><b>Diagram(5m)</b></p> <p><b>Solution</b></p> <p>Assign class B the responsibility to create an instance of class A if one or more of the following is true: .</p> <p>B aggregates an object. .</p> <p>B contains an object. .</p> <p>B records instances of objects. .</p> <p>B closely uses objects. .</p> <p>B has the initializing data that will be passed to A when it is created (thus B is an Expert with respect to creating A).</p> <p>B is a creator of an object. If more than one option applies, prefer a class B which aggregates or contains class A</p>
6	<p><b>(i).Compare cohesion and coupling (Nov/Dec 2018) with suitable example. (8m) (Nov/Dec 2015) BTL5</b></p> <p><b>Answer:</b> pg.no: 285,290 in Craig Larman book</p> <ul style="list-style-type: none"> <li>• <b>Coupling (4m)</b> is a measure of how strongly one element is connected to, has knowledge of, or relies on other elements.</li> <li>• An element with low (or weak) coupling is not dependent on too many other elements; "too many" is context-dependent, but will be examined. These elements include classes, subsystems, systems, and so on.</li> <li>• <b>Cohesion(4m)</b> (or more specifically, functional cohesion) is a measure of how strongly related and focused the responsibilities of an element are.</li> <li>• An element with highly related responsibilities, and which does not do a tremendous amount of work, has high cohesion. These elements include classes, subsystems, and so on.</li> </ul> <p><b>(ii).Summarize and state the role and patterns while developing system design. (5m) (Nov/Dec 2015) BTL5</b></p> <p><b>Answer:</b> pg.no:153,278 in Craig Larman book</p> <p><b>Explanation(5m)</b></p>

	A pattern is a named problem/solution pair that can be applied in new context, with advice on how to apply it in novel situations and discussion of its trade-offs.
7	<p><b>(i).Generalize your idea on Controller pattern with example (7m) BTL6</b></p> <p><b>Answer:</b> pg.no:302 in Craig Larman book</p> <p><b>Explanation(5m)</b></p> <ul style="list-style-type: none"> <li>• Assign the responsibility for receiving or handling a system event message to a class representing one of the following choices: - Represents the overall system, device, or subsystem (facade controller).</li> <li>• Represents a use case scenario within which the system event occurs, often named Handler, Coordinator, or Session (use-case or session controller).</li> <li>• Use the same controller class for all system events in the same use case scenario.</li> <li>• Informally, a session is an instance of a conversation with an actor.</li> <li>• Sessions can be of any length, but are often organized in terms of use cases (use case sessions).</li> </ul> <p><b>Diagram(2m)</b></p> <p><b>(ii).Generalize the concepts of Façade, session and bloated controller. (6m)</b></p> <p><b>Answer:</b> pg.no:461,308 in Craig Larman book</p> <p><b>Façade(2m):</b></p> <ul style="list-style-type: none"> <li>• The first category of controller is a facade controller representing the overall system, device, or a subsystem</li> <li>• The facade could be an abstraction of the overall physical unit, such as a Register; a class representing the entire software system, such as POSSystem</li> </ul> <p><b>Session(2m):</b></p> <ul style="list-style-type: none"> <li>• A session is an instance of a conversation with an actor.</li> <li>• Sessions can be of any length but are often organized in terms of use cases (use case sessions).</li> </ul> <p><b>Bloated(2m):</b></p> <ul style="list-style-type: none"> <li>• Bloated Controllers: has low cohesion unfocused and handling too many areas of responsibility</li> <li>• The controller performs many of the tasks to fulfill the system event, without delegating the work.</li> </ul>
8	<p><b>Describe about the implementation model (Mapping design to code) and give the NextGen POS program solution. (13m) BTL1</b></p> <p><b>Answer:</b> pg.no:371 in Craig Larman book</p> <p><b>Definition(2m)</b></p> <p>The design model can be more or less close to the implementation model depending on how you map its classes to classes or similar constructs in the implementation language</p> <p><b>Explanation(8m)</b></p> <p>Mapping design to code for NextGen POS program</p> <p><b>Diagram(3m)</b></p>

<b>PART C</b>	
1	<p><b>Create the observer pattern by using your own application and explain the sections of the design pattern. (15m) BTL6</b></p> <p><b>Answer:</b> pg.no: 463 in Craig Larman book</p> <p><b>Definition(2m)</b></p> <ul style="list-style-type: none"> <li>• Observer pattern is used when there is one-to-many relationship between objects such as if one object is modified, its dependent objects are to be notified automatically.</li> </ul> <p><b>Explanation(10m)</b></p> <ul style="list-style-type: none"> <li>• Observer pattern falls under behavioral pattern category.</li> <li>• Observer pattern uses three actor classes.</li> <li>• Subject, Observer and Client.</li> <li>• Subject is an object having methods to attach and detach observers to a client object.</li> <li>• We have created an abstract class Observer and a concrete class Subject that is extending class Observer.</li> <li>• ObserverPatternDemo, our demo class, will use Subject and concrete class object to show observer pattern in action.</li> </ul> <p><b>Diagram(3m)</b></p>
2	<p><b>Develop the foundation code for Next Generation POS system (15m) BTL6</b></p> <p><b>Answer:</b> pg.no: refer notes in Craig Larman book</p> <p><b>Explanation(6m)</b></p> <p><b>Coding(6m)</b></p> <p><b>Diagram(3m)</b></p> <p>Class Payment</p>  <pre> package com.foo.nextgen.domain;  public class Payment  {     private Money amount;      public Payment( Money cashTendered ){ amount = cashTendered; }      public Money getAmount() { return amount; }  } </pre>
3	<p><b>Generalize the design issues in implementation of Singleton pattern. (15m) BTL6</b></p> <p><b>Answer:</b> pg.no: 442 in Craig Larman book</p> <p><b>Explanation(10m)</b></p> <p><b>Diagram(5m)</b></p>

	<ul style="list-style-type: none"> <li>• They deviate from the Single Responsibility Principle</li> <li>• Singleton classes cannot be sub classed.</li> <li>• Singletons can hide dependencies.</li> <li>• Programmers often resort to the idea of Dependency Injection to overcome this problem. When dependency Injection is used, Singleton instance is not retrieved inside the class but is passed through the constructor or a property</li> </ul>
4	<p><b>Explain the GRASP pattern(Creator,Information Expert, Low coupling) by using Monopoly game. (15m) (April/May 2017,May/June 2016) BTL5</b></p> <p><b>Answer:</b> pg.no:271,277 in Craig Larman book</p> <p><b>Explanation(12m)</b></p> <p><b>The Creator pattern</b></p> <p>Name: Creator</p> <p>Problem: Who creates an object A?</p> <p>Solution: Assign class B the responsibility to create an instance of class A if one of these is true</p> <p><b>Information Expert pattern</b></p> <p>Name: Information Expert</p> <p>Problem: What is a basic principle by which to assign responsibilities to an object</p> <p>Solution: Assign a responsibility to the class that has the information needed to respond to it.</p> <p><b>Low Coupling</b></p> <p>Name: Low Coupling</p> <p>Problem: How to reduce the impact of change?</p> <p>Solution: Assign responsibilities so that (unnecessary) coupling remains low. Use this principle to evaluate alternatives.</p> <p><b>Diagram(3m)</b></p>
5	<p><b>Analyze and categories of Design pattern. Analyze the creational pattern by using with Maze game. (15m) BTL4</b></p> <p><b>Answer:</b> pg.no:45,Refer notes</p> <p><b>Diagram(5m)</b></p> <p><b>Explanation(10m)</b></p> <p><b>The Creator pattern</b></p> <p>Name: Creator</p> <p>Problem: Who creates an object A?</p> <p>Solution: Assign class B the responsibility to create an instance of class A if one of these is true</p>

<b>UNIT 5- TESTING</b>	
<b>Object Oriented Methodologies – Software Quality Assurance – Impact of object orientation on Testing – Develop Test Cases and Test Plans</b>	
<b>PART A</b>	
1	<b>Define Software Quality Assurance. BTL1</b> <ul style="list-style-type: none"> <li>• (SQA) is a set of activities for ensuring quality in software engineering processes. It ensures that developed software meets and complies with the defined or standardized quality specifications.</li> <li>• SQA is an ongoing process within the Software Development Life Cycle (SDLC) that routinely checks the developed software to ensure it meets the desired quality measures.</li> </ul>
2	<b>What is TDD? BTL1</b> <ul style="list-style-type: none"> <li>• Test-driven development starts with developing test for each one of the features. The test might fail as the tests are developed even before the development.</li> <li>• Development team then develops and refactors the code to pass the test.</li> </ul>
3	<b>Give the advantages of test driven development. BTL2</b> <ul style="list-style-type: none"> <li>• Writing the tests first requires you to really consider what do you want from the code</li> <li>• Fast feedback</li> <li>• Creates a detailed specification</li> <li>• Reduces time spent on rework</li> <li>• Less time spent in the debugger</li> <li>• Identify the error/problem quickly</li> </ul>
4	<b>Define refactoring. Nov/Dec 2016 BTL1</b> <b>Refactoring</b> is changing a software system by improving its internal structure without changing its external behavior, i.e. it is a technique to restructure the code in a disciplined way
5	<b>List the activities and goals of refactoring. BTL1</b> <ul style="list-style-type: none"> <li>• remove duplicate code</li> <li>• improve clarity</li> <li>• make long methods shorter</li> <li>• remove the use of hard - coded literal constants</li> </ul>
6	<b>Summarize the issues in OO testing. (Nov/Dec 2015) BTL2</b> <ul style="list-style-type: none"> <li>• Basic unit of unit testing</li> <li>• Implication of Encapsulation</li> <li>• Implication of Inheritance</li> <li>• Implication of Genericity</li> <li>• Implications of Polymorphism</li> <li>• Implications for testing processes</li> </ul>
7	<b>Summarize class testing. (Nov/Dec 2018) BTL5</b> <ul style="list-style-type: none"> <li>• <b>Class testing</b> is the base of object-oriented software testing.</li> <li>• It involves three aspects: testing each method, testing the relations among class methods and testing the inheriting relation between class and subclass</li> </ul>
8	<b>Conclude on the need of Integration testing. BTL5</b> <ul style="list-style-type: none"> <li>• <b>Integration Testing</b> is a level of software testing where individual units are combined and tested as a group.</li> <li>• The <b>purpose</b> of this level of testing is to expose faults in the interaction between integrated units. Test drivers and teststubs are used to assist in Integration Testing.</li> </ul>
9	<b>Generalize the need of GUI testing. BTL6</b> <ul style="list-style-type: none"> <li>• <b>GUI testing</b> is the process of testing the system's Graphical User Interface of the Application UnderTest.</li> </ul>

	<ul style="list-style-type: none"> <li>• GUI testing involves checking the screens with the controls like menus, buttons, icons, and all types of bars - toolbar, menu bar, dialog boxes and windows</li> </ul>
10	<p><b>Analyze the need for OO system testing. (Nov/Dec 2018) BTL4</b></p> <ul style="list-style-type: none"> <li>• The aim of System Testing is to ensure that the System will function correctly and properly when all functions/features are bundled as a whole.</li> </ul>
11	<p><b>Differentiate OO integration testing and OO system testing. May/June 2016 BTL2</b></p> <ul style="list-style-type: none"> <li>• <b>System Testing</b> is testing of the software application as a whole to check if the system is complaint with the user requirements.</li> <li>• <b>Integration testing</b> tests the interface between modules of the software application</li> </ul>
12	<p><b>Point out the meaning of unit testing. BTL4</b></p> <ul style="list-style-type: none"> <li>• <b>Unit Testing</b> is a level of software testing where individual units/ components of a software are tested.</li> <li>• The purpose is to validate that each unit of the software performs as designed</li> </ul>
13	<p><b>List the 2 levels of Integration testing. BTL1</b></p> <ul style="list-style-type: none"> <li>• component integration testing</li> <li>• system integration testing</li> </ul>
14	<p><b>Examine on static view on classes. BTL3</b></p> <p>The static view describes the structure of business objects that are sent as message arguments from the sender to the receiver of the message</p>
15	<p><b>Illustrate about Unit testing. BTL3</b></p> <ul style="list-style-type: none"> <li>• Unit Testing is a level of software testing where individual units/ components of a software are tested.</li> <li>• The purpose is to validate that each unit of the software performs as designed.</li> <li>• A unit is the smallest testable part of any software.</li> <li>• It usually has one or a few inputs and usually a single output.</li> </ul>
16	<p><b>Point out the use of atomic system function (ASF). BTL4</b></p> <p><b>Atomic System Function (ASF):</b> is an action that is observable at the system level in terms of port input and output events.</p> <p>It begins with a port input event, traverses one or more MM-Paths, and terminates with a port output event</p>
17	<p><b>Interpret the method/message path (MM-path). BTL2</b></p> <p>An MM-Path in object-oriented software is a sequence of method executions linked by messages.</p>
18	<p><b>Design the 4 controls commonly used in GUI design. BTL6</b></p> <ul style="list-style-type: none"> <li>• Input Controls</li> <li>• Navigational Components</li> <li>• Informational Components</li> <li>• Containers</li> </ul>
19	<p><b>List the types of system modeling BTL1</b></p> <ul style="list-style-type: none"> <li>• Functional modeling</li> <li>• Systems architecture</li> <li>• Business process modeling</li> <li>• Enterprise modeling</li> </ul>
20	<p><b>Summarize about GUI testing BTL5</b></p> <ul style="list-style-type: none"> <li>• GUI testing is the process of ensuring proper functionality of the graphical user interface (GUI ) for a given application and making sure it conforms to its written specifications.</li> <li>• GUI testing processes can be either manual or automatic, and are often performed by third -</li> </ul>

	party companies, rather than developers or end users.
21	<p><b>Define unit. BTL1</b></p> <ul style="list-style-type: none"> <li>• A single, cohesive function</li> <li>• A function which, when coded, fits on one page <math>f</math></li> <li>• The smallest separately compilable segment of code</li> <li>• The amount of code that can be written in 4 to 40 hours</li> <li>• A task in a work breakdown structure</li> <li>• Code that is assigned to one person</li> </ul>
22	<p><b>Define ASF. BTL1</b></p> <ul style="list-style-type: none"> <li>• An Atomic System Function (ASF) is an input port event, followed by a set of MM-Paths, and terminated by an output port event.</li> <li>• An atomic system function is an elemental function visible at the system level.</li> </ul>
23	<p><b>Differentiate Internal and External event BTL4</b></p> <ul style="list-style-type: none"> <li>• <b>External event:</b> It is also known as a system event, is caused by something (for example, an actor) outside our system boundary. SSDs illustrate external events.</li> <li>• <b>Internal event:</b> It is caused by something inside our system boundary. In terms of software, an internal event arises when a method is invoked via a message or signal that was sent from another internal object.</li> </ul>
24	<p><b>Define temporal event. BTL1</b></p> <p>Temporal event is caused by the occurrence of a specific date and time or passage of time. In terms of software, a temporal event is driven by a real time or simulated-time clock.</p>
25	<p><b>List out the types of Events. BTL2</b></p> <ul style="list-style-type: none"> <li>• External event</li> <li>• Internal event</li> <li>• Temporal event</li> </ul>
<b>PART B</b>	
1	<p><b>Describe in detail about coding and testing in OOAD. (13m) BTL1</b></p> <p><b>Answer:</b> pg.no:376 in Craig Larman book</p> <p><b>Explanation(10m)</b></p> <ul style="list-style-type: none"> <li>• Unit Testing for Object-Oriented Systems</li> <li>• Test all features of a class object</li> <li>• Units should be tested in isolation</li> <li>• Test sequences of methods</li> <li>• Inheritance presents problems in testing</li> <li>• Flattened classes</li> <li>• Units</li> <li>• The smallest chunk that can be compiled by itself</li> <li>• A single procedure/function</li> <li>• Something so small it would be developed by one person</li> <li>• Classes and Methods = Units?</li> </ul> <p><b>Diagram(3m)</b></p>
2	<p><b>(i).Discuss in detail about the different types of testing in OOAD. (8m) (May/June 2016) BTL2</b></p>

	<p><b>Answer:</b> pg.no:168, Refer notes</p> <p><b>Functional Testing (4m)</b></p> <p>Test methods as black boxes</p> <p>Tests based on specification</p> <p><b>Structural Testing (4m)</b></p> <p>'Set' and 'Get' methods for attributes</p> <p><b>(ii). Describe the two views of OO unit testing. (5m) BTL2</b></p> <p><b>Answer:</b> pg.no:386 in Craig Larman book</p> <ul style="list-style-type: none"> <li>• <b>UNIT TESTING (5m)</b></li> </ul> <p>Is a level of software testing where individual units/ components of a software are tested.</p> <ul style="list-style-type: none"> <li>• The purpose is to validate that each unit of the software performs as designed.</li> <li>• A unit is the smallest testable part of any software.</li> <li>• It usually has one or a few inputs and usually a single output.</li> <li>• In procedural programming, a unit may be an individual program, function, procedure, etc.</li> <li>• In object-oriented programming, the smallest unit is a method, which may belong to a base/ super class, abstract class or derived/ child class. (Some treat a module of an application as a unit.)</li> </ul>
3	<p><b>(i) Discuss briefly about the issues in OO testing. (7m) (April/May 2017)(Nov/Dec 2018) BTL2</b></p> <p><b>Answer:</b> pg.no:385 in Craig Larman book,</p> <p><b>Issues(7m)</b></p> <ul style="list-style-type: none"> <li>• Many individual units within that module.</li> <li>• Unit testing frameworks, drivers, stubs, and mock/ fake objects are used to assist in unit testing.</li> </ul> <p><b>(ii). Describe the two levels of integration in OO integration testing. (6m) BTL2</b></p> <p><b>Answer:</b> pg.no:169, refer notes</p> <p><b>Integration Testing(6m)</b></p> <ul style="list-style-type: none"> <li>• It is a systematic technique for constructing the program structure while conducting tests to uncover errors associated with interfacing.</li> <li>• The object is to take unit tested modules and build a program structure that has been dictated by design.</li> <li>• Top-down testing,</li> <li>• Bottom-up testing,</li> </ul>
4	<p><b>(i). What is OO testing? (5m) (Nov/Dec 2015) BTL1</b></p> <p><b>Answer:</b> pg.no:385 in Craig Larman book</p> <p><b>Definition(2m)</b></p> <p><b>Explanation(3m)</b></p> <p>In object-oriented systems, testing encompasses three levels, namely, unit testing, subsystem testing, and system testing.</p> <p><b>(ii) Examine in detail about the concepts of OO testing in OOAD(8m)(Nov/Dec 2015) BTL1</b></p> <p><b>Answer:</b> pg.no:385 in Craig Larman book</p> <p><b>Definition(2m)</b></p> <p>The different types of test cases that can be designed for testing object-oriented programs are called grey box test cases. Some of the important types of grey box testing are –</p> <p><b>Explanation(6m)</b></p> <ul style="list-style-type: none"> <li>• <b>State model based testing</b> – This encompasses state coverage, state transition coverage, and state transition path coverage.</li> <li>• <b>Use case based testing</b> – Each scenario in each use case is tested.</li> </ul>

	<ul style="list-style-type: none"> <li><b>Class diagram based testing</b> – Each class, derived class, associations, and aggregations are tested.</li> <li><b>Sequence diagram based testing</b> – The methods in the messages in the sequence diagrams are tested.</li> </ul>
5	<p><b>(i).Briefly summarize about class testing. (7m) BTL5</b>  <b>Answer:</b> pg.no:168,Refer notes  <b>Class Testing(7m)</b></p> <ul style="list-style-type: none"> <li>In unit testing, the individual classes are tested. It is seen whether the class attributes are implemented as per design and whether the methods and the interfaces are error-free.</li> <li>Unit testing is the responsibility of the application engineer who implements the structure.</li> </ul> <p><b>(ii).Explain the implications of Encapsulation and polymorphism. (6m) BTL5</b>  <b>Answer:</b> pg.no:414 in Craig Larman book  <b>Explanation (4)</b>  <b>Encapsulation</b> is a development technique which includes creating new data types (classes) by combining both information (structure) and behaviors, and restricting access to implementation details.  <b>Polymorphism</b> is ability to apply different meaning (semantics, implementation) to the same symbol (message, operation) in different contexts.  <b>Diagram(2m)</b></p>
<b>PART C</b>	
1	<p><b>Explain in detail about the implication of Composition and Encapsulation with the example of Winder shield wiper system. (15m) BTL5</b>  <b>Answer:</b> pg.no:264 in Craig Larman book  <b>Explanation(6m)</b>  Check attributes get set correctly I Initialised to the right value, eg: sizeIndex = [ 31, 28, 31, 30, 31, 30, 31, 31, 30, 31, 30, 30 ]  Find errors in calculation + instead of *  Wrong method calls year.increment() instead of month.increment()  <b>Calculation(6m)</b>  Redundant code  Incorrect boundary values I for (int i = 0; i ≤ 5; i++) VS for (int i = 0; i &lt; 5; i++)  Error Messages  Program efficiency is not so important  <b>Diagram(3m)</b></p>
2	<p><b>Explain in detail about (i) Software Quality Assurance (8m) BTL1</b>  <b>Explanation (8m)</b>  <b>Answer:</b> U-5 Refer Notes pageno.5  <b>(ii) Develop Test cases &amp; Test Plans (7m) BTL2</b>  <b>Explanation (7m)</b></p>

3	<p><b>Analyze the Unit, Integration, and system testing for currency converter application. (15m) BTL4</b></p> <p><b>Answer:</b> pg.no:385 in Craig Larman book</p> <p><b>Explanation(10m)</b></p> <p>The currency converter has the following requirements:</p> <ul style="list-style-type: none"> <li>• The user can input an amount into an input box</li> <li>• The user can select the currency to convert to</li> <li>• When selecting a currency, a flag is displayed for that currency</li> <li>• Clicking a ‘compute’ button outputs the equivalent amount into an output box</li> <li>• There is no limit on the number of conversions that can be performed</li> </ul> <p><b>Diagram(5m)</b></p>
4	<p><b>Develop the foundation code for Next Generation POS system (15m) BTL6</b></p> <p><b>Answer:</b> pg.no:refer notes in Craig Larman book</p> <p><b>Explanation(6m)</b></p> <p><b>Coding(6m)</b></p> <p><b>Diagram(3m)</b></p> <p>Class Payment</p>  <pre> package com.foo.nextgen.domain;  public class Payment  {     private Money amount;      public Payment( Money cashTendered ){ amount = cashTendered; }      public Money getAmount() { return amount; }  } </pre>

**OMD551      BASICS OF BIOMEDICAL INSTRUMENTATION      3 0 0 0****OBJECTIVE**

- To study the methods of recording various bio potentials
- To study how to measure biochemical and various physiological information
- To understand the working of units which will help to restore normal functioning To understand the use of radiation for diagnostic and therapy
- To understand the need and technique of electrical safety in Hospitals

**UNIT I BIO POTENTIAL GENERATION AND ELECTRODE TYPES      9**

The origin of Bio-potentials and its propagation, types of electrodes – surface, needle and microelectrodes and their equivalent circuits, Recording problems – measurement with two electrodes.

**UNIT II BIOSIGNAL CHARACTERISTICS AND ELECTRODE CONFIGURATIONS      9**

Biosignal characteristics – frequency and amplitude ranges, ECG Einthoven's triangle, standard 12 lead system, EEG – 10–20 Electrode system, unipolar, bipolar and average mode, EMG – unipolar and bipolar mode.

**UNIT III SIGNAL CONDITIONING CIRCUIT      9**

Need for Bio-amplifier – Differential Bio-amplifier, Impedance matching circuit, Isolation amplifiers, Power line Interference, Right leg driven ECG amplifier, Band pass filtering.

**UNIT IV MEASUREMENT OF NON-ELECTRICAL PARAMETERS      9**

Temperature, respiration rate, pulse rate measurement, Blood pressure: indirect method – Auscultatory method, direct methods: electronic manometer, systolic and diastolic pressure, Blood flow and cardiac output measurement: indicator dilution method, dye dilution method, Ultrasonic blood flow measurement.

**UNIT V BIO-CHEMICAL MEASUREMENT      9**

Blood gas analyzers and non-invasive monitoring, colorimeter, sodium potassium analyzer, spectrophotometer, blood cell counter, Auto analyzer.

**TOTAL: 45****TEXTBOOKS**

1. Leislie Cromwell, "Biomedical instrumentation and measurement", Prentice Hall of India, New Delhi, 2007.
2. John. G. Webster, "Medical Instrumentation Application and Design", 3<sup>rd</sup> Edition, Wiley India Edition, 2007

**REFERENCES**

1. Khandpur, R.S., "Handbook of Biomedical Instrumentation", TATA McGraw-Hill, New Delhi, 2003.

2. Joseph J.Carr and John M.Brown, "Introduction to Biomedical equipment Technology", John Wiley and Sons, New York, 2004.

JIT-2106

**UNIT I BIO POTENTIAL GENERATION AND ELECTRODE TYPES**

The origin of Bio-potentials and its propagation, types of electrodes – surface, needle and microelectrodes and their equivalent circuits, Recording problems – measurement with two electrodes.

**PART \* A**

<b>Q.No.</b>	<b>Questions</b>
1	<p><b>What is Resting potentials? (MAY 2015)BTL1</b></p> <p>The membrane of excitable cells readily permits the entry of <math>K^+</math> ions and <math>Cl^-</math> ions, while it effectively blocks the entry of <math>Na^+</math> ions. Therefore the concentration of <math>Na^+</math> ions inside the cell becomes much lower than that outside the cell. Since the <math>Na^+</math> ions are positive, the outside cells are more positive than the inside. Thus the charge balance is not achieved. Thus a potential difference is developed across the membrane. This membrane potential caused by the different concentration of ions is called the resting potential of the cell</p>
2	<p><b>What is action potentials? (MAY 2015)BTL1</b></p> <p>When a cell membrane is excited by some form of externally applied energy, the membrane changes its electrical characteristics and begins to allow some of the <math>Na^+</math> ions to enter. The movement of <math>Na^+</math> ions into the cell constitutes ionic current which further reduces the barrier of the membrane to <math>Na^+</math> ions. The net result in <math>Na^+</math> ions rush into the cell and try to balance with the ions outside. At the same time <math>K^+</math> ions present inside the cell try to leave the cell. But they are unable to move as rapidly as <math>Na^+</math> ions. As a result, the cell has a slightly positive potential. This potential is called as action potential</p>
3	<p><b>What is meant by depolarization and repolarisation of a cell? BTL1</b></p> <p><b>Depolarisation:-</b></p> <p>When the impulse reaches the muscle, the polarized condition (-90mv) is altered. i.e., the resting membrane potential is abolished. The interior of the muscle becomes positive and outside becomes negative. This condition is called as depolarization.</p> <p><b>Repolarisation:-</b></p> <p>With in a short period, the muscles obtain the resting electrical potential once again. Interior of the muscle becomes negative and outside becomes positive. So, the polarized state of the muscle is re-established. This process is called as repolarization</p>

4	<p><b>What is absolute refractory period?BTL1</b></p> <p>A short period of time during which the cell cannot respond to any stimuli is called as absolute refractory period. The time period is about 1ms.</p>
5	<p><b>Give the Nernst equation which is used to derive action potentials (or) Write down the nernst equation.</b> BTL1</p> <p>Nernst equation is given as</p> $V_t = - \frac{kT}{q} \ln \left[ \frac{[K^+]_i}{[K^+]_o} \right] = - 94.9 \text{ Mv}$
6	<p><b>What is Half-cell potential? (MAY 2011)BTL1</b></p> <p>A characteristic potential difference established by the electrode and its surrounding electrolyte which depends on the metal, concentration of ions in solution and temperature. The voltage developed at an electrode-electrolyte interface is called as half cell potential or electrode potential.</p>
7	<p><b>What are the different types of electrodes used in bipolar measurement? (MAY 2012)BTL1</b></p> <p>The types of biopotential electrodes are,</p> <ul style="list-style-type: none"> <li>• Surface Electrode</li> <li>• Micro Electrode and</li> <li>• Needle Electrode</li> </ul>
8	<p><b>What is Relative refractory period? BTL1</b></p> <p>The period followed by absolute refractory period is the relative refractory period. During this period another action potential can be triggered, but a much stronger stimulation is required.</p>
9	<p><b>Name few bioelectric signals.BTL1</b></p> <p>Some of the bio electric signals are,</p> <ul style="list-style-type: none"> <li>• ECG (Electrocardiogram)</li> <li>• EEG (Electroencephalogram)</li> <li>• EOG (Electrooculogram)</li> <li>• EMG (Electromyogram)</li> <li>• PCG (Phonocardiogram)</li> </ul>
10	<p><b>What is ECG? (NOV 2012)BTL1</b></p>

	The Electrocardiograph is the instrument by which the electrical activities of the heart are recorded. The graphical registration of electrical activities of the heart is called as Electrocardiogram
11	<b>The contraction of skeletal muscle is termed as what? Give its specifications. (MAY 2014) BTL5</b> The contraction of skeletal muscle is termed as electromyogram (EMG). The EMG signal ranges from 0.1mV to 0.5mV. The frequency components of the EMG signal vary from 20Hz to 10 KHz, which are in the audio range.
12	<b>Define the term Conduction velocity. BTL1</b> The elapsed time 't <sub>1</sub> ' (latency) between the stimulating impulse and muscle's action potential is measured. Now the two electrodes are repositioned with the distance separation as l <sub>2</sub> metres. Among the distances l <sub>1</sub> and l <sub>2</sub> , l <sub>2</sub> < l <sub>1</sub> . The latency is now measured as 't <sub>2</sub> ' seconds. The conduction velocity, v = (l <sub>1</sub> - l <sub>2</sub> ) / (t <sub>1</sub> - t <sub>2</sub> )
13	<b>Enlist the electrodes used for recording EEG. ( MAY 2014)BTL1</b> <ul style="list-style-type: none"> <li>• Scalp electrode,</li> <li>• Sphenoidal electrode,</li> <li>• Nasopharyngeal electrode,</li> <li>• Electrocorticographic electrode,</li> <li>• Intracerebral electrode.</li> </ul>
14	<b>Mention the important bands of frequencies in EEG and their importance. ( MAY 2011)BTL1</b> Alpha waves (8-13)Hz – to monitor the level of consciousness Beta waves (13-30)Hz – to monitor cerebral and mental activity Theta waves (4-8)Hz – to analyse the emotional stress in adults Delta waves (0.5-4)Hz – to study sleep disorders and brain tumour
15	<b>Define Phonocardiogram. (MAY 2011)BTL1</b> The Phonocardiogram is the graphical representation of the sound recording connected with the pumping action of the heart.
16	<b>Differentiate between heart sounds and murmurs.BTL4</b>

	S.No	<b>Heart Sounds</b>	<b>Murmurs</b>
	1	They have transient characteristics	They have noisy characteristics
	2	Short duration	Long duration
	3	Heart sounds are due to the opening and closing of the valves	Murmurs are due to the turbulent flow of blood in the heart and large vessels.
17	<b>Mention the importance of PCG signals. (JUNE 2009)BTL1</b> The presence of higher frequencies (murmurs) in the PCG indicates a possible heart disorder like Rheumatic valvular lesions, murmur of aortic stenosis and murmur of mitral stenosis		
18	<b>Compare the signal characteristics of ECG and PCG. (NOV 2011)( MAY 2013)BTL2</b> <b>Phonocardiogram:</b> A graphic record of heart sounds. <b>Electrocardiogram:</b> A record of the electrical activity of the heart.		
19	<b>Mention the normal amplitude and frequency of EMG signal ( MAY 2011)BTL1</b> The EMG signal ranges from 0.1mV to 0.5mV. The frequency components of the EMG signal vary from 20Hz to 10 KHz and they are restricted to the frequency range of 20Hz to 200Hz for clinical purpose using a low pass filter		
20	<b>What are the electrodes used for recording EMG?( MAY 2016) BTL1</b> The electrodes used for recording EMG are, <ul style="list-style-type: none"> <li>• Surface electrode</li> <li>    Metal Disc electrode, Disposable electrode</li> <li>• Needle electrode</li> <li>    Unipolar and Bi polar electrode</li> <li>• Metal Disc electrode, Disposable electrode</li> </ul>		
21	<b>Define latency in EMG.( NOV 2015). BTL1</b>		

	The elapsed time between the stimulating impulse and muscle's action potential is called latency
22	<p><b>State all or none law.(NOV2016) BTL1</b></p> <p>In nerve and muscle cells, repolarization occurs so rapidly following depolarization that the action potential appears as a spike of 1 ms total duration. But for heart, action potential is from 150 to 300 ms and so it repolarizes much more slowly. When a cell is excited, the action potential is always the same for any given cell. This is known as all- or- nothing law.</p>
23	<p><b>What is meant by conduction velocity? (NOV 2016) BTL1</b></p> <p>Conduction velocity is defined as the rate at which an action potential moves down a fiber or is propagated from cell to cell. It is also called as Nerve conduction rate.</p>
24	<p><b>Draw the electrical equivalent circuit of a surface electrode. BTL1</b></p> <p><b>Fig. electrical equivalent circuit</b></p>

**PART \* B**

**Explain in detail about microelectrodes with suitable diagram.(13M) (Nov/Dec-2016) BTL1**

**Answer: Page 21-Dr.M.ARUMUGAM**

**Biopotential:**

(3M)

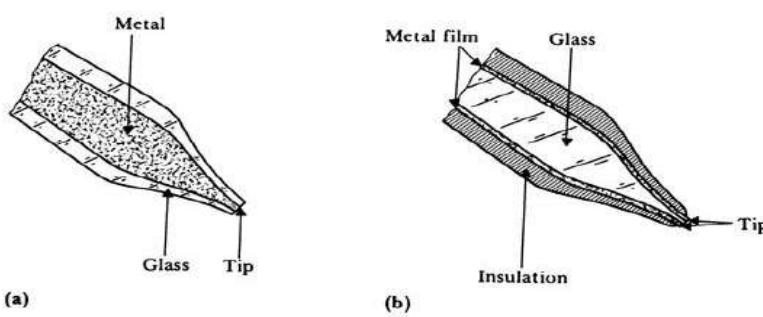
**Types :**

1. Micro Electrodes--- Bio electric potential near or within a single cell
2. Metal Type—Tip must be tungsten or stainless steel
3. Micro pipette---It is a glass micropipet with size of 1 micron, It is filled with electrolyte
4. Skin surface electrode —Measure ECG,EEG,EMG
5. Needle electrode ---Penetrate the skin to record EEG

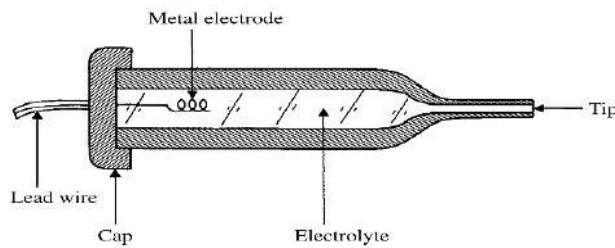
**Microelectrodes:**

(6M)

- Used to measure bio-potential signals at the cellular level
- Due to small dimensions (mm), impedance levels - high
- Soamplifier needs very high input impedance



### Micropipette Electrodes :(4M)



**Explain in detail about PCG.(OR) Explain the origin of different heart sounds.(May/June-2014)(13M)**

BTL1

**Answer: Page 133-Dr.M.ARUMUGAM**

**PCG:**

(2M)**Phonogram.:**

Graphic record of the heart sounds

**Phonocardiogram:** sound - from the heart

**Phonocardiograph :**instrument -measure the heart sounds

**Aim:**pick up the different heart sounds- filter out and to display them (or) record them.

**Heart sounds-** acoustic phenomena resulting from the vibrations of cardiac structures.

2

**Acoustic events-** heart can be divided into two categories

- Heart sounds
- Murmurs

**Heart sounds(2M)**

Four Groups :**1)Valve closure sounds****Ventricular Filling sounds** **3)Valve opening Sounds**

**4)Extra cardiac sounds**

**Physical characteristics of sound**

- Frequency
- Amplitude
- Quality

**Origin of the heart sounds:**

(5M)

four separate heart sounds - during the sequence of one complete cardiac cycle.

**First heart sound:** It is produced by a sudden closure of mitral and tricuspid valves associated with myocardial contraction.

- Timing: The low frequency vibrations occur approximately 0.05 sec after the onset of QRS complex of ECG.
- Duration: 0.1 to 0.12 sec.
- Frequency : 30 – 50 Hz
- Auscultatory area: The first heart sound is best heard at the apex of the mid pericardium.

**Second heart sound:** It is due to the closure of semi lunar valves (ie) the closure of aortic and pulmonary valves

- Timing : T 0.03 – 0.05 sec after the end of T wave of ECG
- Duration : 0.08 – 0.14 sec
- Frequency : 250 Hz
- Auscultatory Area: It is best heard in the aortic and pulmonary areas.

**Third heart sound:** It arises as the ventricles relax and the internal pressure drops well below the pressure in atrium.

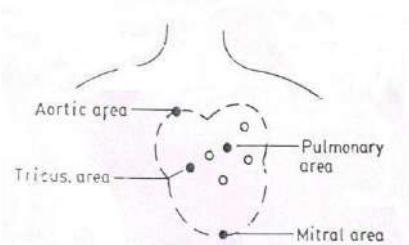
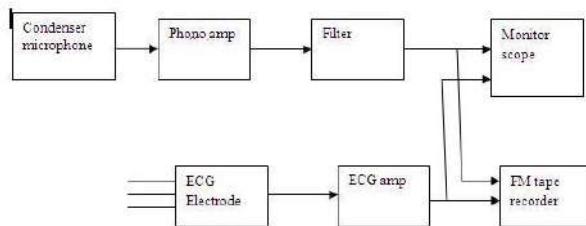
- Duration : 0.04 – 0.08 sec
- Frequency : 10 – 100 Hz
- Auscultatory Area: It is best heard at the apex and left lateral position after lifting the legs.

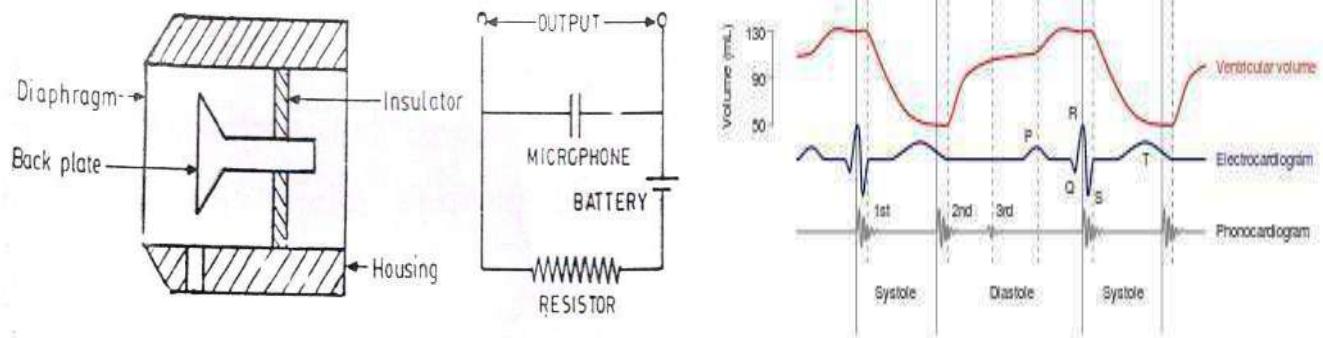
**Fourth heart sound:** Also called as atrial sound. It is caused by an accelerated flow of blood into the ventricles or due to atrial contraction, occurs immediately before the first heart sound.

- Timing : it starts at 0.12-0.18 sec after the onset of p-wave
- Duration :0.03-0.06 sec
- Frequency :10-50 Hz
- Auscultatory Area: Because of its low frequency, it is inaudible

**Heart murmurs**

Murmurs are sounds related to non – laminar flow of blood in the heart and the great

**PCG RECORD SETUP :(4M)**

**Fig. PCG Record Setup****Fig. PCG waveform**

**Explain in detail about unipolar and bipolar electrode with suitable diagram.(13M) (Nov/Dec-2016)**

BTL1

**Answer: Page 21-Dr.M.ARUMUGAM**

**Biopotential:**

(3M)

**Types :**

6. Micro Electrodes--- Bio electric potential near or within a single cell
7. Metal Type—Tip must be tungsten or stainless steel
8. Micro pipette---It is a glass micropipet with size of 1 micron, It is filled with electrolyte
9. Skin surface electrode —Measure ECG,EEG,EMG
10. Needle electrode ---Penetrate the skin to record EEG

**Unipolar electrode**--Single wire inside a needle

(3M)

**Bipolar electrode**--Two wires inside a needle

Mostly used for contacting with internal body tissues

(2M)

(a) Insulated needle electrode .

(2M)

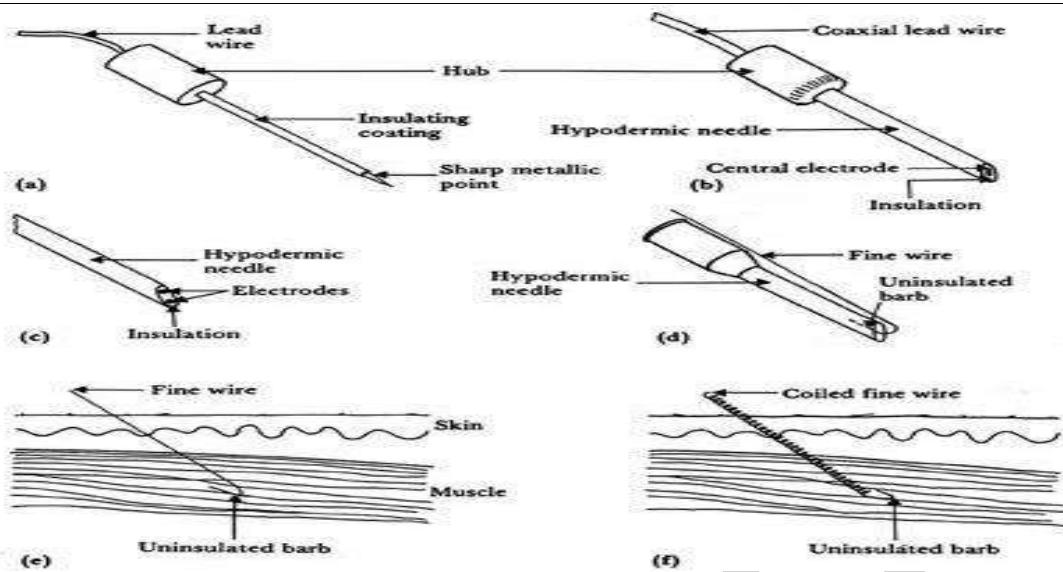
(b) Coaxial needle electrode .

(3M)

(c) Bipolar coaxial electrode .

(d) Fine -wire electrode connected to hypodermic needle, before being inserted .

(e) Coiled fine -wire electrode in place



**Explain in detail about chemical electrode. Describe the measurement of pH of blood using pH meter.(13M) (Nov/Dec-2014) (Nov/Dec-2013)(May/June-2016)BTL1**

**Answer: Page: 21-Dr.M.ARUMUGAM**

**Chemical electrode.**

#### pH Electrode:

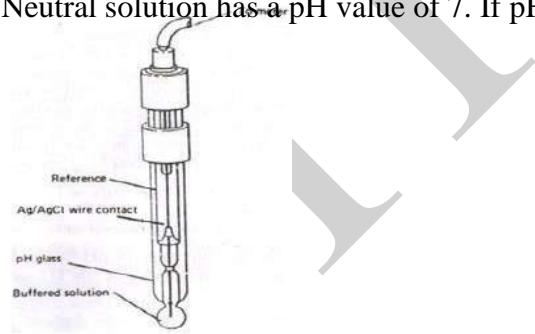
Chemical balance -human body in identified - measurement of pH contentof blood and other body fluids.

PH is defined as the logarithmic of reciprocal of H<sup>+</sup> ion concentrations.

$$PH = \log_{10} 1 / [H^+]$$

$$= - \log_{10} [H^+]$$

Neutral solution has a pH value of 7. If pH < 7, it is acidic, pH >7 it is basic. (2M+2M)



#### PO<sub>2</sub> Electrode:(4M)

The oxygen electrode - piece of platinum wire embedded - insulating glass holder with the end of the wire exposed to the electrolyte solution into which oxygen is allowed to diffuse through the membrane

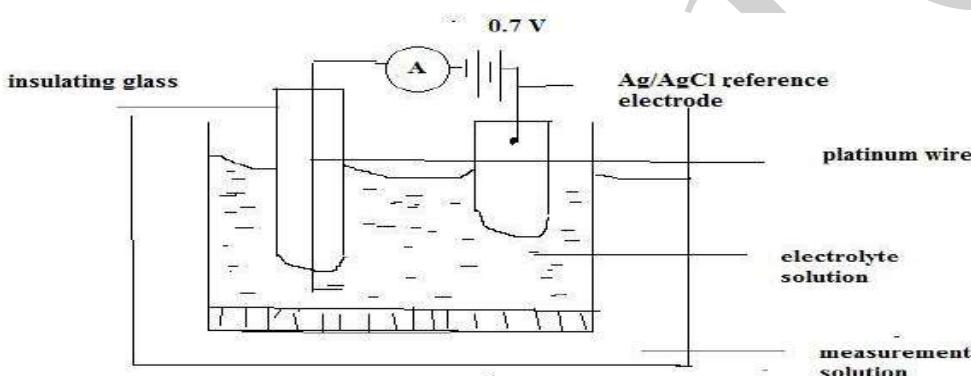
The bottom of the vessel containing electrolyte- membrane permeable to oxygen and the top of vessel is sealed.

Ag - AgCl electrode is used A voltage of 0.7V is applied between the platinum wire and the reference electrode using a battery. The negative of the battery - platinum wire through an ammeter.

Reduction of oxygen takes place at platinum wire. Hence an oxidation-reduction current is developed and is proportional to the partial pressure of oxygen.

#### **Advantages :(1M)**

- The oxygen electrode - monitor the partial pressure of oxygen- biological fluids.
- It is available in integrated version consisting of platinum electrode and reference electrode in the same enclosure called Clark electrode



#### **PCO<sub>2</sub> Electrode:(4M)**

It consists of a standard glass PH electrode covered with rubber membrane permeable to CO<sub>2</sub>. Between the glass surface and membrane there is a thin film of water. The solution under test contains dissolved CO<sub>2</sub> is presented to the outer surface of rubber membrane. After equilibrium PH of aqueous film is measured by glass electrode and interpreted in terms of PCO<sub>2</sub>.

**Explain in detail about surface electrode with suitable diagram.(13M) (Nov/Dec-2016) BTL1**

**Answer: Page 21-Dr.M.ARUMUGAM**

**5 Biopotential: (3M)**

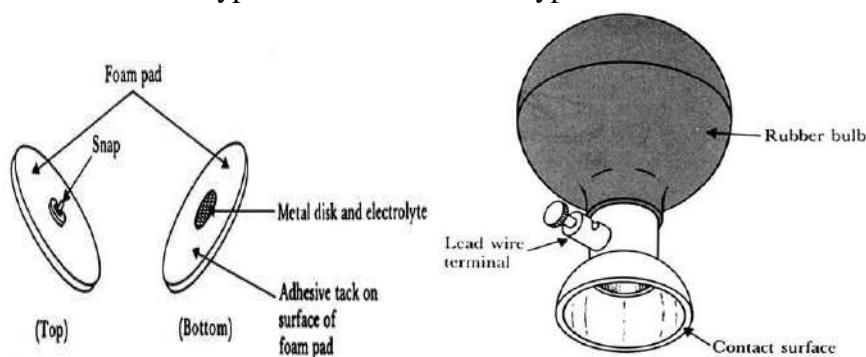
#### **Types :**

11. Micro Electrodes--- Bio electric potential near or within a single cell
12. Metal Type—Tip must be tungsten or stainless steel

13. Micro pipette---It is a glass micropipet with size of 1 micron, It is filled with electrolyte
14. Skin surface electrode —Measure ECG,EEG,EMG
15. Needle electrode ---Penetrate the skin to record EEG

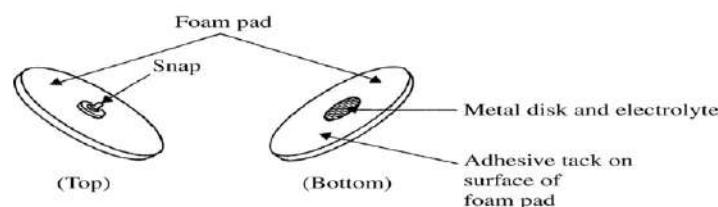
### Surface Electrodes :(5M)

- These are placed in contact with the skin of the subject
- Early stages immersion electrodes were used.
- A bucket of saline water is used
- An improvement of immersion electrode is the plate electrode.
- Another old type electrode is suction type



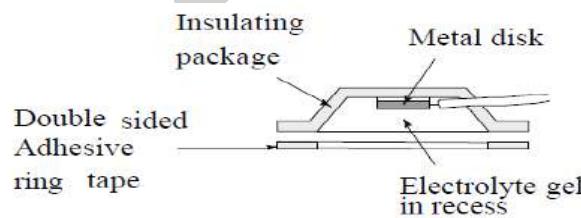
### Metal-Plate Electrodes :(2M)

- consists of a metallic conductor in contact with the skin.
- An electrolyte soaked pad or gel is used to establish and maintain the contact.



### Floating electrodes:(3M)

Conductive paste reduces effect of electrode slippage and resulting motion artifact



### PART\* C

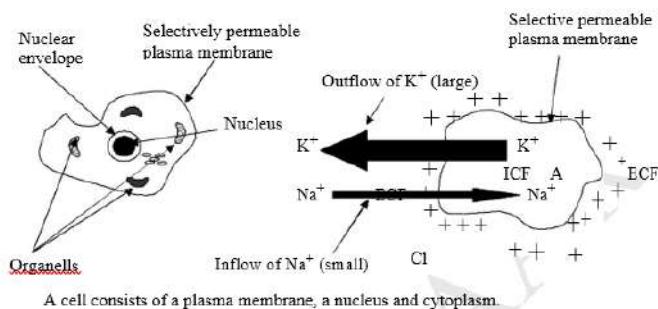
**Discuss in detail about the origin of action potential and resting potential with necessary equation and also draw the action potential wave form.(15M)(Nov/Dec- 2014)(May/June 2016)BTL6**

**Answer: Page4-Dr.M.ARUMUGAM**

**Origin of biopotential:**

Cell is the basic building unit of human body.

**Structure of cell :**(2M)



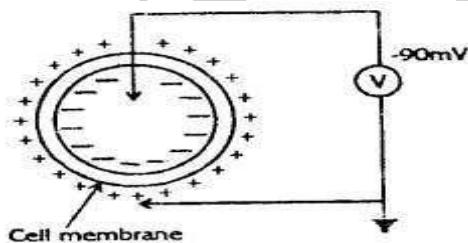
(2M)

**Plasma membrane:** It is selectively permeable to (various ions such as)  $\text{Na}^+$ ,  $\text{K}^+$  and intracellular anions. The fluid inside the plasma membrane called the **intracellular fluid** (ICF). The fluid outside the plasma membrane is called the **extracellular fluid** (ECF). The plasma membrane separates the cell's contents from its surroundings.

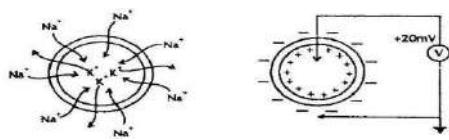
1

**Resting membrane potential:**(4M)

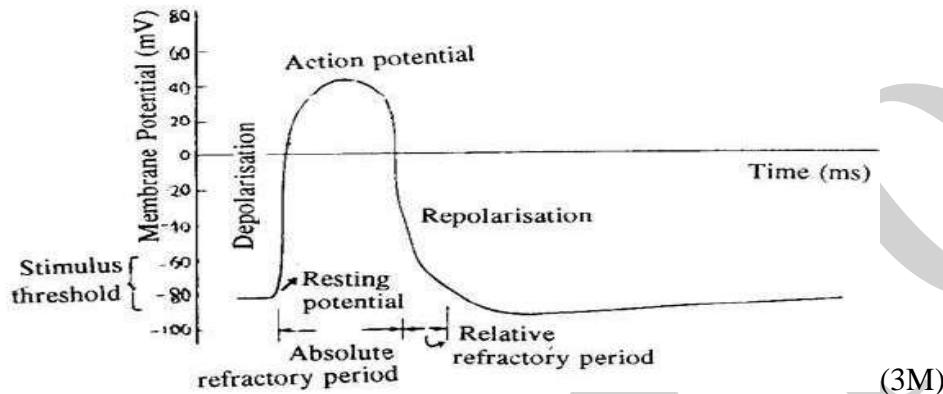
- $\text{Na}^+$  is large in the ECF while  $\text{K}^+$  is large in the ICF.
- When the cell is at rest, the inflow of  $\text{Na}^+$  is very small but the outflow of  $\text{K}^+$  is large.
- Due to these facts, the inside of the cell membrane is more negative than its outside. This leads to a potential difference across the cell membrane called the **resting membrane potential** (RMP). This has a value of 70mV to 90mV.



**Action potential:**(4M)



- When cell is excited, the permeability of the plasma membrane to  $\text{Na}^+$  suddenly increases 600 times greater than that to  $\text{K}^+$  & a sudden large inflow of  $\text{Na}^+$  takes place.
- As the inflow of  $\text{Na}^+$  exceeds the outflow of  $\text{K}^+$  by several times, the membrane potential suddenly decreases from 70mV to zero and then shoots up to 40mV.
- This positive shoot over the neutral level (0mV) is called the action potential. Once generated, the action potential travels down the nerve for a long distance.
- After certain (very short) period, the permeability of the plasma membrane returns to equilibrium conditions causing the membrane potential to return to the resting value i.e., RMP value.



**Absolute refractory period:** During a short period after the generation- actionpotential, the cell does not respond to any stimulus at all-**absolute refractory period**.

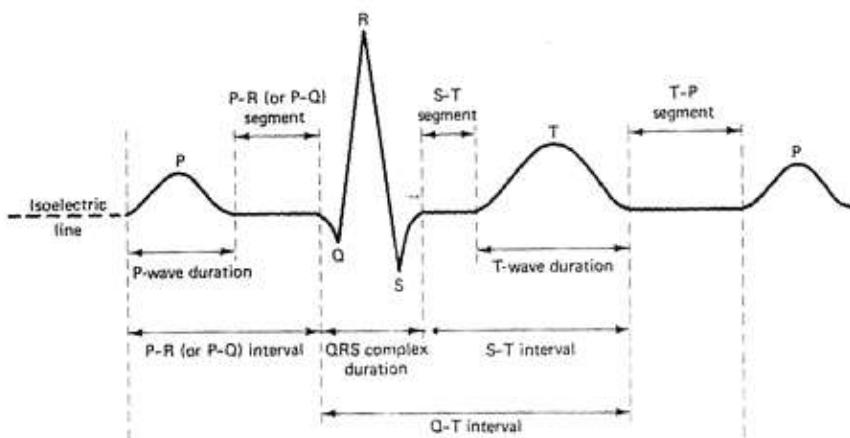
**Relative refractory period:** It is the time period between the instant when themembrane potential becomes negative again and the instant when the membrane potential returns to RMP. During this period, the cell responds to a stimulus but less strongly than usual.

## UNIT II BIOSIGNAL CHARACTERISTICS AND ELECTRODE CONFIGURATIONS

Biosignal characteristics – frequency and amplitude ranges, ECG Einthoven's triangle, standard 12 lead system, EEG – 10–20 Electrode system, unipolar, bipolar and average mode, EMG – unipolar and bipolar mode.

### PART \* A

Q.No.	Questions
1	<b>Draw ECG waveform with specification. (May 2015) BTL 1</b>


**State Beer's law (NOV 2016). BTL1**

A law stating that the concentration of an analyte is directly proportional to the amount of light absorbed, or inversely proportional to the logarithm of the transmitted light. Beer's law

$$A = abc = \log(100/\%T) 2 - \log \%T$$

2

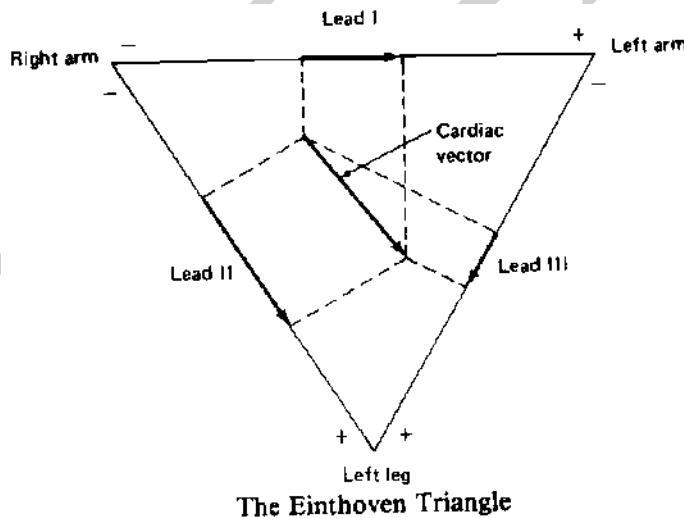
where:

A = absorbance a = absorptivity

b = light path of the solution in cm

c = concentration of the substance of interest

%T = per cent transmittance—the ratio of transmitted light to incident light

**Draw Einthoven's triangle. BTL1**


3

**What is stroke volume?(MAY 2013) BTL1**

It is defined as amount of blood pumped out by each ventricle during each beat.  
Normal value is 70ml.

4

5	<p><b>List out the various EEG signals with amplitude and frequencies. (Or) List the names and frequency bands of EEG signals ( MAY 2011)BTL1</b></p> <p>Alpha waves (8-13)Hz – to monitor the level of consciousness</p> <p>Beta waves (13-30)Hz – to monitor cerebral and mental activity</p> <p>Theta waves (4-8)Hz – to analyse the emotional stress in adults</p> <p>Delta waves (0.5-4)Hz – to study sleep disorders and brain tumour</p>																									
6	<p><b>What are korotk off sounds?BTL1</b></p> <p>In the Blood pressure (BP) measurement, when the systolic pressure exceeds the cuff pressure, then the doctor can hear some crashing, snapping sounds through the stethoscope. These sounds are called as korotkoff sounds.</p>																									
7	<p><b>What is cardiac output? What are the methods of measurement of cardiac output? BTL1 (NOV 2016)(MAY 2015)(NOV 2014)</b></p> <p>Cardiac output is the amount of blood delivered by the heart to the aorta per minute. For normal adult, the cardiac output is 4- 6 liters /min. The cardiac output is measured by using three methods. They are Fick_s Method, Indicator dilation method, Measurement of cardiac output by impedance change.</p>																									
8	<p><b>Give the EMG signal characteristics. BTL 1</b></p> <p>The EMG signal ranges from 0.1mV to 0.5mV. The frequency components of the EMG signal vary from 20Hz to 10 KHz and they are restricted to the frequency range of 20Hz to 200Hz for clinical purpose using a low pass filter</p>																									
9	<p>Give the ECG signal characteristics. BTL 1</p> <table border="1" data-bbox="192 1290 1432 1691"> <thead> <tr> <th>S. No</th> <th>Wave/ Segment</th> <th>Cause</th> <th>Amplitude (mV)</th> <th>Duration (sec)</th> </tr> </thead> <tbody> <tr> <td>1</td> <td>P Wave</td> <td>Depolarisation of atria</td> <td>0.25</td> <td>0.12 to 0.22</td> </tr> <tr> <td>2</td> <td>R Wave (QRS Complex)</td> <td>Repolarisation of atria and Depolarisation of ventricles</td> <td>1.6</td> <td>0.07 to 0.1</td> </tr> <tr> <td>3</td> <td>T Wave</td> <td>Repolarisation of ventricles</td> <td>0.1 to 0.5</td> <td>0.05 to 0.15</td> </tr> <tr> <td>4</td> <td>U Wave</td> <td>Slow repolarisation of intra ventricular (Purkinje fibers) system</td> <td>&lt;0.1</td> <td>0.2</td> </tr> </tbody> </table>	S. No	Wave/ Segment	Cause	Amplitude (mV)	Duration (sec)	1	P Wave	Depolarisation of atria	0.25	0.12 to 0.22	2	R Wave (QRS Complex)	Repolarisation of atria and Depolarisation of ventricles	1.6	0.07 to 0.1	3	T Wave	Repolarisation of ventricles	0.1 to 0.5	0.05 to 0.15	4	U Wave	Slow repolarisation of intra ventricular (Purkinje fibers) system	<0.1	0.2
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10	<p><b>Calculate the stroke volume in millilitres if the cardiac output is 5.2 litres/minute and heart rate is 76 beats/minute. (DEC 2009)BTL3</b></p> <p><math>Q = 5.2 \text{ litres/minute}</math>; <math>HR = 76 \text{ beats/minute}</math></p>																									

	<b>Stroke volume = <math>\frac{Q}{HR} = \frac{5.2 \times 1000}{76} = 68.42 \text{ ml}</math></b>
11	<p><b>What are plethysmographs and plethysmography?(NOV-2005) BTL1</b></p> <p>Plethysmography is the process used to measure the volume changes in any part of the body that result from the pulsations of blood occurring with each heart beat. These measurements are useful in the diagnosis of arterial obstructions and pulse wave velocity measurement which may lead to determine the heart rate. Plethysmograph produces a waveform that is similar to the arterial pressure waveform.</p>
12	<p><b>What is systole and Diastole? BTL</b></p> <p>Systole is the period of contraction of the ventricular muscles to pump the blood out from the ventricles in to the pulmonary artery and the aorta.</p> <p>Diastole is the period of dilation of heart chambers to get filled with blood. (Or) Diastole is the period of relaxation of ventricles to get filled with blood.</p>
13	<p><b>Define tidal volume (MAY 2011)(DEC 2009) BTL1</b></p> <p>Tidal volume (TV) is the volume of gas inspired or expired during each normal, quiet respiration cycle.</p>
14	<p><b>Define residual volume (MAY 2011)(JUNE 2007) BTL1</b></p> <p>Residual volume (RV) is the volume of gas remaining in the lungs at the end of a maximal expiration.</p>
15	<p><b>Name any two methods of respiration rate measurement. (APR 2004) BTL1</b></p> <p>The methods used to measure respiration rate are,</p> <ul style="list-style-type: none"> <li>• Thermistor method</li> <li>• Impedance pneumography</li> <li>• CO<sub>2</sub> method of respiration rate measurement</li> </ul>
16	<p><b>How is the respiration rate measured? (DEC 2011) BTL1</b></p> <p>Respiration rate is measured by one of the method</p> <ul style="list-style-type: none"> <li>• Thermistor method</li> <li>• Impedance pneumography</li> <li>• CO<sub>2</sub> method of respiration rate measurement</li> </ul>
17	<p><b>Write down the demerits of indirect method of blood pressure measurement. (APR 2005) BTL1</b></p> <p>The demerits of indirect method of blood pressure measurement (Sphygmomanometer) are,</p> <ul style="list-style-type: none"> <li>• Does not provide continuous recording of pressure variations.</li> </ul>

	<ul style="list-style-type: none"> <li>• Less repetition rate and</li> <li>• The measured value depends up on the experience of the doctor and his hearing capability.</li> </ul>
18	<p><b>Which transducer is used for measuring temperature? Why?(JUNE 2012) BTL1</b></p> <ul style="list-style-type: none"> <li>• Thermistor</li> <li>• High sensitivity.</li> </ul>
19	<p><b>What is the principle used in pulse rate measurement? (JUNE 2012) BTL1</b></p> <p>Photo electric sensor is used to measure the pulse rate. It consists of light source and LDR. During the contraction of the heart, the blood flow to the finger tip will increase, will reduce the amount of light fall on LDR and during relaxation the amount of light will increase. This change in resistance per minute will be measured as pulse rate.</p>
20	<p><b>How is the pulse rate measured? (MAY 2011) BTL1</b></p> <p>The pulse rate is measured using one of the following methods:</p> <ul style="list-style-type: none"> <li>• Electrical impedance method</li> <li>• Strain gauge method</li> <li>• Photoelectric method</li> <li>• Microphone method</li> </ul>
21	<p><b>List the various indirect methods for measurement of blood pressure.(NOV 2015) BTL1</b></p> <p>Automatic blood pressure measuring apparatus using korotkoff's method.</p> <ul style="list-style-type: none"> <li>• The Rheographic Method.</li> <li>• Differential Auscultatory Technique.</li> <li>• Oscillometric Measurement method.</li> <li>• Ultrasonic Doppler shift method.</li> </ul>
22	<p><b>How does the pH value determine the acidity and alkalinity in blood fluid.( NOV 2015) BTL1</b></p> <p>pH is the measure of Hydrogen ion concentration ,expressed logarithmically. The acidity or alkalinity of a solution depends on its concentration of Hydrogen ions. Increasing the concentration of hydrogen ions makes a solution more acidic, decreasing the concentration of hydrogen ions makes it more alkaline.</p>
23	<p><b>State the different types of test performed using auto analyzer. (MAY 2016) BTL1</b></p> <p>Glucose, BUN, ammonia, bilirubin, uric acid, cholesterol, triglycerides, total calcium, total protein, albumin, creatinine, phosphorus, and serum enzymes</p>

	e.g. Kodak Ektachem
<b>PART*B</b>	
1	<p><b>With a neat block diagram, explain the working of ECG recorder. (13M)</b>  <b>(May/June-2013)(May/June-2014)(Nov/Dec-2014) (Nov/Dec-2016) (May/June-2014)(May/June-2013) (Apr/May 2019)</b></p> <p>BTL1</p> <p><b>Answer: Page 117-Dr.M.ARUMUGAM</b></p> <p><b>Electrocardiography:</b>      Technique -electrical activities of the heart - studied.</p> <p><b>Electrocardiograph:</b>      Instrument -electrical activities of the heart - recorded.</p> <p><b>Electrocardiogram:</b>      Record or graphical registration - electrical activities - heart.</p> <p><b>ECG Recorder (4M)</b></p> <ul style="list-style-type: none"> <li>• Patient cable and Defibrillator Protection Circuit</li> <li>• Lead selector switch</li> <li>• Calibrator</li> <li>• Bio-amplifier</li> <li>• Auxiliary Amplifier</li> <li>• Isolation Power Supply</li> <li>• Output Unit</li> <li>• Power switch</li> </ul>

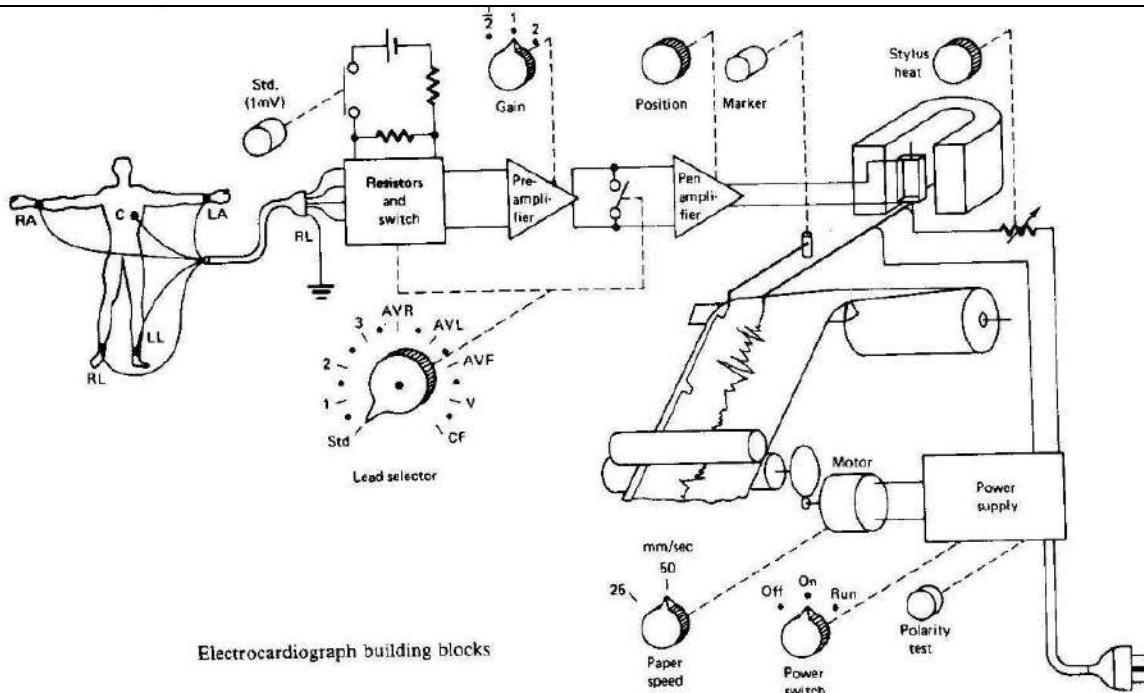


Fig. ECG recorder

(5M)

**With the neat diagram explain the formation of various Lead systems used for recording ECG. Describe the standard 12 lead configuration used in ECG and also describe the typical ECG waveform.(13M)**

(May/June-2013)(May/June-2014)(Nov/Dec-2014) (Nov/Dec-2016) (May/June-2014)(May/June-2013)  
(Apr/May 2019)

BTL1

2

**Answer: Page 117-Dr.M.ARUMUGAM**  
**Electrocardiography:**

Technique -electrical activities of the heart - studied.

(2M)

**Electrocardiograph:**

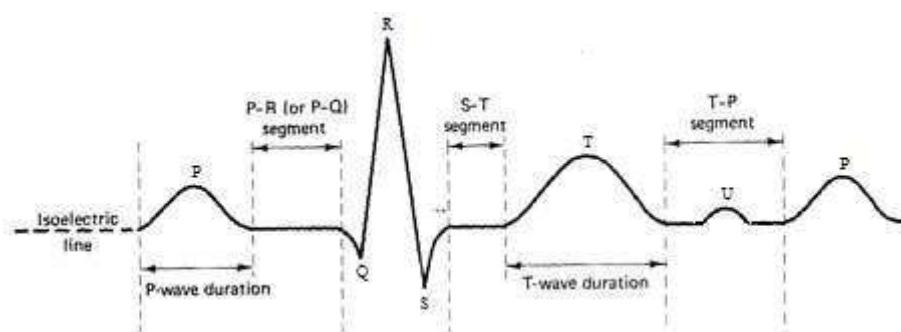
Instrument -electrical activities of the heart - recorded.

**Electrocardiogram:**

Record or graphical registration - electrical activities - heart.

**ECG Wave:** (2M)

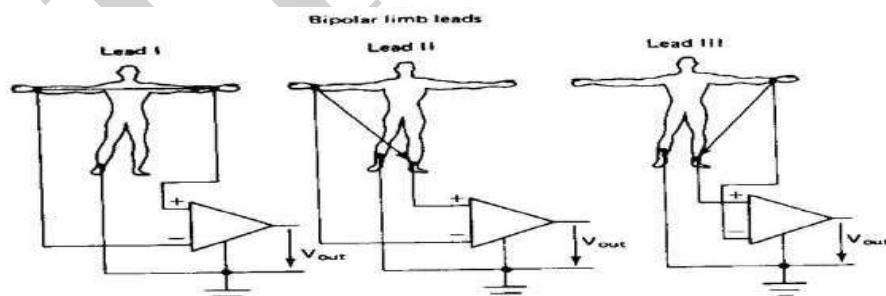
S. No	Wave/ Segment	Cause	Amplitude (mV)	Duration (sec)
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3	T Wave	Repolarisation of ventricles	0.1 to 0.5	0.05 to 0.15
4	U Wave	Slow repolarisation of intra ventricular (Purkinje fibers) system	<0.1	0.2

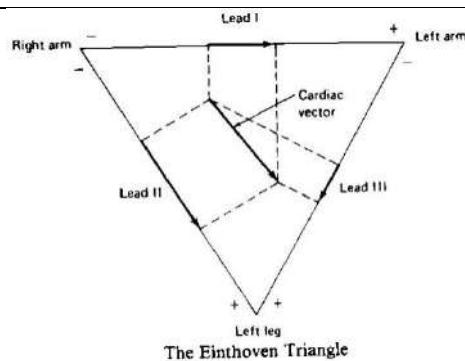
**Fig.ECG waveform****Bipolar limb leads or Standard leads or Einthoven lead system (2M)**

1. Lead I
2. Lead II
3. Lead III

**Augmented unipolar limb lead or Wilson Lead System**

4. aVR
5. aVL 6. aVF

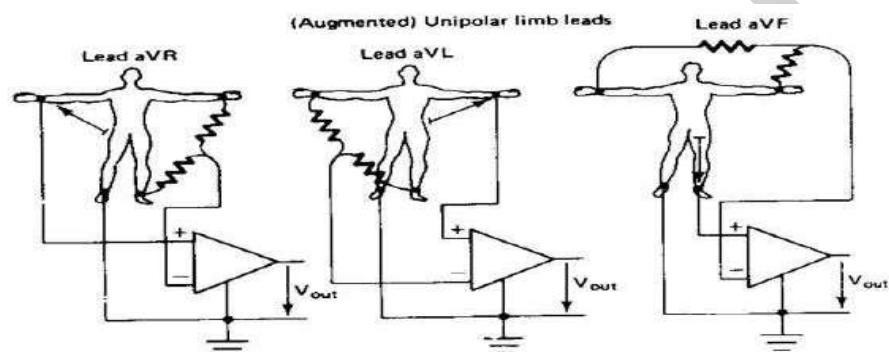
**Unipolar chest leads****Fig. unipolar chest leads****Einthoven Triangle: (1M)**



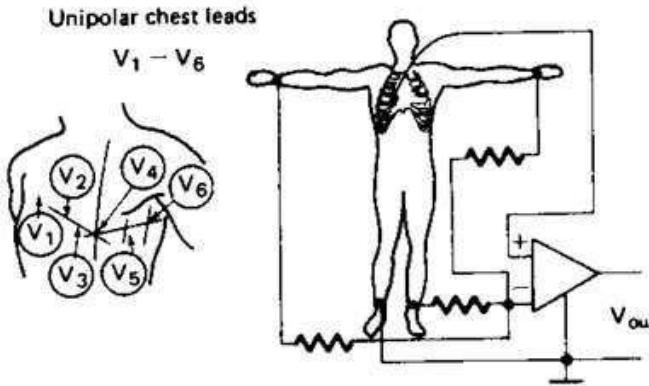
The R wave nominal voltage from different lead is as given below.

Lead I	-	0.53 mv (0.07 – 1.13)mv
Lead II	-	0.71 mv (0.18 – 1.68)mv
Lead III	-	0.38 mv (0.03 – 1.31)mv

### Unipolar Chest Lead: (4M)



- V<sub>1</sub>** Fourth intercostal space, at right sternal margin.
- V<sub>2</sub>** Fourth intercostal space, at left sternal margin.
- V<sub>3</sub>** Midway between V<sub>2</sub> and V<sub>4</sub>.
- V<sub>4</sub>** Fifth intercostal space, at mid-clavicular line.
- V<sub>5</sub>** Same level as V<sub>4</sub>, on anterior axillary line.
- V<sub>6</sub>** Same level as V<sub>4</sub>, on mid-axillary line.



- 3** Draw the block diagram of an EEG unit and explain the different parts in it. Give the origin of brain waves and describe the 10-20 electrode (or) placement of electrode. (or) Discuss the characteristics and frequency bands of EEG signal.(13M) (May/June2016)(Nov/Dec-2013)BTL1

Answer: Page 144-Dr.M.ARUMUGAM

**EEG :(2M)**

**Electroencephalography:** Electrical activities - brain are studied.

**Electroencephalograph:** Instrument - electrical activities- brain are recorded.

**Electroencephalogram:** Record or graphical registration -electrical activities of the brain.

**Significance of EEG:**

EEG - diagnosis of neurological disorders and sleep disorders.

EEG is primarily used for diagnosis including the following

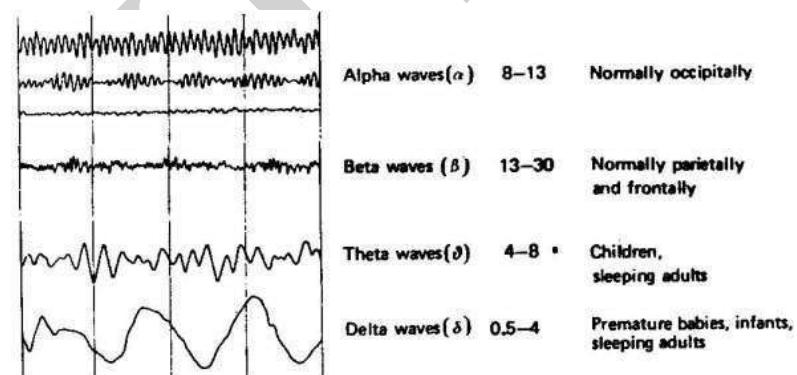
- Helps to detect and localize cerebral brain lesions.
- Aid in studying epilepsy
- Assist in diagnosing mental disorders
- Assist in studying sleep patterns
- Allow observation and analysis of brain responses to sensory stimuli.

**EEG electrodes** transform ionic currents from cerebral tissue into electrical current used - EEG (2M) preamplifier.

**5 types of electrodes are used.**

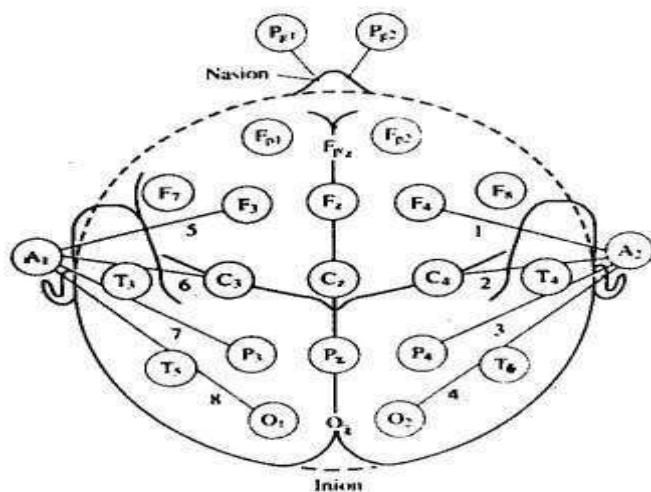
1. **Scalp:** silver pads, discs or cups, stainless steel rods, chlorided silver wires.
2. **Sphenoidal:** Alternating insulated silver and bare wire and chlorided tip inserted through muscle tissue by a needle.
3. **Nasopharyngeal:** Silver rod with silver ball at the tip inserted through the nostril.
4. **Electrocorticographic:** Cotton wicks soaked in saline solution that rests on brain surface.

Intracerebral: sheaves of Teflon coated gold or platinum wires used to stimulate the brain.

**EEG Waves: (2M)**

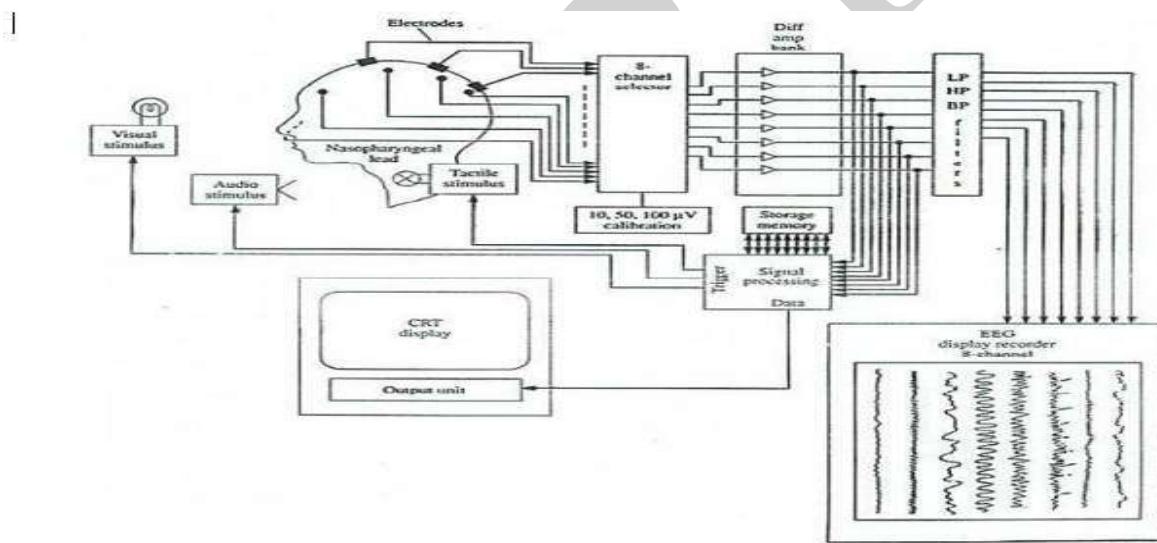
**Fig. EEG Waves**

### Placement of Electrodes: (4M)



**Fig. Placement of Electrodes**

### EEG Recorder: (5M)



**Fig: Modern EEG Unit**

### Analysis of EEG:

- Level of consciousness
- Brain Tumors
- Epilepsy (1)Grandmal 2)Peritmal )

### Application:

- Epilepsy – EEG is very helpful to find acuteness of epilepsy.
- Anesthetic level – It is helpful to find the depth of intensity of anesthesia

- Brain injury – If there is a scar on the cerebral cortex, it creates irritative effect on the nearby healthy cortex. It is identified by EEG waveform.
- Monitor during surgery – Doctor to find patient's conditions.
- Effect of Yoga – Identified by EEG for a normal person initially EEG is recorded.

**Explain in detail about EMG.(13M) (May/June-2013) (May/June-2016) BTL1**

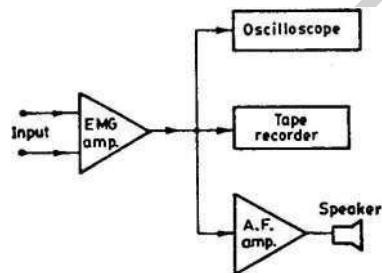
**Answer: Page: 153-Dr.M.ARUMUGAM**

**Electromyography :(2M)**

- Electromyography -recording and interpreting the electrical activity of muscle's action potential.
- The action potentials occur - positive and negative polarities - given pair electrodes
- EMG -like random noise wave form.
- The contraction of a muscle produces action potentials.

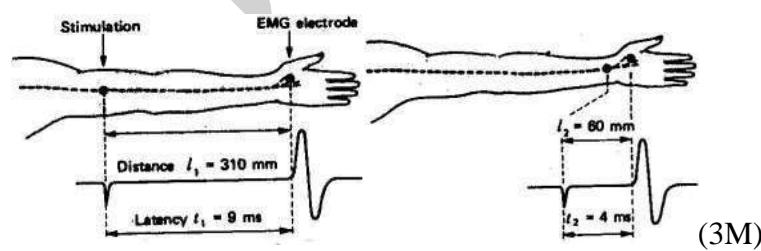
**Recording setup: (8M)**

- surface electrodes or needle electrodes pick-up the potentials produced by the contracting muscle fibers, surface electrodes - from Ag-AgCl and are in disc shape.
- The surface of the skin is cleaned and electrode paste is applied. The electrodes are kept - place by means of elastic bands. So, the contact impedance - reduced below 10 kilo ohms.
- **two conventional electrodes:** bipolar and unipolar type electrodes. In the case of bipolar electrode, the potential difference between two surface electrodes resting on the skin is measured. unipolar electrode, the reference surface electrode - placed on the skin and the needle electrode which acts as active electrode, inserted - muscle. Because of the small contact area, these unipolar electrodes have high impedances from 0.5 to 100 Mega ohms.



**Fig. Recording setup**

**Determination of conduction velocities in motor nerves:**



**Fig. conduction velocity**

	<p>The conduction velocity, <math>v = (l_1 - l_2) / (t_1 - t_2)</math></p> <p>The conduction velocity in peripheral nerves is normally 50 m/s, it's below 40m/s, there is some disorder in that nerve conduction.</p>																									
	<p><b>Describe the typical ECG waveform.(13M)</b></p> <p>(May/June-2013)(May/June-2014)(Nov/Dec-2014) (Nov/Dec-2016) (May/June-2014)(May/June-2013) (Apr/May 2019)</p> <p>BTL1</p> <p><b>Answer: Page 117-Dr.M.ARUMUGAM</b></p> <p><b>Electrocardiography:</b></p> <p>Technique -electrical activities of the heart - studied. (4M)</p> <p><b>Electrocardiograph:</b></p> <p>Instrument -electrical activities of the heart - recorded.</p> <p><b>Electrocardiogram:</b></p> <p>Record or graphical registration - electrical activities - heart.</p> <p><b>ECG Wave: (5M)</b></p>																									
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Part\*C

**With the neat diagram explain the formation of various Lead systems used for recording ECG. Describe the standard 12 lead configuration used in ECG and also describe the typical ECG waveform.(15M)**

(May/June-2013)(May/June-2014)(Nov/Dec-2014) (Nov/Dec-2016) (May/June-2014)(May/June-2013)  
(Apr/May 2019)

BTL1

**Answer: Page 117-Dr.M.ARUMUGAM**

**Electrocardiography:**

Technique -electrical activities of the heart - studied.

(4M)

**Electrocardiograph:**

Instrument -electrical activities of the heart - recorded.

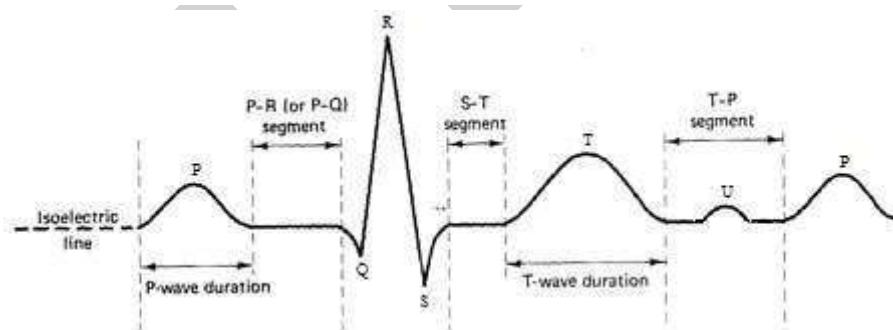
**Electrocardiogram:**

Record or graphical registration - electrical activities - heart.

**ECG Wave: (3M)**

1

S. No	Wave/ Segment	Cause	Amplitude (mV)	Duration (sec)
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4	U Wave	Slow repolarisation of intra ventricular (Purkinje fibers) system	<0.1	0.2



**Fig. ECG waveform**

**Bipolar limb leads or Standard leads or Einthoven lead system (3M)**

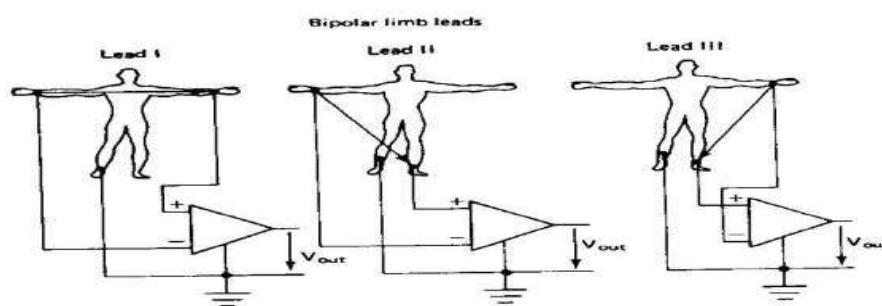
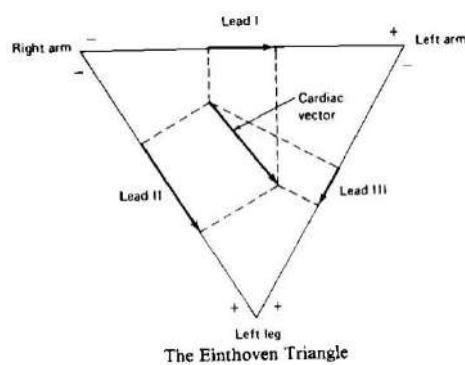
6. Lead I
7. Lead II

## 8. Lead III

**Augmented unipolar limb leador Wilson Lead System**

9. aVR

10. aVL 6. aVF

**Unipolar chest leads****Fig. unipolar chest leads****Einthoven Triangle: (2M)**

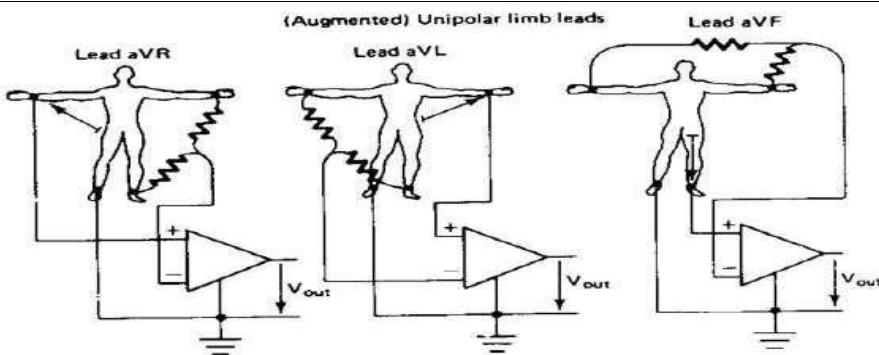
The R wave nominal voltage from different lead is as given below.

Lead I	-	0.53 mv (0.07 – 1.13)mv
--------	---	-------------------------

Lead II	-	0.71 mv (0.18 – 1.68)mv
---------	---	-------------------------

Lead III	-	0.38 mv (0.03 – 1.31)mv
----------	---	-------------------------

**Unipolar Chest Lead: (3M)**



**V<sub>1</sub>** Fourth intercostal space,  
at right sternal margin.

**V<sub>2</sub>** Fourth intercostal space,  
at left sternal margin.

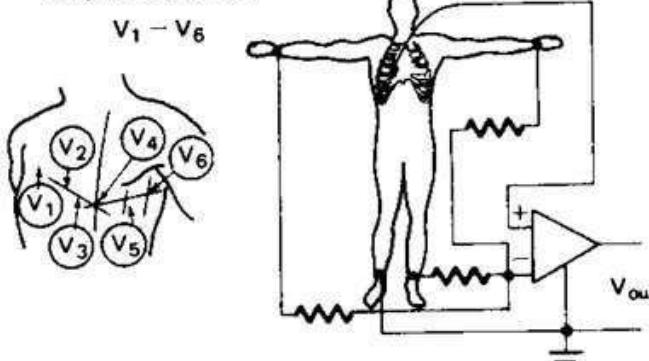
**V<sub>3</sub>** Midway between V<sub>2</sub> and V<sub>4</sub>.

**V<sub>4</sub>** Fifth intercostal space, at  
mid-clavicular line.

**V<sub>5</sub>** Same level as V<sub>4</sub>, on an-  
terior axillary line.

**V<sub>6</sub>** Same level as V<sub>4</sub>, on mid-  
axillary line.

Unipolar chest leads



**Discuss the characteristics and frequency bands of EEG signal and its application.(13M)**  
**(May/June2016)(Nov/Dec-2013)BTL1**

**Answer: Page 144-Dr.M.ARUMUGAM**

**EEG : (4M)**

**Electroencephalography:** Electrical activities - brain are studied.

**Electroencephalograph:** Instrument - electrical activities- brain are recorded.

**Electroencephalogram:** Record or graphical registration -electrical activities of the brain.

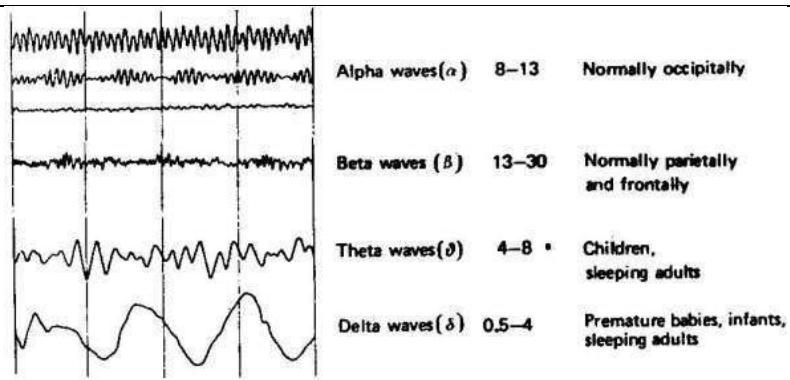
**Significance of EEG:**

EEG - diagnosis of neurological disorders and sleep disorders.

EEG is primarily used for diagnosis including the following

- Helps to detect and localize cerebral brain lesions.
- Aid in studying epilepsy
- Assist in diagnosing mental disorders
- Assist in studying sleep patterns
- Allow observation and analysis of brain responses to sensory stimuli.

**EEG Waves: (6M)**

**Fig. EEG Waves****Application:** (5M)

- Epilepsy – EEG is very helpful to find acuteness of epilepsy.
- Anesthetic level – It is helpful to find the depth of intensity of anesthesia
- Brain injury – If there is a scar on the cerebral cortex, it creates irritative effect on the nearby healthy cortex. It is identified by EEG waveform.
- Monitor during surgery – Doctor to find patient's conditions.
- Effect of Yoga – Identified by EEG for a normal person initially EEG is recorded.

**UNIT III SIGNAL CONDITIONING CIRCUIT**

Need for Bio-amplifier – Differential Bio-amplifier, Impedance matching circuit, Isolation amplifiers, Power line Interference, Right leg driven ECG amplifier, Band pass filtering.

Q.No.	Questions
1	<p><b>List the characteristics needed for bioamplifier (or) What are the requirements of a biological amplifier (MAY 2013), (NOV 2013)( MAY 2016)BTL4</b></p> <ul style="list-style-type: none"> <li>• Gain</li> <li>• Frequency response</li> <li>• Common-mode rejection</li> <li>• Noise &amp; drift</li> <li>• Input impedance</li> <li>• Electrode polarization.</li> </ul>
2	<p><b>Which type of electrode is applied in the case of external stimulation and what is the current range? BTL 1</b></p> <p>The paddle shaped electrodes are applied on the surface of the chest and the current range is 20-150mA.</p>
3	<p><b>Mention the types of pacemaker based on modes of operation of the pacemaker. BTL 1</b></p> <p>Based on modes of operation, the pacemaker are classified into 5 types,</p>

	<p>a) Ventricular Asynchronous pacemaker (Fixed Rate Pacemaker)      b) Ventricular Synchronous pacemaker      c) Ventricular inhibited pacemaker (Demand pacemaker)      d) Atrial synchronous pacemaker (Standby pacemaker)      e) Atrial Sequential ventricular inhibited pacemaker</p>												
4	<p><b>Differentiate between internal and external pacemaker (Or) Distinguish between internal pacemakers and external pacemakers (MAY 2011)BTL 4</b></p> <table border="1"> <thead> <tr> <th>S.No</th><th>External Pacemaker</th><th>Internal Pacemaker</th></tr> </thead> <tbody> <tr> <td>1</td><td>The pacemaker is placed outside the body. It may be in the form of wrist watch or in the pocket, from that one wire will go into the heart through the vein.</td><td>The pacemaker is miniaturized and is surgically implanted beneath the skin near the chest or abdomen with its output leads are connected directly to the heart muscle.</td></tr> <tr> <td>2</td><td>It does not need the open chest surgery</td><td>It requires a minor surgery to place the circuit.</td></tr> <tr> <td>3</td><td>Mostly these are used for temporary heart irregularities</td><td>Mostly these are used for permanent heart damages.</td></tr> </tbody> </table>	S.No	External Pacemaker	Internal Pacemaker	1	The pacemaker is placed outside the body. It may be in the form of wrist watch or in the pocket, from that one wire will go into the heart through the vein.	The pacemaker is miniaturized and is surgically implanted beneath the skin near the chest or abdomen with its output leads are connected directly to the heart muscle.	2	It does not need the open chest surgery	It requires a minor surgery to place the circuit.	3	Mostly these are used for temporary heart irregularities	Mostly these are used for permanent heart damages.
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3	Mostly these are used for temporary heart irregularities	Mostly these are used for permanent heart damages.											
5	<p><b>What is fibrillation? (Or) What is meant by fibrillation?</b>BTL 1</p> <p>The heart is able to perform its important pumping function only through precisely synchronized action of the heart muscle fibres. A condition in which this necessary synchronism is lost is known as fibrillation.</p>												
6	<p><b>Differentiate between internal defibrillator and external defibrillator.</b> BTL 4</p> <table border="1"> <thead> <tr> <th>S.No</th><th>Internal Defibrillator</th><th>External Defibrillator</th></tr> </thead> <tbody> <tr> <td>1</td><td>It is used when the chest is opened</td><td>It is on the chest</td></tr> <tr> <td>2</td><td>Large spoon shaped electrodes are used</td><td>Paddle shaped electrodes are used.</td></tr> <tr> <td>3</td><td>Voltage is in the range of 50 – 1000V</td><td>Voltage is in the range of 1000 – 10000V</td></tr> </tbody> </table>	S.No	Internal Defibrillator	External Defibrillator	1	It is used when the chest is opened	It is on the chest	2	Large spoon shaped electrodes are used	Paddle shaped electrodes are used.	3	Voltage is in the range of 50 – 1000V	Voltage is in the range of 1000 – 10000V
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7	<p><b>Mention the types of defibrillators.</b> BTL 1</p> <p><b>AC defibrillator:</b> Here a current burst of 60Hz with 6A is applied to the chest of patient through appropriate electrode</p> <p><b>DC defibrillator:</b> Here a capacitor is charged to a high DC voltage and then rapidly discharged through electrodes across the chest of the patient.</p>												

8	<p><b>Calculate energy stored in a <math>16\mu\text{F}</math> capacitor of a defibrillator that is charged to a potential of 5000V (dc).BTL 3</b></p> <p>Given: <math>C = 16\mu\text{F}</math>; <math>V = 5000\text{V}</math></p> $E = \frac{1}{2} CV^2 = \frac{1}{2} \times 16 \times 10^{-6} \times (5000)^2 = 200 \text{ Joules.}$
9	<p><b>Classify the defibrillator based on applied voltage.BTL2</b></p> <p>Based on the nature of the voltage applied, the defibrillators can be classified into 6 types.</p> <ul style="list-style-type: none"> <li>• A.C Defibrillator</li> <li>• D.C Defibrillator</li> <li>• Synchronized D.C Defibrillator</li> <li>• Square pulse Defibrillator</li> <li>• Double square pulse Defibrillator</li> <li>• Biphasic D.C Defibrillator</li> </ul>
10	<p><b>Draw the circuit of DC defibrillator and give its output specifications.(MAY 2011) BTL 1</b></p> <p>The wave is <b>monophasic</b> and the peak value of the current is nearly 20 A.</p>
11	<p><b>Draw the defibrillator output waveform and indicate the output energy level. (Or) Draw the circuit of DC defibrillator and give its output specifications.( JUNE 2012)( MAY 2011) BTL 1</b></p> <p>Energy = 400 joules (max)</p>

12	<p><b>When does the need for pacemaker arise? what is its function?.(NOV 2015) BTL 1</b></p> <p>In abnormal situation, if the natural pacemaker i.e Sino-Atrial node ceases to function or becomes unreliable or if the triggering pulse does not reach the heart muscles, the natural and normal synchronization of the heart action gets disturbed which inturn changes the ECG waveform.Hence a pacemaker is needed to regulate the heart rate by giving external electrical stimulation.</p>
13	<p><b>Why are asynchronous pacemakers no longer used? (MAY 2016) BTL 1</b></p> <p>By using this pacemaker ,heart rate cannot be increased to match greater physical effort.</p> <ul style="list-style-type: none"> <li>• If it is fixed in atrium, Atrium beat at a fixed rate.</li> <li>• If ventricle beat at a different rate then it leads to Ventricular Fibrillation.</li> </ul>
14	<p><b>Why do we need a Heart Lung machine? ( MAY 2016) BTL 1</b></p> <p>Cardiopulmonary bypass (CPB) is a technique that temporarily takes over the function of the heart and lungs during surgery, maintaining the circulation of blood and the oxygen content of the patient's body. The CPB pump itself is often referred to as a heart-lung machine or "the pump".</p>
15	<p><b>What is arteriovenous (AV) graft surgery? BTL 1</b></p> <p>Arteriovenous (AV) graft surgery creates a synthetic access point into the body's circulatory system to perform dialysis. Dialysis removes wastes and extra fluid from your blood when the kidneys can no longer perform this function. This is known as kidney failure. AV graft surgery allows blood to flow from your body to the dialysis machine and back into your body after filtering.</p>
16	<p><b>Define heart lung Machine? or What is the need for Heart lung Machine?(MAY 2016) BTL 1</b></p> <p>Cardiopulmonary bypass (CPB) is a technique that temporarily takes over the function of the heart and lungs during surgery, maintaining the circulation of blood and the oxygen content of the body. The CPB pump itself is often referred to as a heart-lung machine or "the pump".</p>
17	<p><b>What is meant by AV fistula and AV graft? BTL 1</b></p> <p>An AV fistula is a direct connection between the patient's artery and one of their nearby veins. This is the absolute BEST access a patient can have because it is all their own tissue. The fistula resists clotting and infection.</p>

	An AV graft (sometimes called a bridge graft) is an indirect connection between the artery and vein, most commonly a plastic tube is used, but donated cadaver arteries or veins can also be used.
18	<p><b>Why asynchronous pacemakers (Fixed rate pacemakers) no longer used? (NOV 2016) BTL 1</b></p> <p>Using fixed rate pacemaker the heart rate cannot be increased</p> <p>Simulation with a fixed impulse frequency results in the ventricles and atria beating at different rates. This varies the stroke volume of heart and causes some loss in cardiac output.</p> <p>Possibility of ventricular fibrillation will be more.</p> <p>There may be competition between the natural heart beats and pacemaker beats.</p>
	<p><b>What is meant by Demand Pacemaker? (NOV2013) BTL 1</b></p> <p>It is a form of artificial pacemaker usually implanted into cardiac tissue because its output of electrical stimuli can be inhibited by endogenous cardiac electrical activity.</p>
<b>PART*B</b>	
1	<p><b>Draw the circuit diagram of an ECG isolation amplifier and explain its operation. (13M)BTL1</b></p> <p><b>Answer: Page: 86-Dr.M.ARUMUGAM</b></p> <p><b>ECG isolation amplifier :(3M)</b></p> <p>The signals from the different leads - LPF. This filtering reduces- interference caused by electron surgery and radio frequency emission. The filter circuit - following by high voltage and over voltage protection circuit so that amplifier can withstand large voltage. Now the signals are fed into lead selected switch and then the output is given to a d.c amplifier.</p> <p style="text-align: right;">(5M)</p>

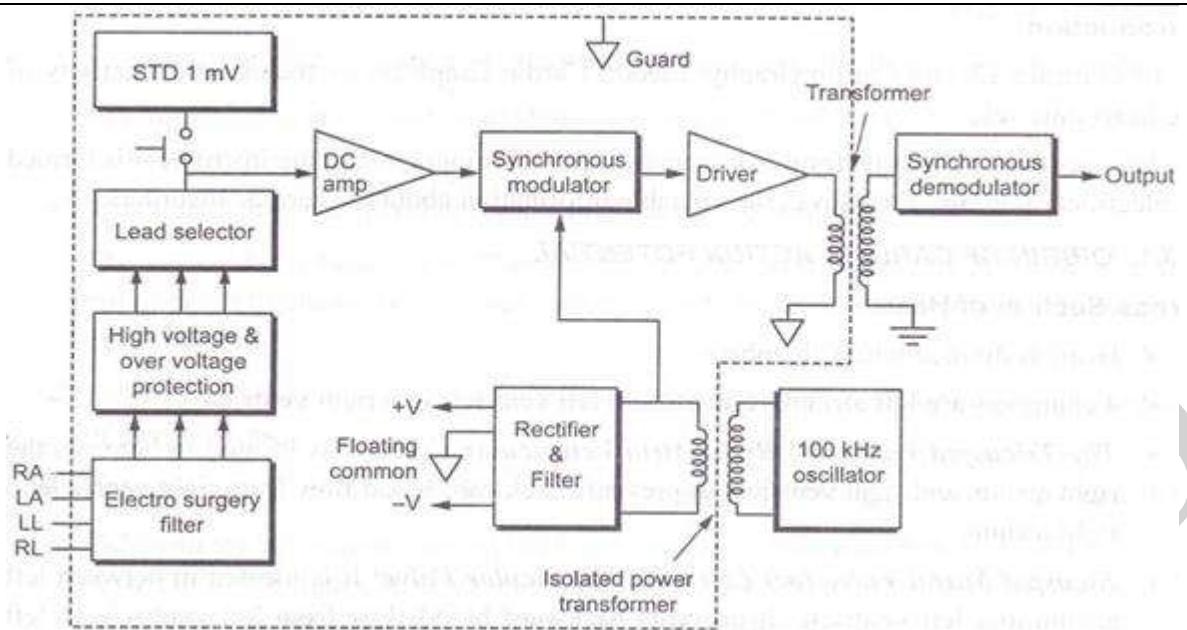


Fig. ECG isolation amplifier

(5M)

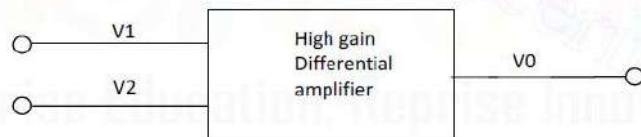
- The d.c amplifier also receives a standard d. c voltage of 1mV through a push button. The primary of an isolated power transformer is connected was 100 KHz oscillator.
- The secondary of that transformer along with rectifier and filter circuits is used to obtain isolated power supply. The synchronous modulator modulates the ECG signal from the d.c amplifier.
- Another transformer is used to deliver the output from driver of modulator to synchronous demodulator. The demodulator output is used as the input f power amplifier.
- The perfect shielding of preamplifier circuit enables to achieve higher CMRR. The line frequency interference is eliminated by introducing a notch filter after power amplifier.

**With neat sketch explain differential Bio-amplifier. BTL 1****Answer: Page: 123-Dr.M.ARUMUGAM**

Basic differential amplifier using BJT

(6M)

2

**Fig. 1.12 Block diagram of Differential amplifier**

Types of operation

Common mode and Differential mode operation

(9M)

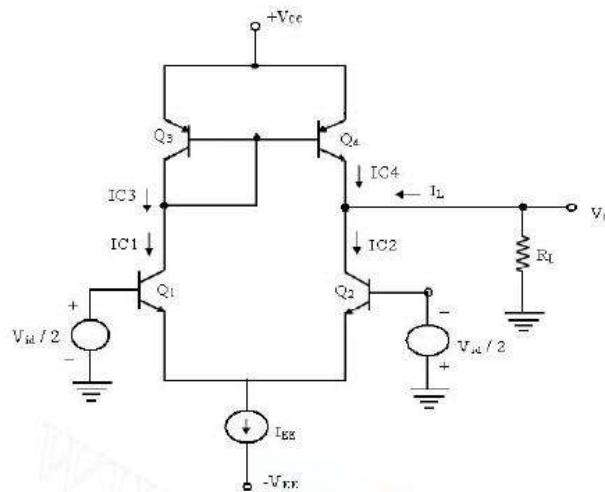


Fig. 1.13 BJT differential amplifier with current mirror active load

**Elaborate the need for implementing bio-amplifier in medical field. (10M) BTL1**

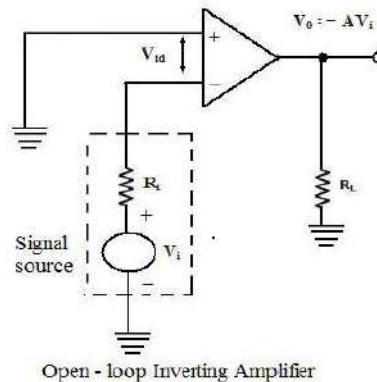
**Answer: Page: 112-Dr.M.ARUMUGAM**

- |   |                           |
|---|---------------------------|
| 3 | High gain (2M)            |
|   | Low Noise (2M)            |
|   | Enhanced accuracy (2M)    |
|   | Easy to implement (2M)    |
|   | Increased efficiency (2M) |

**Draw the inverting and non-inverting bioamplifier circuits of an op-amp in closed loop configuration. Obtain the expressions for the closed loop gain in these circuits. (10M) (BTL2)**

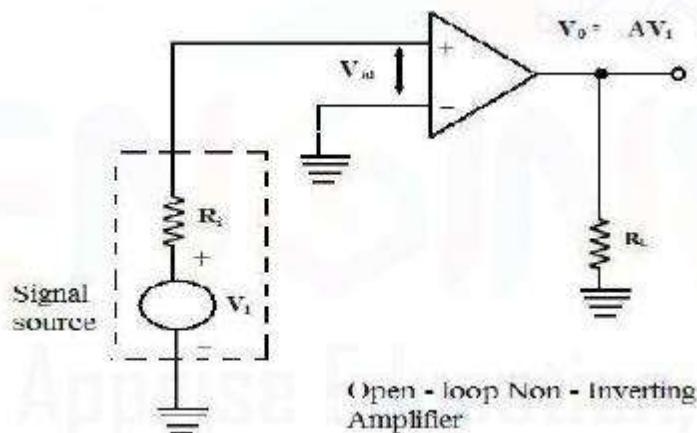
**Answer: Page: 105-Dr.M.ARUMUGAM**

**Inverting amplifier (5M)**



$$A_{CL} = \frac{V_o}{V_i} = -\frac{R_f}{R_1} \text{ where, } A = \text{closed loop gain}$$

**Non – Inverting amplifier (5M)**



$$A_{CL} = \frac{V_o}{V_i} = 1 + \frac{R_f}{R_2} \quad \text{where } A = \text{closed loop gain}$$

**PART \*C**

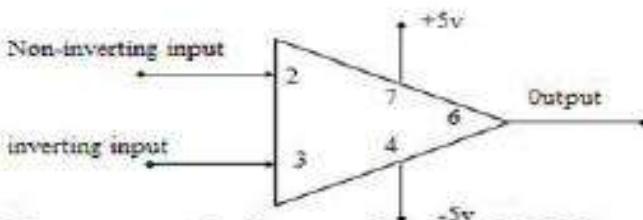
**Explain about Ideal Op-amp in detail with suitable diagrams.(15M) BTL 2**

**Answer: page 41 – 48 LIC D. Roy Choudhury**

**Ideal op-amp**

(6M)

### Op-amp symbol



**Ideal characteristics**

(1M)

**Open loop voltage gain  $A=\infty$**

(2M)

**Input impedance  $R_i = \infty$**

(2M)

**Output impedance  $R_o = 0$**

(2M)

**Bandwidth BW =  $\infty$**

(1M)

**Zero offset  $V_0 = 0$ , when  $V_1=0, V_2=0$**

(1M)

**$V_d = V_1 - V_2$**

**1**

**Explain how electrical hazards can be rectified in hospitals. (OR )**

**Explain the working of ground fault interrupter (10M)(Nov/Dec 2016) BTL1**

**2**

**Answer: Page: 337-Dr.M.ARUMUGAM**

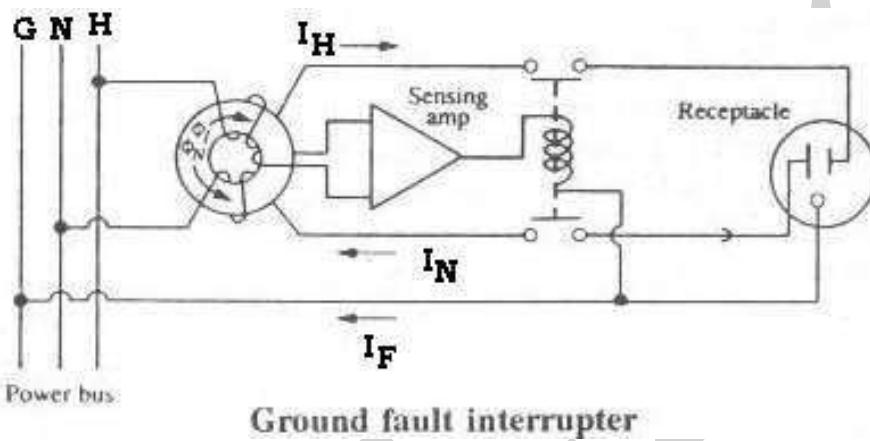
**DEVICES TO PROTECT AGAINST ELECTRICAL HAZARDS: (2M)**

Several devices are available to protect patients and health care workers from hazardous electrical currents. These range from devices to protect against high-voltage macroshock hazards to procedures that minimize the probability that a microshock will occur.

### **Ground Fault Interrupter (GFI): (2M)**

A ground fault interrupter (GFI) protects against a shock that occurs if a person touches the hot lead with one hand and the ground with the other. The GFI opens the power lead if the hot lead current differs by more than approximately 2mA from the neutral lead current for duration of longer than 0.2 second.

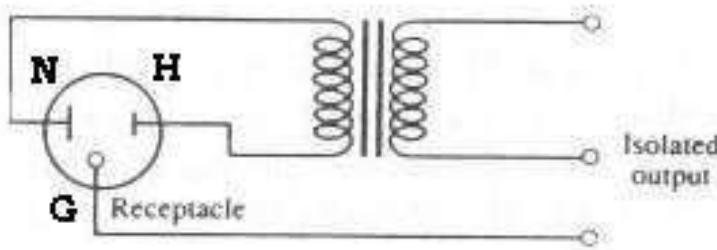
The GFI shown below consists of a magnetic coil on which the hot lead and the neutral lead are wound with the same number of turns, but in opposite directions



**Ground fault interrupter**

### **ISOLATION TRANSFORMER: (2M)**

The isolation transformer provides a second means of protecting against an H-Lead to G-Leadmacroshock. It also prevents sparks when the H lead touches ground, a particularly important protection in an explosive or flammable environment, such as when flammable anesthetics or excessive oxygen is present.

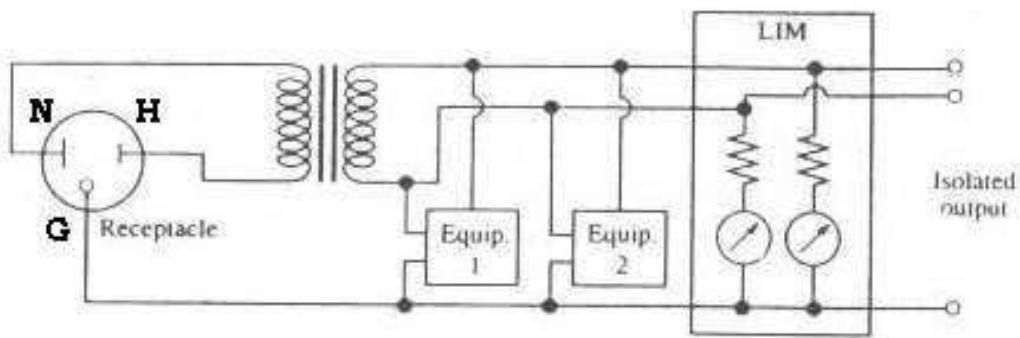


**An isolation transformer**

### **LINE ISOLATION MONITOR:(2M)**

Line isolation monitor (LIM) puts relatively large impedance from either secondary lead through an ammeter to ground of the isolation transformer. If there is a conductive path through the equipment as

shown in Figure below, the meter in the LIM will read a current. The meter on the LIM is calibrated to read what current would flow through a short-circuit fault if it should occur from either secondary to ground. An alarm in the LIM is usually set off when it is calculated that a short-circuit fault between a secondary lead and ground would draw 2 to 5 mA of current. This alarm merely indicates that the backup system has failed and the equipment is no longer isolated.



### **Precautions to minimize Electric shock: (2M)**

The following are the precautions to be taken care to minimize the hazards due to electric shock.

- In the hospitals, use only apparatus with 3 wire power cords.
- Provide isolated input circuits on monitoring equipment.
- Periodically check the ground wire continuity of all equipment.
- Staff should be trained to recognize potentially hazardous conditions.
- The functional controls of the equipment should be clearly marked and the operating instructions must be permanently displayed so that they can be easily familiarized.
- The human assist devices such as pacemaker, ventilators, respirators, dialysers must be properly grounded.
- The mechanical construction of the equipment must be such that the patient or operator should not be injured by the equipment if properly handled.
- The connectors and the probes used in the lab must be standardized to avoid the leakage current which may be picked up by the transducer.
- High voltage and current operating equipment must not be placed where the patient monitoring equipment is connected.
- A potential difference of not more than 5mW should exist between the ground points of one outlet to other outlet.
- The patient equipment ground point must be individually connected to receptacle ground point.

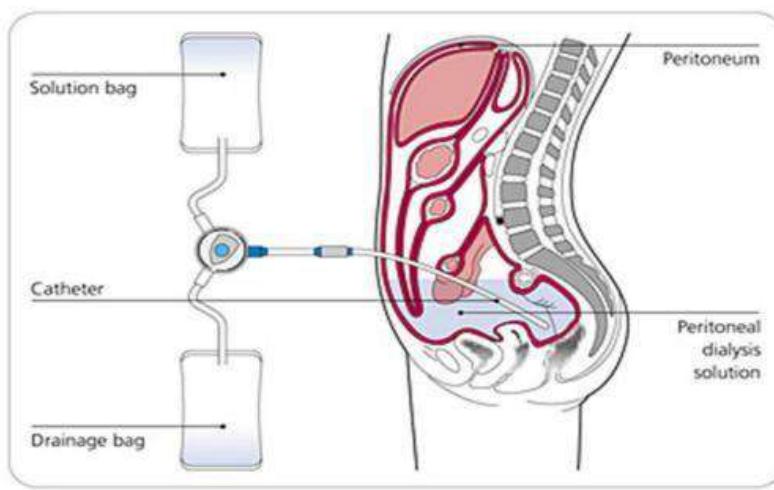
**Discuss in detail about peritoneal dialysis (Nov/Dec 2016) (8M)BTL 6**

**Answer: Page: 211-Dr.M.ARUMUGAM**

### **PERITONEAL DIALYSIS :**

- Peritoneal dialysis (PD) is a treatment for patients with severe chronic kidney disease. This type of dialysis uses the patient's peritoneum in the abdomen as a membrane across which fluids and dissolved substances are exchanged from the blood. Fluid is introduced through a permanent tube in the abdomen and flushed out either every night while the patient sleeps (automatic peritoneal dialysis) or via regular exchanges throughout the day (continuous ambulatory peritoneal dialysis).
- PD is used as an alternative to hemodialysis though it is far less commonly used in many countries, such as the United States.
- It has comparable risks but is significantly less costly in most parts of the world, with the primary advantage being the ability to undertake treatment without visiting a medical facility.
- The primary complication of PD is infection due to the presence of a permanent tube in the abdomen.

3



- A doctor will place a soft tube, called a catheter, in your belly a few weeks before the treatment.
- When the peritoneal dialysis treatment started, dialysis solution of water with salt and other additives flows from a bag through the catheter passed into the belly.
- When the bag is empty, one can disconnect the catheter from the bag and cap it so that the patient can move around and do their normal activities.
- While the dialysis solution is inside the belly, it soaks up wastes and extra fluid from the body. After a few hours, patient drain the used dialysis solution into a drain bag.

- |  |  |
|--|--|
|  | <ul style="list-style-type: none"> <li>Then the used dialysis solution, which is now full of wastes and extra fluid, disposed</li> </ul> |
|--|--|

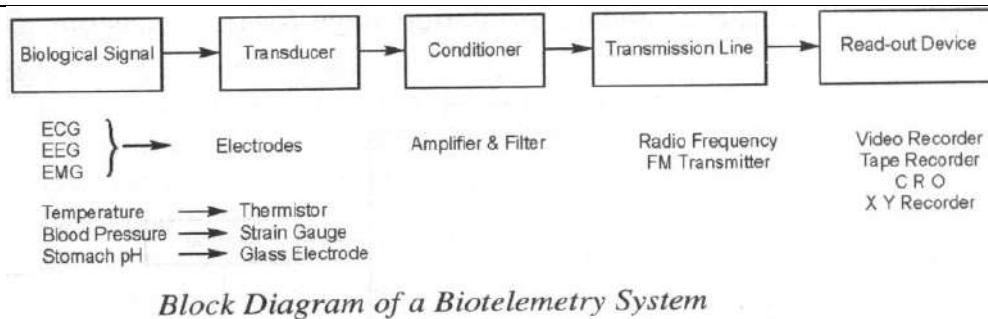
#### **UNIT IV MEASUREMENT OF NON-ELECTRICAL PARAMETERS**

Temperature, respiration rate, pulse rate measurement, Blood pressure: indirect method – Auscultatory method, direct methods: electronic manometer, systolic and diastolic pressure, Blood flow and cardiac output measurement: indicator dilution method, dye dilution method, Ultrasonic blood flow measurement.

#### **PART \*A**

Q.No.	Questions
1	<p><b>What is total lung capacity and vital capacity? BTL1</b></p> <p><b>Lung capacity</b> The total lung capacity is the amount of gas contained in the lungs at the end of maximal inspiration.</p> <p><b>Vital Capacity</b> The vital capacity (VC) is the maximum volume of gas that can be expelled from the lungs after a maximal inspiration.</p>
2	<p><b>What are systolic and diastolic pressures? (NOV2013) BTL1</b></p> <p>The heart pumping cycle is divided into two major parts systole and diastole. Systole is defined as the period of contraction of the heart muscles specifically the ventricular muscle at which time blood is pumped into the pulmonary artery and the aorta.</p> <p>Systolic pressure is 120 mm Hg(average value). Diastole is the period of dilation of the heart cavities as they fill with blood. Diastolic pressure is 80 mm Hg (average value).</p>
3	<p><b>What is cardiac output? What is the value of cardiac output if the stroke volume is 7.ml and heart rate is 70 BPM.(MAY 2016) BTL1</b></p> <p>Cardiac output (Q) = stroke volume (SV) x heart rate (HR)<math>70 \times 70 = 4900</math> ml/minutes</p>
4	<p><b>What is a radio-pill? Mention the application. (MAY-2016) BTL1</b></p> <p>The radio pill is capable of measuring various parameters. With the help of radio pill type devices, it is possible for use to measure or sense temperature, pH, enzyme activity, and oxygen tension values. These measurements can be made in association with transducers. Pressure can be sensed by using variable inductance, temperature can be measured by using temperature-sensitive transducer.</p> <p>Radio is a silicon-coated capsule containing a miniature radio transmitter that can be swallowed by a patient. During its passage through the digestive tract a radio pill transmits information about internal conditions (acidity, etc.).</p>
5	<p><b>What is principle of telestimulation? (NOV-2014)BTL1</b></p> <p>Telestimulation is the measurement of biological signals over long distance.</p>
6	<p><b>Define Let-go current (NOV-2016)BTL1</b></p> <p>Let – go current is the minimum current to produce muscular contraction. For men—about 16mA</p>

	For Women—about 10.5 Ma
7	<b>Define – Micro Shock (NOV-2013) BTL1</b> A physiological response to a current allied to the surface of the heart that results in unnecessary stimulation like muscle contractions or tissue injury is called as micro shock.
8	<b>Define – Macro Shock (NOV 2014) BTL1</b> A physiological response to a current applied to the surface of the body that produces unwanted stimulation like tissue injury or muscle contractions is called as macro shock.
9	<b>What is meant by diathermy? (NOV -2014) BTL1</b> Diathermy is the treatment process by which, cutting coagulation of tissues are obtained.
10	<b>List the types of diathermy. BTL4</b> The types of diathermy are i)Short wave diathermy ii)Microwave diathermy iii)Ultrasonic diathermy iv)Surgical diathermy
11	<b>What are the different types of current that are used for medical applications? BTL1</b> The different types of current are Threshold current, pain current, let-go current, paralysis current, fibrillation and defibrillation current.
12	<b>What are the devices used to protect against electrical hazards? BTL1 (MAY2016) (MAY 2014)BTL1</b> i).Ground fault interrupt ii).Isolation transformeriii) Line isolation monitor
13	<b>What are the application of Bio-Telemetry? (MAY 2013) BTL1</b> The most common usage for biotelemetry is in dedicated cardiac care telemetryunits or step-down units in hospitals. Although virtually any physiological signal could be transmitted, application is typically limited to cardiac monitoring.
14	<b>What are the choices of radio carrier frequency for medical telemetry purpose? (NOV 2016)BTL1</b> The biosignals are amplified to radio frequency range of few hundred KHz to about 300 KHz and then they are transmitted by transmitter antenna's.
15	<b>What is the use of ultrasonic diathermy? ( DEC 2011)BTL1</b> Ultrasonic diathermy can be used to cure few diseases like Neuritis, Arthritis, Skin ulcers
16	<b>Draw the block diagram of Bio-telemetry system.( DEC 2008)BTL1</b>

*Block Diagram of a Biotelemetry System***List the applications of Bio-Telemetry. (MAY 2011)BTL4**

Monitoring ECG even under ergonomic conditions.

17

Monitoring the health of astronauts in space.

Patient monitoring in an ambulance and other locations away from hospital.

Research on unanesthetized animals.

**Mention the advantages of a Bio-telemetry System ( MAY 2011)(JUNE 2009)(JUNE 2007)BTL1**

Major advantage of using biotelemetry is removing the cables from patient and providing a more comfortable medium to patient. Patient needs to carry only a small transmitter.

18

Isolation of patient from high voltage completely. Transmitters in the patient side work with batteries without any danger of electrical shock.

**Differentiate between ‘Macroshock’ and ‘Microshock’ with respect to current applied to heart. BTL4**

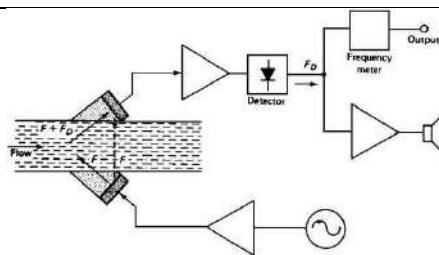
S. No	Micro shock	Macros hock
1	A physiological response to a current applied to the surface of the heart that results in unwanted stimulation like muscle contraction or tissue injury is called micro shock.	A physiological response to a current applied to the surface of the body that results in unwanted stimulation like muscle contraction or tissue injury is called macros hock
2	The current rating is in micro amps	The current rating is in milli amps and Amphere
3	It is introduced due to leakage current, static electricity and interruption of power	This is introduced due to short circuit, improper grounding and using 2 pin sockets

**What are the causes of leakage current? (Or) How do electrical hazards occur due to medical equipments? (DEC 2010)BTL1**

20

- Ungrounded equipment
- Broken ground wire
- Unequal ground potentials

21	<p><b>What is the principle of Diathermy (NOV 2015) BTL1</b></p> <p>In diathermy, a high-frequency electric current is delivered via shortwave, microwave, or ultrasound to generate deep heat in body tissues. The heat can be used to increase blood flow or to relieve pain. Diathermy also can be used as a surgical tool to seal off blood vessels or destroy abnormal cells</p>
	<p><b>PART*B</b></p> <p><b>Explain the working principle of blood flow meter.Discuss about the various methods for determining cardiac output. (May/June-2016)(Nov/Dec-2016) (May/June-2013) (Nov/Dec-2013)(May/June-2013)(13M) (Apr/May 2019)BTL1</b></p> <p><b>Answer: Page: 233 -Dr.M.ARUMUGAM</b></p> <p><b>BLOOD FLOW METERS :(2M)</b></p> <ul style="list-style-type: none"> <li>• Blood flow meters - monitor the blood flow -various blood vessels and to measure the cardiac output .Electromagnetic flow meters, Ultrasonic flow meters and laser base blood flow meters - widely used to measure the blood flow rate. Flow rates are expressed in lit/min or ml/min (cm<sup>3</sup>/min)</li> </ul> <p><b>PRINCIPLE: (2M)</b></p> <ul style="list-style-type: none"> <li>• Electromagnetic induction</li> <li>• Ultrasound transmission or reflection</li> <li>• Thermal convection</li> <li>• Radiographic principles</li> <li>• Indicator (dye or thermal) dilution</li> <li>• Magnetic Blood Flow Meter:</li> </ul> <p>Waveforms used in magnetic blood flow meter and error signals induced by the current</p> <p>(a) Sine Wave      (b) Square Wave      (c) Trapezoidal wave</p> <p><b>Ultrasonic blood flow meter :(2M)</b></p>



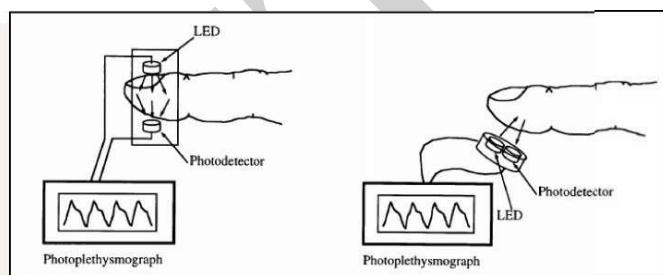
### Thermal Dilution Method :(2M)

- A bolus of chilled saline solution -injected - blood circulation system (right atrium)- decrease in the pulmonary artery temperature- artery puncture is not needed - technique. Several measurements - relatively short time .A standard technique for measuring cardiac output in critically ill patients.

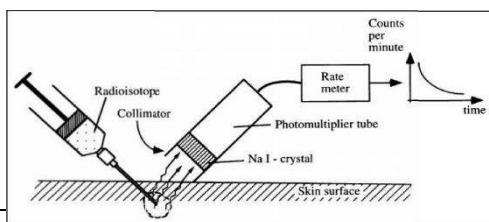
### Photoelectric Method

- A beam of IR-light is directed to the part of the tissue which is to be measured for blood flow (e.g. a finger or ear lobe).

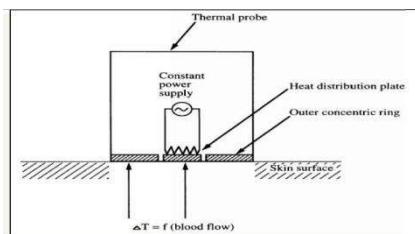
The blood flow modulates the attenuated / reflected light which is recorded. The light that is transmitted / reflected is collected with a photo detector (5M)



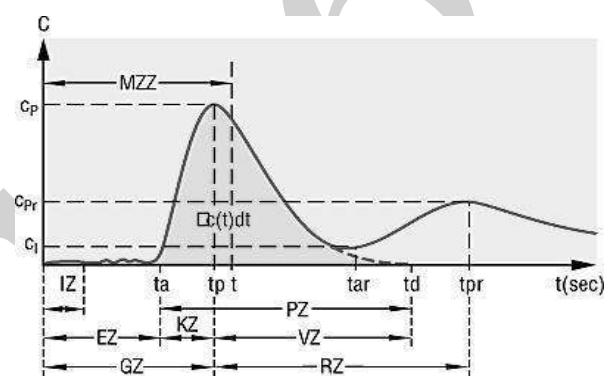
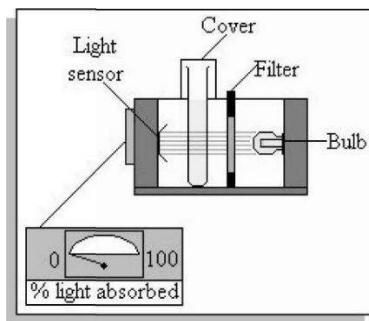
### Radioisotopes



### Thermal Convection Probe



### Indicator Dilution Methods Dye Dilution Method



**How lung volume can be measured? Explain with necessary diagram.(13M)(Nov/Dec-2014) May/June-2016)BTL1**

**Answer: Page: 202-Dr.M.ARUMUGAM**

**LUNG VOLUME :(3M)**

- Ventilation
- Distribution
- Diffusion

2

**Ventilation:**

Ventilation deals with the determination of the ability of body to displace air volume quantitatively and the speed with which it moves the air. Spiro meters are used in the ventilation measurement.

**Distribution:**

It indicate the degree of lung obstructions for the flow of air and also determine the residual volume of air that cannot be removed from the lungs. Pneumotachometers are used to measure the instantaneous rate of volume flow of respiration gases.

**Diffusion.**

It indicate the lung ability to exchange gas with the circulatory system or the rate at which gas is exchanged with the blood stream. Gas analyzers are used in the diffusion measurements.

**Lung volumes and capacities :**

(8M)

Pulmonary function analyzers - determine the lung volumes and capacities. These parameters depend on individuals physical characteristics and condition of breathing mechanism.

TLC – Total Lung Capacity.

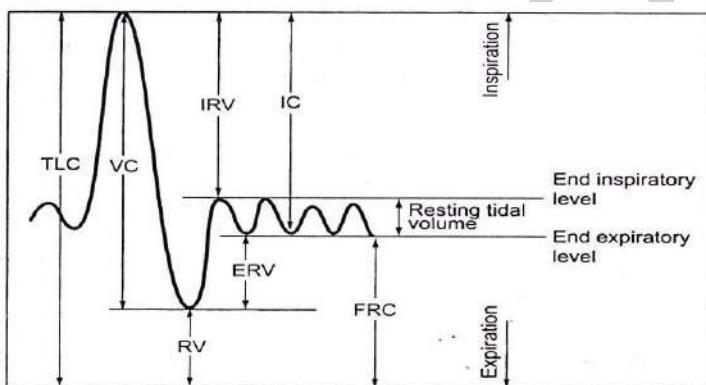
vital capacity (VC) - residual volume (RV).

TV- Tidal Volume

. IRV→ Inspiratory Reverse Volume, E

RV → Expiratory Reverse Volume.

.RV - extra volume



(2M)

IC→ Inspiratory Capacity.

FRC→ Functional Residual Capacity.

FVC → Forced VitalCapacity ,FEC→ Forced Expiratory Volume

FVC is the total amount of air. FEV is the maximum amount of gas.

3	<b>Explain how respiration rate can be measured give its normal values.(13M) (Nov/Dec-2016) (ANY TWO METHOD)BTL1</b>  <b>Answer: Page:43 -REFER NOTES</b>
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### **Measurement of Respiration rate: (2M)**

- Thermistor placed in front of the nostril
- Displacement transducer put across the chest
- Impedance electrodes

The respiratory signal from any one of these transducers is amplified and the time interval is measured between two successive pulses.

The measuring range is 0-50 respiration / minute.

The methods used to measure respiration rate are,

- Thermistor method
- Impedance Pneumography
- CO<sub>2</sub> measurement of respiration rate
- Displacement method

### **Thermistor Method: (2M)**

- thermistor - placed in front of the nostrils by means of a suitable holding device to detect the difference in temperature between the inspired and expired air.
- Since the inspired air passes through the lungs and respiratory tract, its temperature is increased while coming out. This change in temperature is detected by using thermistor.
- Incase the difference in temperature of the outside air and expired air is small, the thermistor can be initially heated to an appropriate temperature and the variation of its resistance in synchronous with the respiration rate can be detected
- thermistor - placed as part of a voltage dividing circuit or in a bridge circuit whose unbalance signal can be amplified to obtain the respiration rate.

### **Displacement Method: (2M)**

- During each respiratory cycle, the thoracic volume changes. These changes can be sensed by means of displacement transducer.
- The transducer is held by an elastic band which goes around the chest.
- The respiratory movement results in resistance changes of the strain gauge element connected as one arm of a wheatstone bridge circuit. Bridge output varies with chest expansion and yields signals corresponding to respiratory activity.
- Changes in the chest circumference can also be detected by a rubber tube filled with mercury. The tube is fastened firmly around the chest

- During inspiration, the chest expands and the rubber tube increases in length and the resistance of the mercury from one end of the tube to the other end changes. The change in resistance can be measured by sending a constant current through it and measured in terms of change in voltage during each respiratory cycle.

### Impedance Pneumography: (3M)

Impedance Pneumograph is based on the fact that the impedance across the chest changes during each respiratory cycle.

low voltage 50 to 500KHz AC signal is applied to the chest of the patient through surface electrodes and the modulated signal is detected.

High value fixed resistors are connected in series with each electrode to create a constant AC current source. The signal voltage applied to the differential AC amplifier is the voltage drop across the resistance representing patient's thoracic impedance.  $E_o = I \cdot (R \pm \Delta R)$

Where,

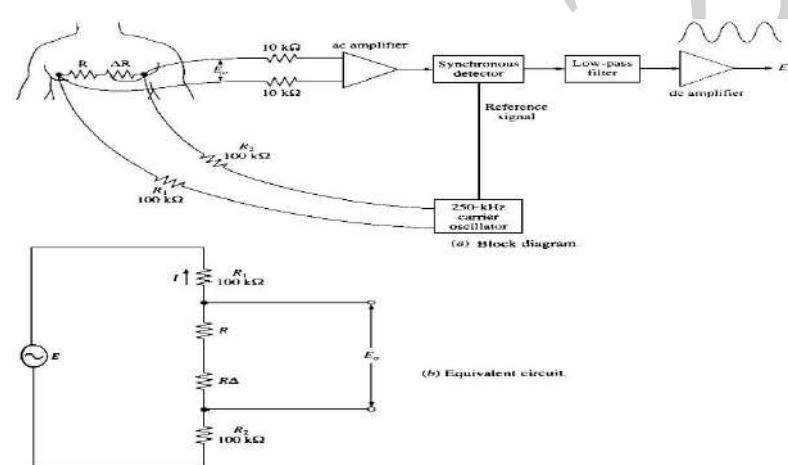
$E_o$  – Output potential in volts.

$I$  – Current through the chest in amps.

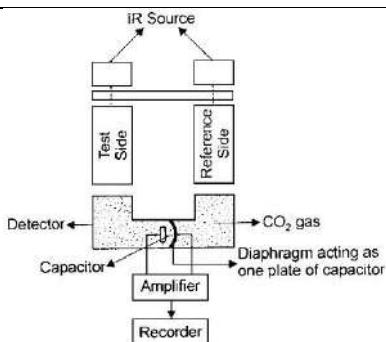
$R$  – Chest impedance without respiration in ohms.

$\Delta R$  – Change of chest impedance caused by respiration in ohms.

(6M)



**CO<sub>2</sub> method of respiration rate measurement:** Respiration rate can also be measured by continuously monitoring the CO<sub>2</sub> contained in the subject's alveolar air.



When infrared rays are passed through the expired air containing a certain amount of CO<sub>2</sub> some of the radiations are absorbed by it. There is a proportional loss of heat energy associated with the rays.

The detector converts this heat loss of the rays into an electrical signal. This signal is used to obtain the average respiration rate.

Two beams of equal intensity of infrared radiations from the infrared source fall on one half of each of the condenser microphone assembly.

The infrared rays from the infrared source are chopped at 25 KHz by the chopper motor. A disc is connected to the spindle of the chopper motor.

The detector has two identical portions separated by a thin flexible metal diaphragm. One is called test side and the other is called as reference side.

The detector is filled with a sample of pure CO<sub>2</sub>. Because of absorption of CO<sub>2</sub> in the analysis cell, the beam falling on the test side of the detector is weaker than that falling on the reference side.

The gas in the reference side would be heated more than that on the analysis side. As a result, the diaphragm is pushed slightly to the analysis side of the detector.

The diaphragm forms one plate of the capacitor.

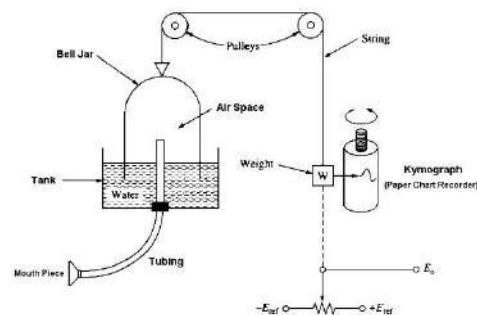
The voltage developed across the diaphragm is amplified, shaped and suitably integrated to give the respiration rate.

### **Spirometer:**

Conventional spirometer is shown in figure below. This instrument uses a bell jar, suspended from above, in a tank of water. An air hose leads from a mouthpiece to the space inside of the bell above the water level. A weight is suspended from the string that holds the bell in such a way that it places a tension force on the string that exactly balances the weight of the bell at atmospheric pressure.

When no one is breathing into the mouthpiece, the bell will be at rest with a fixed volume above the water level. But when the subject exhales, the pressure inside the bell increases above atmospheric pressure causing the bell to rise. Similarly, when the patient inhales, the pressure inside the bell decreases. The bell will rise when the pressure increases and drop when the pressure decreases.

The change in bell pressure changes the volume bell, which also causes the position of the counterweight to change. We may record the volume changes on a piece of graph paper by attaching a pen to the counterweight or tension string.



### Bell-Jar mechanical Spirometer

The chart recorder is a rotary drum model called a kymograph. It rotates slowly at speeds between 30 and 2000 mm/min.

Some spirometers also offer an electrical output that is the electrical analog of the respiration waveform. Most frequently the electrical output is generated by connecting the pen and weight assembly to a linear potentiometer.

If precise positive and negative potentials are connected to the ends of the potentiometer, then the electrical signal will represent the same data as the pen.

**Explain about blood pressure measurement.(OR)Explain the principle of Sphygmomanometer. (13M)(Nov/Dec-2016) (Nov/Dec-2013)(May/June-2013)BTL1**

**Answer: Page: 43 -REFER NOTES**

### BLOOD PRESSURE MEASUREMENT :

Pressure is defined as force per unit area  $p = F / A$  (2M)

P = pressure in Pascal, F= force,

A=Area

3

Pressure - increased by increasing the applied force or by decreasing the area.

**Hydrostatic pressure:** If the force in a system under pressure is not varied then pressure is known as Hydrostatic pressure

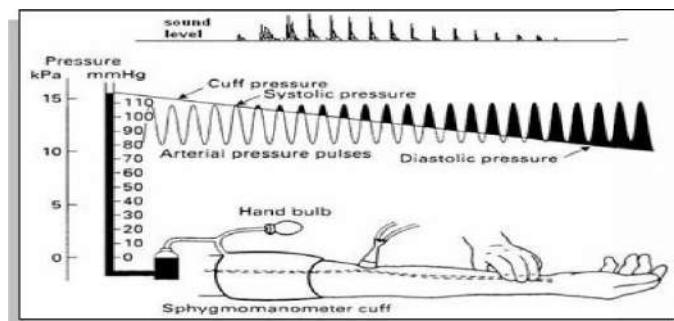
**Hydrodynamic pressure:** If the force in a system under pressure is varied then pressure is known as Hydrodynamic pressure

### Methods :

- Indirect method using sphygmomanometer(2M)

- Direct method

### Indirect method using sphygmomanometer:(4M)



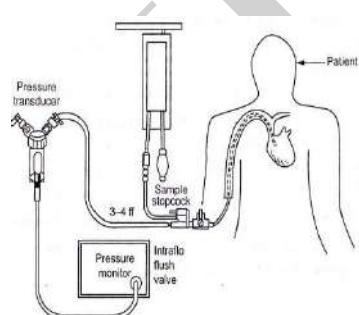
Then doctor slowly reduces the pressure in the cuff & he watch the mercury column when the systolic pressure exceeds the cuff pressure. Then doctor can hear some crashing, snapping sound through stethoscope -korotkoff sound.

Korotkoff sound - vanished when the pressure drops below the diastolic pressure. Pressure reading in the mercury column during onset of korotkoff sound is noted as systolic pressure usually 120 mmHg. Pressure reading - mercury column at which korotkoff sound - disappeared is noted as diastolic pressure usually 80 mmHg for normal persons. Korotkoff sound is disappeared at some point. That is known as muffling.

### Advantages :

- Method is very simple
- Painless techniques
- There is no hazardous surgical procedure involved. Disadvantages
- Effective result depend on the fact how accurately doctor read pressure values when koratkoff sound is heard.

### Direct method:



### Probe used in Direct blood pressure measurement:(3M)

Catheter tip probe sensor mounted at the tip of the probe. Pressure exerted on the tip is converted to the corresponding electrical signal. In fluid filled catheter type. Pressure exerted on the fluid filled column is transmitted to external transducer. This transducer converts pressure in to electrical signal.

	<p><b>Direct method of blood pressure measurement:</b></p> <p>Here fluid filled catheter is used. Before inserting catheter into blood vessel, fluid filled system should be completely flushed out. Usually sterile saline is used for this purpose. Because blood clotting is avoided.</p> <p>M2 reading = peak systolic value - peak to peak pressure value.</p>
5	<p><b>Explain the working of temperature measurement?(8M)BTL1</b></p> <p><b>Answer: Page: 47-REFER NOTES</b></p> <p>The variation in the temperature is a direct result of the variation in blood pressure. The metabolic rate and temperature have a close relation.</p> <p>Body temperature is one of the indicators of a person being normal.</p> <p>Basically two types of temperature measurement can be obtained from the human body</p> <ul style="list-style-type: none"> <li>• Systemic</li> <li>• Skin surface</li> </ul> <p><b>Systemic Temperature: (4M)</b></p> <p>Systemic temperature is the temperature of the internal regions of the body. This temperature is maintained by balancing the heat generated by the active tissues of the body (muscles &amp; Liver) and the heat lost by the body to the environment.</p> <p>Systemic temperature is measured by using temperature sensing devices placed in mouth, under the armpits or in the rectum.</p> <p>The normal oral (mouth) temperature of a healthy person is 37°C. The normal under arm temperature of a healthy person is 36°C and The normal rectum temperature of a healthy person is 38°C.</p> <p>The systemic body temperature can be measured more accurately at the tympanic membrane in the ear.</p> <p>Even for the healthy person, the temperature will not be constant. It will vary about 1 to 1 ½ °C in the early morning compared to the late afternoon.</p> <p>The temperature control center for the body is located deep within the brain. Here the temperature of the blood is monitored and its control functions are coordinated.</p> <p>If the surrounding temperature is warm, then the body is cooled by perspiration due to secretion of the sweat glands and by increased circulation of blood near the surface. The body acts as a radiator.</p> <p>If the surrounding temperature becomes too low, then the body conserves heat by reducing the blood flow near the surface to the minimum required for maintenance of the cells. At the same time metabolism is increased.</p> <p><b>Surface of Skin temperature: (4M)</b></p>

Surface or skin temperature is a result of a balance but here the balance is between the heat supplied by blood circulation in the local area and the cooling of that area by conduction, radiation, convection and evaporation. Thus skin temperature is a function of the surface circulation, environmental temperature, air circulation around the area from which the measurement is to be taken and perspiration.

To obtain a meaningful skin temperature measurement, it is usually necessary to have the subject remain with no cloth covering the region of measurement in a fairly cool ambient temperature.

### **Measurement of systemic Body temperature:**

#### **Mercury Thermometer:**

Mercury thermometer is the standard method of temperature measurement.

Mercury thermometer is used where continuous recording of temperature is not required.

Mercury thermometers are inexpensive, easy to use and sufficiently accurate.

#### **Electronic Thermometer:**

Now-a-days electronic thermometers are available as a replacement of mercury thermometer. IT has disposable tip and requires only less time for reading and also much easier to read the value.

Electronic thermometers are used where continuous recording and accuracy of the temperature is necessary.

Two types of electronic temperature sensing devices are found in biomedical applications. They are,

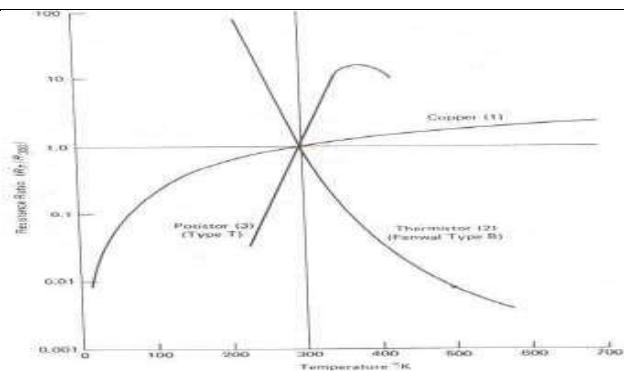
- Thermocouple
- Thermistor

Thermistors are variable resistance devices formed into disks, Beads, Rods or other desired shapes. They are manufactured from mixtures of oxides of various elements such as nickel, copper, magnesium, manganese, cobalt, titanium and aluminium.

After the mixture is compressed into shape, it is shaped at a high temperature into a solid mass. The result is a resistor with a large temperature coefficient.

Most metals show an increase in resistance of about 0.3 to 0.5 percent per °C temperature rise and the thermistors show decrease in resistance by 4 to 6 percent per °C temperature rise.

A Comparison of resistance Vs Temperature curves for copper, thermistor, posistor is as shown below.



### Skin temperature Measurement:

Although the systemic skin temperature remains very constant throughout the body, skin temperature can vary several degrees from one point to another. The range is usually from about 30 to 35°C (85 to 95°F). Exposure to ambient temperatures, the covering of fat over capillary areas, and local blood circulation patterns are just a few of the many factors that influence the distribution of temperatures over the surface of the body. Often, skin temperature measurements can be used to detect or locate defects in the circulatory system by showing differences in the pattern from one side of the body to the other.

Skin temperature measurements from specific locations on the body are frequently made by using small, flat thermistor probes taped to the skin. The simultaneous readings from a number of these probes provide a means of measuring changes in the spatial characteristics of the circulatory pattern over a time interval or with a given stimulus.

The human skin has been found to be an almost perfect emitter of infrared radiation. That is, it is able to emit infrared energy in proportion to the surface temperature at any location of the body. If a person is allowed to remain in a room at about 21°C (70°F) without clothing over the area to be measured, a device sensitive to infrared radiation can accurately read the surface temperature. Such a device, called an infrared thermometer.

### PART \*C

**Explain the working of pulse measurement?(15M)BTL1**

**Answer: Page: 47-REFER NOTES**

The pulse can be felt by placing the finger tip over the radial artery in the wrist or some other locations where an artery seems just below the skin.

- 1      The pulse pressure and waveform are indicators for blood pressure and blood flow. The instrument used to detect the arterial pulse and pulse pressure waveform is called as plethysmograph.  
 The pulse waveform travels at 5 to 15 m/sec depending up on the size and rigidity of arterial walls.  
 The methods used to detect volume (pulse) change due to blood flow are,
- Electrical Impedance changes

- Strain Gauge or microphone (mechanical)
- Optical change (Changes in density) (5M)

### **Electrical Impedance changes:**

Electrical Impedance method measures the impedance change between 2 electrodes caused by the change in blood volume between them.

The change in the impedance (0.1 ohm) may be as small as compared to the total impedance (Several hundred ohms).

The impedance is measured by applying an alternating current between electrodes attached to the body.

An alternating current (10 – 100 KHz) is used.

### **Strain Gauge or microphone (mechanical):**

The mechanical method involves the use of strain gauge connected to a rubber band placed around the limb or finger.

Expansion in the band due to change in blood volume causes a change in resistance of the strain gauge.

A sensitive crystal microphone is placed on the skin surface to pick up the pulsation. (5M)

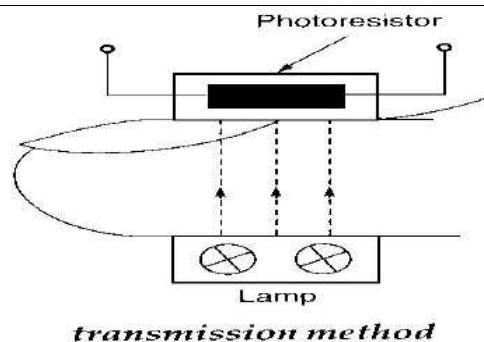
### **Optical change (Changes in density):**

The most commonly used method to measure blood volume change is photo electric method. In this method we have 2 types of method

- Transmittance method
- Reflectance method

### **Transmittance method: (5M)**

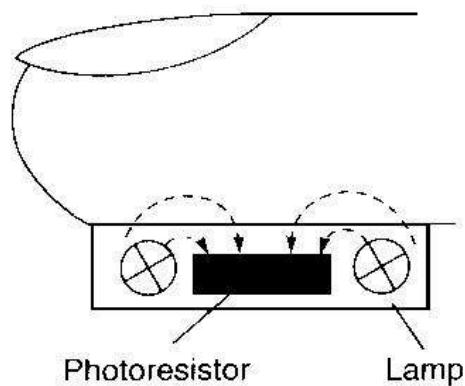
In transmittance method, a light emitting diode (LED) and photoresistor are mounted in an enclosure that fits over the tip of the patient's finger. The light is transmitted through the finger tip of the subject's finger and the resistance of the photoresistor is determined by the amount of light reaching it. With each contraction of the heart, blood is forced to the extremities and the amount of blood in the finger increases. It alters the optical density with the result that the light transmission through the finger reduces and the resistance of the photoresistor increases accordingly.



The photoresistor is connected as part of a voltage divider circuit and produces a voltage that varies with the amount of blood in the finger. This voltage that closely follows the pressure pulse and its waveshape can be displayed on an oscilloscope or recorded on a strip-chart recorder.

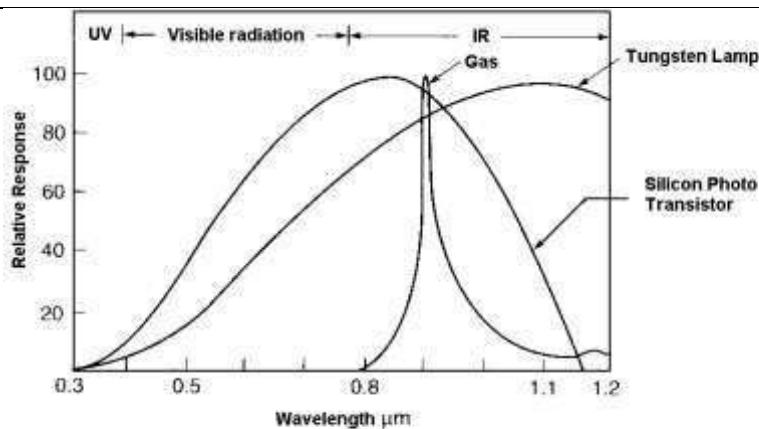
#### **Reflectance method:**

The arrangement used in the reflectance method of photoelectric plethysmography is shown in the figure below.



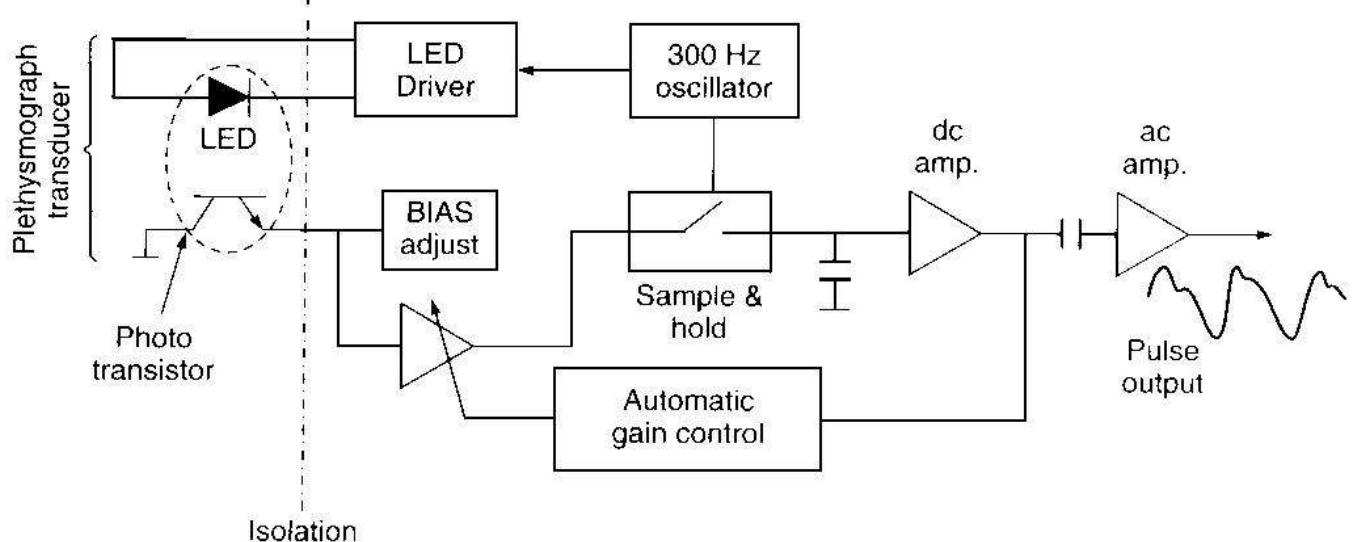
The photoresistor is placed adjacent to the exciter lamp. Part of the light rays emitted by the LED is reflected and scattered from the skin and the tissues and falls on the photoresistor.

The quantity of light reflected depends upon the amount of blood filling the capillaries and, therefore, the voltage drop across the photoresistor, connected as a voltage divider, will vary in proportion to the volume changes of the blood vessels.



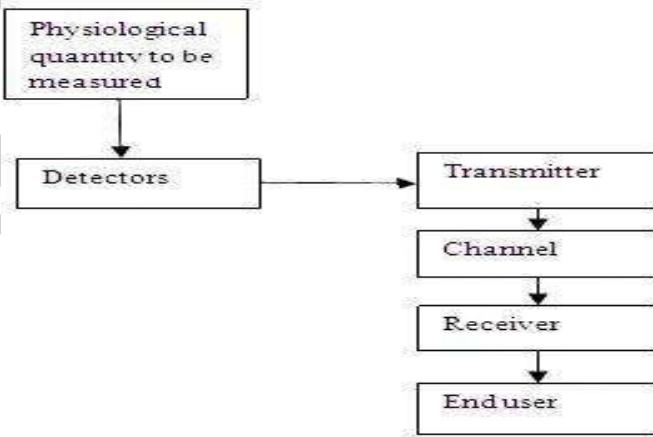
*Relative spectral response for silicon phototransistor and the radiant spectral distribution of a tungsten lamp and a gallium-arsenide lamp*

The LED phototransistor-photoplethysmograph transducer (Lee et al, 1975) consists of a Ca-As infrared emitting diode and a phototransistor in a compact package measuring 6.25 x 45 x 4.75 mm. The peak spectral emission of the LED is at 0.94mm with a 0.707 peak bandwidth of 0.04mm. The phototransistor is sensitive to radiation between 0.4 and 1.1mm as shown above.



*Block diagram for processing plethysmographic signal*

The circuit consists of two parts, a LED oscillator - driver, which produce 300 Hz, 50S- infrared light pulses to the finger probe attached to the patient, and a phototransistor that picks up the attenuated light. The electrical signal obtained from the phototransistor is amplified and its peak value is sampled and filtered. An automatic gain control circuit adjusts the amplifier gain to yield a constant average pulse height at the output.

	<p>The ac component with a frequency in the heart rate range (0.8-5 Hz) is further amplified to output the plethysmographic pulse rate form. This signal is transmitted across the isolation barrier, demodulated, low-pass filtered and transmitted to the analog multiplexer resident on the CPU board.</p>
	<p><b>Discuss in detail about Telemetry Principles. (10M) (Nov/Dec-2013)(May/June-2014)BTL6</b>  <b>Answer: Page: 312-Dr.M.ARUMUGAM</b></p> <p><b>Design considerations for a telemetry system(2M)</b></p> <ul style="list-style-type: none"> <li>• Simplicity of the telemetry system</li> <li>• Transmission should be with maximum fidelity</li> <li>• Telemetry components should be less weight and size</li> <li>• High reliability and stability is must</li> <li>• Power consumption should be small</li> <li>• Shielding of the cable is a must in wire based transmission</li> </ul> <p><b>Telemetry system:</b></p> <ul style="list-style-type: none"> <li>• information regarding - quantity being measured transmitted to a remote location for application like data processing</li> <li>• recording or displaying.</li> <li>• In other words telemetry means measuring at a distance. Therefore it becomes essential to transmit data through some form of communication channels.</li> </ul> <p><b>Methods of classification of telemetry system:(2M)</b></p> <p>2</p> <ul style="list-style-type: none"> <li>• On the basis of the characteristics of electric signal such as voltage current position,frequency and pulse</li> <li>• Based on form of data transmitted –analog and digital</li> <li>• Based on transmission of distance –short distance type or long distance type</li> <li>• Based on whether user has control over transmission channel or not.</li> <li>• The physiological quantity to be measured by a suitable detector and given to the transmitter. The electrical telemetry system is broadly classified as DC systems and AC systems.</li> </ul>  <pre> graph TD     A[Physiological quantity to be measured] --&gt; B[Detectors]     B --&gt; C[Transmitter]     C --&gt; D[Channel]     D --&gt; E[Receiver]     E --&gt; F[End user]   </pre>

(6M)

**DC telemetry system:**

The signal is transmitted through a telemetry or communication channel which uses direct transmission via cables in order to convey the desired information . This is known as land line telemetry.

**AC telemetry system:**

It is used both for land line and radio frequency air borne telemetry techniques. Electronics means are used for sensors that provide an AC output or voltage to frequency converter. The data is available in the form of current or voltage which is generally weak . Hence It is modulated with carrier signals for transmission. These modulated signals are demodulated at the receiving end which means recovering the original signal from carrier wave. Basically there are three types of modulation

**Amplitude modulation:**

In this type of modulation the amplitude of the carrier is varied in accordance with the signal to be transmitted.

**Frequency modulation:**

In this type of modulation the instantaneous frequency of the carrier is varied in accordance with the amplitude of the modulating signal.

**Phase modulation:**

Here phase angle is varied in accordance to be transmitted signal.

**Communication channels(or) Transmission media:**

The most widely used communication channels are cables and electromagnetic radiation radio links. Optical ,ultrasonic and magnetic induction data links are also used for many applications. Land line telemetry utilizes cables or wires to transmit data. When data is to be transmitted for more than 1km radio links are preferred. For frequency above 30MHz microwave links are used. For short range transmission up to 50m frequency modulation used.

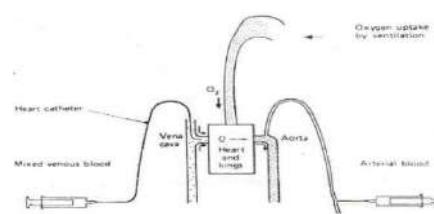
**Discuss about the various methods for determining cardiac output.(15M)(May/June-2013)BTL1**

**Answer: Page: 246 -Dr.M.ARUMUGAM**

**Flick's Method: (4M)**

Determination of cardiac output - analysis of gas-keeping - organism. The cardiac output is calculated by continuously infusing oxygen into blood or removing it from the blood and measuring the amount of oxygen in blood before and after its passage. Let  $I$  be the amount of infused or removed oxygen per unit time.  $I$  is equal to the difference between amount in blood arriving at and departing from it.

$$I = CAQ - CVQ$$



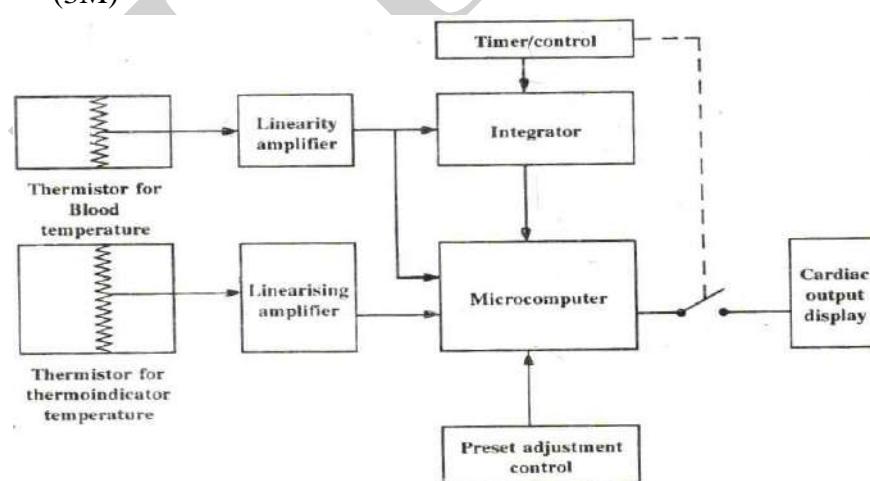
**Indicator Dilution Method: (3M)**

- This is based on the principle that if we introduce an indicator in the blood circulation
- and then measuring the concentration of indicator with respect to time. We can estimate the volume flow of blood. Let  $M$  mg of an indicator is injected into the right heart. After passing through the right heart, lungs and left heart, the indicator appears - arterial circulation. The presence of the indicator- peripheral artery - detected by a detector. The output of the detector - directly proportional - concentration of indicator.
- The detector is displayed on a chart recorder with respect to time. Let an increment in volume  $dv$  passes the sampling site in time  $dt$ . Let the mass of indicator in  $dv = dm$

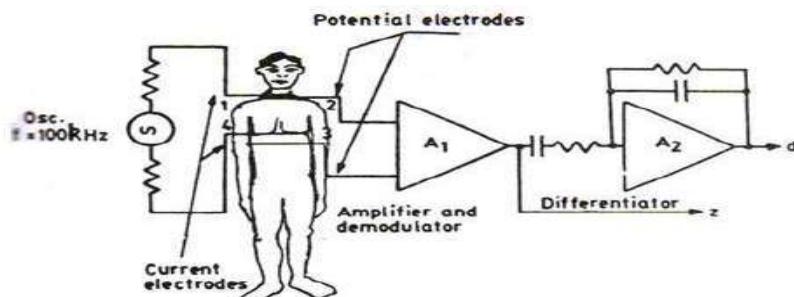
**Thermo Dilution Method. :**

(3M)

Thermo dilution method - adapted to measure cardiac output. A bolus of about 10ml of 5% dextrose in water at room temperature is injected as a thermal indicator into right atrium. After mixing- detected in the pulmonary artery by means of a thermistor mounted at the tip of a miniature catheter probe. The temperature difference between the injectate temperature and the circulating blood temperature in the pulmonary artery is measured. The reduction in temperature is integrated w.r.t time and the meter reads the cardiac output.



	<b>Measurement of cardiac output by impedance change.</b>	(2M)
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**UNIT V BIO-CHEMICAL MEASUREMENT**

9

Blood gas analyzers and non-invasive monitoring, colorimeter, sodium potassium analyzer, spectrophotometer, blood cell counter, Auto analyzer

**PART\*A**

Q.No.	Questions
1	<b>State different types of tests performed by auto analyzer.(MAY2016) BTL1</b> <ul style="list-style-type: none"> <li>• Mixing</li> <li>• Reaction</li> <li>• Colorimetric determination</li> </ul>
2	<b>What is thermograph? (NOV 2015)BTL1</b> The instrument used to record the temperature distribution over the surface of the body or skin is called as thermograph.
3	<b>List out the applications of thermography (MAY 2011)BTL1</b> Thermography is used in diagnosing many diseases like breast cancer, Rheumatic diseases, burns, perniones, joint diseases and location of placenta.
4	<b>Mention the types of lasers used in medical field (Or) What types of lasers are used for patient treatment (Or) What are the applications of lasers in medicine?BTL1</b> CO <sub>2</sub> Laser – Surgery, Dental treatment Nd – YAG – Surgery, dental treatment, Photocoagulation Argon ion – Ophthalmology (Photocoagulation of small blood vessels in eye) Ruby laser – Retinal treatment, dental treatment

5	<p><b>What are the types of lasers used for therapeutic purposes? (APR 2005)BTL1</b></p> <p>The types of lasers used for therapeutic purpose are, CO<sub>2</sub>, Ruby, Nd-YAG, Argon ion.</p>
6	<p><b>Mention the advantages of LASER in surgery.BTL1</b></p> <p>Highly sterile Highly localized and precise Non contact surgery Dry-field, almost bloodless surgery Short periods of surgical time.</p>
7	<p><b>List out the properties of LASER. (Or) List out the characteristics of LASER .BTL1</b></p> <p>Monochromaticity Spatial and temporal coherence Directionality Brightness.</p>
8	<p><b>What is the principle of cryogenic technique? Give any two medical application of the same. (Or) What is meant by Cryogeny? (APR 2004)BTL1</b></p> <p>Tissues can be killed when their temperature is below –20C. When the tissues are at –20C, there is a formation of ice crystals and increase of salt concentration within the cells. Thus necrosis of the tissue takes place. This method of killing diseased cells is called as cryogenic surgery or cryogenic technique.</p> <p>The process of freezing the cells by applying agents at very low temperature is called as cytogeneses.</p> <p>Application:</p> <ul style="list-style-type: none"> <li>Cancer Therapy</li> <li>Dermatology</li> <li>Rhythm disorders of heart</li> <li>Treatment of arrhythmia</li> </ul>
9	<p><b>Explain the principle of telemedicine. (MAY 2008)BTL1</b></p>

	Telemedicine is a rapidly developing application of clinical medicine where medical information is transferred via telephone, the internet or other networks for the purpose of consulting and sometimes remote medical procedures or examinations.
10	<p><b>State the applications of telemedicine. (MAY 2016)BTL1</b></p> <ul style="list-style-type: none"> <li>• Tele radiology.</li> <li>• Tele cardiology.</li> <li>• Tele education.</li> <li>• Tele consultation</li> </ul>
11	<p><b>What is meant by single channel telemetry? ( NOV 2015)BTL1</b></p> <p>In a majority of the situations requiring monitoring of the patients by wireless telemetry, the parameter which is most commonly studied is the electrocardiogram. It is known that the display of the ECG and cardiac rate gives sufficient information on the loading of the cardiovascular system of the active subjects</p>
12	<p><b>Bring out the clinical applications of endoscopy (NOV 2015)BTL1</b></p> <p>A health care provider may use endoscopy for any of the following:</p> <p>investigation of symptoms, such as symptoms in the digestive system including nausea, vomiting, abdominal pain, difficulty swallowing and gastrointestinal bleeding.</p> <p>confirmation of a diagnosis, most commonly by performing a biopsy to check for conditions such as anemia, bleeding, inflammation, and cancers of the digestive system.</p> <p>giving treatment, such as cauterization of a bleeding vessel, widening a narrow esophagus, clipping off a polyp or removing a foreign object.</p>
13	<p><b>List the types of pumping sources used in LASER? ( MAY 2016)BTL1</b></p> <p>The pump source is the part that provides energy to the laser system. A helium–neon (HeNe) laser uses an electrical discharge in the helium-neon gas mixture, a Nd:YAG laser uses either light focused from a xenon flash lamp or diode lasers, and excimer lasers use a chemical reaction</p>
14	<b>What is medical thermography? Mention its applications.(NOV 2014)BTL1</b>

	<p>Thermography is the process of recording true thermal image of the surfaces of objects under study. It displays images representing the thermal radiation of skin areas. Thermogram contain both qualitative and quantitative information relevant to the image itself and to temperature. Medical applications of thermography</p> <p>Tumors Inflammation Diseases of peripheral vessels Orthopedic diseases</p>
15	<p><b>Define - Endoscopes and mention some of its types.(MAY 2014)BTL1</b></p> <p>Endoscope is a tubular optical instrument to inspect or view the body cavities which are not visible to the naked eye normally. Types of endoscopes are cardio scope, bronchoscope, laparoscope, horoscope, gastro scope etc.</p>
16	<p><b>List the applications of Endoscope.BTL1</b></p> <p>Endoscopes are used in hospitals for examination, treatment of disease and surgery</p>
17	<p><b>Define the physical factors which affect the amount of infrared radiation from the human body.(NOV 2016)BTL1</b></p> <p>Emissivity Reflection Transmittance and absorption</p>
18	<p><b>List the types of pumping sources used in LASER .(MAY 2016)BTL1</b></p> <ul style="list-style-type: none"> <li>➤ Optical pumping</li> <li>➤ Electrical pumping</li> <li>➤ Gas dynamic pumping</li> </ul>
19	<p><b>What is meant by telemedicine? BTL1</b></p> <p>Telemedicine is the remote diagnosis and treatment of patients by means of telecommunications technology.</p>
20	<p><b>What is the use of laparoscope? BTL1</b></p>

	The laparoscope is used for analyzing abdominal related diseases and to perform operations in the abdominal region.
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**PART\*B**

**Explain the working principle of auto analyzer(May/June-2014)(8M)BTL1**

**Answer: Page: 39-REFER NOTES**

**AUTO ANALYZER :(2M)**

The autoanalyzer - measures blood chemistry and displays - graphic readout.

**ELEMENTS:**

(4M)

**Sampler** - aspirates samples, standards, and wash solutions - autoanalyzer system.

**Proportioning pump and manifold** - introduces (mixes) samples with reagents to effect the proper chemical color reaction to be read by the colorimeter. It also pumps fluids at precise flow rates to other modules, as proper color development depends on reaction time and temperature.

1

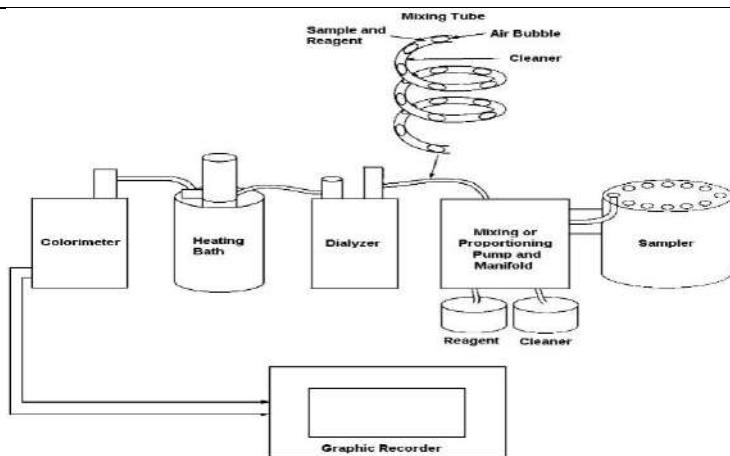
**Dialyzer** - separates interfacing substances from the sample material by permitting selective passage of sample components through a semipermeable membrane.

**Heating bath** - heats fluids continuously to exact temperature (typically 37°C incubation, equivalent to body temperature). Temperature - critical to color development.

**Colorimeter** - monitors the changes in optical density of the fluid stream flowing through a tubular flow cell. Color intensities (optical densities) proportional substance concentrations are converted to equivalent electrical voltages

**Recorder** – Converts optical density electrical signal from the colorimeter into a graphic display on a moving chart.

(2M)



**Describe the operation of the automatic blood cell counter..(13M) (May/June 16)(Nov/Dec-14) (Nov/Dec-2012)BTL1**

**Answer: Page: 274-Dr.M.ARUMUGAM**

#### **BLOOD CELL COUNTER COUNT -TWO METHOD:(5M)**

- Electrical method called aperture impedance change
- Optical method called flow cytometry

The platelets are involved in the clotting of blood. The red blood cells in the blood consist of hemoglobin.

When the hemoglobin in the blood decreases, anemia is produced. The amount of hemoglobin is normally 130-170 g/l for men and 120-160 g/l for women. To determine retain proportion of blood cells in a given volume of blood, hematocrit or packed cell volume is used. The packed cell volume is the ratio between the height of the packed cells and height of blood in the tube. Normal range of packed cell volume for men is 42-54% and for women is 37-47%.

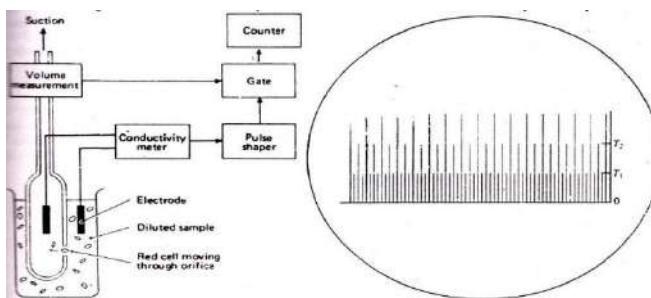
The number of red blood cells can be counted using a microscope, but the microscopic counting is time consuming. Now-a-days automatic red blood cell counters are used.

#### **Automatic Red Blood Cell Counter:(8M)**

This method is based on the fact that red cells have a higher electrical resistivity than the saline solution in which they are suspended. Fig .shows the automatic blood cell A diluted blood sample is drawn through a small orifice by means of a section pump. The electrodes are placed such that one in the surrounding sample chamber and other in the suctioned blood. The electrodes are attached with the conductivity bridge such that their resistance forms one arm of bridge. Before suctioning, the resistance of the electrode arm is equal to  $R$ .

The threshold is first set to zero and the counter output is given by the total number of particles (WBCs + RBCS + platelets) per litre. Then the threshold is set to  $T_1$  and the counter gives the total number RBCS

and WBCS per litre. After that the threshold is set to T2 and the counter reads the total number of WBCS per litre.



**Explain in detail about blood gas analysers. Describe the measurement of pH of blood using pH meter.(13M) (Nov/Dec-2014) (Nov/Dec-2013)(May/June-2016) BTL1**

**Answer: Page: 21-Dr.M.ARUMUGAM**

#### pH Electrode:

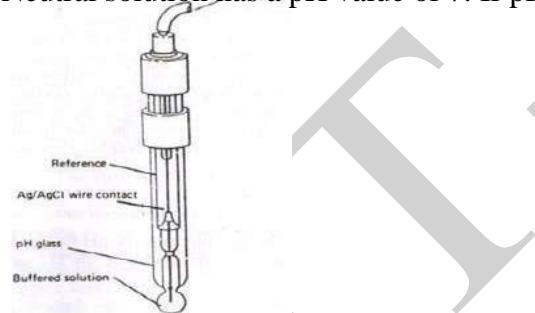
Chemical balance -human body in identified - measurement of pH contentof blood and other body fluids.

PH is defined as the logarithmic of reciprocal of H<sup>+</sup> ion concentrations.

$$\text{PH} = \log_{10} 1 / [\text{H}^+]$$

$$= - \log_{10} [\text{H}^+]$$

Neutral solution has a pH value of 7. If pH < 7, it is acidic, pH > 7 it is basic. (2M+2M)



#### PO<sub>2</sub> Electrode:(4M)

The oxygen electrode - piece of platinum wire embedded - insulating glass holder with the end of the wire exposed to the electrolyte solution into which oxygen is allowed to diffuse through the membrane

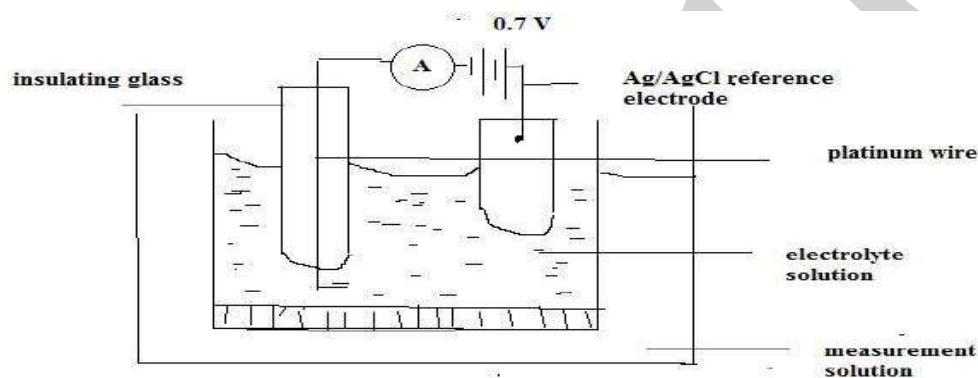
The bottom of the vessel containing electrolyte- membrane permeable to oxygen and the top of vessel is sealed.

Ag - Agcl electrode is used A voltage of 0.7V is applied between the platinum wire and the reference electrode using a battery. The negative of the battery - platinum wire through an ammeter.

Reduction of oxygen takes place at platinum wire. Hence an oxidation-reduction current is developed and is proportional to the partial pressure of oxygen.

#### **Advantages :(1M)**

- The oxygen electrode - monitor the partial pressure of oxygen- biological fluids.
- It is available in integrated version consisting of platinum electrode and reference electrode in the same enclosure called Clark electrode



#### **PCO<sub>2</sub> Electrode:(4M)**

It consists of a standard glass PH electrode covered with rubber membrane permeable to CO<sub>2</sub>. Between the glass surface and membrane there is a thin film of water. The solution under test contains dissolved CO<sub>2</sub> is presented to the outer surface of rubber membrane. After equilibrium PH of aqueous film is measured by glass electrode and interpreted in terms of PCO<sub>2</sub>.

#### **Describe the working principle and operation of colorimeter.(13M) BTL1**

**Answer: Page: 284-Dr.M.ARUMUGAM**

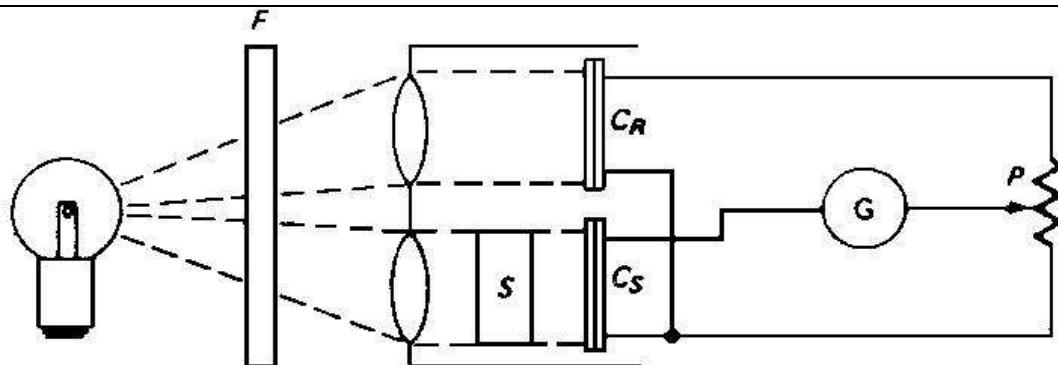
**4**

Transmittance  $T = I_1/I_0$  (2M)

Absorbance or optical density  $A = \log(1/T)$  (2M)

When an interference filter is used to select a given wavelength, it is called filter photometer (3M)

Filter photometer diagram (6M)

**Filter photometer****PART\*C**

**Describe the operation of the blood cell counter. Explain the principle of operation of Coulter counter. what is its applications.(15M) (May/June 16)(Nov/Dec-14) (Nov/Dec-2012)BTL1**

**Answer: Page: 274-Dr.M.ARUMUGAM**

**BLOOD CELL COUNTER COUNT -TWO METHOD:(4M)**

- Electrical method called aperture impedance change
- Optical method called flow cytometry

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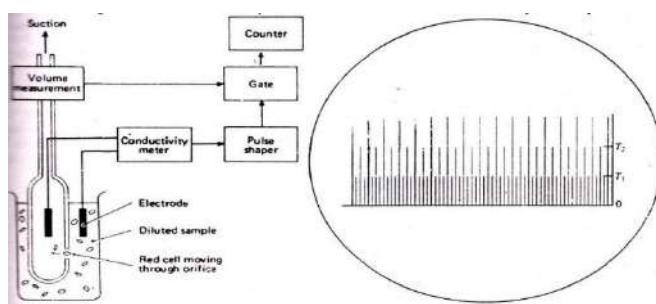
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The threshold is first set to zero and the counter output is given by the total number of particles (WBCs + RBCS + platelets) per litre. Then the threshold is set to T1 and the counter gives the total number RBCS

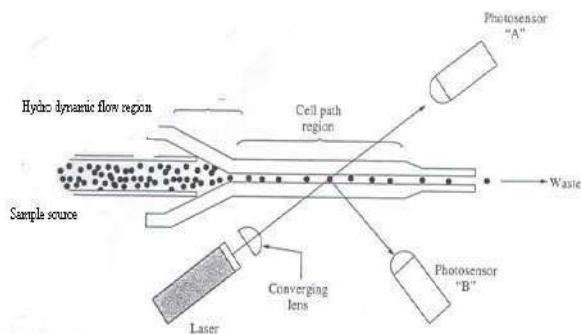
and WBCS per litre. After that the threshold is set to T2 and the counter reads the total number of WBCS per litre.



### Laser Blood Cell Counter:(5M)

This is a modern technique which gives the number of RBCs, WBCs and Platelets , hematocrit and concentration of hemoglobin. The basic Principle is that the angle of scattered light intensity is different for different sized particles. The sample blood is heavily diluted to reduce the number of particles counted to one at a time. A sheath fluid is directed around the blood stream to confine it to the center of aperture through which a laser beam is passed. Thus the blood cells are illuminated by the laser light and they scatter light.

The scattered light from platelets and red blood cells are directed into two photo detectors. The output of the photo detector is given to a digital voltmeter which gives the density of red blood cells or platelets. To separates WBCs from RBCs, we can destroy the RBCs by a lying agent. This frees the hemoglobin from the blood and its concentration can be measured. Once again the measurements are made by which the concentration of WBCs can be measured.



2	<p>Elaborate spectrophotometer and its application in Bio-chemical measurement. (15M) BTL1</p> <p><b>Answer: Page: 286-Dr.M.ARUMUGAM</b></p> <p>Diffraction grating or prism is used as a monochromator to get different spectral components or wavelengths. (4M)</p> <p>Light from a halogen lamp passes through an entrance slit s1 (2M)</p> <p>Incident on a concave reflector which focuses the light on a diffraction grating to disperse light. (3M)</p> <p>From reflector light beam directs to the sample through a narrow slit s2 (2M)</p> <p>Sensitive photodetector D detects transmitted light. (2M)</p> <p>Generation of electrical output (2M)</p> <p>Diagram:</p> <p style="text-align: center;"><b>Filter photometer</b></p>