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ARM Cortex-A72

The **ARM Cortex-A72** is a microarchitecture implementing the ARMv8-A 64-bit instruction set designed by ARM Holdings' Austin design centre. The Cortex-A72 is a 3-way decode out-of-order superscalar pipeline.[1] It is available as SIP core to licensees, and its design makes it suitable for integration with other SIP cores (e.g. GPU, display controller, DSP, image processor, etc.) into one die constituting a system on a chip (SoC). The Cortex-A72 was announced in 2015 to serve as the successor of the Cortex-A57, and was designed to use 20% less power or offer 90% greater performance.[2][3]

Contents

Overview

- Pipelined processor with deeply out-of-order, speculative issue 3-way superscalar execution pipeline
- DSP and NEON SIMD extensions are mandatory per core
- VFPv4 Floating Point Unit onboard (per core)

ARM Cortex-A72

General Info	
Launched	2016
Designed by	ARM Holdings
Cache	
L1 cache	80 KiB (48 KiB I-cache with parity, 32 KiB D-cache with ECC) *per core*
L2 cache	512 KiB to 4 MiB
L3 cache	None
Architecture and classification	
Min. feature size	16 nm
Microarchitecture	ARMv8-A
Physical specifications	
Cores	1–4 per cluster, multiple clusters[1]

Products, models, variants	
Product code name(s)	Maya
History	
Predecessor	ARM Cortex-A57
Successor	ARM Cortex-A73

- Hardware virtualization support
- Thumb-2 instruction set encoding reduces the size of 32-bit programs with little impact on performance.
- TrustZone security extensions
- Program Trace Macrocell and CoreSight Design Kit for unobtrusive tracing of instruction execution
- 32 KiB data (2-way set-associative) + 48 KiB instruction (3-way set-associative) L1 cache per core
- Integrated low-latency level-2 (16-way set-associative) cache controller, 512 KB to 4 MB configurable size per cluster
- 48-entry fully associative L1 instruction translation lookaside buffer (TLB) with native support for 4 KiB, 64 KiB, and 1 MB page sizes
- 32-entry fully associative L1 data TLB with native support for 4 KiB, 64 KiB, and 1 MB page sizes
  - 4-way set-associative of 1024-entry unified L2 TLB per core, supports hit-under-miss
- Sophisticated branch prediction algorithm that significantly increases performance and reduces energy from misprediction and speculation
- Early IC tag –3-way L1 cache at direct-mapped power*
- Regionalized TLB and μBTB tagging
- Small-offset branch-target optimizations
- Suppression of superfluous branch predictor accesses

Chips

- Broadcom BCM2711 (used in Raspberry Pi 4[4])
- Snapdragon 650, 652, and 653

See also

- Comparison of ARMv8-A cores

References

1. "Cortex-A72 Processor" (http://www.arm.com/products/processors/cortex-a/cortex-a72-processor.php). ARM Holdings. Retrieved 2014-02-02.
2. Frumusanu, Andrei (3 February 2015). "ARM Announces Cortex-A72, CCI-500, and Mali-T880" (http://www.anandtech.com/show/8957/arm-announces-cortex-a72). Anandtech. Retrieved 29 March 2017.
3. Frumusanu, Andrei (23 April 2015). "ARM Reveals Cortex-A72 Architecture Details" (http://www.anandtech.com/show/9184/arm-reveals-cortex-a72-architecture-details). Anandtech. Retrieved 29 March 2017.
4. "Raspberry Pi 4 on sale now from $35" (https://www.raspberrypi.org/blog/raspberry-pi-4-on-sale-now-from-35/). *Raspberry Pi*. 2019-06-24. Retrieved 2019-06-24.

External links

- Official website (http://www.arm.com/products/processors/cortex-a/cortex-a72-processor.php)
- ARM Cortex-A72 Technical Reference Manuals (http://infocenter.arm.com/help/index.jsp?topic=/com.arm.doc.100095_0001_02_en/index.html)