OV5640 Camera Module

Hardware Application Notes

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Sensor datasheet is the official document of OmniVision. Software/hardware/dual camera applicaton notes are application guide lines for reference. If there are any difference between sensor datasheet and application notes, please follow sensor datasheet and kindly report the difference to OVT FAE.

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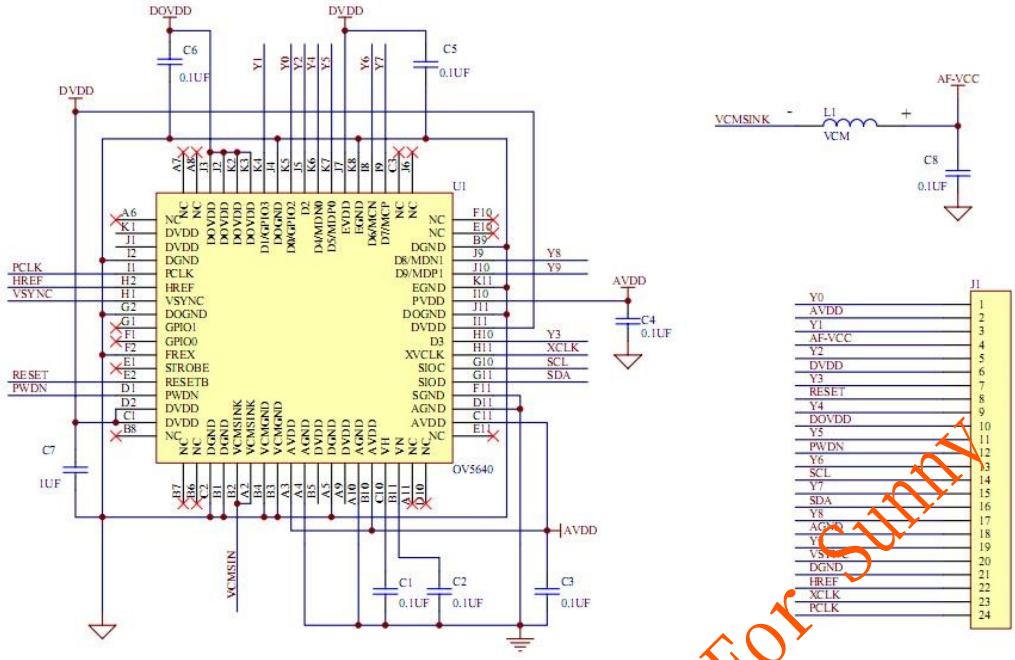
1. OV5640 Camera Module Reference Design



Note:

1. PWND, active HIGH as DOVDD to power down OV5640, should be connected to ground outside of module if unused
2. RESETB. Active LOW to reset OV5640, should be connected to DOVDD outside of module if unused
3. AVDD is 2.6-3.0V of sensor analog power (clean). 2.8V is recommended. AVDD must be 2.5V+-5% for OTP write, and OTP read does not have such requirement
4. DVDD is 1.5V±5% of sensor digital power(clean). Using the internal DVDD regulator is strongly recommended
5. DOVDD. 1.8V recommended is 1.7V-3.0V of sensor digital IO power(clean)
6. sensor AGND and DGND should be separated and connected to a single point outside PCB, Do not connect inside module
7. Capacitors should be close to the related sensor pins
8. D[9:0] is sensor 10 bit RGB RAW output. D[9:2] is sensor 8-bit YUV/RGB output

For OV5640 camera module, below two kinds of power supplies are recommended:

A. 2 External Power Supplies
   - DOVDD = 1.8V, DVDD generated by internal regulator
   - AVDD = 2.8V
   - Support both Power Down and Power Off mode for power saving.

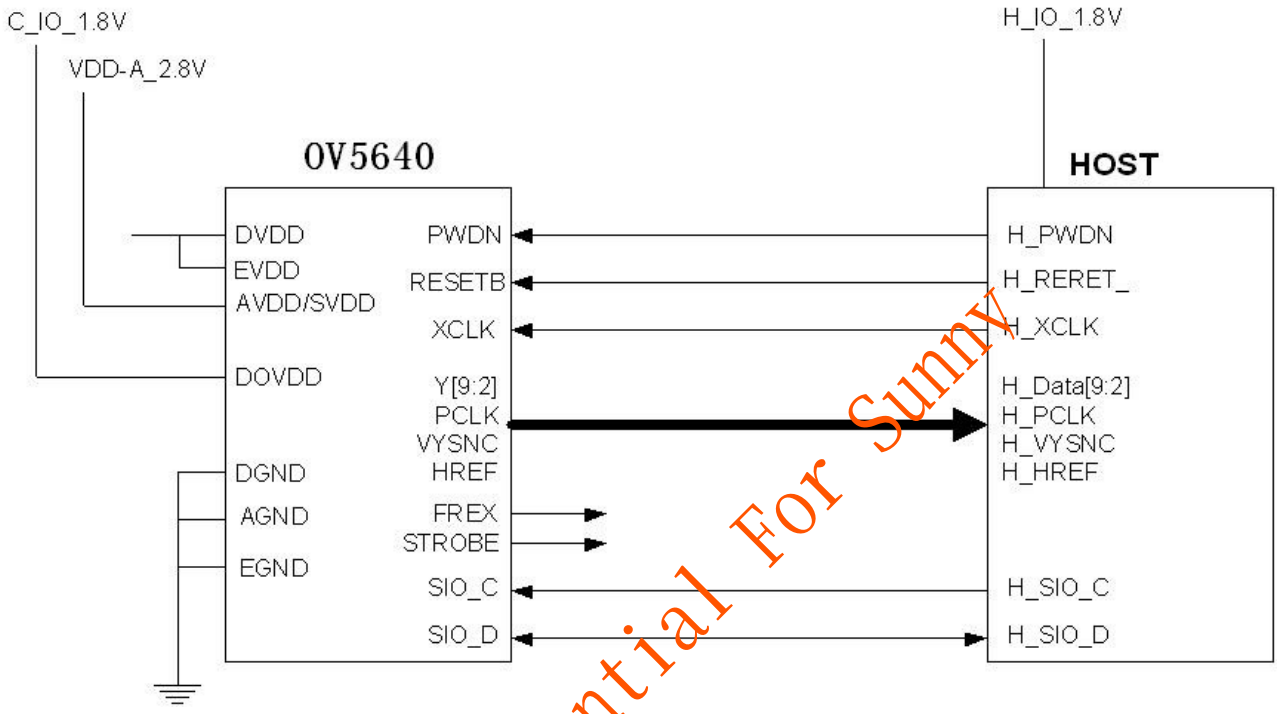
B. 3 External Power Supplies

- DOVDD = 2.8V
- DVDD = 1.5V
- AVDD = 2.8V
- Use Power Off mode for power saving. Power Down mode is not supported for power saving.

2. OV5640 Interface with Host

2.1 Host 1.8V IO and 5640 1.8V IO

For those hosts can support 1.8V IO.



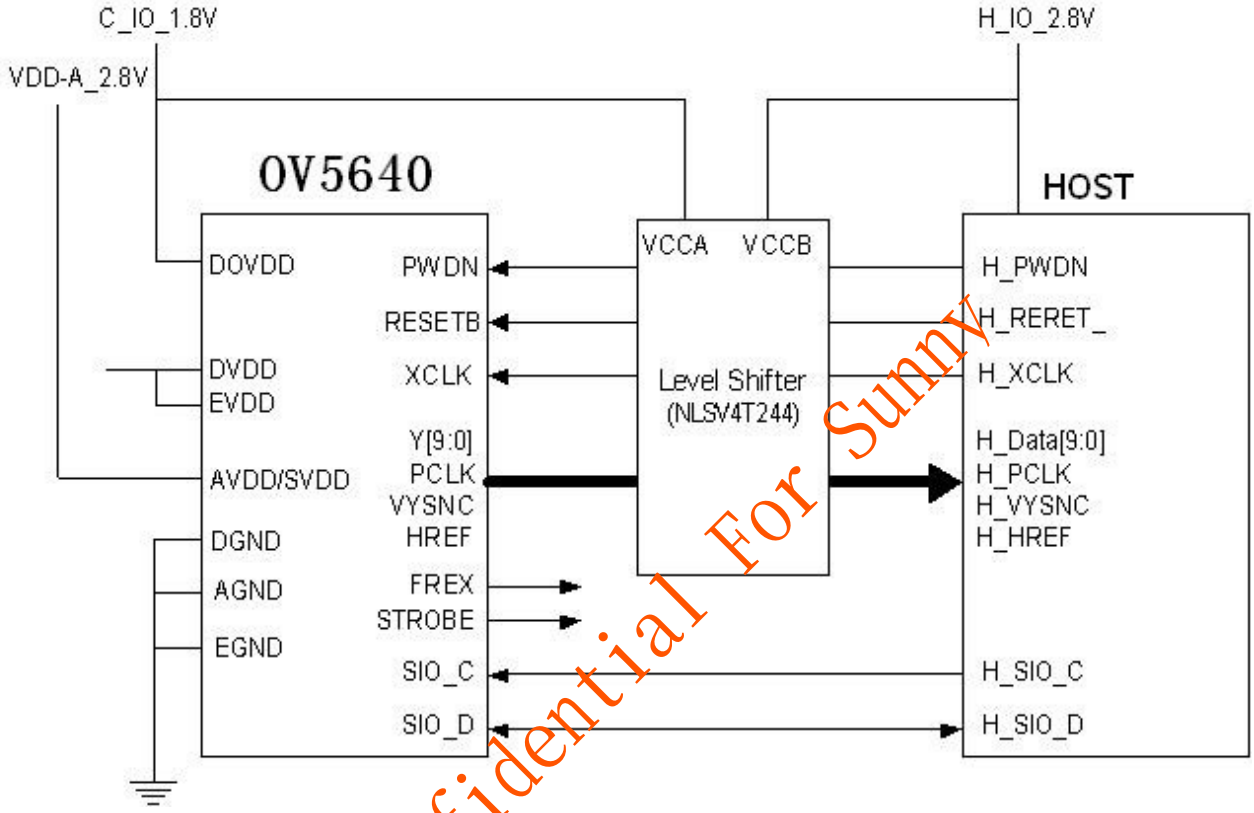
2.2 Host 2.8V IO and 5640 1.8V IO

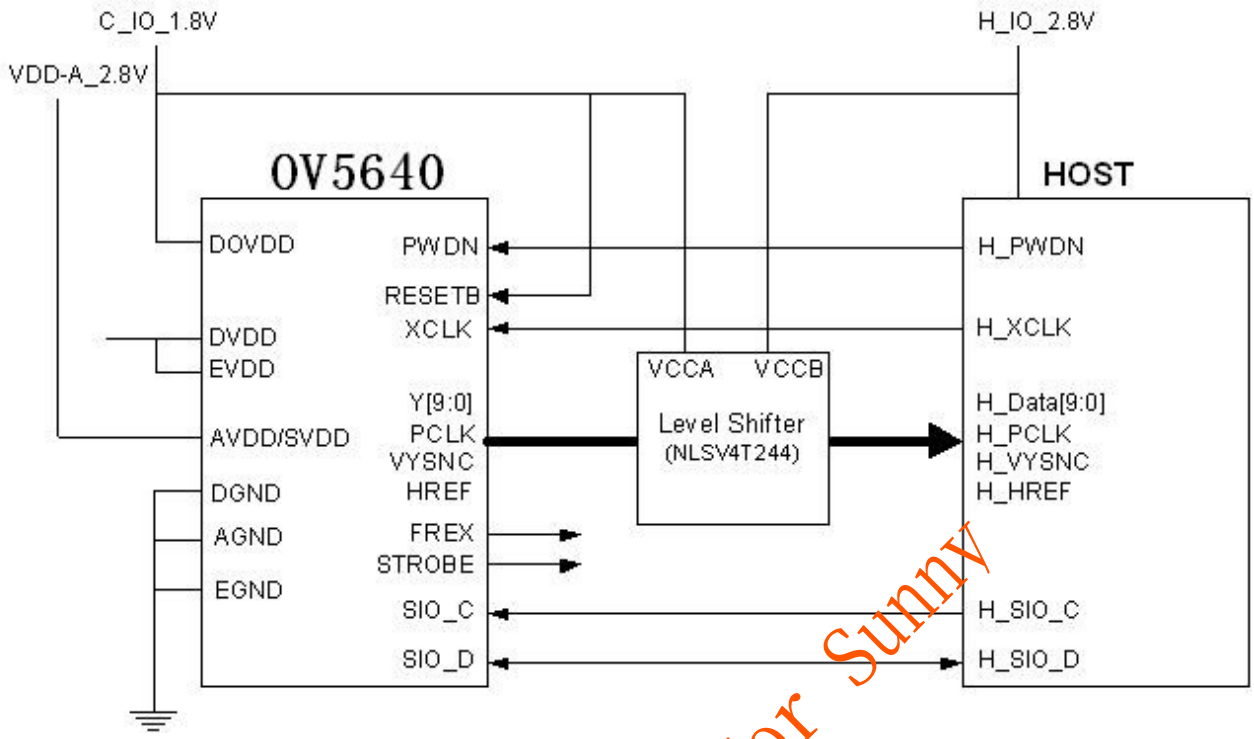
However, for some legacy phones or baseband chips, they only accepts 2.8V IO signals, for this kind of application, we suggest 5640 use 1.8V with level shift in between 5640 and host for all video signals.

In this case, 5640 works in the 1.8V IO, and host works in required 2.8V IO. For this case:

1) OV5640 output pins (HREF/HSYNC, VSYNC, DATA0~9, PCLK, FREX, STROBE, GPIO1~2) are tri-state when sensor is in standby mode (PWDN pin is high). Please make sure that it would not cause any problem(current leak) for other devices' input. You may put 10kohm pull-down resistor on all tri-state pins if tri-state is an issue for level-shifter or host chip.
2) Add level-shifter for all video signals -- HREF/HSYNC, VSYNC, DATA0~9, PCLK.
3) Sensor SCL and SDA can tolerance high voltage. So it is no problem for 5640 to use 1.8V IO and I2C pull up resistors connect to 2.8V.
4) Sensor PWDN and XCLK are no problem for 2.8V signal. PWDN can directly connect to 2.8V for sensor power down. If has extra level shift pins, add level shift for these two pins as well.

5) For RESETB pin, please don't provide 2.8V signal since 5640 has internal pull-up resistor to IO power. If provide 2.8V signal on this pin, it will cause power leak (from 2.8V signal to the sensor 1.8V IO power through the pull-up resistor and diode). Here are some solutions.
   a) Host drive this pin to low for reset mode, and change it to floating/input in operating mode and let sensor internal pull-up resistor to drive high (1.8V).
   b) Add level-shifter for RESETB as well.





2.3 Host 2.8V IO and 5640 2.8V IO

OV5640 also support 2.8V IO. If use 2.8V IO, the 1.5V DVDD must be supplied by external power. And power off mode is recommended for power saving. Power down mode is not supported for power saving.

3. OV5640 Camera Interface Reference for Camera Phone

3.1 Pin Definition

The video port of OV5640 has 10-bit, D[9:0]. For 10-bit RGB raw output, please use D[9:0]. For 8-bit YCbCr or 8-bit RGB raw or 8-bit RGB 565 output, please use D[9:2].

The Href and Hsync signal is on the same pin – Href. The function of this pin could be selected by SCCB setting.

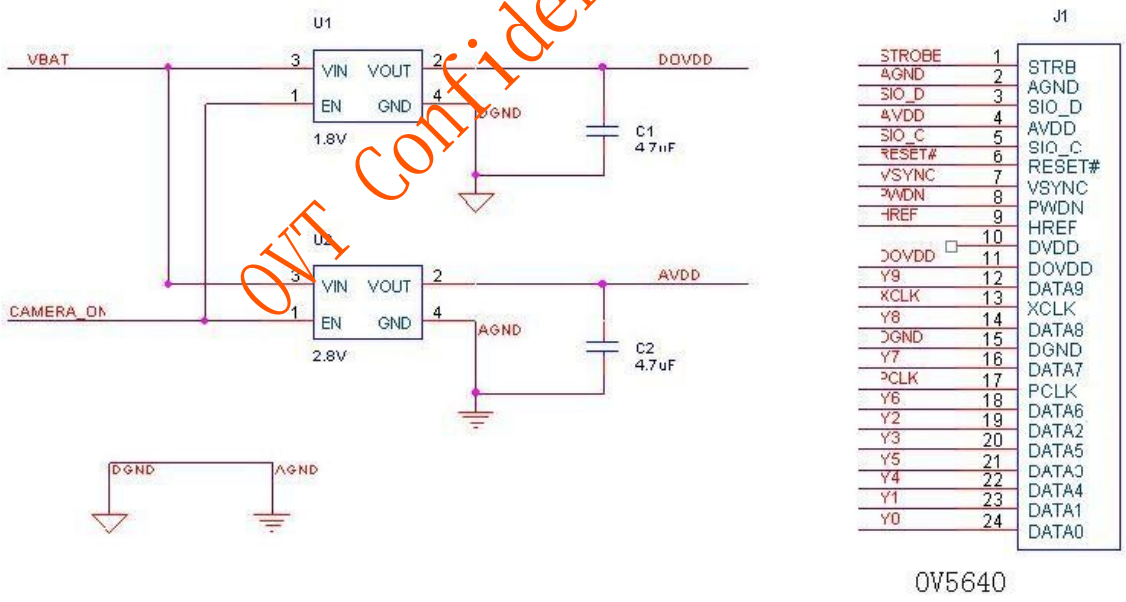
The SIO_C and SIO_D bus should have external pull up resistors, the typical value of the pull up resistors is 5.1K.

RESET# is active low with internal pull-up resistor. Reset# should be controlled by backend chip for proper power up sequence.

PWDN is active high with internal pull-down resistor. PWDN should be controlled by backend chip for proper power up sequence.

3.2 Power Supply

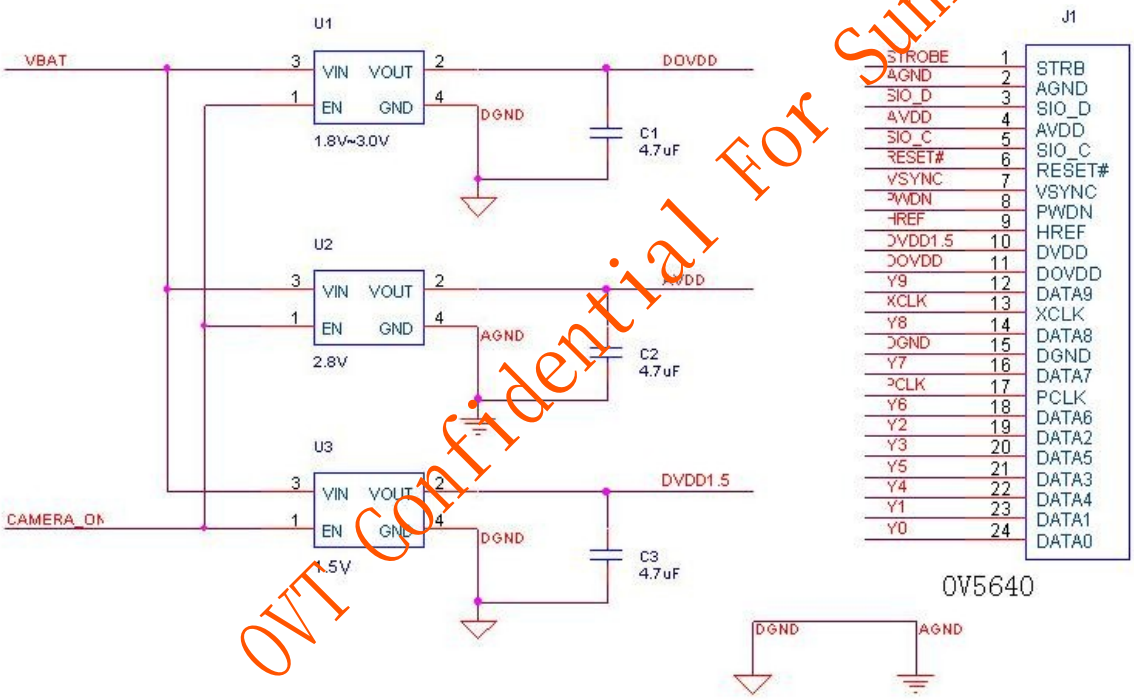
If DOVDD uses 1.8V, then DVDD is generated by internal regulator. So 2 regulators should be used.



If DOVDD uses 2.8V, then DVDD is supplied from external power supply. So 3 regulators should be used. Power down mode is not supported for power saving here.

Note:

The AGND and DGND should be separate inside module and connected together on phone PCB very close to camera module connector.



4. OV5640 Camera Operation

4.1 Power Saving Modes

There are 2 kinds of power saving modes: power down mode and power off mode.

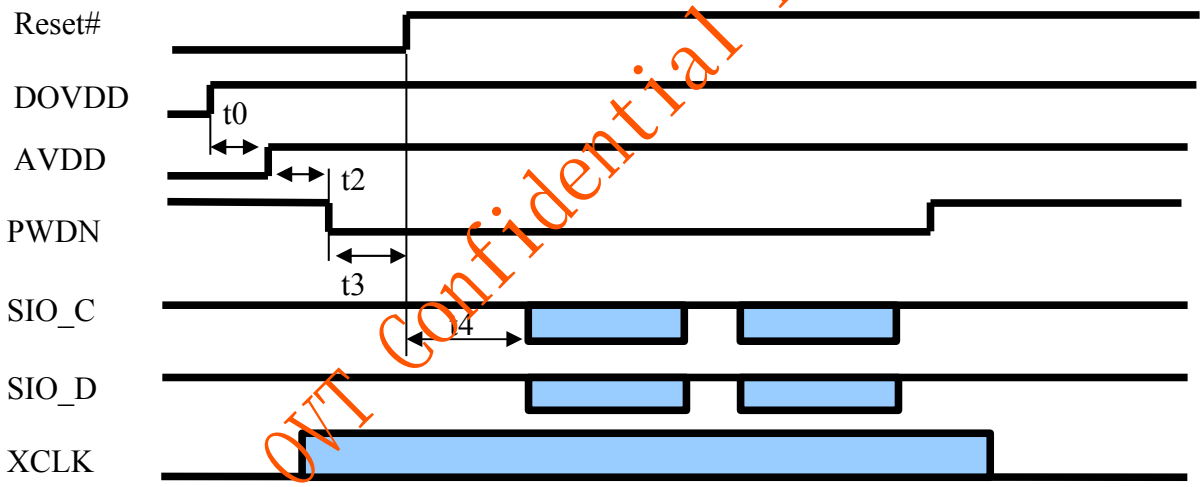
Power down mode means that in power saving mode, all the power supplies to camera module are kept. The cameras are set into power down mode by pull high PWDN pin.

Power off mode means that in power saving mode, all the power supplies to camera module are cut.

4.2 Camera Operation in Power Down Mode

To support power down mode for power saving, the DOVDD of OV5640 should be 1.8V and DVDD is generated by internal regulator. If DOVDD of OV5640 is higher than 1.8V, the power down mode can not be used for power saving. But it still could be used for sharing SCCB bus with other I2C device or share single DVP port with other cameras.

4.2.1 Battery On



t0: >= 0ms. Delay from DOVDD stable to AVDD stable.
t2: >= 5ms. Delay from AVDD stable to sensor power up stable.
t3: >= 1ms. Delay from sensor power up stable to Reset# pull high.
t4: >=20ms. Delay from Reset pull high to SCCB initialization.

Step 1:
Reset# is applied to OV5640 camera module. PWDN is pulled high.

Step 2:
DOVDD and AVDD powers are applied. The 2 powers could be applied simultaneously. If applied separately, the power on sequence should be DOVDD first, and AVDD last.

Step 3:
after 5ms of AVDD reaching stable, pull PWDN to low.

Step 4:
after 1ms of PWDN go low, pull high Reset#.

Step 5:
After 20ms, initialize OV5640 by SCCB initialization. Please find the settings from "OV5640 Camera Module Software Application Notes" or contact with OmniVision local FAE.

Step 6:
Pull high PWDN. Set OV5640 to power down mode.

Step 7:
Pull XCLK low.

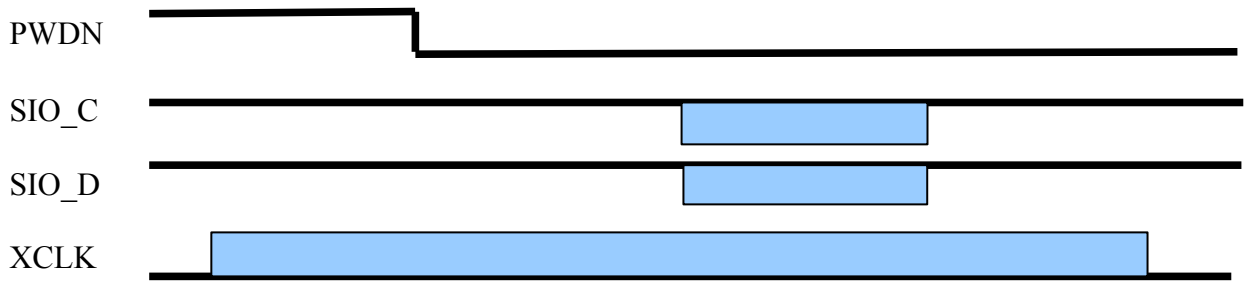
After battery on, OV5640 camera should be initialized first, then set to power down mode.

4.2.2 Wake up From Power Down

Step 1:
Apply XCLK

Step 2:
after 10ms, Pull low PWDN

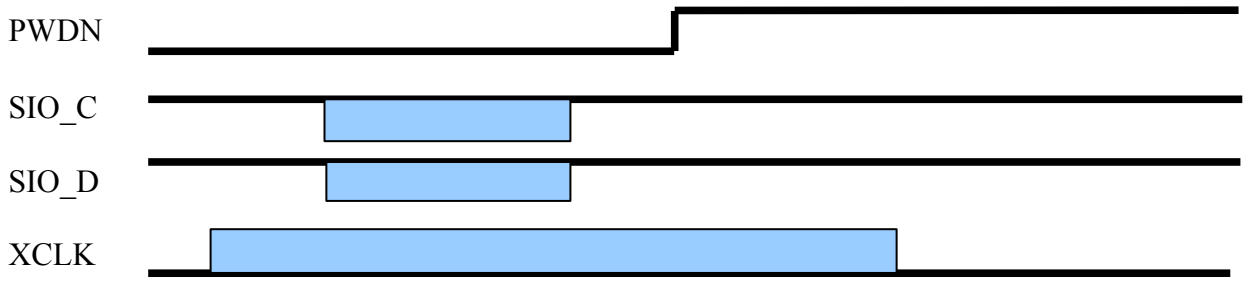
Optional Step 3:
Full SCCB Initialization. Please find the settings from "OV5640 Camera Module Software Application Notes" or contact with OmniVision local FAE.



4.2.3 Power Down

Step 1:
Pull PWDN pin high.

Step 2:
Pull XCLK low



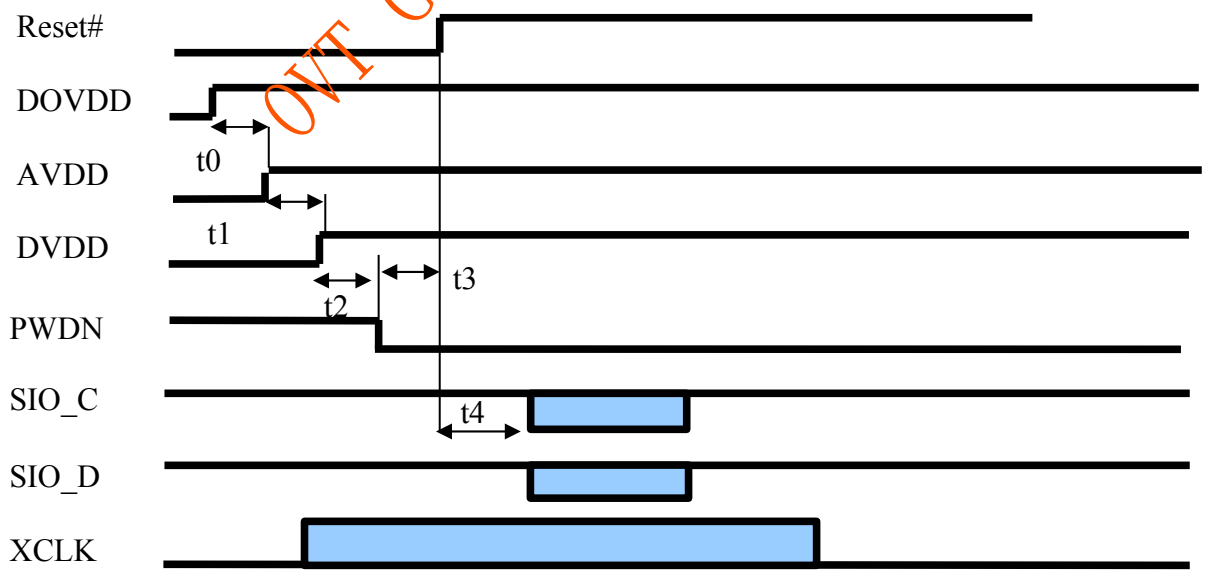
4.3 Camera Operation in Power Off Mode

If DOVDD of OV5640 is higher than 1.8V, and DVDD is generated by internal regulator, the voltage drop across the internal regulator is too big. There is potential over heat issue. So the DVDD should be provided by external power supply to prevent over heat if DOVDD is higher than 1.8V. In this situation, power down mode is not supported. Power off mode is used for power saving.

4.3.1 Battery On

No operation. Camera module is power off.

4.3.2 Camera On



t0: >= 0ms. Delay from DOVDD stable to AVDD stable.
t1: >= 0ms. Delay from AVDD stable to DVDD stable.
t2: >= 5ms. Delay from DVDD stable to sensor power up stable.
t3: >= 1ms. Delay from sensor power up stable to Reset# pull high.
t4: >=20ms. Delay from Reset pull high to SCCB initialization.

Step 1:
Reset# is applied to OV5640 Camera Module.

Step 2:
DOVDD, DVDD and AVDD powers are applied. The 3 powers could be applied simultaneously. If applied separately, the power on sequence should be DOVDD first, AVDD second and DVDD last.

Step 3:
after 5ms of last power applied, pull low PWDN.

Step 4:
after 1ms. Pull high Reset#.

Step 5:
After 20ms, initialize OV5640 by SCCB initialization. Please find register setting from "OV5640 Camera Module Hardware Application Notes" or contact OmniVision local FAE for initialization settings.

Note: If there is no powerdown pin in your module, this means powerdown pin is connect with GND.

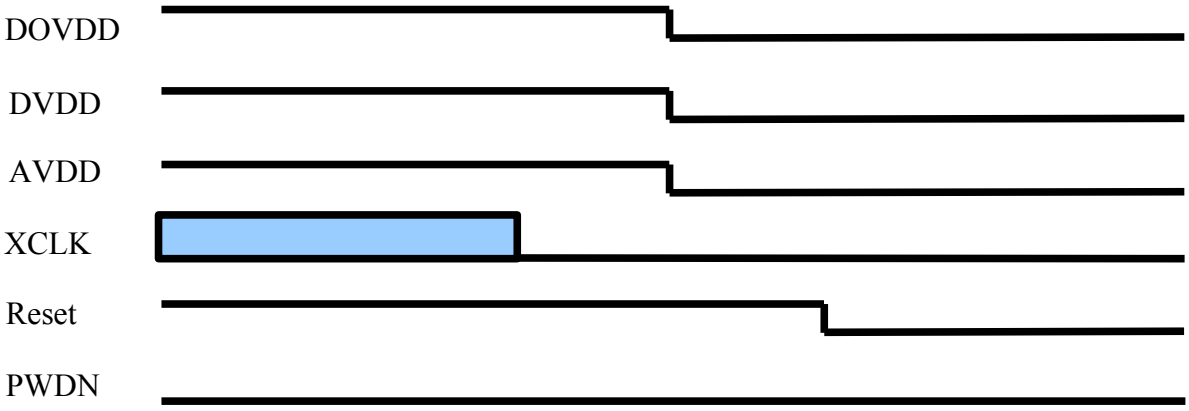
4.3.3 Camera Off

Step 1.
Pull low XCLK,

Step 2.
Turn off AVDD, DVDD and DOVDD. The 3 powers could be turned off simultaneously. If turned off separately, DVDD should be turned off first, AVDD second and DOVDD third.

Step 3.

Pull Low PWDN and RESET



5. SCCB Bus sharing

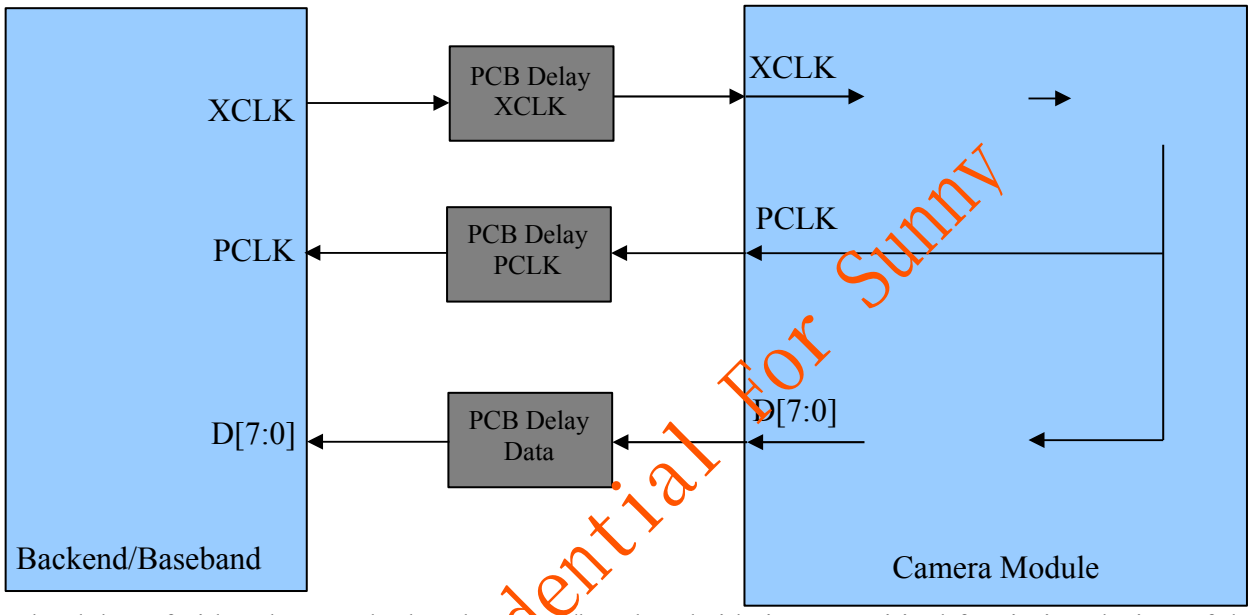
The SCCB bus of OV5640 camera module could be shared with other I2C device. When OV5640 is working, the read/write operation is separated by device address. The device address of OV5640 is 0x78 for write and 0x79 for read. I2C read/write to address other than the 2 address above will not affect SCCB registers of OV5640.

If device address of OV5640 conflict with other I2c devices, OV5640 should be put into power down mode or power off mode to access other I2c device. When OV5640 camera module is power down or power off, the SCCB Bus is leave free. The SCCB of OV5640 doesn't affect the read/write of other I2C device.

6. Timing Considerations for Phone PCB Design

There are 2 clock signal for OV5640 camera module. One is the main clock (input clock) XCLK, the other is the pixel clock (output clock) PCLK. Some backend/baseband chips may use XCLK as pixel sample clock, some backend/baseband chips may use PCLK as pixel sample clock. **It is recommended to use PCLK as pixel sample clock.**

Let's look at the clock distribution first.



So the delay of video data to clock at backend/baseband side is very critical for timing design. If the delay is over the spec. of backend/baseband chip, the backend/baseband chip can not get video data correctly. The incorrect video data may have wrong color, fixed or moving horizontal lines.

From the clock distribution diagram above, the delays are:

Delay_XCLK = 0

Delay_PCLK = PCB_Delay_XCLK + Internal_Delay + PLL_Delay + PCB_Delay_PCLK

Delay_Data = PCB_Delay_XCLK + Internal_Delay + PLL_Delay + PCLK_to_Data_Delay + PCB_Delay_Data

6.1 Sample with PCLK

If Backend/baseband sample video data with PCLK, the clock data delay is

clock_data_delay = Delay_Data – Delay_PCLK

= PCLK_to_Data_Delay + PCB_Delay_Data – PCB_Delay_PCLK

The clock data delay is not related with PCB delay of XCLK.

If PCB is carefully designed so that the wire length of PCLK and Data are same, then PCB_Delay_Data = PCB_Delay_PCLK, the clock data delay is

clock_data_delay = PCLK_to_Data_Delay, not related to PCB layout

6.2 Sample with XCLK

If Backend/baseband sample video data with PCLK, the clock data delay is

clock_data_delay = Delay_Data – Delay_XCLK

= PCB_Delay_XCLK + Internal_Delay + PLL_Delay + PCLK_to_Data_Delay + PCB_Delay_Data

The data to clock delay at Baseband/Backend chip are much bigger than sampled with PCLK. And the delay is highly depend on PCB layout. So if XCLK is used to sample video data, it is very likely to have timing issue which would cause incorrect video data.

6.3 Using EMI/ESD Device

If EMI/ESD device are used in phone design, the PCB delay increase very much. It should be very careful to manipulate the delays to meet timing spec. of backend/baseband chips.

1. Try to use PCLK as sample clock of video data.
2. XCLK and PCLK should not share ESD/EMI device with other signals. Use dedicate ESD/EMI device or R/C filters for XCLK and PCLK. So that the delay on XCLK and PCLK could be adjusted later.
3. For dual camera module, use single ESD/EMI device or single R/C filter for XCLK and PCLK to minimize clock delay.
4. Carefully layout PCB to keep XCLK wire as short as possible, PCLK wire the same length as data lines.
5. Minimize the length of FPC of camera module.

7. Hardware Check List

7.1 Check Hardware Design

7.1.1 Module Function

Check camera module function with USB 2.0 test board (Module interface board may be needed, please contact with module maker). The module should display image correctly on PC.

Check module schematic design, pin definition match with camera interface of phone. Analog ground and digital ground are separated inside camera module.

7.1.2 Check Camera Interface of Phone

Pin definition matches with camera module design.

AVDD is supplied by separate regulator. DVDD and DOVDD could be supplied by separate regulator or shared regulator with other circuits. The voltage of each power supplied are within sensor specification.

If there is a long flex cable to connect camera module to main board of phone, please make sure the ground of camera module is not shared with other circuits. For flip type phone, share camera ground with LCD module would cause very strong power/ground noise.

7.2 Check if Camera Module is Working

Evidence of camera module working

PCLK output

HREF, VSYNC outputs

D[9:0] output

Check procedures

a. Voltages of power supplies are within sensor specification

b. input clock is correct

c. all input signals are in correct state

PWDN = in active, Reset = in active, SIO_D = H, SIO_C = H

d. for OV5640 and later, please check SCCB initialization waveform to make sure SCCB initialization is completed.

If all the check are passed, the camera module still can not work, please check if the camera module is damaged or contact OmniVision local FAE.

7.3 Check SCCB

a. Check SCCB connection: Pull up resistors exist. Recommended value is around 4.7K.

b. SCCB write speed should not be too fast for first debug. Recommended not over 100K. The write speed could be increased up to 400K later on.

c. Simple ways to check SCCB

SCCB read could be verified by read register 0x0a, 0x0b (version).

SCCB write could be verified by write register 0x11 and check PCLK frequency.

d. To make sure SCCB read/write are correct, please use oscilloscope to capture whole waveforms of SCCB initialization.

e. Make sure the SCCB device ID is correct for read/write operation.

SCCB address is 0xc0/0xc1 for CIF sensors

SCCB address is 0x42/0x43 for VGA sensors

SCCB address is 0x60/0x61 for 1.3M and 2.0M sensors

SCCB address is 0x78/0x79 for 3.0M， 5.0M sensors

f. If SCCB soft reset is used, please wait at least 2~5ms after SCCB soft rest.

7.4 Check Camera Interface

a. Check polarity of HREF(HSYCN), VSYNC, PCLK, make sure the polarity of camera module matches with backend or baseband side.

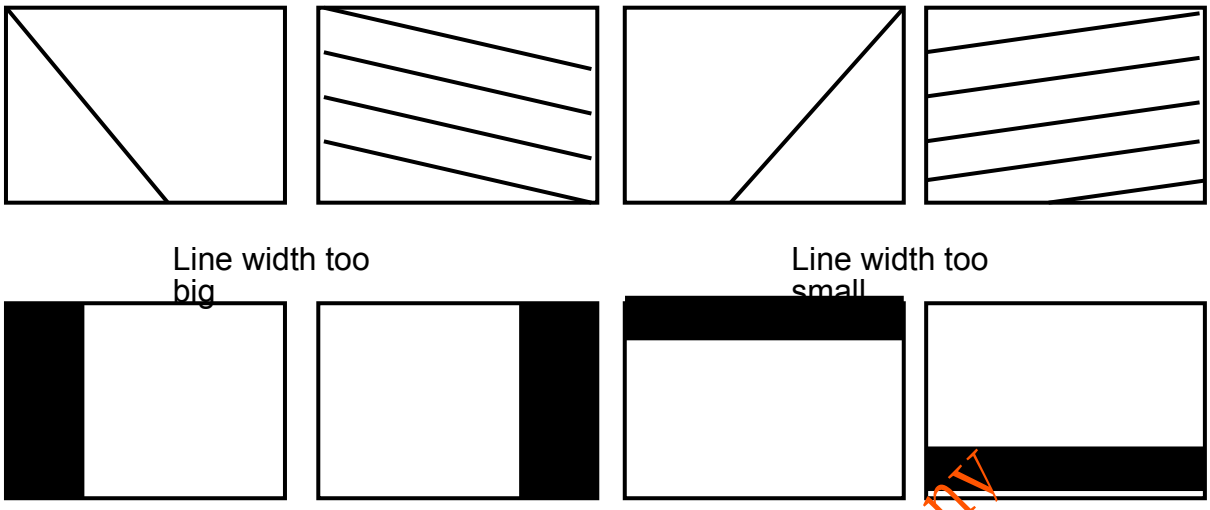
b. Check sample clock. Please pay attention to baseband/backend sample with MCLK. In this case, the clock divider inside sensor could not be turned on. Please also pay attention to possible timing issues listed in section 5.

c. check window position.

If camera interface uses HREF, then the window position is defined by sensor.

If camera interface uses HSYNC, then the window position is defined by backend / baseband.

7.5 Some Typical Issues

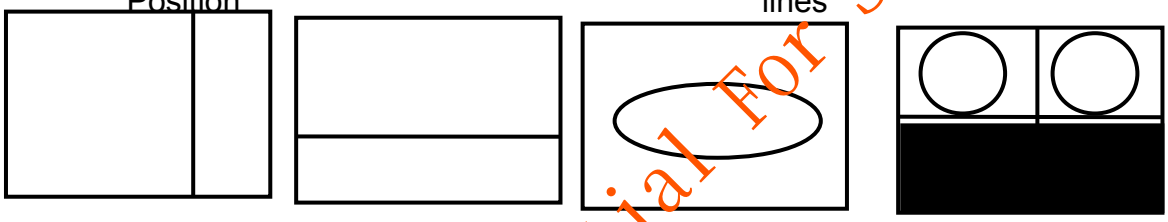


Line width too big

Line width too small

Wrong Window Position

In sufficient output lines

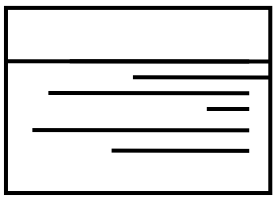


Horizontal Sync Issue

Vertical Sync Issue

Sample Rate too High

Sample rate too low



Timing Issue

7.6 Image Direction

7.6.1 Sensor 4:3, LCD 3:4

Full screen display is not full view angle

Full view angle display is not full screen

Full view angle

Full Screen

Camera module

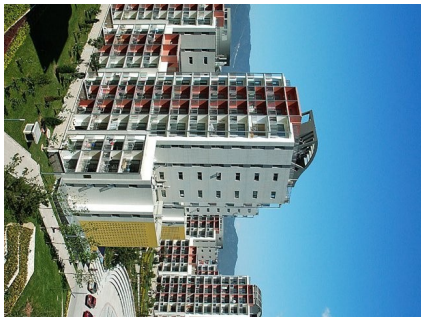
7.6.2 Sensor 3:4, LCD 3:4

Sensor rotate 90 degree in camera module

Picture scan line direction should be changed by phone

Full Screen and Full view angle on LCD

Full view angle & Full Screen



Change scan line direction of camera

7.7 Check Color/Brightness

a. There are only red/green color in picture

Y and U/V exchanged.

b. R/B exchange

U/V exchange

c. color/brightness not continuous

check connection of d[9:0]

7.8 Check Image Center

Place an object in front of camera module, check if the picture is on center of LCD. If not, the output window of camera is not correct.

Revision History