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**CS210- Lab 12:**

**Study of multi- Cycle Processor/Pipelined MIPS processor**

**Task 1: Study the given pipeline implementation of the processor, and identity error in the design (if any) . Convert the following C code to MIPS assembly, test the code in MIPS pipelined version(Given) .**

**for(i = 0; i < 100; i++)**

**A[i] = i;**  (**30 points)**

**Answer 1:**

**MIPS code:**

addiu $t0,$0,0

addiu $t1,$0,100

addiu $t2,$0,1

addiu $t5,$0,4

addiu $t4,$0,0

#stored at address 0

addiu $s0,$0,0

for:

slt $t3,$t0,$t1

beq $t3,$t4,done

sw $t0,0($s0)

add $s0,$s0,$t5

add $t0,$t0,$t2

beq $0,$0,for

**done:**

**The assembled code:**

24080000

24090064

240a0001

240d0004

240c0000

24100000

0109582a

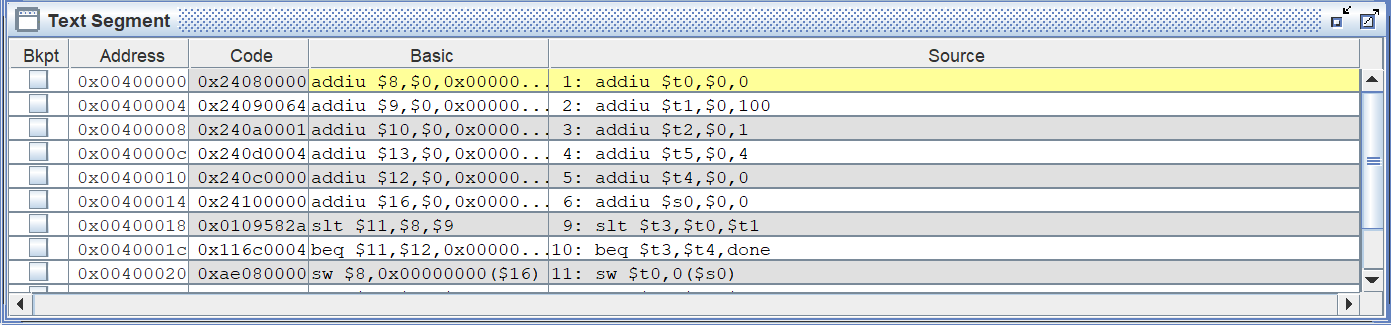
116c0004

ae080000

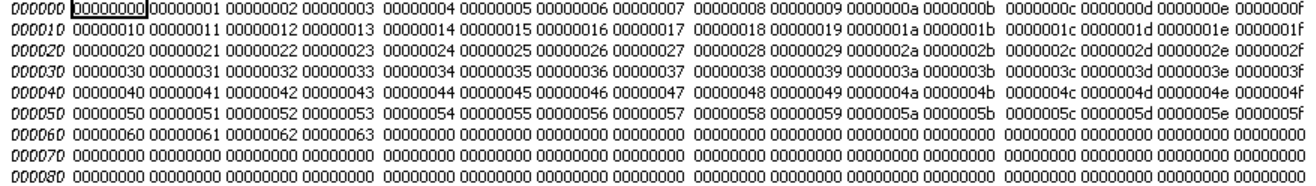
020d8020

010a4020

1000fffa



**The numbers stored in memory:**

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Numbers stored in RAM are shown above.

**Task 2:** ***Write ASCII values of your name full name to the memory using appropriate instruction, and write program to find the sum of those values using the given pipeline MIPS design. Computer the number of cycles required and compare with number of cycles that you got in previous(Multi-cycle implementation).* Enter the relevant information in the r*ecord* for demonstration*.***

**(30 points)**

**Answer 2:**

**MIPS code:**

#Name->atul pande

# a->97->61

# t->116->74

# u->117->75

# l->108->6c

# p->112->70

# n->110->6e

# d->100->64

# e->101->65

addiu $s0,$0,0

# for 'a'

addiu $t0,$0,0x61

sw $t0,0($s0)

# for 't'

addiu $t0,$0,0x74

sw $t0,4($s0)

# for 'u'

addiu $t0,$0,0x75

sw $t0,8($s0)

# for 'l'

addiu $t0,$0,0x6c

sw $t0,12($s0)

# for 'p'

addiu $t0,$0,0x70

sw $t0,16($s0)

# for 'a'

addiu $t0,$0,0x61

sw $t0,20($s0)

# for 'n'

addiu $t0,$0,0x6e

sw $t0,24($s0)

# for 'd'

addiu $t0,$0,0x64

sw $t0,28($s0)

# for 'e'

addiu $t0,$0,0x65

sw $t0,32($s0)

**The assembled code:**

24100000

24080061

ae080000

24080074

ae080004

24080075

ae080008

2408006c

ae08000c

24080070

ae080010

24080061

ae080014

2408006e

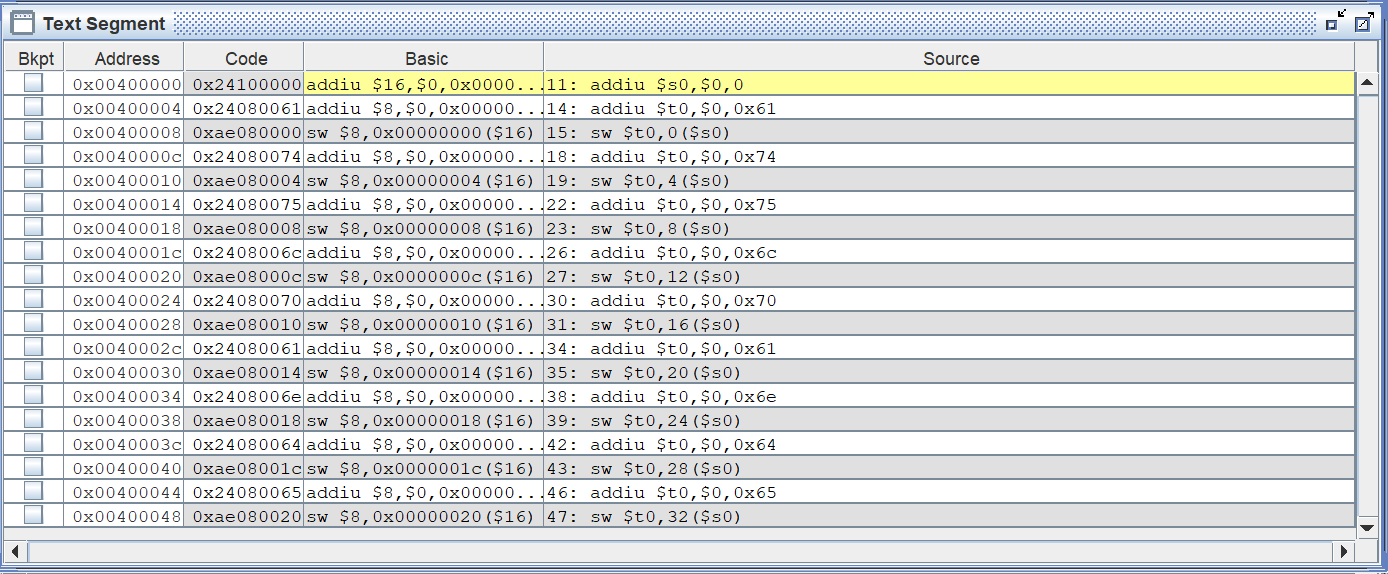
ae080018

24080064

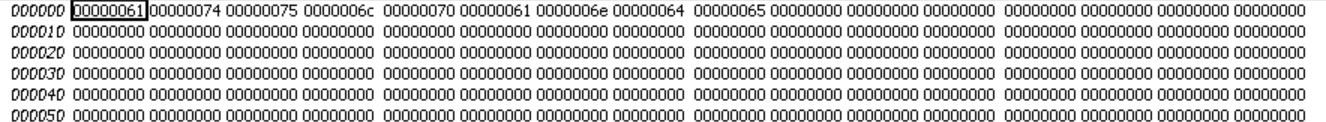
ae08001c

24080065

ae080020

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**The ASCII values stored in memory:**

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The ASCII values stored in memory.

**Calculation of CPI:**

Due to delay the CPI of multicycle processor is generally greater than the ideal case of 1.

Cpi of multicycle:

Addui(R-type)->10

Sw->9 times

Both addiu and sw are 4 cycle each:

(10\*4+9\*4)/19= 4

In pipeline processor the first two instructions take 6 cycles since there is no delay. However, since the instructions are only R-type and sw each instruction has to wait for mem/reg write before reg read is operated.   
Therefore CPI is:  
3\*17+2(The first two instructions) = 53-16 (forwarding) cycles. CPI=37/19 = ~1.947

**Task 3: Add one new instructions to the given architecture and test using new test program.**

**(40 points)**

Implemented in attached circ file.

Max of two numbers implemented.

Max(a,b) implemented where a and b are input.