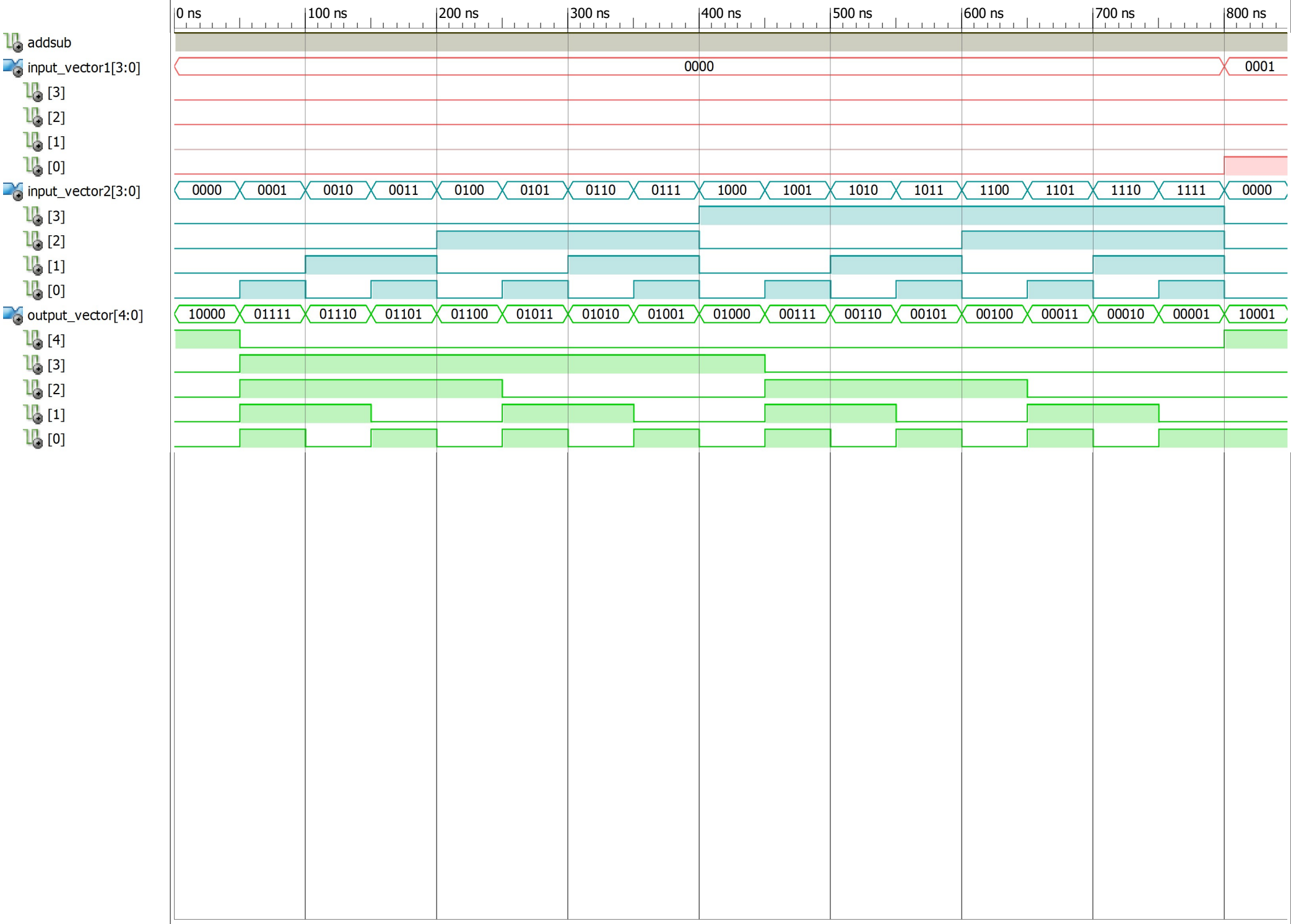
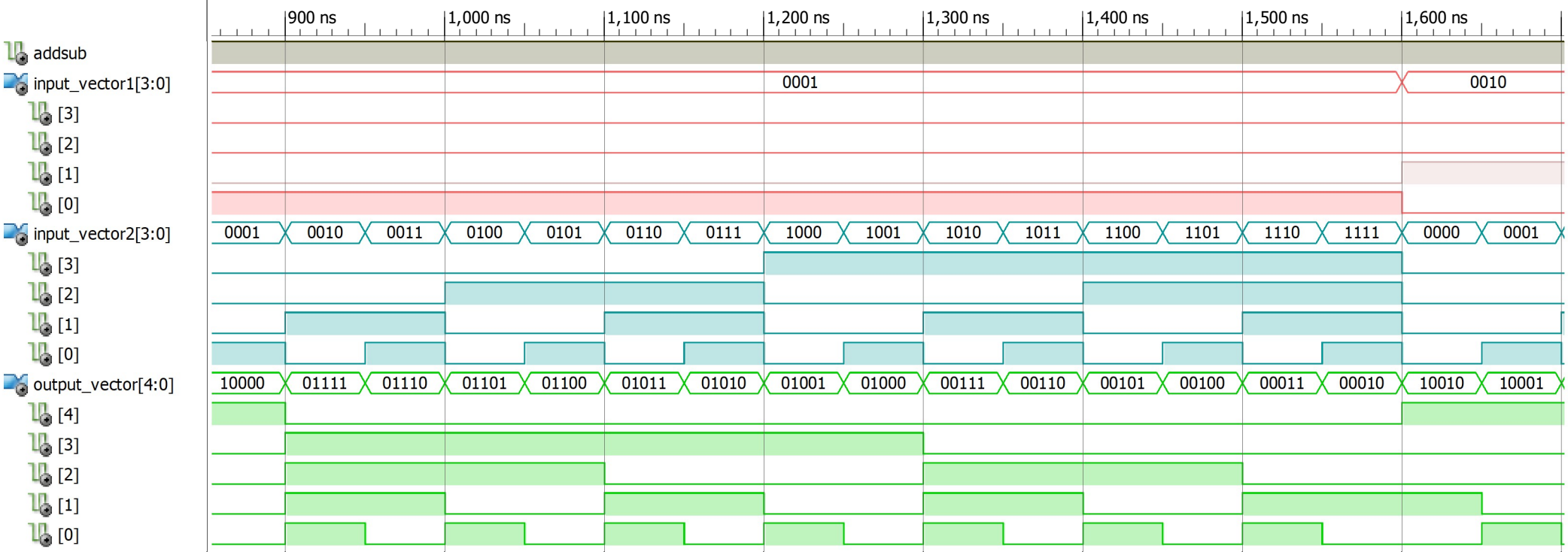
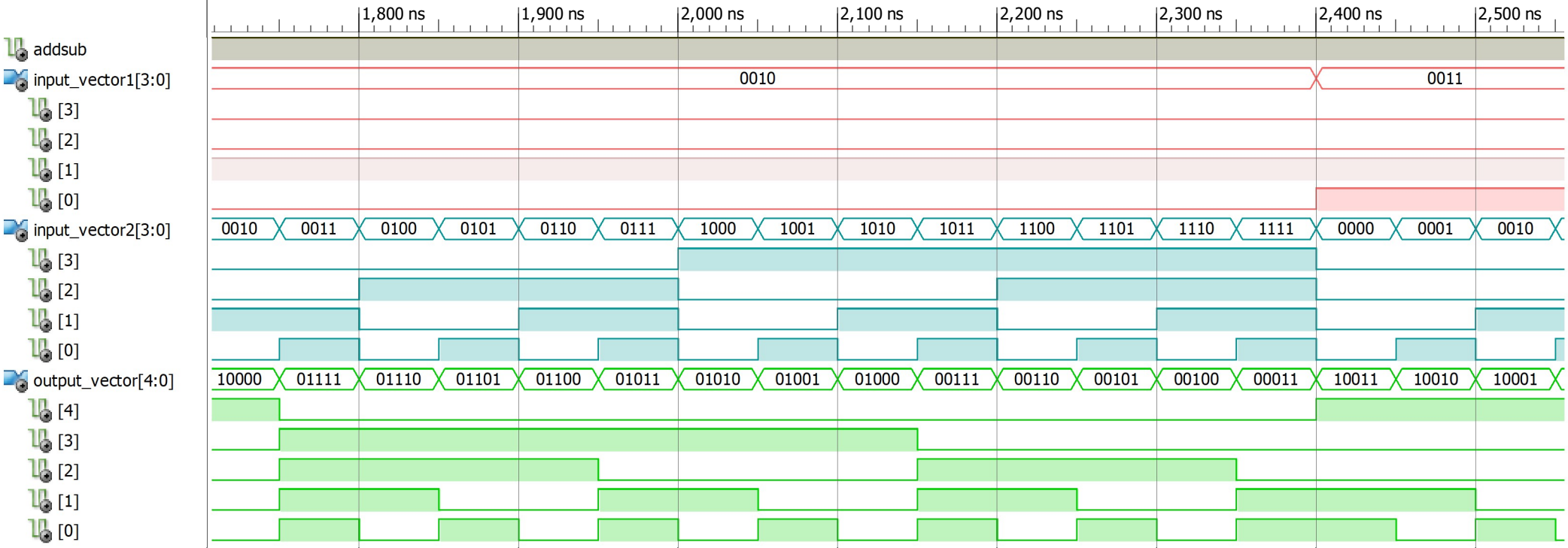
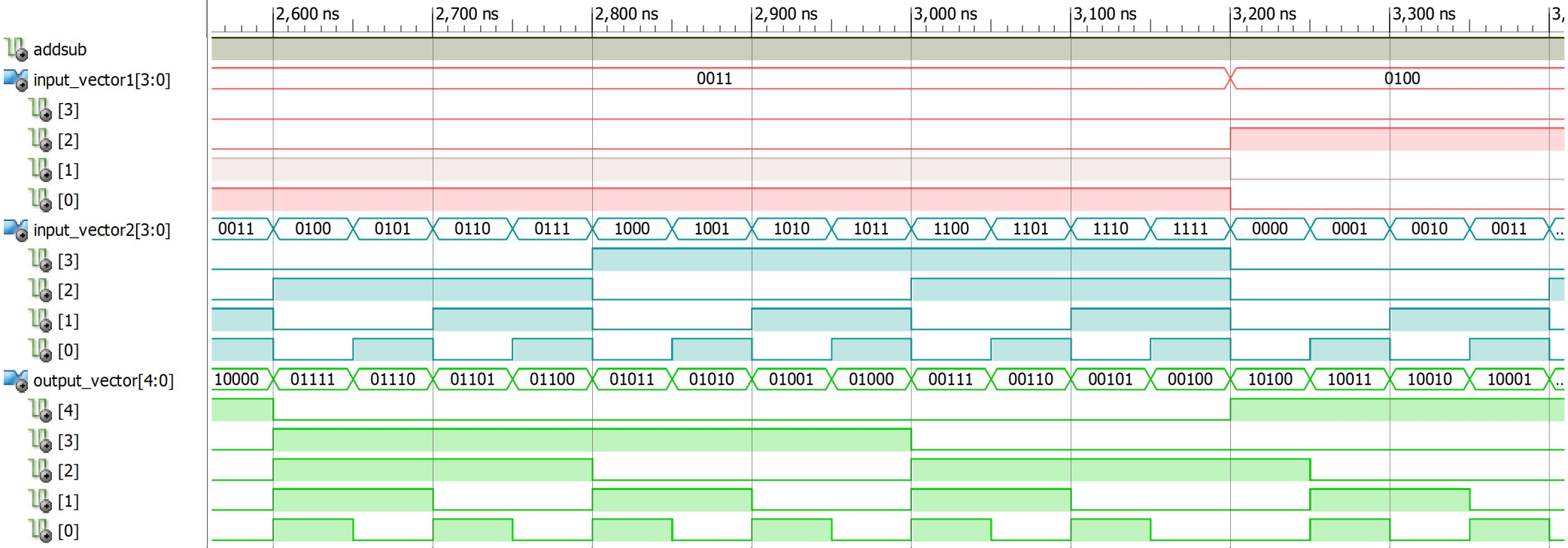
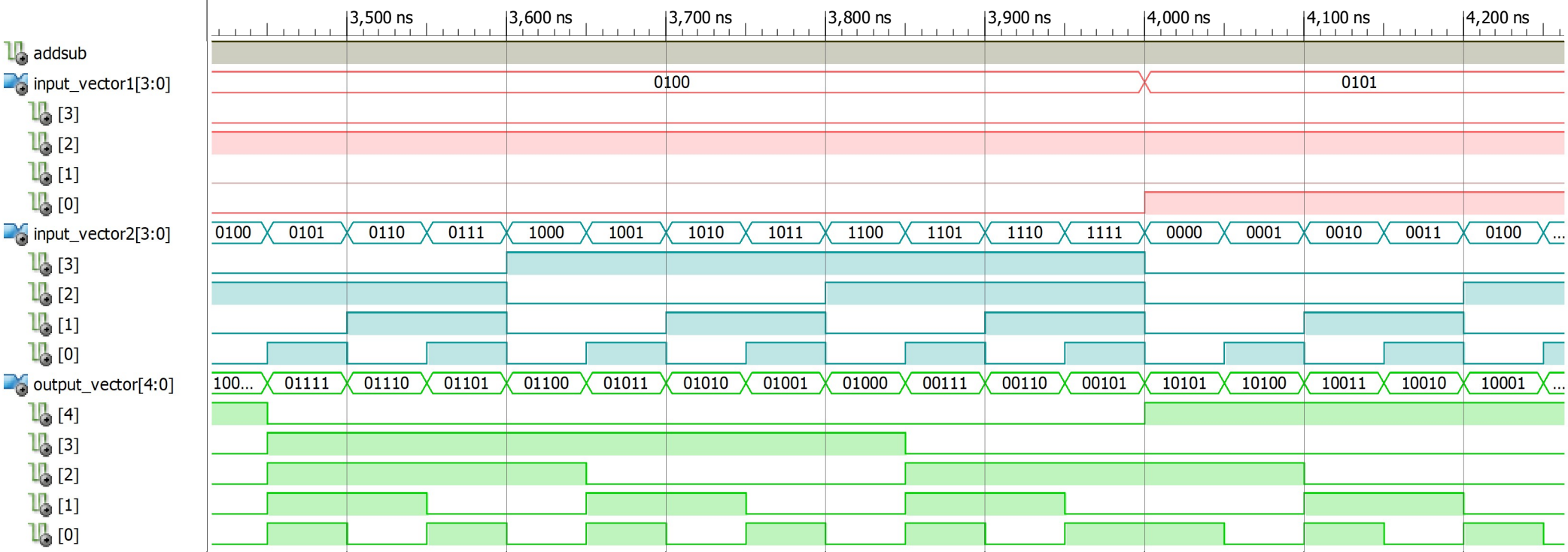
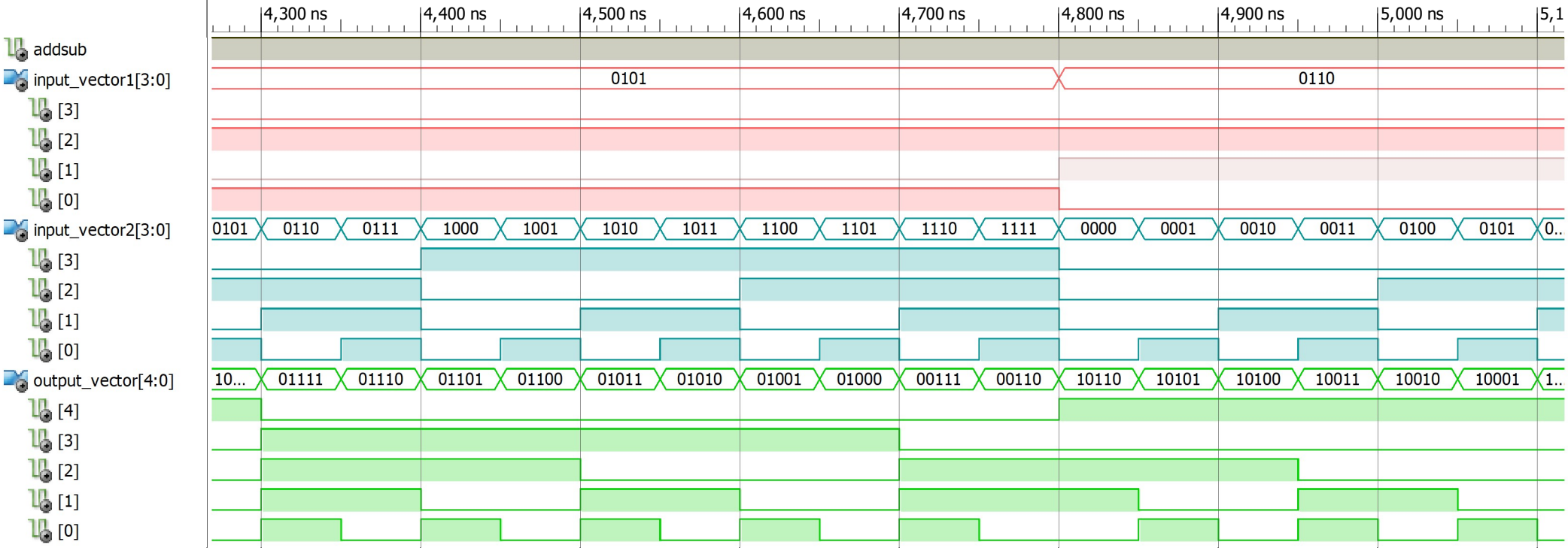

0 ns
100 ns
200 ns
300 ns
400 ns
500 ns
600 ns
700 ns
800 ns
addsub
input_vector1[3:0]
[3]
[2]
[1]
[0]
0000
0001
input_vector2[3:0]
0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 0000
[3]
[2]
[1]
[0]
output_vector[4:0]
10000 01111 01110 01101 01100 01011 01010 01001 01000 00111 00110 00101 00100 00011 00010 00001 10001
[4]
[3]
[2]
[1]
[0]

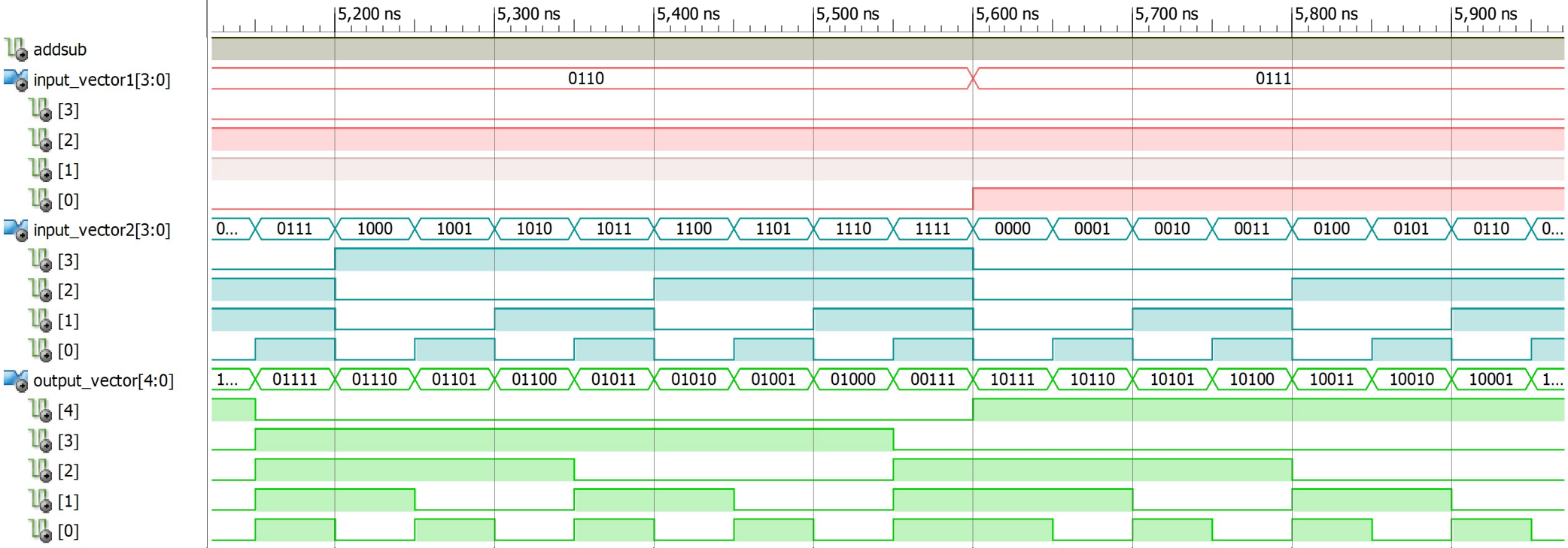

900 ns
1,000 ns
1,100 ns
1,200 ns
1,300 ns
1,400 ns
1,500 ns
1,600 ns
addsub
input_vector1[3:0]
[3]
[2]
[1]
[0]
0001
0010
input_vector2[3:0]
0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 0000 0001
[3]
[2]
[1]
[0]
output_vector[4:0]
10000 01111 01110 01101 01100 01011 01010 01001 01000 00111 00110 00101 00100 00011 00010 10010 10001
[4]
[3]
[2]
[1]
[0]

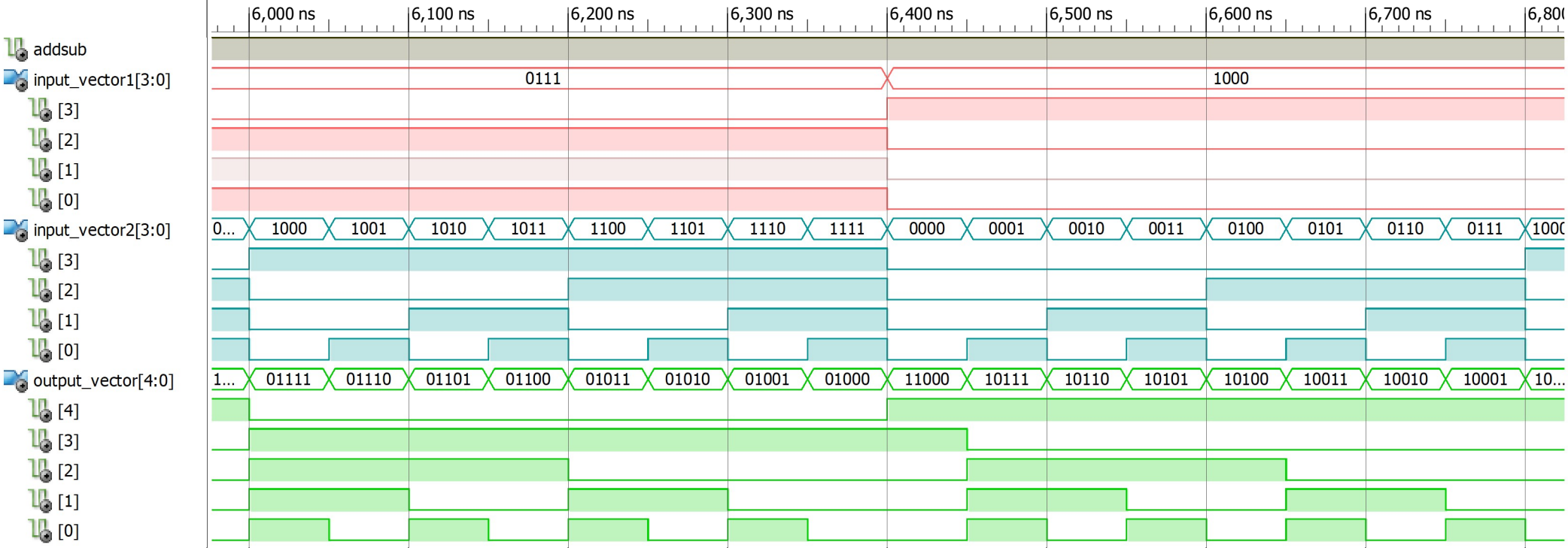

1,800 ns
1,900 ns
2,000 ns
2,100 ns
2,200 ns
2,300 ns
2,400 ns
2,500 ns
addsub
input_vector1[3:0]
[3]
[2]
[1]
[0]
0010
0011
input_vector2[3:0]
0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 0000 0001 0010
output_vector[4:0]
10000 01111 01110 01101 01100 01011 01010 01001 01000 00111 00110 00101 00100 00011 10011 10010 10001

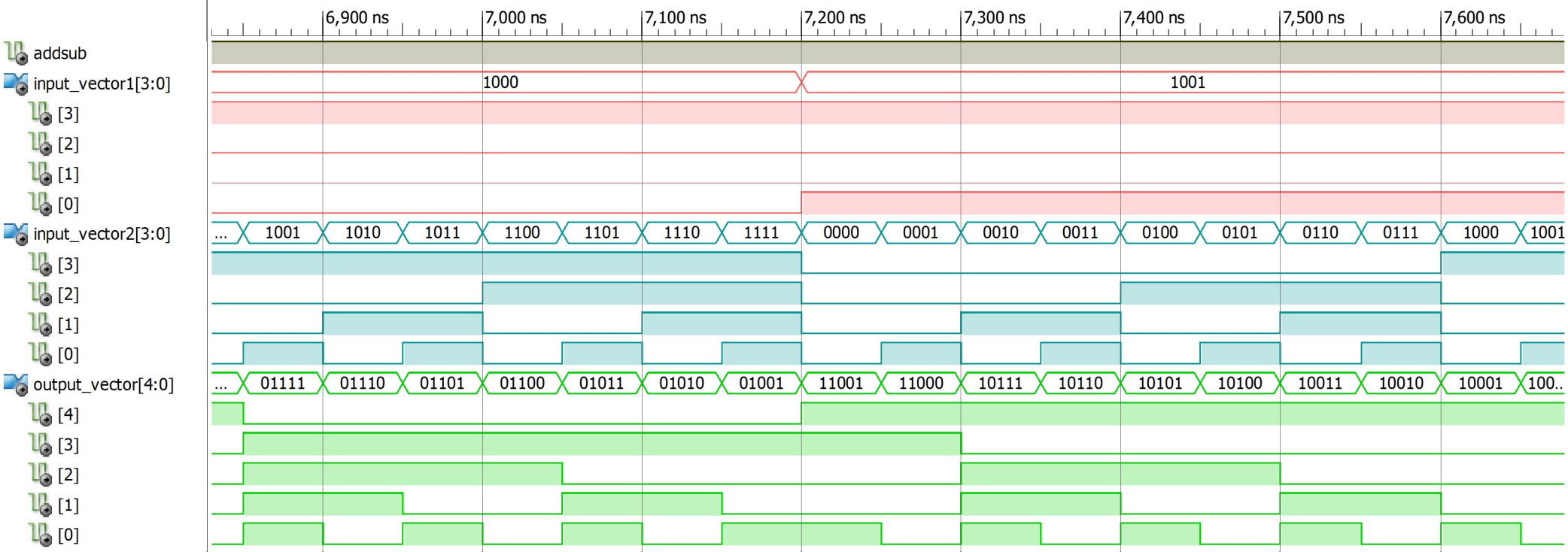

2,600 ns
2,700 ns
2,800 ns
2,900 ns
3,000 ns
3,100 ns
3,200 ns
3,300 ns
addsub
input_vector1[3:0]
0011
0100
[3]
[2]
[1]
[0]
input_vector2[3:0]
0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 0000 0001 0010 0011
[3]
[2]
[1]
[0]
output_vector[4:0]
10000 01111 01110 01101 01100 01011 01010 01001 01000 00111 00110 00101 00100 10100 10011 10010 10001
[4]
[3]
[2]
[1]
[0]

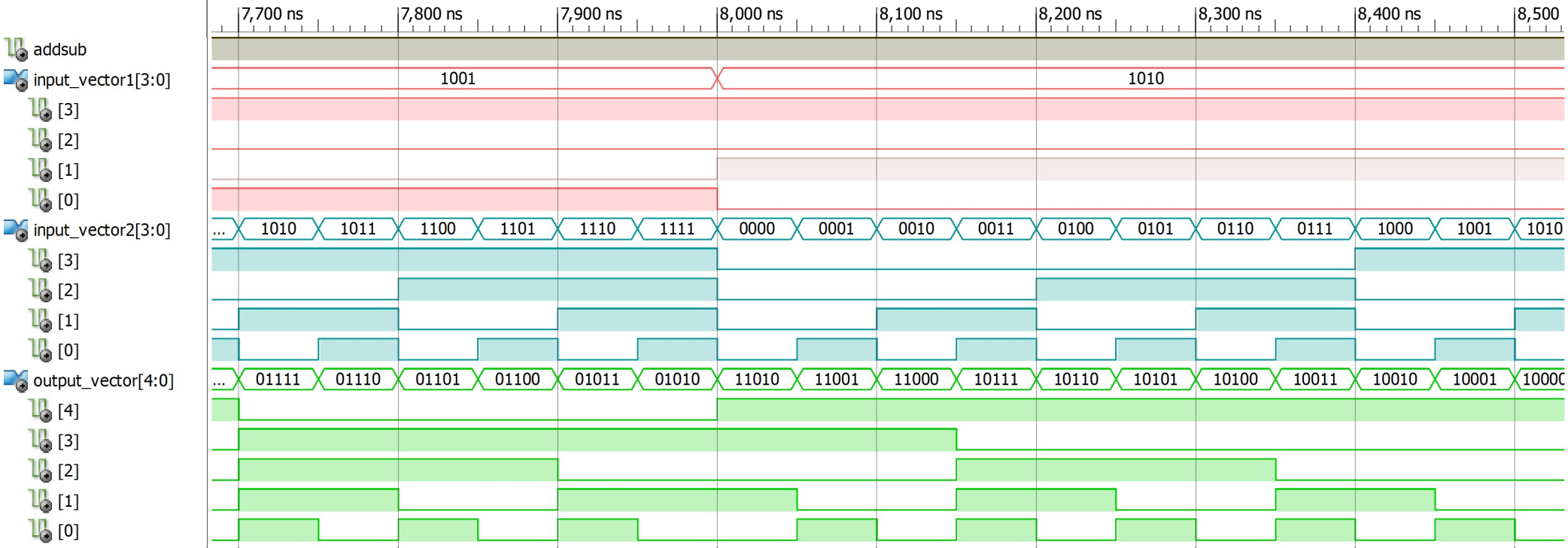

3,500 ns
3,600 ns
3,700 ns
3,800 ns
3,900 ns
4,000 ns
4,100 ns
4,200 ns
addsub
input_vector1[3:0]
[3]
[2]
[1]
[0]
0100
0101
input_vector2[3:0]
0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 0000 0001 0010 0011 0100 ...
[3]
[2]
[1]
[0]
output_vector[4:0]
100... 01111 01110 01101 01100 01011 01010 01001 01000 00111 00110 00101 10101 10100 10011 10010 10001 ...
[4]
[3]
[2]
[1]
[0]

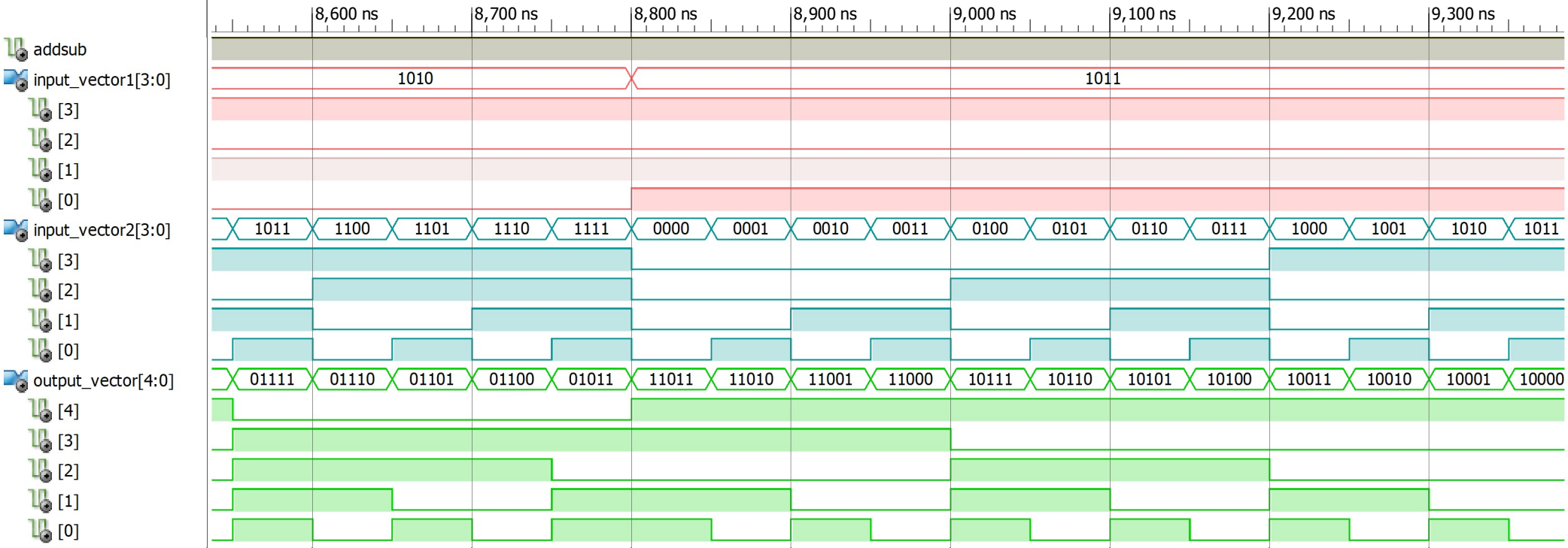

4,300 ns
4,400 ns
4,500 ns
4,600 ns
4,700 ns
4,800 ns
4,900 ns
5,000 ns
addsub
input_vector1[3:0]
0101
0110
[3]
[2]
[1]
[0]
input_vector2[3:0]
0101 0110 0111 1000 1001 1010 1011 1100 1101 1110 1111 0000 0001 0010 0011 0100 0101
[3]
[2]
[1]
[0]
output_vector[4:0]
10... 01111 01110 01101 01100 01011 01010 01001 01000 00111 00110 10110 10101 10100 10011 10010 10001
[4]
[3]
[2]
[1]
[0]

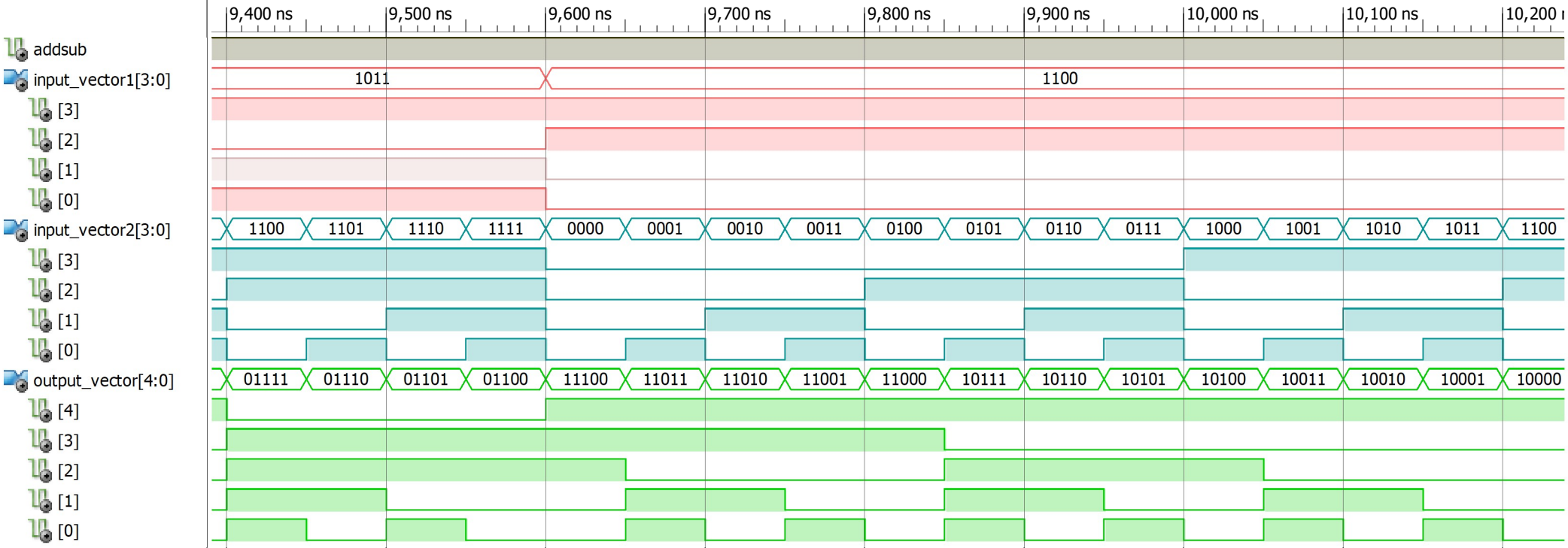

5,200 ns
5,300 ns
5,400 ns
5,500 ns
5,600 ns
5,700 ns
5,800 ns
5,900 ns
addsub
input_vector1[3:0]
0110
0111
[3]
[2]
[1]
[0]
input_vector2[3:0]
0... 0111 1000 1001 1010 1011 1100 1101 1110 1111 0000 0001 0010 0011 0100 0101 0110 0...
[3]
[2]
[1]
[0]
output_vector[4:0]
1... 01111 01110 01101 01100 01011 01010 01001 01000 00111 10111 10110 10101 10100 10011 10010 10001 1...
[4]
[3]
[2]
[1]
[0]

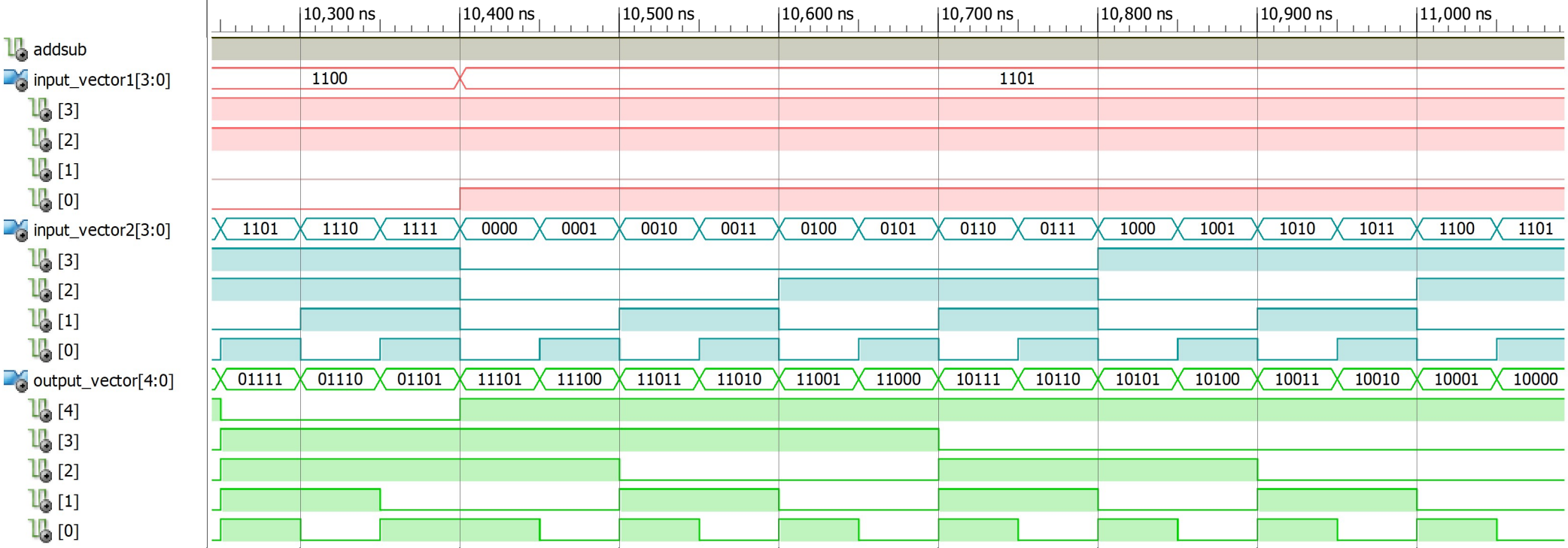

6,000 ns
6,100 ns
6,200 ns
6,300 ns
6,400 ns
6,500 ns
6,600 ns
6,700 ns
addsub
input_vector1[3:0]
0111
1000
[3]
[2]
[1]
[0]
input_vector2[3:0]
0...
1000
1001
1010
1011
1100
1101
1110
1111
0000
0001
0010
0011
0100
0101
0110
0111
[3]
[2]
[1]
[0]
output_vector[4:0]
1...
01111
01110
01101
01100
01011
01010
01001
01000
11000
10111
10110
10101
10100
10011
10010
10001
10...
[4]
[3]
[2]
[1]
[0]

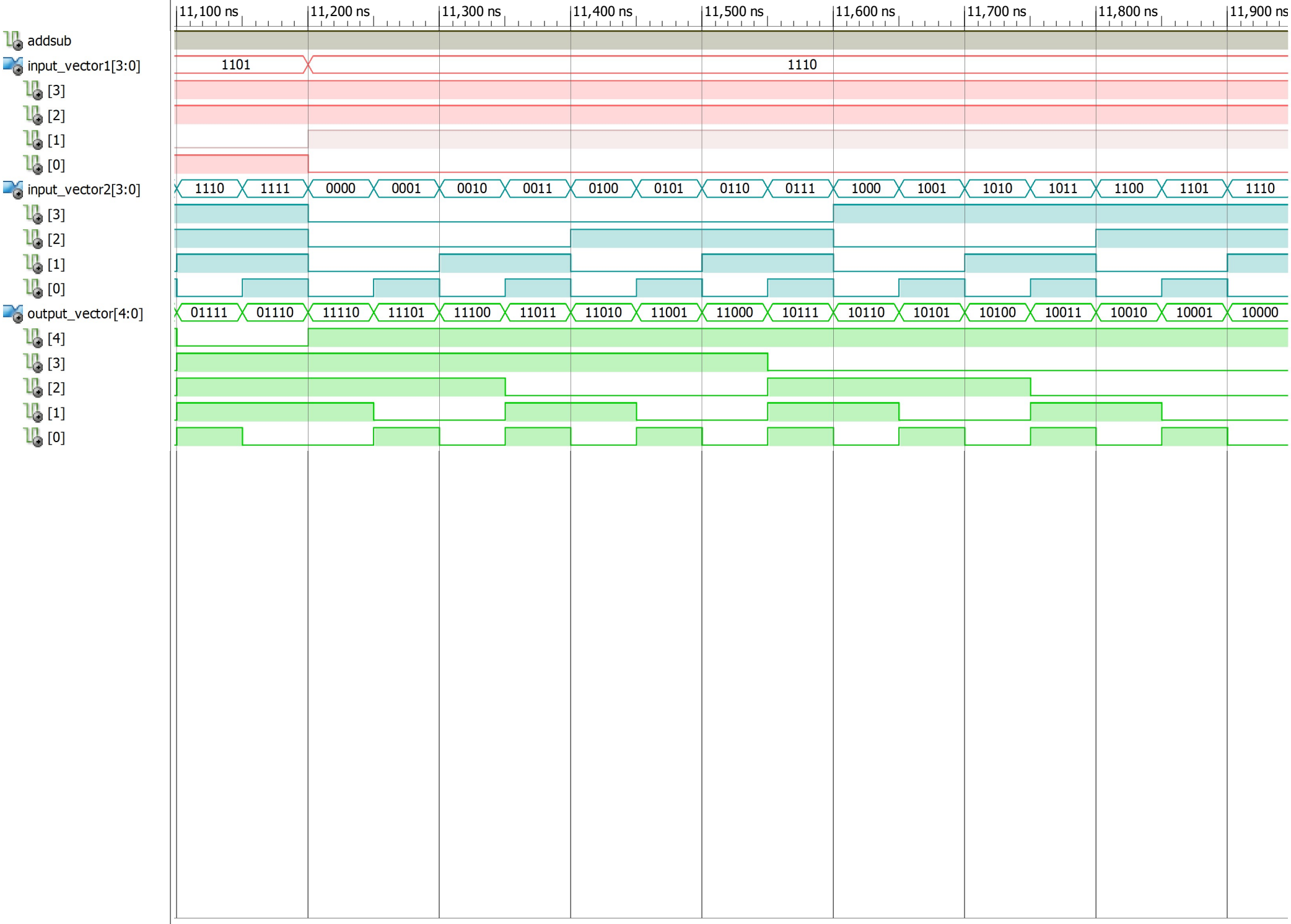

6,900 ns
7,000 ns
7,100 ns
7,200 ns
7,300 ns
7,400 ns
7,500 ns
7,600 ns
addsub
input_vector1[3:0]
[3]
[2]
[1]
[0]
1000
1001
input_vector2[3:0]
[3]
[2]
[1]
[0]
... 1001 1010 1011 1100 1101 1110 1111 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001
output_vector[4:0]
[4]
[3]
[2]
[1]
[0]
... 01111 01110 01101 01100 01011 01010 01001 11001 11000 10111 10110 10101 10100 10011 10010 10001 100..

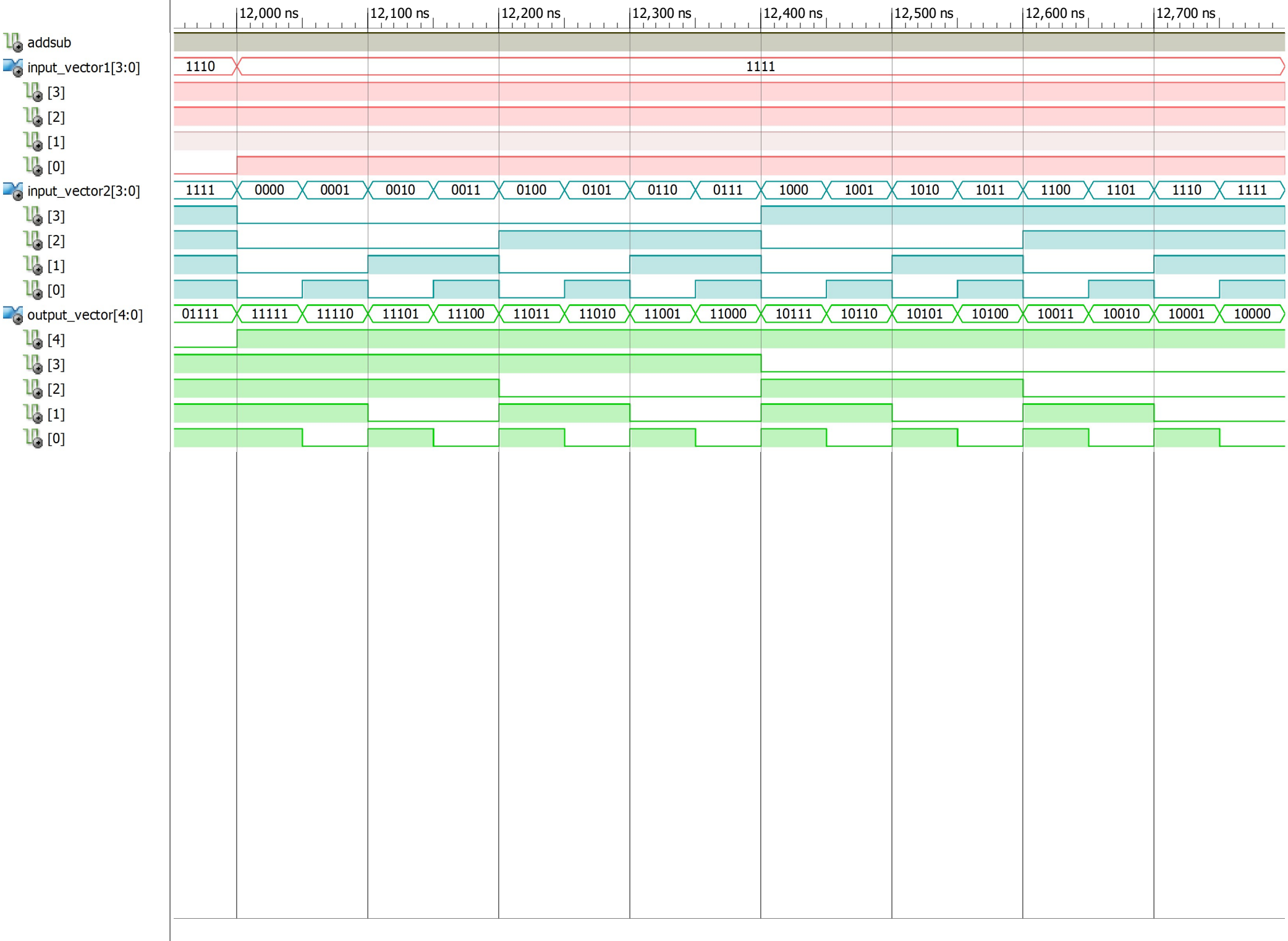

7,700 ns
7,800 ns
7,900 ns
8,000 ns
8,100 ns
8,200 ns
8,300 ns
8,400 ns
8,500
addsub
input_vector1[3:0]
[3]
[2]
[1]
[0]
1001
1010
input_vector2[3:0]
[3]
[2]
[1]
[0]
... 1010 1011 1100 1101 1110 1111 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010
output_vector[4:0]
[4]
[3]
[2]
[1]
[0]
... 01111 01110 01101 01100 01011 01010 11010 11001 11000 10111 10110 10101 10100 10011 10010 10001 10000


8,600 ns
8,700 ns
8,800 ns
8,900 ns
9,000 ns
9,100 ns
9,200 ns
9,300 ns
addsub
input_vector1[3:0]
1010
1011
[3]
[2]
[1]
[0]
input_vector2[3:0]
1011 1100 1101 1110 1111 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011
[3]
[2]
[1]
[0]
output_vector[4:0]
01111 01110 01101 01100 01011 11011 11010 11001 11000 10111 10110 10101 10100 10011 10010 10001 10000
[4]
[3]
[2]
[1]
[0]


9,400 ns
9,500 ns
9,600 ns
9,700 ns
9,800 ns
9,900 ns
10,000 ns
10,100 ns
addsub
input_vector1[3:0]
1011
1100
[3]
[2]
[1]
[0]
input_vector2[3:0]
1100 1101 1110 1111 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100
[3]
[2]
[1]
[0]
output_vector[4:0]
01111 01110 01101 01100 11100 11011 11010 11001 11000 10111 10110 10101 10100 10011 10010 10001 10000
[4]
[3]
[2]
[1]
[0]


10,300 ns
10,400 ns
10,500 ns
10,600 ns
10,700 ns
10,800 ns
10,900 ns
11,000 ns
addsub
input_vector1[3:0]
1100
1101
[3]
[2]
[1]
[0]
input_vector2[3:0]
1101 1110 1111 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101
[3]
[2]
[1]
[0]
output_vector[4:0]
01111 01110 01101 11101 11100 11011 11010 11001 11000 10111 10110 10101 10100 10011 10010 10001 10000
[4]
[3]
[2]
[1]
[0]


11,100 ns
11,200 ns
11,300 ns
11,400 ns
11,500 ns
11,600 ns
11,700 ns
11,800 ns
11,900 ns
addsub
input_vector1[3:0]
1101
1110
[3]
[2]
[1]
[0]
input_vector2[3:0]
1110 1111 0000 0001 0010 0011 0100 0101 0110 0111 1000 1001 1010 1011 1100 1101 1110
[3]
[2]
[1]
[0]
output_vector[4:0]
01111 01110 11110 11101 11100 11011 11010 11001 11000 10111 10110 10101 10100 10011 10010 10001 10000
[4]
[3]
[2]
[1]
[0]


12,000 ns
12,100 ns
12,200 ns
12,300 ns
12,400 ns
12,500 ns
12,600 ns
12,700 ns
addsub
input_vector1[3:0]
1110
1111
[3]
[2]
[1]
[0]
input_vector2[3:0]
1111
0000
0001
0010
0011
0100
0101
0110
0111
1000
1001
1010
1011
1100
1101
1110
1111
[3]
[2]
[1]
[0]
output_vector[4:0]
01111
11111
11110
11101
11100
11011
11010
11001
11000
10111
10110
10101
10100
10011
10010
10001
10000
[4]
[3]
[2]
[1]
[0]