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Medical Physics (Bharathiar University)

DEPARTMENT OF CA & IT

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DEPARTMENT OF COMPUTER APPLICATIONS AND INFORMATION TECHNOLOGY

SUBJECT NAME : MICROPROCESSOR AND ASSEMBLY LANGUAGE PROGRAMMING
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Unit – I
Introduction to microprocessors : Evolution of microprocessors – Single-chip

Microcomputer – Embedded Microprocessors – Bit- Slice processors – Microprogramming – RISC and CISC Processors – Scalar and Superscalar Processors – Vector Processors – Array Processors – Symbolic Processors – Digital Signal Processors. Intel 8086 – Pin Description of Intel 8086 – Operating modes of 8086 – Register organization of 8086 – BIU and EU – Interrupts – 8086 based computer system – Addressing Modes of 8086

Introduction to Microprocessor

1. The central processing unit (CPU) of a digital computer , built into a single IC is called microprocessor .
2. The word length of a microprocessor may be 8 – bit , 16 – bit , 32 – bit , 64 – bit . 3. A 8 bit microprocessor process 8-bit data at a time.16-bit microprocessor process 16-bit data at a time. A 32-bit microprocessor process 32-bit data at a time and a 64-bit microprocessor process 64-bit data at a time
4. A computer whose CPU contains more than one microprocessor is called a MULTIPROCESSOR system.

Evolution of Microprocessor

Intel 4004:
The first microprocessor is Intel 4004. It's a 4-bit microprocessor and introduced in the year 1971 by the intel corporation

Intel 4040:
It is the enhanced version of Intel 4004. Many companies introduced 4-bit microprocessor

PPS:
- 4 bit processor

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- By Rock Well International
- Widely used in toys instrumentation and commercial applications

T3472:
- By Toshiba
- Widely used in toys instrumentation and commercial applications

Intel 8008:
In 1972 Intel introduced the first 8-bit microprocessor

In this we are using PMOS technology.It is very slow and not compatible TTL circuit

Intel 8080:

- 8 bit processor – 1973
- Used NMOS technology
- Faster , higher density than PMOS
- The draw back of 8080 was that it requires 3 power supplies

Intel 8085:

In 1975 Intel introduced a improved version 8 bit processor is Intel 8085
It requires Only one +5v power

Other 8 bit processors:

- MC 6800 , MC 6809 – Motorola
- Z80 , Z800 – Z I log
- NSC 800 – National semi conductor
- PPS 8 bit , RCA , COSMAC – By Rock Well

16 bit processors:

- Intel 8086 – 1978
- Intel 80186 , 8088 , 80188 , 80286
- Motorola 68000 , 68010 , 68012
- Fairchild 9440
- Z8000
- NSC'S PACE , INS 8900
- Texas instruments – TMS 9900 series

12 bit processors:

- Intersils IM6100
- Toshiba T3190
- 8088 – Widely used in PC
- 80286 – Popular , costlier PC

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32 bit Microprocessor:

- I APX 32 Intel the first 32 bit processor produced by Intel

- Intel – 80386 (popular desktop)
- 486 , Pentium , Pentium pro , Pentium II , Pentium III , Pentium IV
- AMD – K5 , K6 , K7 (AMD – Advanced Micro Device)
- Cyrix – 586 , 686 , 6X86MX
- Motorola – 68020 , 68030 , 68040
- NSC – 32032 , 32332 , 32C532
- Z80000 – Z I log
- Intel & Motorola – 32 bit RISC (RISC – Reduce Instruction Set Computing or Computer)
- Intel 80960 (embedded control apply)
- Motorola 88100
- Motorola + IBM + Apple – 32 bit – power PC601 , 603 , 604
- Intel 80376 - 32 bit CISC (CISC – Complex Instruction Set Computer) (embedded apply)

64 bit Microprocessor:

- SUN'S ULTRASPARC
- Power PC 620
- MIPS' R4000 , R5000 , R10000 , 12000
- Intel PA8000 (Intel + hp)
- Intel i860 (1989) – 64 bit RISC for industrial control only

Microprocessor of desired word length:

- ALU – built as modules – bit slice

SINGLE CHIP MICROCOMPUTER:-

- A computer is made upon single chip is called single chip microcomputer which have CPU , EPROM , RAM , Input Output Processor.

Purpose of A/D converter:

- Powerful microcomputer have A/D converter , DMA channels and ……

Intel 8048 series:

- 8048 , 8748 , 8041 , 8741 , 8021 , 8035 these are all the best processor of 8048 series.

Intel 8051 series:

- It is powerful 8 bit microcontroller
- It was enhanced instruction set including instruction for multiple and division large memory capacity , full diplex serial port , Boolean processor , power saving modes of

operation , selected function like AD converter , DMA channels , pulse with modulator , watch , dog timer.

- Members – 80C51BH (one of the model) , 80C31BH , 87C51 , 8X52 , 8X54 , 8X58 (X can be X= 0 , 3 , 7)
- 80151 and 80251 (advanced version of 8051 – 1955)
- High performance , increase memory addressing , official high level language support , enhanced instruction set.
- 8XC251SA , 8XC251SB , 8XC251SP , 8XC251SQ (X can be X= 0 , 3 , 7)

16 bit microcontroller:-

In 1983 Intel introduced 8096

Members:

- 80C194 , 83C194 , 8XC198 , 8XC196KB / KC / KR / KQ / JK / JQ / KT.
- 8XC196NT / NP / NV / MC / MD / MH , 802365A.
- 80C198 , 83C198 low cost members of MCS 96 family.
- 8XC196KB High performance , 16 bit microcontroller which has 40 I/O lines , dynamic bus width.

Motorola 32 bit microcontroller:

- IBM manufactures 403GA , 32 bit RISC embedded controller which is used in office automations (printer , fax , machine)
- Consumer electronics , video games , telecommunication and networking PDA (PDA – Personal Digital Assistant)
- Motorola 68060 an extension 68000 is used for high embedded processor market.

EMBEDDED MICROPROCESSOR:

It is classified into 2 types

- Event control
- Data control

Intel 80960:

- Embedded version of 386 , 486 , 80186 , 80188
- **Integrated microprocessor** contains addition computer components besides the CPU itself
  The additional components are: interrupt controller, DMA channels , clock generator , DRAM , refresh control unit , peripherals , CS unit , local bus controller.

Other versions of 80186/80188 microprocessor are:

80C186/80C188,80C186XL/80C188XL,80C186EA/EB/EC,80188EA/EB/EC. 4

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Embedded versions of 486 microprocessor:

- Embedded Ultra low power Intel 486GX
- Embedded Ultra low power Intel 486SX
- Embedded Intel 486SX

Embedded version of 386 microprocessor are:

386CXSA,386CXSB,386EX,386SXSA embedded microprocessor

Intel 80376 :

- 32 bit embedded microprocessor
- It is designed for embedded data control applications. It is also used in switching networks, medical instrumentations and LAN controllers
- It is also used in upgrading 16-bit 80C186 applications into 32-bit system Motorola's EC603e is a 32 bit embedded processor which operates at 300 MHz. The important feature of Motorola's are: 423 MIPs,7.4 SPECint95,300 MHz clock,4w power consumption,255 pin CBGA(ceramic ball grid array),0.25 microprocessor technology.

Intel 80960:

- 32 bit embedded microprocessor
- Laser printer controller

Versions:

- 80960 SA / SB / KM / KB / CA / MC / CF / JA / JR / HA / HD / HT.

i 960(80960):

- Sophisticated industrial control option
- Image processing,garphics,networking,complex industrial automation

Intel 80186 , 80188 :

- Data control
- 16 bit microprocessor

BIT SLICE PROCESSOR:

- Customized processor
- 4 bit RALU multiprogramming sequences carry look ahead generator.
- Desired number of ALU'S 8 / 16 / 32 bit

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- Micro codes – instruction set
- Control section – trailered for each application
- Cost – effective

i) AMD 2901 , 2903 :

- 4 bit ALU slice
- Quotient register
- Decoder – 9 bit micro instructions
- RAM shifter
- Q shifter
- Multiplexers
- ALU – shift right / left by pairs of combinational shifters & add / sub.
- Avg – mul / div
- ALU – generate count signal

ii) AMD 2902:

- 4 bit ALU
- One 2902 IC
- Inter control using ripple carry scheme
- Delay
- Use carry look ahead generator

iii) AMD 2909 , 2910:

- 4 bit bipolar device
- Cascade able 4 bit slice
- Two 2909 to generate 8 bit address
- Three 2909 – 12 bit address
- Contain 4 bit register
- 4 * 4 bit stack

- Micro program counter
- Logic circuit for cascading
- Micro programming – 2909 used a component to control
- 2910 – improves versions of 2909

MICRO PROGRAMMING:

- CPU – control unit :
  - Software
  - hardware

- RISC based
- Control signals – electronic circuit
- Microprogramming – micro instructions

- Op code & micro instruction – micro code
- Use ROM (control memory) – to store
- CISC – software design
- Checking error easy in micro program
- Hard –wired X ?
- Emulation – computer having Micro programmed control unit instruction of other computer execution.
- Dynamic programming – RAM
- CISC – use micro programming – Intel 486 , Pentium , Motorola 68040……..
- RISC – Intel 80960 , Power PC , SUN'S SPARC , MIPS micro program

Instruction – fetch next instruction

- Micro programmer sequencer

CISC AND RISC PROCESSOR:

- RISC processor not in use microprogramming technique.
- CISC processor uses microprogramming technique.
- At present CISC processor are popular widely used.
- The RISC processor use simple and frequently use instruction employing hardwired control technique.
- RISC processors are cheap & faster than CISC processors.
- The advantage of CISC over RISC is that it can run a larger number of already existing software.

The important features of RISC processors are:

- ❖ Few instruction types and addressing modes.

- ❖ Simple and Hi – speed
- ❖ RISC instructions involve only register to register operations.
- ❖ Large numbers of general purpose registers are used to make processor register intensive.
- ❖ Most of this computation at performs using register's rather than memory.
- ❖ Large cache is involves.
- ❖ Hardwired control is used and microprogramming is not used.

 Development of CISC has become saturated.

 The control section and the instruction decoder become very complex when number of instruction increased.

 RISC processors being faster than CISC have better feature.

SCALAR AND SUPER SCALAR PROCESSORS:

 Scalar processor executes scalar data.

 Simple scalar processor executes instruction with fixed points operands. Powerful scalar processor executes both integer and floating points operands. Modern scalar processors contain both integer unit and floating point unit on same thing. It can be either CISC or RISC .

Example for CISC:

1) Intel 386 , 486
2) Motorola 68040
3)

Example for RISC:

1) Intel I 860
2) Motorola – MC 88100
3) AMD 29000

 Intel I 860 , M 88100 has on chip floating point unit.

 SUN'S SPARC and AMD 29000 use off chip.

 All these processor uses 32 bit instructions.

 A super scalar contains multiple and executes more than one instructions per cycle.

 Ex. Pentium , power pc , DEC's , alpha etc……..

VECTOR PROCESSOR:

 Perform vector computation.
 An array of some type operands “vector”.
 Vector operand – an ordered ser of “n” elements.

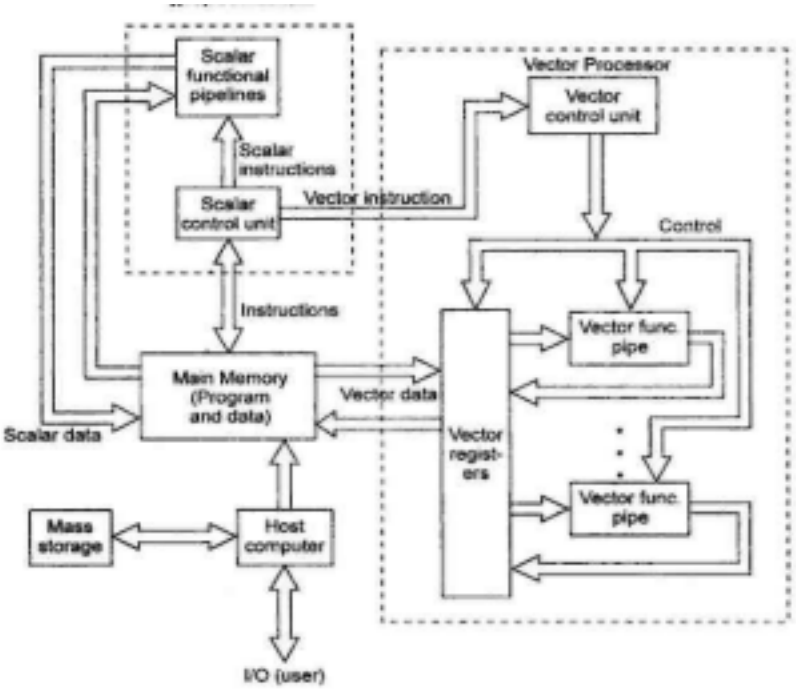

Fig. 1.2 The Architecture of Vector Supercomputer

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 A vector processor is a co-processor specially designed to perform vector computations. It is often built on the top of a scalar processor.
 Figure 1.2 shows the architecture of a vector supercomputer. As shown in the figure it contains a vector processor attachod to a scalar processor, there is a host computer which is used to load the program and data in Lhe main memory.
 The scalar control unit first decodes the instruction.
 If the decoded instruction is for scalar operation or a program control operation, the scalar processor executes it using the scalar functional pipelines.
 If the decoded instruction is for vector operation, it is sent to the vector control unit- The vector control unit supervises the flow of vector operands between the main memory and the functional pipelines of the vector processor.
 The vector operands arc held in a vector register. A vector register is actually a bank of scalar registers.
 Each scalar register contains one element of a vector operand.
 The vector data low is coordinated by the control unit.

 A vector processor contains a number of vector functional pipelines.

ARRAY PROCESSOR:

 For vector computation.
 Is a SIMD need not host processor (control processor / control unit).
 Synchronous processor – containing (multiple ALU'S -> local memory.
 Host processor is a scalar process.
 Control processor executes scalar of control type instruction directly.

Difference between VECTOR AND ARRAY PROCESSORS:

 Vector processor – multiple vector pipe line.
 Array processor – number of processing elements

EXAMPLE:

1) Illiac - IV , BSP (Burroughs Scientific processors).

SYMBOLIC PROCESSOR:

 It also called PROLOG (Program Logic) or CISC processor.
 Used in array like machine intelligence , knowledge based system , pattern recognition , text retrieval.
 The operation needed for artificial intelligence are logic inference , compare , search , pattern matching , filtering , unification , etc…….

DIGITAL SIGNAL PROCESSOR:

 Accept digitized signal information , perform mathematic operations on it & give result(host processor / output device).
 Most DSP accept analog signal (ADC).
 Process & send to host processor (DAC).
 Intel 2920 – 1st DSP.

Intel 2920 :

- ❖ 24 bit processor.
- ❖ Analog multiplexer.
- ❖ ADC.
- ❖ DAC .
- ❖ EPROM / ROM – (192 words 24 bit each).
- ❖ Scratch pad memory.
- ❖ Binary shifter.
- ❖ Clock logic.
- ❖ Sample & hold .
- ❖ Program counter .
- ❖ Operate its analog circuit simultaneously with digital circuit.
- ❖ Multiplexer – 4 input channels.
- ❖ De multiplexer – 8 input channels.
- ❖ Operations frequency – 6.6 MHZ
- ❖ Supply - +/- 5v.

Functions:

- ❖ Low pass & band – pass filtering.
- ❖ Reification.
- ❖ Limited functions.
- ❖ Up to 25 bit multi & division.
- ❖ Approximately to non – linear functions such as square law and algorithm.
- ❖ Logical operations.
- ❖ Input and output multiplexing.
- ❖ Threshold detection.
- ❖ Wave from generation .
- ❖ Logical output for decision type .
- ❖ Analog output for multi frequency DSP oscillators.

- Later DSP chips excluded analog input & output.
- A analog multiplexer , filters , sample and hold circuit , fast analog digital converter , output register .
- The analog include registers , DAC , de multiplexer , filters , amplifiers , ……
- Complex operations like differentiation and integrations are carried out easy.

Some important DSP'S:

- ❖ Texas instruments – TMS 32010
- ❖ TMS 32020 , TMS 320C25
- ❖ NEC micro PD 7720
- ❖ NEC micro PD 77230
- ❖ NEC micro PD 7281
- ❖ Analog device ADSP2100
- ❖ National LM32900
- ❖ Philips PCB5010
- ❖ Thomson TS68930
- ❖ AT&T DSP 32
- ❖ OK 1 NSM6992
- ❖ Matsushita MN1900
- ❖ Fujitsu MB8764

TMC 320C25:

- ❖ 16 / 32 bit data word with 32 bit array.
- ❖ 4 K word ROM.
- ❖ 512 word RAM.
- ❖ 100 ns cycle time (nano second).
- ❖ 80 K word of chip memory .
- ❖ 13.2 ms estimated 1024 point , complex FFT times (micro second)
- ❖ 2 buses

NEC micro PO7281:

- Specially designed of DIP(Digital Image Processor) such as restoration , enhancement , Compression & pattern recognition.
- Can be used to simple FFT / numeric processing.
- First VLSI device to use a practical (Very Large Scale Intergated Circuit) data flow architecture.
- Designed to words with a host processors.

8086 MICROPROCESSOR:

- 16 bit microprocessor.
- 40 pin IC .
- 3 versions , 8086 , 80861 , 80862 .
- 20 address lines .
- Address 1MB of memory.

PIN DESCRIPTION:

- AD0 – AD15 – bi directional.

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- Address / data.
- 16 low AD8 – AD7.
- 16 high AD8 – AD15.
  - AD16 – AD19 (output) Address / status lines.
  - AD10 / 53 - A17 / 59 (output) carry address (TI) , status (T2,T5……..)
  - A18 / S5 (output) S5 – interrupt enable status .
  - A19 / s6 (output)
  - BHE / S7 . low – to carry data , high – status signals.

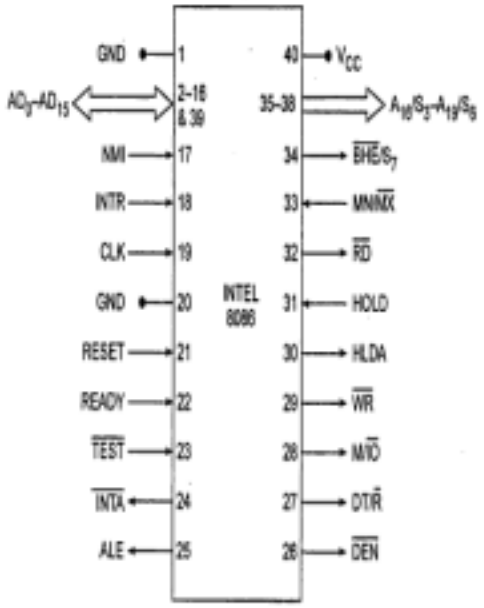

Fig. 2.1(a) Signals of Intel 8086 for Minimum Mode of Operation

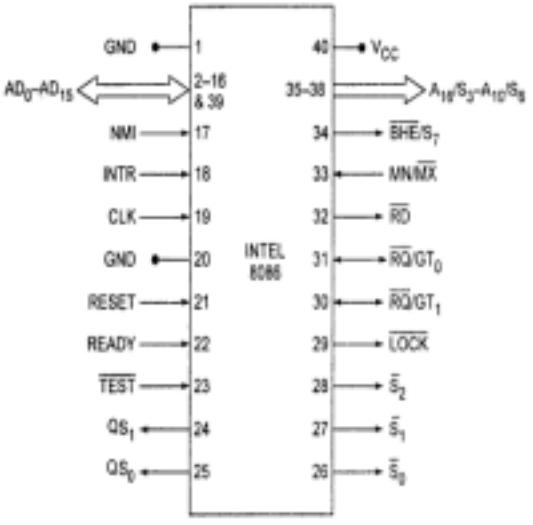

Fig. 2.1(b) Signals of Intel 8086 for Maximum Mode of Operation

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OPERATING MODES OF 8086:

It has two operating modes of operation: minimum and maximum mode. In microcomputer system where only one 8086 microprocessor work as a CPU, it operates in the minimum mode of operation. In a multiprocessor and coprocessor the 8086 operates in the maximum mode of operation. The minimum mode is used in few 8086 based system with few peripheral devices.

Personal computer employing coprocessor configuration runs in maximum mode. When there is large number of CPU's in a system they operate in parallel. The status of the pin MN/~~MX~~ decides the operating mode of 8086. When this pin is high the 8086 in minimum mode. When it is low, the 8086 operates in maximum mode. The 24 to 31 pins of 8086 have alternate function. They issue two sets of signals one when the 8086 operates in the minimum mode of operation and other in the maximum mode of operation.

REGISTER ORGANISATION FOR 8086

MICROPROCESSOR:

 The register organization of 8086 contains 15 registers. They are classified as general purpose register , pointers , index register , segment register , instruction pointer , status .

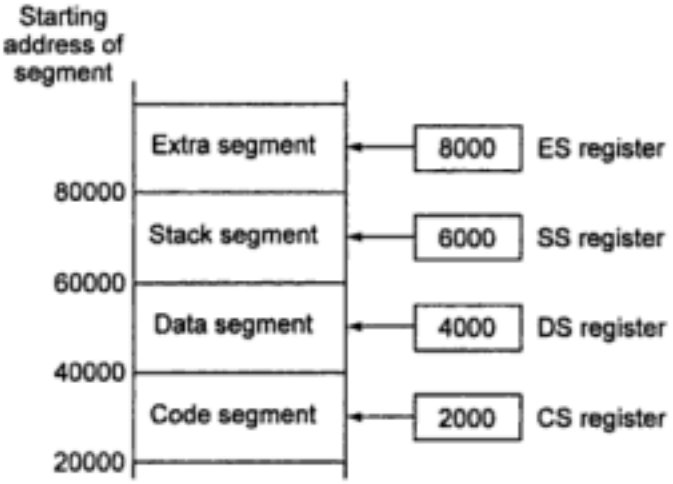


Fig. 2.3 Memory Segmentation in Intel 8086 Based System

General purpose register:

 There are four 16 bit register namely AX , BX , CX , DX .

AX is accumulator
BX is base register
CX is counter

DX is data register

- These register can be used as 16 bit or 8 bit register.
- They are used to hold arithmetic and logic operand and their results.

- AX register access as accumulator and BX , CX , DX are used to store data also server special purpose register.
- If the results of multiplication it more than 16 bit then the low order 16 bit are stored in AX and the high order 16 bit are stored is DX register.
- If the division is of 32 bits the 16 bit the stored is AX and the remainder is DX.

Pointers:

- Stack pointer and base pointer .
- The SD register points to the top address the stack.
- In PUSH , POP , CALL , INT , RETURN instruction.
- Stack address computed is the content of SP and SS.
- The register BP the base pointer for access memory stack . it can be also uses as general purpose register.

Index register:

- There are two index register namely SI and DI.
- They are used is calculating memory or stack address.
- SI indicates they source index and DI indicates the Destination index.
- The content of SI are added the content of DS to get true actual source address of the data.
- The content of DI are address the content of ES to get the actual destination. address of the data .

 The SI and DI register can be also used as general purpose registers.

Segment register:

 There are 4 types namely code segment , data segment , stack segment , extra segment.
 Code segment – Instruction code of programs.
 Data segment – Variable , constant.
 Stack segment – PUSH , POP .
 Extra segment – Destination address memory capacity.
 Starting address + offset address = physical address.
 Extra segment contain destination string instructions.
 8086 uses 20 lines for memory addressing.

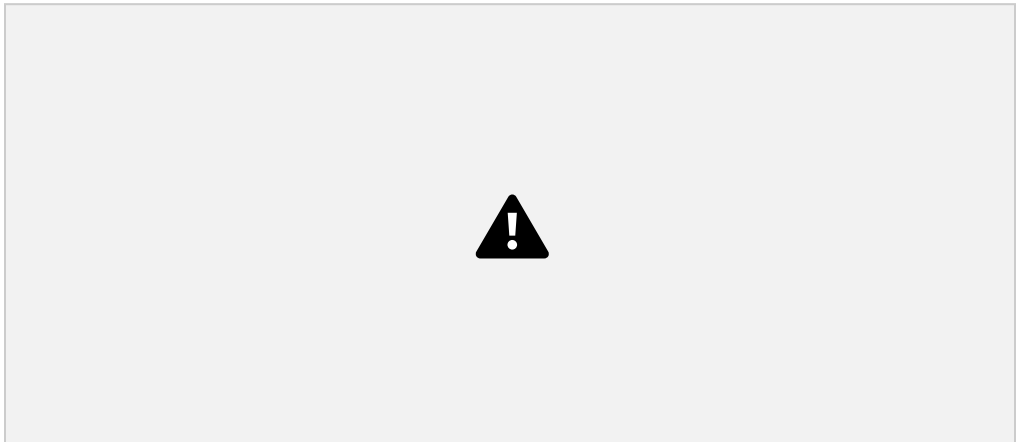
 The four memory segment that the CPU working with any time are called currently active segments.
 Memory location with in memory segment from the starting address and in called an offset address or effective address.
 The 20 bit address sent out by CPU called physical address .
 EX. 2000 + 400 = 2400 there fore physical address 2400.

Instruction Pointer

The instruction pointer acts as program counter .
It points to the next instruction to be executed within currently executive segment.

Status Register

The status register has flags to denote the status of the processor.



Trap Flag:

8086 HAS 16 BIT STATUS REGISTER .
It is also called as flag register (or) program status word .
There are 9 flags and in which 6 are conditional flag and remaining 3 are control flags .

Carry Flag:

If the MSB generates a carry due to addition (or) if borrow is needed at MSB during subroutine this is set to 1 .
If no carry is generated it is reset to 0 .

Parity Flag:

Even Parity :

If there are even number of 1's then the parity flag set to 1.

If it is contains odd number of 1's then the parity flag set to 0 .

Auxillary Carry Flag:

- If there is a carry from bit D3 due to addition (or) borrow is required from bit D4 into D3 during subtraction it is set to 1 .

 It is reset otherwise .

Zero Flag
It is set to 1 if the result of arithmetic (or) logic operation is zero . It is reset otherwise .

Sign Flag:

- It is set to 1 if the MSB of the result of an arithmetic operation is 1.
- It is set to 0 if the MSB of the result is 0 .

Overflow Flag:

The overflow flag is set to 1 to we get that the result as overflown into the sign bit . If sign bit is 0 it indicates (+ ve) number .

If sign bit is 1 it indicates (- ve) number .

Trap Flag:

- It is used for single step controlling .
- The trap flag is set to 1 .
- The program can be runned in single step mode .
  - When an interrupt is regonized the trap flag is automatically clear **.**

Interrupt Flag:

- It is used enable (or) disable interrupts .
- It is set to 1 the interrupt is enable .
- If it is 0 the interrupt is disabled .
- When 8086 is reset the interrupt flag is automatically cleared .

Directional Flag:

It is used in string operations .
If it is set to 1 string bytes are accessed from high memory address from high memory to low memory address .

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BUS INTERFACE AND EXECUTION UNIT

8086 two functional units namely ,

- **Bus interface unit**
  and
- **Execution unit**

Bus Interface Unit:

- BIU handles all interfaces with the external bus and generates memory and I/O addresses .
- The bus interface unit fetches the instruction codes from memory and keeps in a six byte instruction queue .
- It fills the queue whenever the bus is idle.
- The bus interface unit reads data from memory and writes data into memory.

- The execution unit receives 3 instruction .
- From the instruction queue , decodes them and executes them .
- The queue works in FIFO order .
- If the queue is ending is ending the execution unit bit till the queue gets atleast one byte.
- Execution unit also informs the first interface unit back fetch instruction (or) read data from .
- While the execution unit executes the instruction the first interface has fetches the instruction from memory .

Execution Unit:

 The EU also inform BIU where to fetch instructions or read data from. While the EU executes instructions, the BIU fetches instruction codes from the memory. Thus, there is an overlap between instruction execution and instruction fetching.

 The design feature of a processor which provides overlapping among the various operations to be performed by the processor is called pipelining.

 To achieve pipelining, several functional units can bo employed in a microprocessor. They work simultaneously in parallel.

 Each functional unit performs one type of operation.

 In 8086, BIU and EU are two functional units and they work independently in parallel.

Interrupts

Normal program execution is interrupted by an external device / instruction in program.
There are 2 types of interrupts

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1) Software
2) Hardware

The normal program execution of a microprocessor can be interrupted by some external device or by inserting a special instruction in a program. An interrupt caused by an external device is culled hardware interrupt.

A microprocessor has interrupt input lines to receive interrupt signals.
When an external device wants to interrupt the microprocessor, it sends an interrupt signal to the

microprocessor through the interrupt line to which it is connected.

Slow *VO* devices are connected to a microprocessor through an interrupt line. When data are ready, an input device interrupts CPU.

After completing the current instruction at hand the CPU responds to the input device. The CPU executes a subroutine to transfer data from the interrupting device. This subroutine is called interrupt service subroutine (ISS).

When data transfer is completed the CPU returns back to the main program which it was executing before the interrupt occurred.When the normal program execution of a microprocessor is interrupted by a special instruction, it is called software Interrupt.

Interrupts of 8086 :

- Interrupt pointer (or vector)
- Type zero interrupt (divide by zero)
- Type 1 interrupt (single step interrupt)
- Type 2 interrupt (non – mask able interrupt)
- Type 3 interrupt (break point interrupt)
- Type 4 interrupt (overflow interrupt)
- S/w interrupt type 0 to 255
- INTR interrupt type 0 to 255
- priority of 8086 interrupt .

i) H /W interrupt :
- NMI ,INTR
- NMI higher priority than INTR

ii) S /W interrupt :
- Inserting INT instruction in program
- INTO –overflow interrupt

iii) Interrupt pointer :
- 1 kb of memory space .
- the address range from 00000 to 003FF

It has 4 bytes
i) 2bytes for CS
ii)2bytes for IP

Starting address stored in 1 kb - interrupts pointer / vector .
Interrupt pointer table store starting address of ISS .

Types of Interrupts :

Number is assigned to an interrupt

Starting address of ISS for Type 0 is 00000H & Type 1 is 00004H First 5 pointers – dedicated interrupts . pointers divide by 0, single step control, non-maskable interrupt , breakpoint & overflow interrupts.

Type 2 to Type 31 – for advance µp

Type 32 to 255 – for S/W & H /W interrupt .

Type zero interrupt :

Type zero interrupt is divide by zero interrupts .

When the result of division operation is too large to be store in destination register . 8086 perform type zero interrupt .

Type 1 interrupt :

It is single step interrupt .

In a single step interrupt the process or executes one instruction and stops . If the result is correct the user can give command execute the next instruction . The trap flag is set to 1 is automatically perform type 1 interrupt after the execution each instructions.

Type 2 interrupt :

- Type 2 interrupt non-maskable interrupt in this used for emergency situation .

 (ex) :

- The used to safe program and data when power supply fails the external circuit it used detect power failure and sends an interrupt signal to 8086 through non maskable interrupt line .

 The program along data restores when power returns and can be executed again from the point where it was interrupted.

  - An external circuit is used to detect power failure .
- Sends interrupt signal to 8086 through non-maskable interrupt time.
- The program along with the data is restored when power returns and can be executed again from the point where it was interrupted.

Type 3 interrupt :

- (Break point interrupt)
- The break point is inserted in a program for debugging ALP programming .
- To interact implement this type of interrupt INT -3 instruction is used .
- It is inserted temporarily that a point upto which user want s to execute the program and examine the result.

Type 4 interrupt :

- (overflow interrupt)

- When the signed result of an arithmetic operation on two sign numbers . this two large to be stored in the destination register (or) memory location , an overflow error occurs an 8086 sets of flag .
- interrupt the implement type 4 interrupt INT -0 instruction is inserted in the program immediately after arithmetic operation.

S/W type of interrupt :

- S /W interrupt type 0 to 255.
- S/W interrupt is implemented using INT n instruction ,where n can have the values from 0 to 255.
- (for ex) :
- INT 33
- will cause type 33 interrupt .
- the starting address for INT 33 will be 33*4=132 .
- the hexa decimal value of 132 is 84H .
- Instruction pointer value is 84H CS value is 82H in 8086 system many subroutines written for I/P and O/P interfaces.
- They are called Biased .

ex:

- subroutines for reading a character from the keyboard can be called by using S/W interrupt .
- INT R interrupt type 0 to 255.
- INTR is a maskable H/W interrupt .
  - It is enable the IF ,flag it is set to 1 , and disable when set to 0 .

Priority of 8086 Interrupts :

- When two or more interrupts occur simultaneously the interrupts are and handled one by one .
- For this purpose priority is assigned for the interrupts .

INTERRUPT	PRIORITY
Divide error, int n ,into	Highest
NMI	Highest
INTR	Highest
Single step	Lowest

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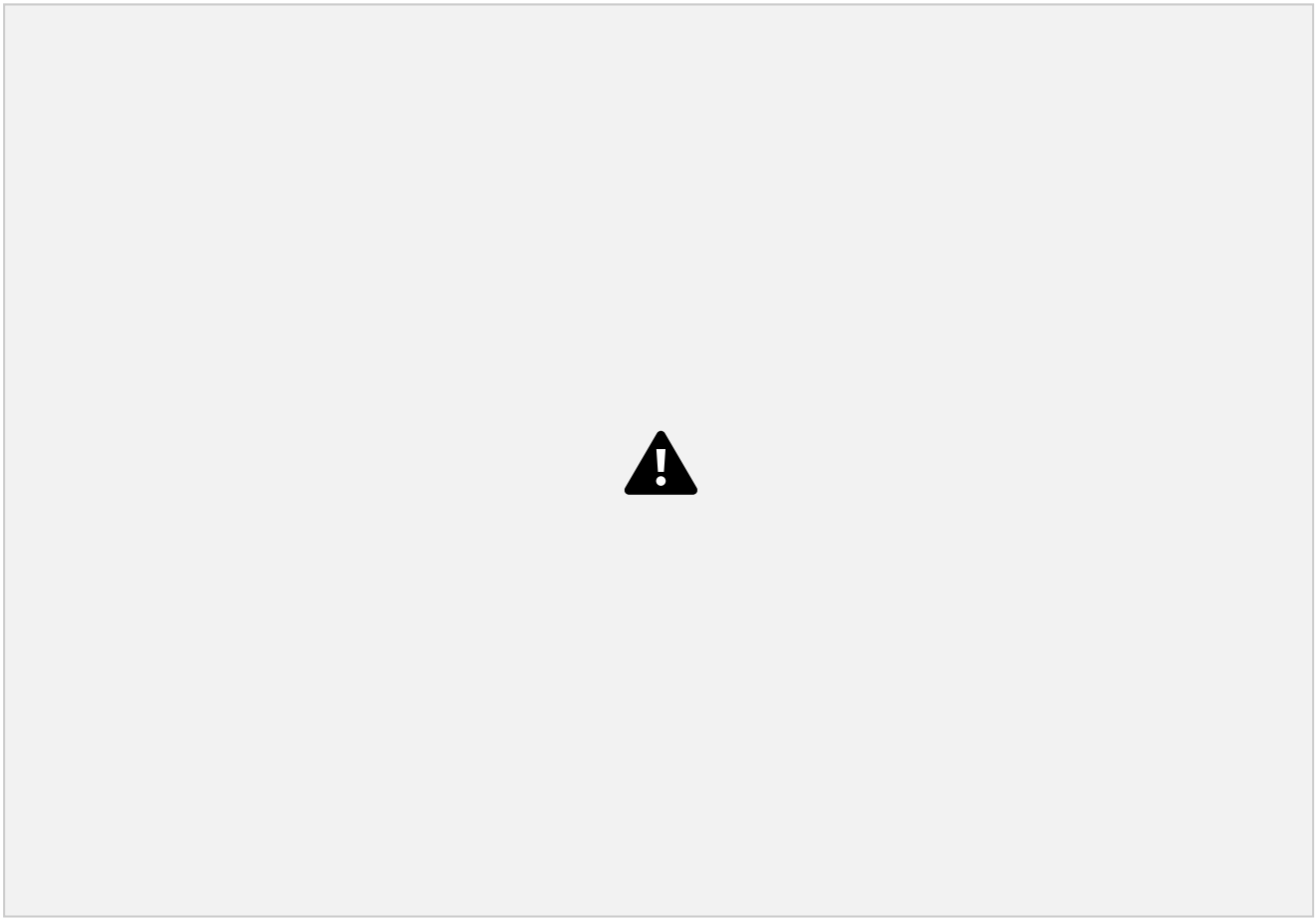
8086 based Computer System



This configuration is used for very small 8086 based system with a few pheripheral devices
. 8282 is an octal latch it is used to latch the address sent out by CPU .
The STB (strobe signal) strobe pin of 8082 it is said to high admit the i/p bits (signals).
The $\overline{OE}$ (output enable) pin .
It is made to enable the O/P of 8282.
The 8286is an octal bus transmission .
T is control PIN (i/p signal) to control direction of data.
8284A is used as CLK generator .

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The important control signals are

- MRDC Memory read command. It is same as BUNK,
- MWTC Memory write command. It is same as **MBMW.**
- IORC I/O read command. It is same as IOR.
- IOWC I/O write command. It is same as IOW.
- AMWC Advanced memory write command. It gives memory an early indication of a write instruction.
- AIOWC Advanced I/O write command. It gives I/O devices an early indication of write instruction.
- INTA Interrupt acknowledge.
- DEN Data enable. It is to be applied to OE of 8286. As OE is low active, DEN is inverted and then applied to OE of 8286.
- DT/R Data transmit/receive.
- ALE Address latch enable.
- The 6288 generates control signals compatible with Intel's multibus architecture, which is suitable for a multiprocessor system.
- An 8086-based computer system uses 8284 clock generator. 8087 math processor, 8259 interrupt controller, 8237 DMA controller. 8255 programmable peripheral interface, etc.

Addressing modes of 8086

1)Register

2)Immediate

3)Displacement

4)Based - Based index, Based index with displacement

5)Indexed

6)Direct addressing

7)Register indirect

- Each instruction performs an operation on the specify operands.
- The operand may reside in a accumulator (or) in a memory location.
- The way by which an operand is specify for an instruction is called the addressing modes.
- There are 8 different addressing modes for 8086.
- Out of 8 addressing modes two addressing modes are provided for instruction which operate the content of register (or) immediate operands.

 Register addressing :

- Move the content of CX heg to BX register .
  - Mov BX ,CX
- In this mode of addressing an 8 bit (or) 16 bit general purpose registers contain the operand .

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Immediate addressing mode :

(Ex): Mov AL ,56H

In this mode of addressing the operand is part of instruction .The remaining 6 addressing modes are used for specify an operand stored in the memory. The memory address of an operand consists of two 16 bit operands (i.e.) starting address of a memory segments and an offset . The offset is added to the starting address of the memory segment to get the memory addressing . 8086 uses 20-bit memory address .The starting address of memory segment missiles in the segment registers.

Displacement: It is an 8 (or) 16 bit immediate value given in the instruction .

Based: It is content of based register is used (BX (or) BP) .

Indexed : It is content of indexed register SI & DI.

Direct addressing : In this mode of addressing an effective address is given in the instruction itself.
(ex):
MOV AL 0300H
The instruction will MOV the content of an offset address 0300H to AL register .

Register indirect address : The operands offset is in the base register BX or in an indexed register (SI (or)DI) specified in the instruction .

MOV CX,BX.

Based addressing : The operands offset is the sum of contents of base register BX (or) BP and an 8-bit (or) 16-bit displacement .
(ex):
ADD AL,[BX+04]

Indexed addressing : The operands offset is computed by adding an 8-bit (or)16-bit displacement for the contents of an Index register [SI (or) DI].
(ex):
ADD AL,[SI+04]

Based indexed addressing mode: The operands offset value is computed by adding the base register (BX) to the contents of an index register (SI (or)DI).
(ex):
ADD AL,[BX+SI]

Based indexed with displacement : The operands offset value is computed by adding the contents of base register (BX (or) BP) to the contents of an index register (SI (or) DI) ,8 bit (or) 16 bit displacement.(ex): ADD AL,[BX+DI+BP]

SAMPLE SUGGESTED QUESTIONS:

OBJECTIVE TYPE QUESTIONS:

1. The maximum number of memory location that can be directly addressed by 8085 is (a) 16 (b) 32 (c) 1024 (d) 65536 Ans: d
2. In I/O mapped mode the number of input or output devices that can be addressed is (a) 256 (b) 8 (c) infinite (d) 65536 ans: a
3. The width of address bus in 8085 is (a) 16 (b) 8 (c) 2 (d) 65536 ans: a 4. A memory cell of static RAM consists of (a) capacitor (b) diode (c) flip-flop (d) X OR gate ans: c
5. When the 8085 is reset, the program counter is set to (a) zero (b) FFFFH (c) 0001H (d) any desired address ans: a
6. Specify the number of register and memory cells in a 1024X8 memory chip? 7. The memory address of the last location of a 1K-byte memory chip is given as FBFFH. Specify the starting address.
8. While executing a program, when MP completes the fetching of the machine code located at the memory address 2057H. What is the content of PC?

9. Basic element of memory is (a) flip-flop (b) buffer (c) encoder (d) diode ans: a 10. Explain in one line about ready pin.

SHORT QUESTIONS:

1. Give an organization of microprocessor based system.
2. Explain about the internal data operations.
3. Explain the following (a) hold (b) reset (c) interrupt
4. Differentiate I/O mapped and memory mapped.
5. Explain any two interfacing devices.
6. What is multiplexing explain.
7. With an example explain about the flags.
8. Explain about data transfer instruction with examples.
9. What is one byte instruction?
10. Write a program to add two numbers?

LONG QUESTIONS:

1. Explain about a microcomputer system with neat diagram?
2. Draw the architecture of 8085 and explain in detail?
3. How are the memory classified. Explain.
4. Draw 1K-byte memory map and explain.
5. Explain about the instruction set of 8085?
6. Write a program to arrange a set of numbers in ascending order?
7. Write a program to find the average of set of numbers?

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DEPARTMENT OF COMPUTER APPLICATIONS AND INFORMATION TECHNOLOGY

SUBJECT NAME : MICROPROCESSOR AND ASSEMBLY LANGUAGE PROGRAMMING
STAFF NAME :
UNIT NO. : I
SEMESTER : III
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CLASS : II BSC IT

Unit – II

8086 Instruction Set – Instruction Groups – Addressing Mode Byte – Segment Register Selection – Segment Override – 8086 Instructions Assembly Language Programs for 8086: Largest Number, Smallest Number in a Data Array – Numbers in Ascending and Descending order – Block Move or Relocation – Block Move using REP instruction – Sum of a series – Multi-byte Addition.

Instruction :

An instruction is a basic command given to a microprocessor or a computer to perform a specified operation on the given data

An instruction has 2 parts

i) Opcode field

ii) Operand field

- The opcode field specifies the operation code i.e. the operation to be performed by the instruction
- The operand filed defines the data on which the computer has to perform the specified operation
- The collection of instructions that a microprocessor is designed to execute is known as instruction set of that microprocessor
- The instruction set of one microprocessor varies from the other.
- 3.1 8086 Instruction Groups
- The instructions for 8086 can be classified or groupedaccording to the functions they perform

INSTRUCTION GROUPS:

i) Data Movement Group

This group includes instructions that involve the data transfer from one place to the other.

Examples: MOV

LDS

XCHG(exchange)

PUSH

POP etc.,

ii) Arithmetic Group

This group includes instructions for addition , subtraction, multiplication, division,

increment, decrement, comparison, decimal adjust etc.,
Examples : ADD
SUB
MUL
DIV
INC
CMP, DAS ETC.,

iii) Logical Group

This group includes instructions that involve logical operations on the the data
Examples : AND
OR
NOT
TEST
XOR etc.

iv) String primitive Group

This group includes instructions for string operations
Examples : LODS
MOVS
STOS
CMPS
SCAS

v) Program Counter Control Group

This group includes instructions like CALL, RET, JMP, JC, JE,JB,JZ,JNB
The LOOP instruction combines DEC, CX and JNZ instructions

vi) Processor control and I/O group

The instructions under this group are CLC, CMC,CLI,STD, STI, MOP, LOCK, WAIT, HLT,IN,OUT

vii) Interrupt Group

Examples are INT, INTO and IRET

viii) Rotate and shift Groups

This group includes instructions for rotation and shifting of data which include RCL, RCR,ROL,ROR,SAL,SHL,SAR, SHR

ADDRESSING MODE BYTE

- The 8086 provides a variety of addressing modes. A byte is used in the instruction code to specify the addressing mode.
- The addressing mode byte is always the second byte of the instruction code. However, there may be one or two additional bytes for displacement associated with the addressing mode byte.

X	X	Y	Y	Y	Z	Z	Z

Mod Reg r/m
(Fig 3.1 a)

X	X				Z	Z	Z

Mod Code r/m
(Fig 3.1 b)

Figure 3.1 shows the format of the addressing mode byte.

- The format for a double-operand instructions is shown In Fig. 3.1 (a) and (b) shows the format for a single-operand instruction (or a instruction involving two operands with one of them being implied or given in the opcode).
- In case of a double-operand instruction the first two bits, XX form the mod field of the addressing mode byte.
- The mod field differentiates between register addressing and memory addressing.
- The next three bits, YYY, form the reg field.
- The reg field specifies register which will be used in operation.
- The last three bits ZZZ form the *r/m* field, where r stands for a register and m for a memory location.
- The *r/m* field specifies the addressing mode for a register or memory operand.

The format for the addressing mode byte has 2 modes of instructions

i) Single - operand instructions

Example :
ROL BX, 1 ; Rotate BX left by one bit
Instruction code = 1101 0001, mod 000 r/m
Where mod and r/m are for BX.
000 in the addressing mode byte is a code

ii) Double – operand instructions

Example
- ADD CX, DX
- ADDCX, [0301]

Instruction code for these instructions is
0000 00dw, mod reg r/m;

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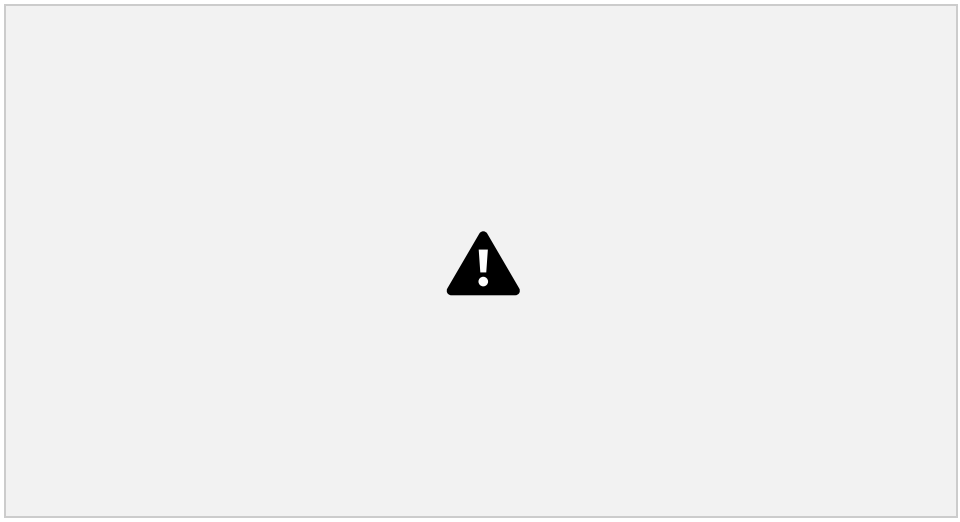
Values for mod, reg and r/m
The mod value 00 is for memory addressing without displacement.
The mod 01 and 10 are for memory addressing with 8-bit and 16-bit displacement.
The mod 11 with w=0 is for register addressing for 8 bit operation
The mod 11 with w=1 is for register addressing for 16 bit operation

Table 3.1 Values for reg

reg	*w = 0*	w= 1
000	AL	AX
001	CL	CX
010	DL	in
011	BL	BX
100	AH	SP
101	CH	BP
110	BH	SI
111	DH	Dl

The values for r/m and mod for different addressing modes are shown as below



Segment Register Selection

 For every instruction which has an operand in a memory location, a suitable segment register is needed to provide the starting address for the memory segment . The content of the segment register is used in the calculation of physical address of the operand. By default 8086 hardware selects a segment register according to the addressing mode of the instruction to be executed.

 The code segment register is used while computing the address for the instruction bytes.

 The data segment register DS is used while computing the address for data residing in a memory location.

 When BX register is used as a base register for offset, DS register is selected as the segment register for physical address computation.

 The stack segment register SS is used for slack reference instructions (i.e. PUSH and CALL). When BP is used as a base register for offset, SS register is selected as the segment register for physical address computation.

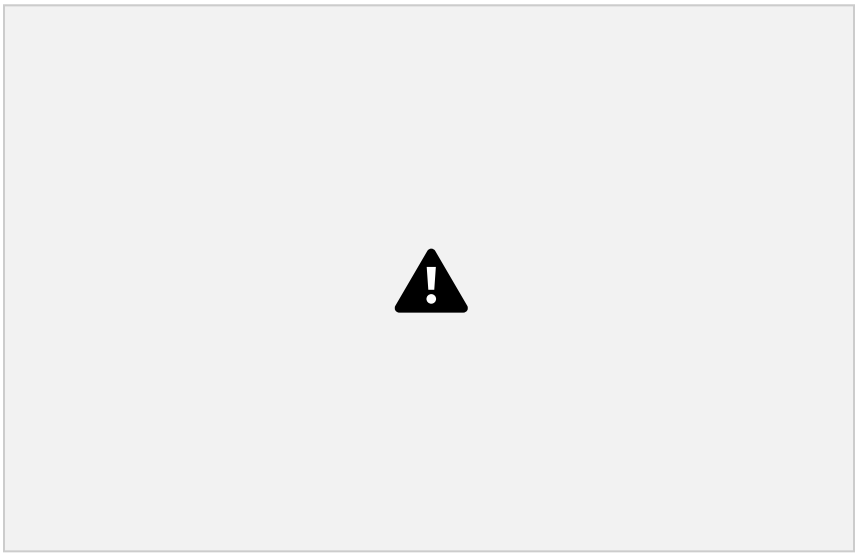
 The extra segment register ES is used for the destination of data in case of string operation and DI register to indicate destination address.

Segment Override

 Every memory addressing mode has a standard default segment register as shown in Table 3.3. In some cases an alternative segment register can be selected by using a segment override prefix byte.

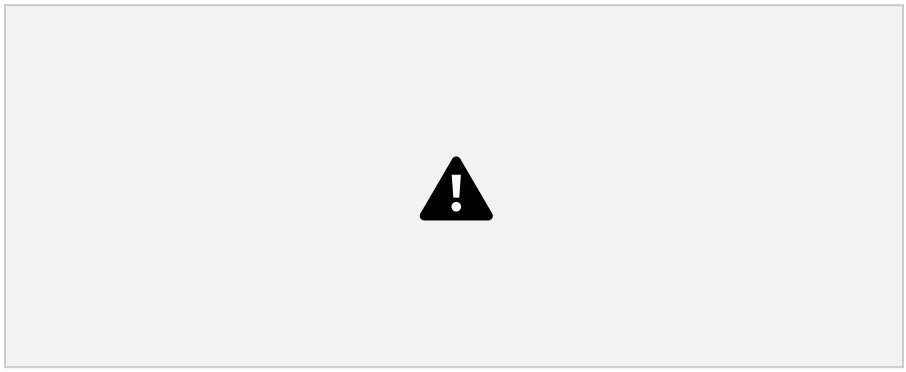
 The override prefix byte immediately precedes the opcode byte of the instruction.

 When override prefix is used, the processor uses a particular segment register



 The override prefix byte format is shown below.

 The two bits rr, in the override prefix byte selects the desired segment register instead of a default segment register.



The default values for rr for different segment registers are shown above

ASSEMBLY LANGUAGE PROGRAMS FOR 8086

PROGRAM TO FIND THE SMALLEST NO IN AN ARRAY

Effective Address	Codes	Label	Mnemonic	Comments
0201	BE,00,03		MOV SI,0300H	Memory address in SI
0204	8B,OC		MOV CX,[SI]	Count in CX
0206	B8,FF,FF		MOV AX,FFFF	Initial value for comparison
0209	46	BCK	INC SI	
020A	46		INC SI	
020B	3B,04		CMP AX,[SI]	Compare previous smaller no with next no
020D	72,02		JB GO	Jump if no in AX is smaller
020F	8B,04		MOV AX,[SI]	Save new smaller
0211	E2,F6	GO	LOOP BCK	Ump to BCK until CX is 0
0213	A3,51,03		MOV[0351],AX	Store smallest
0216	CC		INT 3	Break point

PROGRAM TO FIND THE LARGEST 8 BIT NO IN AN ARRAY

Effective Address	Codes	Label	Mnemonic	Comments
0201	BE,00,03		MOV SI,0300H	Memory address in SI

0204	8B,OC		MOV CX,[SI]	Count in CX
0206	B8,00,00		MOV AL,0000	Initial value for comparison
0209	46	BCK	INC SI	
020A	46		INC SI	
020B	3B,04		CMP AL,[SI]	Compare previous larger no with next no
020D	72,02		JAE GO	Jump if no in AL is larger

020F	8B,04		MOV AL,[SI]	Save new larger
0211	E2,F6	GO	LOOP BCK	Ump to BCK until CX is 0
0213	A3,51,03		MOV[0351],AL	Store largest no in memory
0216	CC		INT 3	Break point

PROGRAM TO ARRANGE NUMBERS IN ASCENDING ORDER

Effective Address	**Codes**	**Label**	**Mnemonic**	**Comments**
0201	BF,02,04		MOV DI,0402H	Memory address for result
0204	BE,00,03		MOV SI,0300H	Memory address for data
0207	8B,14		MOV DX,[SI]	Count to arrange nos in descending order
0209	BF,00,03 **(3)**	BND	MOV SI,03OOH	
020C	B8,FF,FF		MOV AX,FFFF	Initial value for comparison

020F	8B,OC		MOV CX,[SI]	Count to select largest no
0211	46 **(2)**	BCK	INC SI	
0212	46		INC SI	
0213	3B,04		CMP AX,[SI]	Compare previous smaller with next no
0215	72,04		JB	Jump if CF is 1
0217	8B,04		MOV AX,[SI]	New smaller in AX
0219	89,F3		MOV BX,SI	Memory address of smallest in BX
021B	E2,F4 **(1)**	GO	LOOP BCK	Jump (2) until CX is 0
021D	89,05		MOV [DI],AX	Save smallest
021F	89,DE		MOV SI,BX	Memory address of smallest in SI
0221	C7,04,00,00		MOV [SI],0000	Replace smallest by FFFF
0225	47		INC DI	
0226	47		INC DI	
0227	4A		DEC DX	
0228	75,DF		JNZ BND	
022A	CC		INT 3	

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PROGRAM TO ARRANGE NUMBERS IN DESCENDING ORDER

Effective Address	**Codes**	**Label**	**Mnemonic**	**Comments**

0201	BF,02,04		MOV DI,0402H	Memory address for result
0204	BE,00,03		MOV SI,0300H	Memory address for data
0207	8B,14		MOV DX,[SI]	Count to arrange nos in descending order
0209	BF,00,03	BND	MOV SI,03OOH	
020C	B8,00,00		MOV AX,0000	Initial value for comparison
020F	8B,OC		MOV CX,[SI]	Count to select largest no
0211	46	BCK	INC SI	
0212	46		INC SI	
0213	3B,04		CMP AX,[SI]	Compare previous larger with next no
0215	73,04		JAE GO	Jump if CF is 0
0217	8B,04		MOV AX,[SI]	New larger in AX
0219	89,F3		MOV BX,SI	Memory address of largest in BX
021B	E2,F4	GO	LOOP BCK	Jump to BCK until CX is 0
021D	89,05		MOV [DI],AX	Save largest
021F	89,DE		MOV SI,BX	Memory address of largest in SI
0221	C7,04,00,00		MOV [SI],0000	Put zero in memory which contained largest no
0225	47		INC DI	
0226	47		INC DI	
0227	4A		DEC DX	
0228	75,DF		JNZ BND	
022A	CC		INT 3	

BLOCK MOVE OR RELOCATION (BYTE MOVE)

Effective Address	**Codes**	**Label**	**Mnemonic**	**Comments**

0201	B9,00,05		MOV CX,0005H	Count for no of bytes
0204	BE,00,03		MOV SI,0300H	Source address in SI
0207	BF,00,04		MOV DI,0400H	Destination address in DI
020A	A4	(1)	MOVSB	Move byte
020B	E2,FD		LOOP (1)	Jump to (1) until CX is 0
020D	CC		INT 3	Break point

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BLOCK MOVE (WORD MOVE)

Effective Address	Codes	Label	Mnemonic	Comments
0201	B9,00,03		MOV CX,0003H	Count for no of bytes
0204	BE,00,03		MOV SI,0300H	Source address in SI
0207	BF,00,04		MOV DI,0400H	Destination address in DI
020A	A5	(1)	MOVSW	word byte
020B	E2,FD		LOOP (1)	Jump to (1) until CX is 0
020D	CC		INT 3	Break point

BLOCK MOVE (BYTE MOVE) USING REP INSTRUCTION

Effective Address	Codes	Label	Mnemonic	Comments
0201	BE,00,03		MOV SI,0300H	Source address in SI

0204	BF,00,04		MOV DI,0400H	Destination address in DI
0207	B9,05,00		MOV CX,0005H	Count in CX
020A	F2		REP	Repeat string instruction
020B	A4		MOVSB	Move bytes
020C	CC		INT 3	Break point

BLOCK MOVE (WORD MOVE) USING REPINSTRUCTION

Effective Address	Codes	Label	Mnemonic	Comments
0201	BE,00,03		MOV SI,0300H	Source address in SI
0204	BF,00,04		MOV DI,0400H	Destination address in DI
0207	B9,03,00		MOV CX,0003H	Count in CX
020A	F2		REP	Repeat string instruction
020B	A4		MOVSW	Move words
020C	CC		INT 3	Break point

SUM OF A SERIES OF 16 BIT NUMBERS
Sum : 16-bit

Effective Address	Codes	Label	Mnemonic	Comments
0201	BE,00,03		MOV SI,0300H	memory address in SI
0204	8B,0C		MOV CX,[SI]	Count in CX
0206	B8,00,00		MOV AX,0000H	Initial sum is 0000
0209	46	GO	INC SI	
020A	46		INC SI	
020B	03,04		ADD AX,[SI]	Add next no to previous sum
020D	E2,FA		LOOP GO	Disp-6 (2's complement)
020F	A3,50,03		MOV [0350],AX	

0212	CC		INT 3	

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SUM OF A SERIES OF 16 BIT NUMBERS Sum : 32-bit

Effective Address	Codes	Label	Mnemonic	Comments
0201	BE,00,03		MOV SI,0300H	memory address in SI
0204	8B,0C		MOV CX,[SI]	Count in CX
0206	B8,00,00		MOV AX,0000H	Initial sum is 0000
0209	BB,00,00		MOV BX,0000H	MSB of sum is 0000
020C	46	(2)	INC SI	
020D	46		INC SI	
020E	03,04		ADD AX,[SI]	Add next no to previous sum
0210	73,01		JAE (1)	Jump if CF is 0
0212	43		INC BX	Add carry to MSBs of sum
0213	E2,F7		LOOP (2)	Jump to (2)
0215	A3,50,03		MOV [0350],AX	Store LSBs of sum
0218	89,1E,52,03		MOV [0352], BX	Store MSBs of sum
021C	CC		INT 3	Break point

MULTI BYTE ADDITION

Example

40 35 86 9A 42 3C

ADD 85 92 3B 84 6A 15

C5 C7 C2 1E AC 51

Effective Address	Codes	Label	Mnemonic	Comments
0201	FD		CLC	Clear carry flag
0202	BE,00,03		MOV SI,0300H	Address for count
0205	8B,OC		MOV CX,[SI]	Count in CX
0207	BF,02,04		MOV DI,0402H	Address for 2nd no
020A	46	(1)	INC SI	
020B	46		INC SI	Address for 1st no
020C	8B,04		MOV AX,[SI]	Word of 1st no
020E	11,05		ADC [DI],AX	Add words of 1st and 2nd no
0210	47		INC DI	
0211	47		INC DI	
0212	E2,F6		LOOP (1)	
0214	CC		INT 3	Break point

EXPECTED QUESTIONS

1. Explain the steps used by 8085 when it executes a program?
2. Write a program for 8085 to create a time delay and explain how it works. 3. Write an assembly language program for 8085 to convert a BCD number into its binary form.
4. Write an assembly language program for 8085 to perform BCD to seven segments LED code conversion.
5. Explain about the subroutine with an example?
6. Explain the following with an example (i) looping (ii) counting (iii) indexing.
7. Explain in detail about the counters and time delay with examples.
8. What are the logic operations? What is use of rotate instructions?
9. Using compare instruction write a program to find the smallest number? 10. Explain about the different types of addressing techniques with an example?

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DEPARTMENT OF COMPUTER APPLICATIONS AND INFORMATION TECHNOLOGY

SUBJECT NAME : MICROPROCESSOR AND ASSEMBLY LANGUAGE PROGRAMMING
STAFF NAME :
UNIT NO. : I
SEMESTER : III
NO. OF PAGES : 18
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Unit – III
Intel 386 and 486 Microprocessors: Intel 386 and 486 Microprocessor – 486DX Architecture – Register Organization of 486 Microprocessor – Memory Organization– Operating Modes of Intel 486 – Virtual Memory – Memory Managament Unit –Gates – Interrupts and Exceptions – Addressing Modes of 80486 – Pin Configuration

Intel 386 and 486 microprocessors

Intel 386 and 486 are 32 bit processors .Intel 386 contains a memory management unit and four level protection mechanisms on the chip.
The 486 is the next evolutionary step of 386.The 486 micro processor integrates 386 CPU, a floating point co-processor and 8kb or 16 kb cache on a single chip.

The DX4 version of 486 contains 16 kb cache and all other versions contain 8kb cache. It is faster and more powerful than 386 micro processor. The 386 CPU was widely used in 32bit general purpose computers before the introduction of 486 micro processor. The 486 micro processors were widely used in 32bit general purpose computers before the introduction of Pentium processors.

The following are 32bit microprocessors
 Pentium, Pentium pro, Pentium II, Pentium III, Pentium IV
 Intel 80960 (i960) and80376(i376) are 32bit microprocessors for embedded applications
 80960 is the nest evolutionary step from the 8096 microcontroller family. It contains a floating point co-processor on the chip.

Intel 486 microprocessor

Intel 486 is the short term for 80486. It is a high performance 32 bit Microprocessor. It was introduced in 1985. It contains a integrated circuitry of 2 lakhs 75 thousand transistors. A complete memory management unit is on the chip .Highly pipelined and contains 6 functional units

- Bus interface
- Code prefetch
- Instruction Decoder
- Execution
- Segmentation
- Paging

It has eight 32bit general purpose registers

1.EAX
2.EBX
3.ECX
4.EDX
5.ESI
6.EDI
7.EBP
8.ESP

The 16 least significant bits of each general purpose registers can be accessed separately . The name of reg's for 16bit operation are: AX,BX,CS,DX,SI,DI,BP,SP
The reg's for 8 bit operation are: AL,BL,CL,DL or AH,BH,CH,DH.
There are six 16bit segement reg's they are CS,DS,SS,ES,FS,GS.
There are 2 additional data Segemetn reg's available namely FS and GS. Thus it contaisn a total of 4 data Segment reg's DS,CS,SS , ES
These data segment reg's can access 4 different data areas in the memory to permit programs to access different types of data structures
The other reg's are 386 32bit instruction pointer and 32bit staus reg .Four control reg's CR0,CR1,CR2,CR3 7 debug reg's, 2 test reg's, 4 system address reg's

- GDTR(Global Descriptor Table Register)
- IDTR(Intel Descriptor Table Register)
- LDTR(Local Descriptor Table Register)
- TR(Stack State Segment Reg)

Addressing modes of 386

There are 11 addressing modes available in 386. They are

i) Register

ii) Immediate

iii) Direct

iv) Indirect

v) Based

vi) Indexed

vii) Scale indexed

viii) Based – scale Index

ix) Base Index

x) Based Index with Displacement

xi) Based Scaled Index with Displacement

386 has 2 operating modes

- Real mode
- Protrected Mode
  - In real mode, it runs 8086 programs and its physical memory addressing capability is 1MB
  - In protected mode, it has mulit-tasking and production ability. In this mode memory management unit manage 64TB virtual memory

Versions of 386:

There are 3 versions 386DX, 386 SX, 386SL

 386 DX: It has 32 non – multiplexed address lines and 32 data lines

It can directly address upto 4GB of physical memory and its virtual memory addressing capacity is 64TB.The computing power is 12MIPS.It is packed on 132 pin grid array package

 386 SX: Introduced in 1988.Has same 32bit internal architecture as 386DX but only 24 address lines and 16 data lines.It is packed on 100 pin grid array package. Its virtual memory addressing capacity is 64TB.The clock frequency is 20 MHz and reg to reg address time is 0.100 microseconds

 386 SL: Introduced in 1990. It is highly integrated processor developed for smaller portable laptop, notebooks etc., It consumes less power. It has 24 address lines and 16 data lines .It operates at 24 MHz. It has 20MB physical memory and 64TB virtual memory addressing capacity.

Intel 486

 Intel 386 is short form of 80486**.**

 It is an advanced high performance 32bit CHMOS microprocessor was introduced in 1989**.**

 It has a 32bit CPU with all features of 386 and enhancements to improves its speed, computing power, a floating point co-processor or 8kb or 16kb code and data on chip**.**

 It contains 1.2 million transistors. Its has different clock rates for different versions. They are 36,66 & 100 MHz.

 1 micron CHMOS IV processor is used to manufacture 483 microprocessor. It is highly pipelined .It fetches several instructions a head of time to store**.**

 While it executes one instruction, it decodes the other, get operand for the third and fetches the fourth.

 The execution time for one instruction is thus reduced to a great extent. This type of pipeline design is usually provided in a RISC processor.

 The 486 also used this technique to reduce the instruction execution time. The 486 is a CISC processor and not a RISC processor. It executes frequently used instructions in one clock cycle. 486 has 2 verions 486DX, 486SX.

 Both the versions have 32bit address line s and 32bit data lines. 486 DX contains a 386 CPU , an 8kb code and data cache, memory management unit and a floating point math co-processor. The memory addressing of 486DX is 4GB physical and 64 GB virtual memory .

 486Dx is manufactured using CHMOS IV & CHMOS V processors

It is packed in 186 pin grid array package.

 Its computing powers are 54,80 at 60 MHz and 100 MHz resp.The memory addressing of 486SX is 4GB physical and 64 GB virtual memory.
 Clock frequencies for different versions are 20 and 25 MHz.
 Data transfer rate at 25 MHZ is 80MB/sec and computing power at 25MHz. It gives 70% greater performance than a 33MHz Intel 386DX.486SX is manufactured using CHMOS IV & CHMOS V processors.
 It is packed in 186 pin grid array or 196 lead plastic quad float package. A 486SX based computer is cheaper but less powerful than 486DX based computer.

486DX ARCHITECTURE

The 486 DX contains the following functional units
 Bus interface unit
 Code prefetch unit
 Instruction decoding unit
 Control and protection unit
 Execution unit
 Floating point math co-processor unit(FPU)
 Segmentation unit
 Paging unit
 Cache unit

 The execution unit contains ALU reg file and shifter.

 The barrel shifter is a special type of shift reg which can perform multiple no of shifts in a single operation.

 The segmentation unit contains descriptor reg, etc.,

 The paging unit contains paging mechanism, translation look aside buffer etc.,.

 The 486 microprocessor keeps a cache of the most recently accessed pages. This cache is called translation look aside buffer.

 There is a control ROM with the control and protection text unit.

The bus interface unit contains
 Address drivers

 Write buffers
 Data bus transceiver
 Bus control request sequencer
 Burst control
 Cache controller etc.,
 The data bus transceiver is data bus buffer driver

 The bus interface unit interface memory and i/o devices to 486 microprocessor.

The code prefetch unit fetches instructions and keeps them in 32 byte code queue.

 The instruction decoding unit receives the instruction codes from prefetch unit and decodes them.

 Execution unit executes instructions. As the 486 is a CISC processor, micro instruction are generated and the execution unit executes these instructions

 The floating point math co-processor executes trigonometry, logarithmic, exponential and arithmetic instructions.

 It operates on 32,64,80 bit floating point and 32,64 bit integers and 18 digit BCD operands

 The MMU consists of a segmentation and a paging unit.

 The segmentation unit translates logical address into linear address.
 The paging unit translates linear address into physical address. If paging unit is not enabled, then the linear address becomes the physical address.
 Cache is very fast memory unit. It is static RAM, keeps instruction codes and data currently being used.
 These are copied from main memory to cache. As cache is very fast, the microprocessor gets codes and data without wait state. 8kb cache provided in the 486 code and data cache .
 Protection is very essential for a multi user system.486 hardware is designed to provide protection mechanism to isolate OS from user tasks and user tasks from each other.

 It has built-in parity checker / generator. Parity is generated by the 486 during each cycle and is stored in a memory location. Parity is generated for each byte of data.
 The parity pins DP0 – DP3 are used for input and output.

- When the 486 microprocessor reads data, it check parity and generates an error signal, if there is an error.
- This error signal appears on PCHK.

REGISTER ORGANIZATION OF 486 MICROPROCESSOR:

- It contains 8 32-bit general purposes registers: EAX,EBX,ECX,EDX, ESI, EDI,EBP and ESP.
- The low order 16bit of each reg cane be accessed separately as AX,BX,CX,DX,SI,DI,BP,SP.
- Reg's AL,BL,CL,DL,AH,BH,CH,DH can be accessed individually for 8bit operations .
- The prefix E stands for **extended.**
- The 486 has six 16 bit segment registers in which 4 are data segment reg's namely CS,DS,ES,FS GS which can access 4 different data in the memory and permit programs to access different types of data structures
- The instruction pointer EIP is a 32 bit reg which holds the offset of the next instruction to be executed.
- The offset contained in EIP us always relative to the starting address of the code segment contained by CS.
- The low order 16 bits of EIP is used as 16 bit instruction pointer(IP) for 16 bit operation.
- EFlags is a 32bit flag reg.The low order 16bits are used for 16 operation.
- They are useful while executing 8086 and 80386 instructions.
- The reg containing low order 16bits of EFLAGS is called flags, which contain14 flags.
- Out of 16, 6 are conditional flags and remaining flags are control and system flags.

Flags of intel 486 microprocessor:

31 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0

Reserved for INTEL	AC	VM	RF	-	NT	IOPL	OF	DF	IF	TF	SF	ZF		AF		PF	1	CF

The flags may be divided into two groups

- Status (conditional) flags

 Control & system flags

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The six status flags include Carry flag(CF), parity flag(PF),Auxillary Carry Flag(AF), Zero Flag (ZF), Sign Flag(SF), Overflow Flag(OF).The other flags are directional Flag(DF), Interruot Flag(IF), Trace Flag(TF), Virtual mode Flag(VM), Alignment Check(AC), Resume Flag(RF), Nested task(NT), Input / output Privilege level Flag(IOPL).

Carry Flag(CF): It is set to 1 if there is a carry out of MSB after addition or a borrow after subtraction or comparison. It is set to 0 otherwise.

Parity Flag(PF): It is set to 1 if low order 8bit contain even no of 1's **.**It is set to 0 otherwise

Auxiliary Flag (AF): It is set to 1 if there is carry out of bit 3, resulting from an addition or if a borrow is needed from bit 3 for subtraction. It is set to 0 otherwise

Zero Flag(ZF): It is set to 1 if the result of an arithmaetic or logic operation is 0. It is set to 0 otherwise

Sign Flag: It is set to 1 if MSB of the resultof an arithmetic operation is 1.
It is set to 0 otherwise

Overflow Flag: It is set to 1 if an operation results in a signed overflow.
A signed overflow occurs when the operation results in a carry or borrows into the sign bits The overflow flag is set according to overflow at the 7^{th},15ht,31^{st} bit for an 8,16,32 bit operations It is set to 0 otherwise.

The control & system Flags

Directional Flag: It is used to control the direction of string operations.
If D7 is set to 1, ESI and EDI are automatically automated to access the string from higher memory address to lower address. If D7 is set to 0, ESI and EDI are increased automatically from lower memory to higher memory

Interrupt Flag: It enables / disables the external interrupt INTR.
If set to 1, 486 organizes and handles the external hardware maskable interrupt signaled on INTR pin. Otherwise the interrupt on INTR is ignored.

Trap Flag: Allows user to debug a program using single step control.
If TF=1 486 is put in single mode of instruction execution

Virtual Mode Flag: This flag provides virtual 8086 mode operation within the protected mode of 486 microprocessor**.** When flag=1, the 486 is in protected mode, the microprocessor is switched over to virtual 8086 operation**.** The VM bit can be set to 1 only in protected mode.

Alignment Check Flag: The alignment flag, when set to 1, indicates misaligned memory address. Only programs that run at the privilege level 3 generates alignment fault.

Resume (or Restart) Flag: When resume flag is set to 1, a debug fault is ignored on the next instruction**.** By setting this flag some exceptions can selectively be masked while debugging a program
Nested Task: This flag applies to protected mode. It is provided to indicate whether the execution of the current tack is nested within another task**.** When set to 1, it indicates that the current nested task, has valid link to the previous task.

Input / Output Privilege Flag: This is a 2 bit flag which applies to the protected mode**.** It is provided to indicate the max privilege level allowed for the execution.

Segment Descriptor Cache Registers

A segment descriptor cache register is associated with each segment reg's When a segment Reg is loaded with selector for memory reference, the necessary information regarding the segment under consideration is read from the descriptor table. This information is automatically loaded into the segment descriptor register

Control Registers

The 3 control registers CR0,CR1, CR2. CR0 control coprocessor, pagaging mechanism, onchip cache etc…, The 32 bit linear address that causes the last page fault detected, is held by the control register CR2. The control register CR3 holds the physical base address of the directory table. CR1 is reversed for the use in future mechanism.

System addressing registers:
There are 4 system addressing registers namely global descriptor table, interrupt descriptor table, Local descriptor table and task state segment register.

Floating point registers:
The 486 microprocessor contains a floating point unit on the chip. The floating point unit contain 8 data register, a tag word, a control register, a status register, an instruction pointer and a data

pointer.

Debug registers:
The intel 486 contains 6 debug registers, namely DR0-DR3, DR6 and DR7. Debug registers DR0-DR3 hold 4 break points.DR7 set the break point . The DR6 is debug status register. It shows the current state of the breakpoints. DR4 and DR5 are reserved by intel for use in future microprocessor.

Test Registers:
The intel 486 contains 5 test registers namely, TR3-TR7. TR3, TR4 and TR5 are used to test the onchip cache. TR6 and TR7 control the testing of the translation look aside buffer.

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MEMORY ORGANIZATION:

- The 486 handles a byte a word and a double word. A byte is stored in a memory location a word is stored in consecutive memory locations and double word is stored in 4 consecutive memory locations.
  - The memory for intel 486 system is divided into segments. When the processor operates in real mode the segment is 64KB fixed size. In protected mode a segment is of variable size and may vary from 1 byte to 4KB.
  - Memory ca be organized in to 4KB pages, segmentation and paging can be used together to get the advantage of both techniques.
  - The segmentation is useful for an application programmer because it can organize memory in logical modules.
  - The paging is useful for a system programmer to manage the physical memory of the system.
  - The capacity of RAM and ROM present in the system is called physical memory.
  - Segmentation prevents this type of failure because stack is confined in the stack segment which is completely separate and independent from the code and data segments.
  - The address given in a program is called logical address. The segmentation unit translates the logical address into 32 bit linear address.
  - The linear address is the base address of a segment plus an offset within the segment.
  - The paging units translate linear address into physical address. If the paging is not enabled the 32 bit address into physical address.
  - A physical address is an address of a memory location in the ROM or RAM present in the system.

- A logical address contains of a 16 bit selector and 32 bit offset.
- The selector is contained in a segment register. The offset is formed by a combination of one or more address elements: a base, an index and a displacement. The offset is of 32 bits the size of the segment varies up to 2^{32} = 4GB. In protected mode out of 16 bits of the selector 14 bits are used to address 20 bit limit of the segment size and size 12 bit attributes for the memory segment.
- The remaining 2 low order: bit 0 and bit 1 of the selector indicate privilege level for protection.
- Out of 14 bits 13 bits are used as an index into a descriptor table LDT or GDT. Remaining 1 bit is used to indicate whether the segment is LDT or GDT. When it is 0 GDT is selected. When it is 1 LDT is selected.
- In real mode the contents of a segment register selector directly gives 16MSBs of the segment base address.
- The segmentation unit shifts the content of a segment register by 4 bits and adds an offset to the result to get the linear address.
- In protected mode the contents of the segment register does not give the base address directly.
- It acts as an index and points to a local descriptor table or global descriptor table which gives a 32 bit base address and other information regarding the segment.

- To get linear address an offset is added to the base address obtained from LDT or GDT. The linear address thus obtained is translated in to physical address by paging unit.
- A memory model which eliminates segmentation and uses the entire memory space in a single block is called flat memory model.
- The 486 microprocessor does not have means to turn off segmentation but it cam be achieved by providing the same base for all the segments. Also the segment limit 4 GB is kept for all the segments. This type of memory model is known as simple flat model.
- It is useful for dedicated control applications which requires the fastest possible task switching and does not require all the segment based protection features.

OPERANDS MODES OF INTEL 486

The 486 has 2 operating modes: real and protected

Real mode:

- In real mode the memory address capacity is 1MB. The segment register gives 16MSBs of the address directly. It is shifted left by 4 bits and the offset is added to result to get the

physical address.

- Paging is not allowed in real mode. Segments are 64KB size. This mode is used to run 8086 application programs.
- The primary aim of the real mode is to set up the 486 processor in protected mode. When the power is switched on or the processor is reset it is initialized in real mode in which the system tables and register are initialized with appropriate values. Then the processor is switched over to the protected mode.

Protection mode:

- In protection mode the 486 provides memory management and protection facilities. In this mode 32 bit address lines are used to address a memory location. The memory segment size is variable. It varies from one byte to 4GB. In protected mode the selector does not give the MSBx of the memory address directly. But it gives an index into a descriptor table which gives the base address of the segment limit for its size and other attributes.
- A 32 bit offset is added to the base address by the segmentation the protected mode also provides paging facility. The pages are of fixed size of 4KB. It has addressing components: page address and page offset .
- The page address points to a descriptor table similar to the selector. The oriented system is also known as page flat model or demand paged virtual.

VIRTUAL MEMORY:

- In the 486 processor a 16 bit selector and 32 bit offset are used for memory addressing.
- Out of 16 bit of the selector upper 14 bits are used for addressing.

- The lower 2 bit are used for privilege checking. Using 14 bits of the selector 16KB memory segments can be addressed.
- As the maximum size of a segment is 4GB, 64TB memory can be addressed $64T=2^{46}$ logical addresses can be generated. Thus64 TB memory space us virtual memory.
- Using 32 address lines the 486 microprocessor can be address directly only 4GB physical memory. Thus the 64TB memory actually does not exist and hence virtual memory.
- When a programmer prepares a program which needs more memory capacity than the actual memory existing in the system, then the virtual memory technique is used to execute such a program.

 The program is stored in the secondary memory.
 A part of the program which is required currently for execution is loaded into the main memory by the memory management units. Similarly the part of the program which is not currently required is pushed back to the secondary memory.
 While executing a program to and fro movement of its parts between the main and secondary memory is called swapping.
 The 486 processor provides 64TB virtual memory per task . In segment oriented system the size of the segments to be swapped in and out of the physical memory is too large and therefore loading into the memory is a time consuming process. This difficulty is overcome by using paging technique.

MEMORY MANAGEMENT UNIT (MMU)

 In a multiuser/multitasking system tasks must be given independent memory Areas so that they should not interfere either each other and with the operating system but with limited physical memory it is not possible to provide independent memory area to each task.
 To avoid interference memory management is specially needed in a multiuser/multitasking system.
 The operating system software can perform some tasks of memory management but for the complete memory management and protection a hardware unit called memory management unit(MMU)

The important functions of an MMU are:

1. To compute the physical memory address form logical address. First, it computes linear address from logical address. This task is done by the segmentation unit. Then MMU computes physical memory address from the linear address. This task is performed by the paging unit.
2. To provide protection the MMU compares privilege level if the part of a program being executed with the privilege level of the part of the program is higher or equal to the privilege level of system the program is allowed to access the desired memory segment.
3. If an user task needs memory space larger than the physical memory space existing in the system the MMU provides such a memory space by virtual memory techniques.

 When a logical address is received the MMU checks whether the desired memory segment is present in the memory and if present the MMU computes the corresponding physical address.
 If the desired memory segment us not present it interrupts CPU.

- On the receipt of the hard disk into the main memory. To make space in the main memory the MMU moves a least used segment back to the disk.
- The movement of segment from the hard disk to the main memory and vice versa is called swapping.
- The MMU checks whether the desired segment is present in memory or not. If the desired segment is present in memory it is called a " hit" else it is "miss". A hit rate 90-95 is desired.

Advantages:

1. The advantage of segmentation scheme is that a swapped segment corresponds to the data structure used in a program.
2. If paging scheme is used swapping becomes faster because 4KB fixed size pages are used.
3. At any time only a few pages of any program or process to be executed are kept in the main memory.

Disadvantages:

1. In sophisticated computer system the time needed to manage all the descriptor tables, segments, page tables and pages become too large
2. To develop the software to manage all these becomes a complex task.
3. The memory capacity required for all the tables may become excessively large.

GATES:

- A gate is a simply a special type of descriptor.
- All gates in a computer system are specified by the operating system.
- User task can acess the required software segment having higher privilege.

There are 4 types of gates namely

1. Call
2. Trap
3. Interrupt
4. Task

Interrupt Gates:

- Gate description for interrupt or exception subroutines reside in a special descriptor table called interrupt descriptor table IDT.
- It may contain up to 256 descriptor.
- During the process of initialization the base address and the limit for IDT are loaded in to the interrupt descriptor table.
- The type is multiplied by 8 and added to the base address of IDT. The IDT contains gate description for interrupt a trap and task.
- The gate descriptor does not contain the base address for he desired segment.

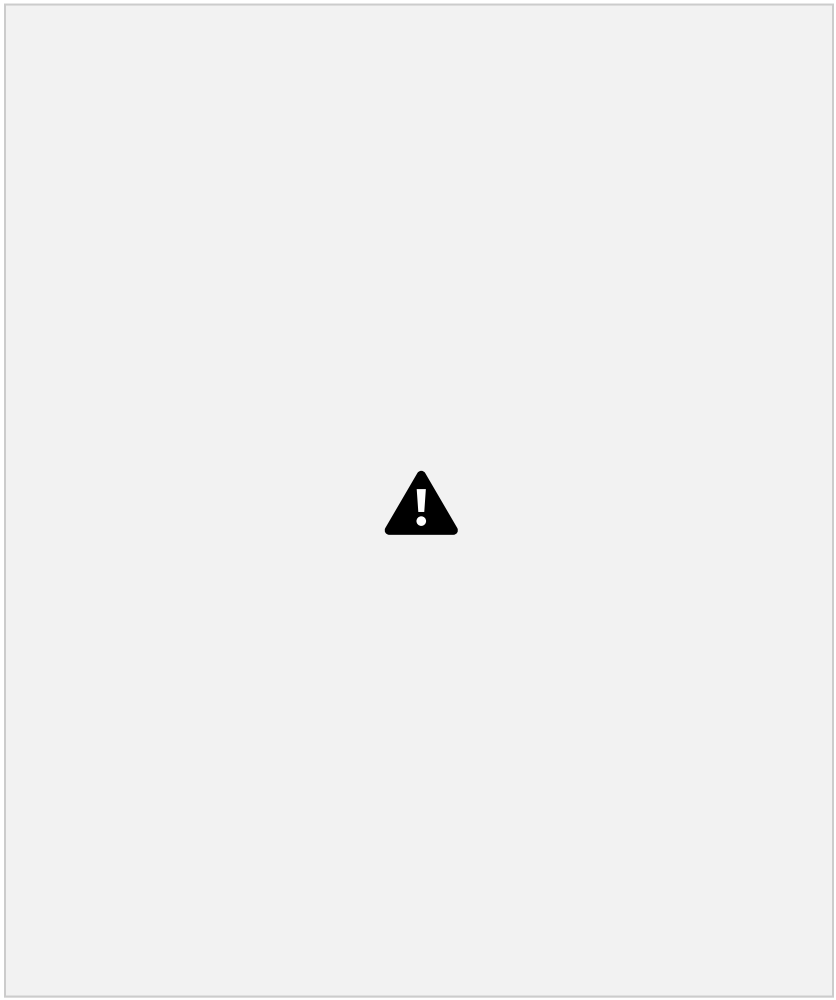
- Rather it contains 8 byte information which includes a 26 bit selector 32 bit offset privilege level etc

Call gate:

- Call gate descriptors resides in the GDL or LDT.
- When an integer segment call occurs the call gate descriptor is fetched from the LDT or GDT.
- This descriptor contains a selector 32bit offset, privilege level, etc. After checking privilege level if it is found that the desired segment is valid the selector obtained from the call gate descriptor is loaded in the CS register.
- The selector is used to find the base address limit etc from another descriptor residing in the LDT or GDT.
- The 32 bit offset obtained from the call gate descriptor is added to the base address of the desired segment to obtain the linear address of the desired subroutine.

INTERRUPTS AND EXCEPTION

Interrupt ponder table for Intel 8086



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- Interrupt and exceptions cause forced transfer of program execution to subroutine or a task.

- The interruption of normal program execution of a microprocessor. Caused by the external events such as request to serve peripheral devices, is called interrupt.

- This type of interrupt is known as hardware interrupt. On the other hand an interruption of microprocessor caused by internal abnormal conditions such as division by zero is called exception.

- The normal program execution of a microprocessor can also interrupted by inserting a special instruction in a program. This type is called software interrupt.

- The 486 microprocessor has 2 interrupt lines NMI and INTR. NMI is a non maskable interrupt where as INTR is a maskable interrupt.
- When the microprocessor is executing NMI subroutine, if NMI occurs again during this period.

- The different types of interrupts or exceptions have been given an identifying number. This number is called interrupt type or interrupt vector. There is a provision of up to 256 types of interrupts/exceptions in 486 microprocessor based system.
- The ways to supply 8bit interrupt vector for different types of interrupts and exceptions are as follows:

1. Exceptions provide the interrupt vector internally.
2. Software interrupt instructions INt n contain or implies the 8 bit vector. 3. The maskable hardware interrupt supplies 8bit vector through interrupt controller in response to interrupt acknowledge signal received from the CPU.
4. The interrupt vector 2 has been assigned to non maskable interrupt NMI.

Interrupt and exception vectors:

Interrupt type	Description
0	Divide error
1	Debug exception
2	NMI interrupt
3	Break point
4	INTO detected overflow
5	BOUND range exceeded

6 Invalid opcode
7 Device not available
8 Double fault
9 Reserved by intel. Not used by 486 CPU 10 Invalid task state segment

11 Segment not present
12 Stack fault
13 General protection
14 Page fault
15 Reserved by intel. Not used by 486 16 Floating point
17 Alignment clock
18 Reserved by intel. Not used by 486 19 Available to programmer.

ADDRESSING MODES OF 8046

The 486 microprocessor has 11 addressing modes. 2 of them are to specify register or immediate operand.

Register Addressing Modes:
In this addressing mode the operand is contained in one of the 8,16,32 bit general purpose registers.

Immediate Addressing Modes:
The operand is included in the instruction itself. It forms a part of the opcode. The remaining 9 addressing modes are to specify memory operands. The linear address of an operand is the sum of the segment bas address and an offset within the segment

Displacement:
It is an 8 or 32 bit immediate value following the instruction.

Base: The contents of any general purpose register can be used as a base address to determine an offset. In other words any general purpose register can be used as a base register.

Index: The contents of any general purpose register except ESP can be used as an index to point to an operand. In other words any general purpose register except ESP can be used as an index register.
Scale: It is a factor to multiply the contents of an index register and may be 1,2,4 or 8 The effective address is an offset within the segment with respect to the starting address of the segment

Effective address or offset =[Base register]+[index register * scaling]+displacement.

Direct Addressing modes:
The operand offset is a part of the instruction itself. It is contained within the instruction as an 8,16 or 32 bit displacement.

Register Indirect Addressing modes: A base register contains offset of an operand. 50

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Based Addressing Modes: The operands offset is computed by adding a displacement to the contents of the register.

Indexed Addressing Modes: A displacement is added to the contents of an index register to form operands offset.

Scaled Index Addressing modes: The contents of an index register is multiplied by a scaling factor, and the result is added to a displacement to form operands offset.

Based scaled index addressing modes: To determine operands offset the content of an index register is multiplied by a scaling factor and the result is added to the contents of a base register.

Based Index Addressing with Displacement: The contents of an index register the contents of a base register and a displacement are all added to form operands offset.

Based scaled index addressing with displacement: The contents of the index register is multiplied by a scaling factor. The result so obtained the contents of a base register and a displacement are all added to form operands offset.

PIN CONFIGURATION AND SIGNAL OF 80486:

A2 –A3, output and A4-A31. Input/output: A2-A31 are address lines. They specify memory or I/O address together with byte enable signals

BE0#-BE3#.: The symbol # indicates a active low signal. BE0#-BE3# together with A0 and A1 specify which data bytes of the data bus will take part in read and write operation. When BE0# becomes Low, data are transferred on D0-D7 lines. Similarly BE1# applies to D8-D15, BE2# applies to D16-D23# applies to D24-D31.

BE0# - BE3#. Output: These are byte enable signals. They are active low signal. They indicate which data bytes of the data bus taken part during read and write.
D0-D13 Input/output: These are data lines.

DP0-DP3: There is one data parity signal for each byte of the data bus.
PCHK#. Output: Parity status. A parity error is indicated when PCK# is low **M/IO. Output:** Memory or I/O access. When it is high the CPU will acess memory. When it is low CPU will access I/O devices.
D/C. Output. Data/Control: when it is high data are transferred. When it is low control signal is transferred.
W/R#. Output. Data/control: When it is high write operation is performed. When it s low read operation is performed.

Logic for M/IO#,D/C# and W/R#

M/IO# D/C# W/R# OPERATION 0 0 0 Interrupt acknowledgement

0 0 1 Halt/special cycle 0 1 0 I/O Read
0 1 1 I/O write
1 0 0 code
1 0 1 Reserved
1 1 0 Memory read 1 1 1 Memory write

LOCK#.Output: It indicates that the current bus cycle is locked. The bus hold is not allowed when LOCK# is asserted, but the address hold is allowed.
PLOCK#.Output: Pseudo lock. It indicates that the current bus transaction needs more than one bus cycle for completion. It happens when 64 bit or 128 bit read/write operation is performed.

ADS#.Output: Address status output. It indicates a valid address on the bus.

RDY#.Output: Non-burst ready. It indicates that external device is ready for read or writes operation.

ADS# and RDY#: These are bus control signals

BRDY#. Input: Burst ready input

BLAST#.Output: Burst ready last signal

BRDY# and BLAST#: These signals are used to control burst mode memory read and write operations. In case of 486 microprocessor the normal memory read operation for reading a line in to the cache from external DRAM takes two clock cycle. If a series of read operations are to be performed from successive memory location of DRAM, it can be done in burst mode which will

take only 1 clock cycle per read operation.

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Signals of INTEL 80486

CLK
A2-A31

BUS ADS#
Control RDY# 32-bit BE3# address
AHOLD BE2# byte bus Cache BE1# Enable invalidationEADS# BE0#
Interrupt RESET
INTR

Data bus

D0-D31

INTEL 486

Signals NMI

Cache

KEN# M/IO#
Cache FLUSH# D/C#
control W/R#

LOCK# Bus cycle

PWT PLOCK# definition Page
Caching PCD
control

FERR# HOLD Numeric IGNNE# HLDA error
reporting BOFF# Bus arbitration
Bus size BS8# BREQ
control BS16#

DP3

Burst BRDY#

control BLAST# DP2 DP1 Parity
Address bit 20 A20M# DP0
mask

PCHK#

Expected Questions:

1. Explain Interrupts and Exceptions with diagram.
2. Describe the Virtual Memory and Memory Management Unit with dig.
3. Describe the pin configuration with diagram.
4. Explain about Operating Modes of Intel 486.
5. Explain about the Addressing Modes of 80486.
6. What is direct memory access explain?

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KAAMADHENU ARTS AND SCIENCE COLLEGE

SATHYAMANGALAM

DEPARTMENT OF COMPUTER APPLICATIONS AND INFORMATION TECHNOLOGY

SUBJECT NAME : MICROPROCESSOR AND ASSEMBLY LANGUAGE PROGRAMMING
STAFF NAME :
UNIT NO. : IV
SEMESTER : III
NO. OF PAGES : 18
CLASS : II BSC IT

Unit – IV
Input devices – Output devices – Memory and I/O addressing – 8086 Addressing and Address Decoding – Programmable I/O Ports – DMA Data Transfer. Other Microprocessors – PowerPC Microprocessors – Pentium Microprocessors –Pentium Pro microprocessor – Alpha Microprocessor – Cyrix Microprocessor –MIPS Microprocessor – AMD Microprocessor

Input devices:
Input devices are used to enter data and instructions in to the computer for processing. It converts data and instructions into binary format which can be accepted by the computer

Keyboard:
In general purpose computer the commonly used input device is a keyboard. We want to enter data which want to process.

Other input devices:
some devices which do not require typing for feeding information. Some examples are scanners, mouse, light pen, joy stick, track ball, touch screen etc.

Embedded computers input devices:
Embedded computers are used for different applications such as automatic control of cars, washing machines, video camera, automatic control in industries like temperature, control of oven, speed control of motors, etc. In many applications we desire that a computer should be able to see the environment. For ex: a robot must have vision to perform its job. Sensors like video camera, CCD camera, are used to provide vision to computer. The computer processes these signals and recognizes and displays the image of the object.

Voice input to computer:
 Data entry into a computer through keyboard is a time- consuming task.

 This task becomes very easy if computer accepts spoken commands and data. Through the voice input to the computer. Voice input devices have been developed for voice recognition.
 Systems have been developed that can understand up to 20,000 words. Each word is displayed on the screen and the user speaks each word in to the microphone. The computer then stores his pronunciation along with computer then stores his pronunciation along with the matching word, which is displayed on the screen. This computerized match is known as voice – template. Next time the user speaks, it quickly matches the pattern of his voice against voice template stored in the memory.
 If the computer finds a match, it selects the word.

output devices :

The output devices receive information from the computer and converts it into a suitable form which can be used by the persons working on computer.
The commonly used output devices in a general purpose computer are CRT screen and printers. In some cases, digital to analog converters are used as output devices to provide control signals to electromagnetic controllers, actuators, relays, etc.

CRT screen:

 A CRT (cathode ray tube) display unit is a commonly used output device. It is also called as monitor. It displays the information received from the computer. The information may consist of texts, images, drawings and graphs. A CRT is vacuum tube with electron gun placed at its back portion. An electron beam emerges from the electron gun and is directed towards the CRT screen.
 A CRT display unit is available either as a monochrome (ie only one co lour) or colour.
 Monochrome monitors are available in green, blue, orange, yellow, pink, amber, red and milky white depending on the type of phosphor used.
 A colour CRT screen works on the same principle as a co lour TV screen. Three types of phosphors: red, blue and green are used to produce colour display. The coating of the three phosphor material is made in such a way that the dots of these phosphors form a triangular pattern and such patterns are spread over the entire screen.
 The three dots of the three different colours are placed in a triangular spot and they are so close that they appear.
 When all the three beams are switched off the spot becomes black one. When all the three beams are switched on the spot becomes white.

Raster scan and vector scan method of Display.

Characters or graphics which are displayed on a CRT screen consist of a number of tiny dots. At a time only one dot is illuminated by the electron beam. The dots are placed on several horizontal lines on the screen.

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Raster scan:

- In raster scan technique the electron beam is directed on a line from left to right. When the electron beam reaches the right hand corner of a line it is turned off and again it begins from the starting point of the next line. This process is repeated and electron beam finally reaches the right hand lower corner of the screen.
- Then, the electron beam is turned off and it again starts from the left hand corner of the top line of the screen.

Vector scan:

- In vector scan technique, the electron beam is directed left or right up or down with the help of deflecting plates. The beam can be directed to any point on the screen directly.
- Only selected dots on the screen are illuminated by this technique. Straight lines can be drawn connecting two points on the screen. It is suitable for displaying graphics consisting of straight lines.
- It is not suitable for displaying graphics consisting of curves

Memory and I/O addressing

- The memory addressing capacity depends on the number of address lines of the CPU. The set of all possible address which can be generated by a CPU is called address space .
- For example intel 8086 microprocessor has 20 address lines and can address 1 MB of memory directly.

There are two technique of addressing an I/O device by the CPU.

1. Memory mapped I/O scheme.
2. I/O mapped I/O scheme.

Memory mapped I/O scheme

- A CPU can address an I/O device just like a memory location is called memory mapped I/O scheme. Only one address space is used by the CPU.
- Some addresses of the address space are assigned to memory location and other are assigned to I/O devices.
- The same address are not assigned to each memory location and I/O devices.

For ex: memory location are assigned the address from 00000 to 4fffff.
The address which have not assigned for ex, 50000, 50001, 50002 etc can assigned to I/O device.

I/O mapped I/O scheme

- Two separate address spaces are used, one for memory location and the other for I/O device. I/O address space is much smaller than the memory address space.

- An address assigned to memory location can be assigned to I/O device. Since the same address can be assigned to a memory location as well as an I/O device, there must be a signal issued by the CPU to distinguish.
- For this purpose Intel 8086 has M / IO. When this signal is high, the address on the address bus is for memory location and when this signal is low , the address on the address bus is for I/O device.

Generation of control signals for memory and I/O devices

Intel issues control signals RD and WR for read and write operation respectively. It also issues a status signal M / IO to distinguish whether read or write operation to performed with memory or an I/O device.

- MEMR .Memory read: It is obtained using OR operation of inverted M/ IO and RD.
- MEMW. Memory write: It is obtained using OR operation of inverted M/ IO and WR.
- IOR. I/O Read. It is obtained using OR operation of M/ IO and RD.
- IOW. I/O Write. It is obtained using OR operation of M/ IO and WR. When

8086 operates in maximum mode of operation the control signal for read and write operations are:
MRDC It is equivalent to MEMR
MWTC It is equivalent to MEMW
IORC it is equivalent to IOR
IOWC it is equivalent to IOW

8086 Addressing and Addressing Decoding:

- The 8086 has 20 address bus. It can directly address up to 1 MB using 20 address lines.
- A memory location stores 1 byte of information and a word(2 byres) is stored in two consecutive memory locations. When the instruction MOV 0300, 1592H is executed, 92 is storeed in the memory location 00300H and 15 is stored in 003001H.
- To read or write a word in one bus cycle, the memory for an 8086 based system is

set up in two banks.

- One memory bank containing all the memory location which have even addresses such as 00000H, 00002H, 00004H etc. The data lines of this bank of memory are connected to the lower eight data lines D_0-D_7 of Intel 8086 microprocessor. This bank is called lower memory bank.
- The other memory bank containing all the memory locations which have odd addresses such as 00001H, 00003H etc.
- The data lines of this bank of memory are connected to the upper eight data lines D_8-D_{15} of Intel 8086 microprocessor.
- This bank is called upper memory bank.
- A_0 is used as a chip enable signal for the lower memory bank containing even addresses.

- BHE signal is used as a chip enable signal for the upper bank of memory which containing odd addresses.
- The external latch is strobed by the ALE signal.
- The address lines A1 – A19 are used to select a memory location in both lower and upper memory banks.
- When an even memory location is to be addressed, A0 goes low and BHE goes high.
- The lower memory bank is enabled and the upper memory bank is disabled. The data is transferred to or from the addressed memory location in the lower bank D_0-D_7.
- When an odd memory location is to be addressed, BHE goes low and A0 goes high.
- This enables upper memory bank and disables lower memory bank. The data is transferred to or from the addressed memory location in the lower bank D_8-D_{15}.

Address Decoders

Several memory and I/O devices are required in a computer system. They are connected to the microprocessor through decoders. The relevant memory chip of I/O device is selected by the decoder. The task f decoding can be performed by a simple decoder such as 74ls138 or 74ls139, a bipolar PROM or PLA(Programmed Logic Array). A PROM is more powerful device than a simple decoder. PLA is also used as address decoder in modern computers.

ROM Address Decoding

- ROM interfacing using 74LS138 decoder. System contains several ROMs or

EPROMs, a simple decoder such as 74LS138 or a PROM decoder can be used for electing a ROM/ EPROM in the system according to the address issued by the microprocessor. The 8086 sends M/Io signal to distinguish whether a memory chip or I/o device is to enabled.

- When M/IO goed high, a memory chip is to be enabled and when it is goes low, an I/O device is to be enabled.
- The decoder 74LS138 has three enable pins G_1, G_2A, G_2B.
- This chip is enabled when G_1 goes highG_2A and G_2B goes low.

A, B, C are selected lines.

- When A,B and C are 000, Y_0 is selected and when selected lines are at logic 001, Y_1 is selected.
- Decoder output Y_7 is used to enable to output of ROMs in lower and upper bank memory.

 A_0 and BHE are been used to enable ROM. A_1 to A_{11} are goes directly to ROM. A_{12} to A_{15} are kept high and applied to G_2B through a NANG gate to enable the decoder. RD is applied to G_2A. M/IO to G_1 to enable the decoder. A_{17} to A_{19} are applied to selected lines.

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ROM interfacing using PROM decoder

ROM interfacing using PROM decoder which has 8 address lines A_0 to A_7. It has 8 bit output O_0 to O_7. M/IO and RD have been used to enable the PROM decoder. A_{12} to A_{19} are applied to PROM decoder. Two pins are connected to output pins O_0. A_0 is used to enable ROM1. BHE is used to enable ROM2. The output O_0 enable both the ROM1 as well as ROM2 Memory location of ROM with even address is to be read, A_0 is made low and BHE to high and O_0 is made low. When odd address is to read, A_0 is made high and O_0 is made low, BHE is low. • ROM1 Contains even address.

- ROM2 Contains odd address.
- A_1 to A_{11} go directly to ROMs and decide the address range.

Alternative ROM interfacing using PROM decoder

A_0 and BHE can be connected to address lines A_0 and A_1 of the PROM decoder. ROM1 will be enabled by O_0 and ROM2 by O_1. Output enable pin of ROM1 OE will be connected to RD. CS2 of PROM decoder will be grounded. To read even address O_0 is made low. To read odd address

O_1 is made low. A_{14} to A_{19} are connected to A_2 to A_7 of the PROM decoder. A_1 to A_{13} will go directly to the ROMs which will decide the address of memory location with in the ROM.

Ram address Decoding

RAM interfacing using 74LS138 decoder. Address lines A_{17} to A_{19} go to the selected lines of the decoder. Address line A_{16} goes to G_2A. The decoder is enabled when A_{16} is low. Address lines A_1 to A_{15} go directly to RAMs. RD is connected to output enable OE of the RAM. WR is connected to W of the RAM. The RAM is connected to the output line Y_7 of the decoder. Y_7 goes low when address lines $A_{17,}$ $A_{18,}$ A_{19} have logic 111. A_0 and Y_7 are applied to an OR gate. The output of the gate is connected to chip enable pin CE of RAM. BHE and Y_7 enable RAM2. ❖ RAM1 Contains even address.

❖ RAM2 contains odd address.

Diagram

RAM interfacing using PROM decoder

In case of RAM, the control signals RD and WR are applied to RAMs. A_0 is connected to A_0 and BHE to A_1 pin of the PROM decoder. The address lines A_{16} to A_{19} are connected to A_2 to A_5 pin of the PROM decoder. Pins A_6 and A_7 of the PROM decoder are grounded. M./IO is inverted and then connected to chip to enable signal of the PROM decoder. The output O_0 is connected to chip to enable pin of RAM1. O_1 is connected to chip to enable of RAM2. Address lines A_1 to A_{15} are connected directly to RAMs.

❖ RAM1 Contains even address and RAM2 contains odd addresses.

❖ When A_0 is low and BHE is high the Output O_0 goes low and RAM1 is enabled.

❖ When is high and BHE is low, the output O_1 goes low and RAM2 is enabled. ❖ The outputs O_0 to O_1 are mede low for writing or reading a word of data.

Interfacing of I/O device through 74LS138

- Intel 8279 has been taken as an example of I/O device. The address lines A_1 goes directly to the I/O device.
- As A_1 may have two binary values, 0 and 1, the 8279 will have two address for its operation.
- The output Y_0 is connected to the chip to enable pin of the 8279.
- The address lines $A_{0,}$ A_2 and A_3 are connected to the selected lines of the decoder. When all these lines go low, Y_0 goes low and the 8279 is enabled.

- G_1 is connected to 5 volt dc to enable the decoder. M/IO is connected to G_2A. when it is low, the decoder is enabled. G_2B is connected to address lines A_4 to A_{15} through a NAND gate.
- When all these address lines go high, G_2B goes low and enables the decoder. D_0 to D_7 are connected to 8279, data must be sent to or read from the 8279 at even address.
- Other I/O devices are connected to other output pins such as $Y_1, Y_2 \ldots. Y_7$.

Diagram

Interfacing of I/O device through PROM decoder.

- The address line A_1 is connected to pin A_0 of the 8279. The output O_0 of the PROM decoder is connected to the chip enable pin CS of the 8279.
- The address line A_0 is connected to A_0 pin of PROM decoder.
- BHE is connected to A_1 of the PROM decoder. Address lines A_3 to A_6 are connected to A_2 to A_7 pins of the PROM decoder.
- The address lines A_7 to A_{15} are inverted M/IO are connected to the chip to enable pin CS of the PROM decoder through NAND gate. When A_0 goes low, output O_0 goes low to enable 8279.
- D_0 to D_7 are connected to 8279, data must be sent to or read from the 8279 at even address. Other I/O devices are connected to other output pins such as $Y_1, Y_2 \ldots. Y_7$.

Interfacing of 8255 using 74LS138

- The 8255.1 is enabled when both the address lines A_0 and the output of the decoder Y_7 go low.
- The 2nd unit 8255.1 is enabled when both Y_7 and BHE go low.
- The address line A_1 and A_2 go directly to 8255 to select internal ports and the control word register of 8255.
- The first unit 8255.1 contains the ports of even address and the lower 8 data lines, D_0 to D_7 are connected to it. A byte can be read from or written to an even addressed port in 8255.1.
- The 2nd unit contains odd address port and the data lines D_8 to D_{15} are connected to it. To input or output a WORD, both 8255.1 and 8255.2 are enabled.

Interfacing of8255 using PROM decoder

The 8255.1 is enabled when the output of he decoder O_0 goes low.
The 8255.2 is enabled when the output of he decoder O_1 goes low. The address lines A_0 and BHE are connected to pins A_0 and A_1 of the PROM decoder. The output O_0 goes low when the address line A_0 is low and BHE is high. The data lines D_0 to D_7 are connected to 8255.1. A byte is read from or written to even address port of 8255.1. A byte can be read from or written to an odd addressed port of 82555.2. To input or output a word, both 8255.1 and 8255.2 are enabled.

Programmable I/O ports

- An I/O port is a place for loading and unloading data. Input or output devices are connected to the microprocessor through I/O ports.
- An input device sends data to an input port. The microprocessor reads data from the input port. An output device sends data to an output port.
- From an output port data are transferred to output devices. An I/O port may be either programmable or non-programmable. A non-programmable port act as an input port if it is connected to the microprocessor to act as an input port.
- A programmable port can be programmed to act either as an input port or output port.

Intel 8212 is an ex for a non-programmable port.
Intel 8255 is a programmable peripheral interface.

Programmable peripheral interface, Intel 8255 and Intel 82C55

Intel 8255 is a programmable peripheral interface(PPI).82C55 is a high performance CHMOS version. CHMOS version consumes less power. Either of the versions contains three programmable 8-bit ports namely port A, port B, port C. The port C can be divided in to two 4-bit ports. Port C_{upper} and port C_{lower}. The 8255 has a total of 4 ports: two 8bit ports and two 4bit ports.

A_0 and A_1

These are used for addressing the ports and control word register of 8255. CS(chip select)

When it goes low the 8255 is selected(enabled)

RD(read)

When it goes low, CPU reads data from an input port of 8255.

WR (write)

When it is goes low, the CPU write control word into the control word register of 8255.

Operating modes of 8255

Intel 8255 has the three operating modes

- ❖ Mode 0 – simple input/output mode

- ❖ Mode 1 – strobe input/output mode
- ❖ Mode 2 – bidirectional bus mode
- ❖ In mode 0, a port can be operated as a simple iput or output port. Each of the four ports can be programmed to be either an input port or output port. No handshake signal is required, data simply written to or read from the specified port.
- ❖ In mode 1, provides strobed input/output mode of operaion only for port A and port B. when a port operates in mode 1, data are transferred from or to this port under certain control signals.ppins of port C are used to provide control(handshake) signals. When both port A and port B operate in mode 1, six pins of port C are used to carry control signas. The combination of mode 1 and mode 0 can also be used. port A may operate in mode 1 while port B in mode 0 or vice versa.
- ❖ In mode 2, port A operates as a bidirectional port. PORT A is used for both sending and receiving data from / to a peripheral device. When port A operates in Mode 2, the port B can operate either in Mode 1 or Mode 0.

Bit set-reset feature(BSR)

- Any of the eight bits of port C can be set or reset individually by sending a suitable bit set/reset control word to 8255.
- When port C is used for control/status operation, it is used to set or reset individual bit as if they are output ports.
- For ex, 8 LED can be connected to pins of Port C, one LED to each pin. Individual LED can be turned on or Off using set/reset feature of Port C.

Control groups

- For the purpose of controlling 4 I/O ports of 8255, they are divided in to two groups, namely Group A and Group B.

Group A contains port A and port C_{upper} for control operation.

Group B contains port B and port C_{lower} for control operation.

A control word is determined, which contains information whether a port will be an input or output port, mode of operation, etc. CPU sends the desired control word to 8255. There are two control blocks which receive commands from read and write control logic and receive control words from the CPU through data bus buffer. The control blocks issues the proper commands to the associated port.

Control word

8255 is a programmable device, a control word is determined to decide the modes and

configuration (whether the particular port will act as an input port or an output port) of its various ports. When a particular port is to act as an input port the corresponding bit for that port set to 1. If a port is to act as an output port the corresponding bit for that port is set to 0.

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Control word for bit set/reset of pins of Port C

Any bit of Port C can be set or reset individually by sending a suitable control word of 8255.

Handshake signals for Input Port in Mode 1

STB(strobe input)

An input device loads data into a port (operating in mode 1) by making STB signal low. The data is latched in to the input latch for the specified port.

IBF (Input Buffer Full)
It is an ack signal sent by 8255 to the peripheral. When it goes high it indicates that data has been received and loaded in to input latch.

INTR(Interrupt request)
It is an active high signal. An input device can interrupt CPU by making this signal high. when INTR goes high, CPU suspends its current operation and reads the data written into the specified port (operating in Mode 1) by the peripheral.

Handshake signals for an output port in mode 1

OBF (output buffer full): When CPU writes data into the specified port 0f 8255, ~~OBF~~ goes low. It is used as a strobe input signal to the peripheral to latch the contents of the specified port. OBF is reset when ACK goes low.

ACK (Acknowledge Request). It is an active high signal low, the peripheral informs 8255 that the data from the specified port has been received

INTR (interrupt Request): It is an active high signal. It is used to interrupt CPU whenever the output buffer is empty.

Handshake signals for an output port in mode 2

The handshake signals for Port A operating in mode 2. Signal for output operations are OBF, ACK and INTE1 . Signals for input operations are: STB, IBF and INTE. When the port A operates in modes 2, port B may operate in Mode 1 or Mode 0. When Port B operates in Mode 1; PC_0, PC_1 and PC_2 are used for its control. When Port B operates in Mode 0; PC_0, PC_1 and PC_2 operates as simple input or output port.

DMA DATA TRANSFER:

- In DMA data transfer scheme, data are directly transferred from an I/O device to memory or vice versa without going through the CPU.

- The I/o device which wants to transfer data using DMA techniques sends a HOLD signal to the microprocessor. On the receipt of HOLD signal from an I/O device. The microprocessor completes its current bus transfer and releases the address and data bus.
- Then its sends acknowledgement signal HLDA to the I/O device to indicates that is has receive the HOLD request and has given up the control of addresses and data buses.
- In DMA data transfer techniques the CPU remains idle while data are being transferred. The CPU becomes active only after the DMA request with drawn by the I/O device.
- The DMA data transfer scheme in which I/O device releases the system, buses only after transferring all the data bytes is called **BURST mode data transfer.** In this mode a complete block of data is transferred. It is used by magnetic disk drives where data transfer cannot be stopped in the mid way without loss of data and therefore block data transfer is must.
- In such case CPU remains inactive for a relatively long period. Another DMA technique call cycle stealing permits DMA controller to use system bus to transfer one or more data bytes and then returns the control of buses to CPU.
- The interference can be eliminated completely by designing the DMA interface in such a manner that bus cycle are stolen only when CPU is not using the system bus.
- This is known as TRANSPERENT DMA.

Programmable DMA controller, Intel 8237 and Intel 82C37:

In Intel 2387, is high performance programmable DMA controller. Its CHMOS version is

82C37. The CHMOS version consumes less power.
$DREQ_0 - DREQ_3$ .DMA request lines. One of these lines is used by an I/O device to send DMA request. DREQ line is kept high until corresponding DACK signal becomes active. **$DACK_0 - DACK_3$** : DMA acknowledgement signals. When DMA request is granted an acknowledgement is sent to I/O device 8237 through this line.
$DB_0 - DB_7$: Data bus. These are bi-directional three state data bus lines. These lines carry $8MSB_S$ of memory address in the beginning of DMA cycle.
$A_0 - A_3$: These are bi-directional LSB_S of the address lines. In the idle cycle these are used as input lines by the CPU to address internal registers for read and write operation. $A_4 - A_7$: these are 4 MSBs of the address lines These are three state uni -directional output lines and are enable only during DMA cycle
HRQ Hold request. The 8237 sends hold request to CPU through this line. HLDA Hole acknowledgement. This is a hold acknowledgement signal sent by CPU to 8237 to indicate that microprocessor has released address and data buses.
MEMR Memory read, It is made low when data are to be are to be transferred from memory to IO device.

Memory to Memory data transfer:
The Bit number 0 of the command register enables or disables memory to memory data transfer. When this bit is set to 1, memory to memory DMA data transfer is enabled and when set to 0 memory to memory data transfer is disabled. Data is read from memory location address location addressed by channel 0 and saved in temporary register 8237. The 8237 indicates a memory write operation to transfer the contents of temporary register to a memory location addressed by channel1.

Modes of DMA data transfer:

Single transfer mode: In this mode, DMA data transfer the 8237 is programmed to make 1 transfer only. After the completion of one data transfer the bus control transfer to microprocessor if the DREQ line is still high. The 8237 again sends request for DMA data transfer to microprocessor

Block transfer mode: The block transfer mode of DMA data transfer automatically transfers the number of bytes indicated by the count register for the channel. The 8237 is activated by DREQ.

Demand transfer mode: In this mode a data transfer until an external EOP input goes low or until the DREQ input becomes inactive.

Cascade mode: This mode, is used to cascade more than one 8237 together for DMA data transfer.

OTHER MICROPROCESSOR:

POWERPC MICROPROCESSOR:
A power PC microprocessor is a high performance super scalar, RISC microprocessor. It is more powerful than competing microprocessor. IBM, APPLE and many other companies are using it in their PC's workstations and servers.The power PC machine includes Microsoft windows NT, IBM's OS/2, MAC OS8.5 and MAC OSX, UNIX. A different versions of power pc microprocessor are 601,602,603,EC603e, 604, 604E, 740 and 750

PowerPC 601 (PPC 601 or MPC 601)

The powerPC 601 which was introduced in the year 1993 is a 32 bit high performance, superscalar RISC microprocessor. It is designed with a 32 bit address bus and 64 bit data bus. It has 32 32 bit general purpose registers and 32 64 bit floating point registers. It executes 3 instructions per clock cycle and is available at 100 and 120 MHZ. It operates at 3.6v. IT is compatible with TTL devices. It uses 0.5 micron process technology contains 2.8 million transistors its size is 74 mm^2 and power consumption is 4watts.

The major functional units contained in the PowerPC 601 are:
1. Instruction Unit

2. Integer Unit
3. Floating Point Unit
4. Memory Management Unit
5. Cache Memory
6. Memory Unit
7. System Interface Unit

The first 3 units are execution units. The instruction unit contain queue an issue logic and a branch processing unit(BPU). The instruction are loaded in to an instruction queue (IQ) from the on chip cache. The queue can store up to 8 instruction which can be loaded from cache in a single clock cycle. The IQ provides storage for all execution units.
The Branch processing unit handles all the branch instructions received by the processor. The

601 uses an advanced technique to predict where a conditional branch will jump. The branch processing unit contains 3 special purpose user control registers: LR, CTR, CR . The LR holds the return pointer for a subroutine, The CTR holds the branch target address and CR holds the result.

PowerPC 602:
The power 602 is designed for graphical, multimedia, voice recognition/ synthesis and other functions that are required in new entertainment education and other information devices. It is a 32bit, 66MHz microprocessor. It includes on chip floating point unit uses superscalar architecture.

Power 603(PPC 603 or MPC603):
The Power 603 was introduced in1993. It has designed for low power consumption. It consumes 1.2 watts at 100 MHz and operates at 3.3 volts. Its versions 603e operate at 300 MHz. It has a 32 bit address bus and 64bit data buses contain an 8KB data cache and an 8KB instruction cache and execute 3 instructions per clock cycle. It contains 2.6 million transistors at 100 MHz it uses 0.5 micron CMOS process technology and it is cheaper and smaller than PowerPC. It is used in notepad, laptop, portable and personal digital assistant.
The 603 contains the following functional units.

1. Instruction Unit
2. Integer Unit
3. Floating point Unit
4. Load/store Unit
5. System Register Unit
6. Data memory management Unit
7. Instruction memory management unit
8. 8KB data cache
9. 8KB instruction cache.
10. completion unit
11. System Interface unit.

PENTIUM MICROPROCESSOR:
Pentium is a 32-bit superscalar, CISC mp developed by intel corporation. It was introduced in the year 1993. It has 32-bit address bus and 64-bit data bus to ALU's to 8KB cache memory, on chip floating point math coprocessor unit, prefetch buffers and a branch target buffer etc.,

The Pentium processor operating at 60 and 66 MHZ contains 3.1 million transistors and

the processor operating at higher frequency contains 3.3 million transistors. It is packed in 273 pingrid array package(PGA). Initially the Pentium was designed to operate at 60 MHZ gradually its frequency raised to 200 MHZ

Register organization: Registers of Pentium processor are same as those of 486 microprocessor except some changes in the control register set the register of integer unit are eight 32 bit general purpose register, 6 16-bit segement registers 1 32-bit flag register and 1 32-bit instruction pointer. The flag in Pentium processor are

Six condition flag: carry, parity, auxiliary, zero, sign and overflow

Control flags: trap flag, interrupt flag, enable, direction, IOPL, RF, alignment and identification flag

Operating mode flag: nested task flag, virtual 8086 mode, virtual interrupt flag, Virtual interrupt pending.

Super Scalar Architecture:

 The Pentium has a super scalar architecture uses RISC microprocessor. The architecture contains more than one execution unit or pipeline known as super scalar architecture. The Pentium being a super scalar microprocessor is designed to have ALU. The dual pipeline are called U-pipeline and V-pipeline. Each pipe line has its own arithmetic logic unit, address generation circuitry and data cache interface. Each pipeline of the Pentium processor executes integer instructions in five stages: prefetch, decode1,decode 2,execute and writeback.

On chip separate cache memory for code and data:

 The Pentium processor contains two 8KB cache memories, one for code and other for data. Both are organized as 2way set associative caches with a 32bit line size. Separate onchip code and data caches increases performance reducing bus conflicts can occur between instruction prefecthes and data.

The data cache in the Pentium mp is configurable to be write-through or write back where as the cache in the 486 mp write through cache.

 The DX4 and DX2 versions of 486 are also available with write back on chip cache.

Advantages: The main memory always contains the same data and cache. The characteristics are desirable in a system with direct memory access transfers. The code cache of Pentium processor is write protected. Each cache has been provided with a translation look aside buffer.

Branch Prediction:

 The full advantage of the CPU pipeline can be taken only when it remains full with the instructions in various stages of execution. In conditional branch it is not clear whether or not the branch is actually to be taken until the condition is tested.

Static branching prediction:

- In the static branch prediction fixed prediction and rules are followed. The branch is automatically assumed to be taken or not.
- If it is assumed to be taken the target instruction is to be fetched and loaded into the pipeline to begin the execution.
- If the branch is assumed to be not taken, the next instruction is simply fetched and loaded into the pipeline.
- In the static branch prediction if the wrong action is taken, the pipeline must be flushed and the correct instruction sequences fetched and loaded. This process may cause delay of three to four clock cycles.

Dynamic branch Prediction:

In the dynamic branch prediction the predicts whether the branch is to be taken or not depending upon the history of the branch actions. A hardware is used maintain a branch history table .

Branch Prediction scheme used by Pentium:

The Pentium processor makes dynamic branch prediction using a branch target buffer(BTB). To efficiently predict branches the Pentium uses two pre fetch buffers. One buffer prefetches code in linear fashion while the other prefetches instruction based on the addresses in the branch target buffer.

Floating-point Unit:

The Pentium processor consists of five functional units and an additional three-stage floating point unit which is parallel with one of the integer pipeline, namely U pipeline.

Power management Features:

The Pentium processor is provided with power management features which reduces the power consumption by putting the processor and in peripherals in low power state when they are idle or doing less intensive work. When the power processor goes low or very low power state, the registers and RAM retain their values. The power management technique used at system level, known as system management mode(SMM),controls power consumed by the computer and peripherals.

PENTIUM PRO MICROPROCESSOR:

Pentium pro microprocessor also contains a second level cache, cache controller and advanced programmable interrupt controller on the chip. The Pentium pro contains 512/256 KB second level cache on addition to first level cache. The data cache is 4 way set associative write back or write through. The second level L2 cache is 4 way set associative write back or write through. Its clock frequencies are :150 MHz, 166 MHz and 200MHz.

Capacity of second level cache

Clock second Level Transistors Microns

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Cache L2 CPU + L2 CPU/L2
150 MHz 256 KB 5.5 + 16 million 0.5/0.5
166 MHz 512 KB 5.5 + 31 million 0.35/0.35 180 MHz 256 KB 5.5 + 16 million 0.35/0.5 200 MHz 256 KB 5.5 + 16 million 0.35/0.5 200 MHz 512 KB 5.5 + 31 million 0.35/0.35

Pentium Pro Architecture:
The Pentium pro has a decoupled 12 stage, super pipelined architecture. It does not use linear instructions sequencing between the traditional 'fetch' and 'execute' phases. It uses a instruction pool. The traditional 'execute' phase is replaced by decoupled 'dispatch'/'execute' and 'retire' phases. The new structure allows instructions to be stored in any order but always be completed in the original program order. The first instruction requires an operand which is not present in the cache memory. This situation is called 'miss'. The Pentium pro
Processor looks ahead into its instructions pool at its subsequent instruction, The second instruction can be executed as their operands are available.
The Pentium pro has ability to execute instructions in any order by predicting program flow. It selects the best order to execute instructions after analyzing the programs data flow. This is called dynamic execution technology.

The Pentium pro processor pipeline
Fetch/ decode unit
It is an inorder unit. It receives the user program instruction stream as input from the instruction cache and decodes them into a series of micro operations. The fetch/decode unit has been designed to be much more intelligent so that it can predict program flow.

Dispatch/execute unit:
It is an out of order unit. It receives dataflow stream. The dispatch unit selects micro operations from the instruction pool after checking their status. The dispatch/execute unit executes instructions in out of order fashion not in a sequence it has been designed to have much more visibility into the program instruction stream so that better scheduling may be achieved.

Retire unit:
This unit checks the status of micro operations in the instructions to know which micro operations have been executed, and can be removed from the pool. The retire unit not only checks which micro operations have been executed. It first reads instruction pool to find out the potential micro operations for retirement and determines which of these micro operations are next in original program order.

Pentium II

Intel has introduced Pentium II microprocessor suitable for multimedia computers. Its clock frequencies are:233,266,300,333,350 and 400 MHZ. Intel has Pentium II at 500 and 700 MHZ. Pentium II is Pentium pro microprocessor with MMX technology. The capacity of L2 cache is 512 KB. It uses 0.25 micron process technology.

Celeron:
Intel's Celeron is a low cost 32 bit processor based on Pentium pro architecture. It was introduced in the year 1999. Its clock rate varies form 266MHZ to 700MHZ. Its versions at 266 MHZ and 300 MHZ did not contain second level onchip cache memory. They contain 7.5 million transistors. It's 300A,333MHZ higher clock versions contain 128KB second level cache within the processor chip. They contain 19 million transistors. The Celeron includes Intel MMX(multimedia Extension) data. The MMX technology provides a set of basic general purpose integer instructions that are easily applied to the needs of a wide diversity of multimedia and communication applications.
It has new instructions for multimedia eight 64bit wide MMX registers and handles the following 4 new data types:

1. Packed bytes - eight bytes can be packed into one 64 bit quantity
2. Packed words- Four 16-bit words can be packed into one one 64bit quantity 3. Packed double word- Two 32 bit double words can be packed in to 64 bit quantity. 4. Quad word-one 64 bit quantity

Pentium III:
Pentium III is a 32 bit processor of Intel corporation. It was introduced in the year 1999. The Pentium III is based on Pentium pro micro architecture. It contains 70 new instructions that enhanced multimedia processing and video streaming. These instructions are implemented using SIMD technology. The family members are: katmai, coppermine, tanner,etc.., Its speed clock for different versions are :700,733,850 and 1000MHZ.
The new instructions extensions are also called internet streaming SIMD instructions. The utilization of SIMD architecture and memory streaming architecture in decoupling memory access for computation improves processor performances.

Pentium IV:
Pentium 4 is a 32 bit CISC processor. It is based on Pentium pro data flow architecture. It contains 42 million transistors. It has 36 address and 64 data lines. It operates at 1.4 and 1.5 GHZ. It uses 0.13 micron process technology. It has a total of 144 SIMD instructions. It uses 850 chipset for I/O and memory interfacing.
Itanium(or Merced) Processor:
It was the first processor of Intel corporation. Itanium based systems will primarily targeted to E

commerce applications and ISPs.

ALPHA MICROPROCESSOR

The 64 bit alpha microprocessor 21064,21164 and 21264 have been developed by digital equipment corporation (DEN). Its clock frequencies:200 MHz, 300MHz, 622 700 and 1000 MHz. They are 64 bit RISC microprocessor.

The alpha microprocessor contains eleven step dual pipelines. Alpha 21064 contains 1.7 million transistors. It has 32 general purpose registers and 32 floating point registers. All registers are 64 bit wide. The processor contains 8KB

Instruction cache and 8 KB data cache. It has 4 independent processing units: integer, floating point, instruction fetch and branching and memory load/store units. The Alpha 21164 contains

9.3 million transistors. Its clock rates are 600 and 633 MHz. SPEC int 92 and SPECfp92 ratings are 300 and 500 respectively. The Alpha 21264 operates at 700 and 1000 MHz. It uses 0.25 process technology.

CYRIX MICROPROCESSOR:

Cyrix is competitor of intel. It has developed 32 bit 586 and 686 microprocessor. The 586 microprocessor is compatible to Pentium microprocessor. Cyrix has designed 6X86Mx microprocessor which is manufactured by IBM. It outperforms Pentium II running at 233MHz. Is different versions are available at 133, 200 and 233 MHz.

MIPS MICROPROCESSOR:

MIPS is a famous company which produces RISC microprocessor. R4000,R5000,MIPS10000,MIPS12000 series etc. These microprocessor are suitable for workstations. There are 64bit RISC microprocessor. It contains 6.4 million transistors. Its SPEC int92 rating is 300 and SPECfp92 rating is 600. It contains 32 general purpose and 32 floating point registers, 5 functional units

AMD(Advanced Micro Devices) Microprocessors:

AMD has developed for 32 bit K5, K6,K6-MMX and K7 microprocessors. K5 is competitor to Pentium microprocessor. It operates at 166,200 and 233MHZ. It can execute all leading operating systems like windows 95/NT/3.X,MSDOS,Nove,Netware,OS/2 warp, UNIX, Solaries.

It can address high end engineering, scientific, design and graphic applications on a desktop. The second generation of K6 processor is K6-2. Its important features are:9.3 million transistors,81 mm square die,0.25 micro process technology,400 MHZ clock. K& is now called Athlon. It operates at 1.1 GHZ. Its bus frequency is 200 MHZ. It uses copper wires rather than aluminum,

to connect circuits.

The code name of the next generation of Athlon chip is Thunderbird. AMD has also developed low cost version of Athlon,called uron. Covette and camaro are low power versions of Athlon and Duron.

EXPECTED QUESTIONS

1. Explain input devices and output devices.
2. Write in detail DMA Data Transfer with neat diagram.
3. Discuss about Pentium Pro microprocessor in detail.
4. Write in detail 8086 Addressing and Address Decoding.
5. Write in detail Programmable I/O Ports.

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KAAMADHENU ARTS AND SCIENCE COLLEGE

SATHYAMANGALAM

DEPARTMENT OF COMPUTER APPLICATIONS AND INFORMATION TECHNOLOGY

SUBJECT NAME : MICROPROCESSOR AND ASSEMBLY LANGUAGE PROGRAMMING
STAFF NAME :
UNIT NO. : V
SEMESTER : III
NO. OF PAGES : 14
CLASS : II BSC IT

Unit – V

MOTOROLA 68000, MOTOROLA 68020, MOTOROLA 68030, MOTOROLA68040 Interfacing of A/D Converter and Applications: Introduction – Interfacing of ADC 0808 or ADC 0809 to Intel 8086 – Bipolar to Unipolar Converter – Sample and Hold Circuit, LF 398 – Microprocessor-based Measurement and Control of Physical Quantities.

MOTOROLA 68000

The 68000 is a 16-bit, 64-pin microprocessor introduced by Motorola in 1979. This was used earlier to build many computers. It contains a circuitry of 70000 transistors. The clock rates for its different versions are: 10MHz, 12.5MHz, 16.67MHz and 25MHz. It has instructions for multiplication and division.
It generates 24 bit address and can directly address 16 MB memory. It contains 32 bit registers many of its instructions perform 32 bit operations.
It has two strobe signals UDS upper data strobe and LDS lower data strobe. The most significant bits of the address are sent on the 23 address lines. The least significant bit of the address decides the status of UDS and LDS depending upon the type of the operand.

REGISTERS:
In arithmetic operations the data register serve as source or destination of the operands. Each of the data register can handle a byte, a word (16 – bit) or 32 bit data. The address register are used to specify operand address. The data registers and the address registers can also be employed as index registers.
Eight 32 bit data register
Seven 32 bit address register
One 32 bit user stack pointer
One 32 bit supervisory stack pointer
One 32 bit program counter
One 16 bit status flag register

OPERATING MODES:
The 68000 has 2 operating modes, user and supervisory modes.
The supervisory mode is also known as privileged mode or operating system mode. The supervisory mode is indented for the use of operating system.
In the supervisory mode the supervisory stack pointer is used for locating the stack top. The user mode, the user stack pointer is used to locate the stack top.

ADDRESSING MODES:
The 68000 provides the following addressing modes.
- Direct addressing
- Immediate addressing
- Register addressing

- Register indirect addressing
- Indexed addressing
- Based addressing
- Based Index addressing
- PC-Relative addressing
- PC-Relative index addressing

Indexed addressing: In this mode of addressing displacement is added to the contents of the base register. This instruction contains a 16 bit signed displacement and an address register holds 32 bit base address.

Based indexed addressing: In this mode the contents of a base register is added to the contents of the index register. An address register is employed to act as a base register.

PC-Relative addressing: In this mode fixed displacement is added to the current value of the program counter to obtain the effective address

.

PC-Relative indexed addressing: The contents of PC are added to the contents of an index register.

STATUS FLAGS:

The 68000 has a 16-bit status flags register.

It has been divided into a users byte(bits 0 to 7) and a supervisory byte (bits 8 to 15) There are 5 status flags in the user's byte. They are:

- Carry C
- Overflow OV
- Zero Z
- Negative N
- Extend X

The supervisory bytes contains the following the status flags:

- Interrupt Mask: 3bits: I0, I1 and I2
- Supervisory state Indicator, S

- Trace Flag, T

EXCEPTIONS:

The 68000 provides following exceptions: External Interrupts

- Internally generated exceptions when normal instructions are exacted: TRAP, TRAPV, CHK and DIVS.

- Execution of privileged instructions in user's mode execution of illegal instructions.
- Single step checking
- Address error
- Reset

Semaphore and protection:
The 68000 provides semaphore. The provision of the supervisory and the user mode of the operation provides protection. The complete protection is provided when external MMU, M68451 is employed.

BERR Bus error
BR Bus request
BG Bus grant
BGACK Bus grant acknowledge
AS Address Strobe
UDS Upper data strobe
LDS Lower data strobe
DTCK Device acknowledge
R/W Read/ Write control
VMA valid memory address
VPA Valid peripheral address
E Enable

MOTOROLA 68020

- The 68020 introduced in 1984 is a 32-bit microprocessor. It uses CMOS technology and contains a circuitry of 2 lakh transistors.
- It has 114 pins packed in a PGA package. Its clock rates are: 12.5, 16.67, 20, 25 or 33 MHz.
- It can directly address up to 4 GB of memory.
- It operates in two operating modes: Supervisory mode and Users mode

REGISTERS:

- The visible registers of 68020, are same as those of 68000.
- The additional registers are supervisor registers.
- The 68020 contains the following registers

 Eight 32-bit data registers
 Seven 32-bit address registers.
 One 32-bit program counter.
 One 32-bit user stack Pointer
 Two 32-bit supervisor stack pointers One 16-bit status register
 One 32-bit vector based register
 One 32-bit cache control register
 One 32-bit cache address register
  SFC and DFC register handle MOVES instructions.

ADDRESSIG MODES:

 The 68020 has 18 addressing modes and includes all the addressing modes of 68000. It also provides some additional addressing modes. It has index scaling and 16 and 32-bit displacement options to the based indexed and PC relative indexed modes.

Based Addressing:In 68020 a 32-bit displacement is added to the contented of a base register to get effective address.

Memory indirect addressing:In this mode the contents of a base register and a displacement are added. This sum points to the memory location which contains a 32 bit address. Base Indexed : A Scaled index is included in based addressing
The content of the base register, a displacement and a scaled index are added to form the effective address.

Memory Indirect Preindexed Addressing: A scaled index is added to the sum of the base register. This resultant quality is used to point the memory location which contains operands address.

PC- Relative Addressing Modes: PC is used in place of base register in addressing computation. The resultant quantity is used to point to the memory location which contains operands address

Exceptions:
The following features are externally generated exceptions:

i. Interrupts
ii. Bus error
iii. Coprocessor detected errors
iv. Reset

The internally generated exceptions are caused by:

1. Certain instructions

The following instructions may cause internal exception: CHK, CHK2, CALLM, RTM, RTE, DIV and all variations of TRAP.

2. Address errors
3. Tracing
4. Break points

5. Illegal instructions
6. Previlege violations.

Pin Configurations:
A0-A31 32 bit address bus D0-D31 32 bit data bus
FC0-FC2 3 bit function code. They are used to identify the address space of each bus cycle. They are similar to S0-S2 of 8086.
SIZ0-SIZ1,Size These signals together with A0 and A1 decide the active sections of the data bus.
~~IPL0-~~IP~~L2~~ Interrupt priority level
~~AVEC~~ Auto vector. Normally an external device identifies by sending an interrupt vector.

IPEND Interrupt pending
CDIS cache disable
~~RMC~~ Read modify write cycle. It is used as intel uses LOCK ~~ECS~~ External cycle start It indicate that a bus cycle is beginning

OCS Operand cycle start
AS Address strobe It indicate that a valid address in the address bus. ~~DS~~ Data strobe It indicates that valid data are placed or to be placed R/W read/write signal
D~~BEN~~ Enable signal for external data buffer
~~DSACK0/~~ D~~SACK1 D~~ata transfer and size acknowlwdge
~~BR~~ Bus request Through this line an external device request for bus control BG Bus grant CPU indicates that bus internal device request for bus control ~~BGACK~~ Bus grant acknowledge The external device acknowledges that it has assumed bus control.
~~BERR~~ Bus error It indicates that an invalid or illegal bus operation is being attempted

MOTOROLA 68030

The 68030 introduced in 1987 contains a 68020 plus a data cache and a memory management unit on the same chip. It was earlier used to built mini computers. It is a 32-bit processor. It is a 32 bit processor. Its direct memory addressing capacity is 4 GB and clock rates of 20MHz, 25 MHz and 33MHz. It has processing speed of 5 MIPS. It is designed to operate in multi user and processing multitasking environment. It has 256 byte instruction cache and 256 byte data cache.To support MMU the 68030 has the following additional registers in addition to those of 68020.

- 32-bit translation control register, TC
- 64-bit CPU root pointer, CRP.
- 64-bit supervisor root pointer, SRP
- 32-bit transparent translation registers, TT0 and TT1

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 16-bit MMU status register, MMUSR. **Pin configuration:**

~~CIIN:~~ Cache inhibit in it prevents data loading into the instruction and data caches.

CIOUT Cache inhibit out.
CBREQ Cache burst request
CBACK Cache burst acknowledge
~~MMUDIS~~ MMU disable
~~STERM~~ Synchronous termination

MOTOROLA 68040
The 68040 introduced in 1989, is a 32-bit processor.It contains a CPU, a floating point co preprocessor, memory management unit and 4 KB data. It contains 1.2 million transistors. Its direct memory addressing capacity is 4GB. Its performance is 3 times that of 68030. At 25MHz its computing power is 20 MIPS

INTERFACING OF A/D CONVERTER AND APPLICATIONS
INTRODUCTION:

 Microprocessor-based system is widely used for instrumentation and control applications.
 The electrical voltage which is obtained as an output of a transducer is in analog form. To measure electrical voltage we use A/D converter to convert analog electrical voltage in binary format acceptable to microprocessor.

INTERFACING OF ADC 0808 OR ADC 0809 TO INTEL 8086

The ADC 0808/ADC 0809 is an 8 –bit A/D converter with an 8-channel multiplexer of national semiconductor.It is a CMOS device and uses successive approximation techniques for analog to digital conversations. External zero or full scale adjustment is not required in case of ADC 0808/ADC 0809. It requires a clock of 10 k Hz to 1280 kHz. Higher the clock frequency less is the conversion time. Which 100 microseconds at 640 kHz. It requires a single 5V supply. The minimum width of the start of conversion pulse is 100 nanoseconds. The ALE pluse width is also 100 ns.

An interface of ADC 0809 to intel 8086 microprocessor through 8255. The clock of ADC has been supplied through IC 7490. The 7490 is a decade counter. The input to 7490 is the clock available at microprocessor kit, 8MHz. It is divided by 10 using 7490. The output 0f 7490 is 800 kHz.

Alternatively clock for A/D converter can also be obtained using programmable timer/counter, Intel 8254 or 8253. The 5Vdc reference voltage should be precision supply.

The pin 9 and 11 for output enable and Vcc can be supplied from the stabilized supply of the laboratory

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BIPOLAR TO UNIPOLAR CONVERTER:

The ADC 0808/ADC 0809 does not accept negative values of voltages. A suitable electronic circuit has been developed which accepts negative voltage signal. Thus the ADC0808/ADC0809 inconjuction with this electronic circuit called bipolar to unipolar converter, will accept positive as well as negative signals . The suitable electronic circuit has been developed which accepts negative voltage signal.

The address of the port of Intel 8255

8255.1 8255.2

Port A FFF8 FFF9
Port B FFFA FFFB
Port C FFFC FFFD
Control word register FFFE FFFF

PROGRAM

Memory address	Machine Label codes	Mnemonics Operands	Comments
0100	BA,FF,FF	MOV DX,FFF	Define ports of 8255.2
0103	B0,9A	MOV AL,9A	
0105	EE	OUT DX,AL	
0106	BA,FD,FF	MOV DX,FFFD	Select multiplexer channel IN3
0109	B8,03,00	MOV ax,03	

010C	EE	OUT DX,AL	
010D	B0,0B	MOV AL,0B	Start of conversion pulse without disturbing multiplexer channel
010F	EE	OUT DX,AL	
0110	B0,03	MOV AL,03	
0112	EE	OUT DX,AL	