

# **Intel® Xeon® Processor E5-1600 / 2600 / 4600 v3 Product Families**

## **Thermal Mechanical Specification and Design Guide**

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**October 2015**



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## Revision History

Revision Number	Description	Date
001	Initial release	September 2014
002	Added Intel® Xeon® processor E5-4600 v3 product families.	June 2015
003	Updated a socket part number on <a href="#">Table 25</a> .	October 2015



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## 1.0 Introduction

This document provides specifications and guidelines for the design of thermal and mechanical solutions for the Intel® Xeon® processor E5-1600, E5-2600, and E5-4600 v3 product families.

The components and information described in this document include:

- Thermal profiles and other processor specifications and recommendations
- Processor Mechanical load limits

The goals of this document are:

- To assist board and system thermal mechanical designers
- To assist designers and suppliers of processor heatsinks

### 1.1 Definition of Terms

**Table 1.**

#### Terms and Descriptions

Term	Description
Bypass	Bypass is the area between a passive heatsink and any object that can act to form a duct. For this example, it can be expressed as a dimension away from the outside dimension of the fins to the nearest surface.
DTS	Digital Thermal Sensor reports a relative die temperature as an offset from TCC activation temperature.
FSC	Fan Speed Control
IHS	Integrated Heat Spreader: a component of the processor package used to enhance the thermal performance of the package. Component thermal solutions interface with the processor at the IHS surface.
Square ILM	Independent Loading Mechanism provides the force needed to seat the 2011-LGA package onto the socket contacts and has 56 × 94mm heatsink mounting hole pattern
Narrow ILM	Independent Loading Mechanism provides the force needed to seat the 2011-LGA package onto the socket contacts and has 56 × 94mm heatsink mounting hole pattern
LGA2011-3 Socket	The processor mates with the system board through this surface mount, 2011-contact socket.
PECI	The Platform Environment Control Interface (PECI) is a one-wire interface that provides a communication channel between Intel processor and chipset components to external monitoring devices.

*continued...*



Term	Description
$\Psi_{CA}$	Case-to-ambient thermal characterization parameter (psi). A measure of thermal solution performance using total package power. Defined as $(T_{CASE} - T_{LA}) / \text{Total Package Power}$ . Heat source should always be specified for $\Psi$ measurements.
$\Psi_{CS}$	Case-to-sink thermal characterization parameter. A measure of thermal interface material performance using total package power. Defined as $(T_{CASE} - T_S) / \text{Total Package Power}$ .
$\Psi_{SA}$	Sink-to-ambient thermal characterization parameter. A measure of heatsink thermal performance using total package power. Defined as $(T_S - T_{LA}) / \text{Total Package Power}$ .
$T_{case}$	The case temperature of the processor measured at the geometric center of the topside of the IHS.
Tcase-Max	The maximum case temperature as specified in a component specification.
TCC	Thermal Control Circuit: Thermal monitor uses the TCC to reduce the die temperature by using clock modulation and/or operating frequency and input voltage adjustment when the die temperature is very near its operating limits.
$T_{CONTROL}$	$T_{CONTROL}$ is a static value below TCC activation used as a trigger point for fan speed control. When DTS > $T_{CONTROL}$ , the processor must comply to the thermal profile.
TDP	Thermal Design Power: Thermal solution should be designed to dissipate this target power level. TDP is not the maximum power that the processor can dissipate.
Thermal Monitor	A power reduction feature designed to decrease temperature after the processor has reached its maximum operating temperature.
Thermal Profile	Line that defines case temperature specification of a processor at a given power level.
TIM	Thermal Interface Material: The thermally conductive compound between the heatsink and the processor case. This material fills the air gaps and voids, and enhances the transfer of the heat from the processor case to the heatsink.
$T_{LA}$	The measured ambient temperature locally surrounding the processor. The ambient temperature should be measured just upstream of a passive heatsink or at the fan inlet for an active heatsink.
$T_{SA}$	The system ambient air temperature external to a system chassis. This temperature is usually measured at the chassis air inlets.
U	A unit of measure used to define server rack spacing height. 1U is equal to 1.75 in, 2U equals 3.50 in, and so forth.
LCC	Low Core Count, refers to silicon die size
MCC	Mid Core Count, refers to silicon die size
HCC	High Core Count, refers to silicon die size

## 2.0 LGA2011-3 Socket Overview

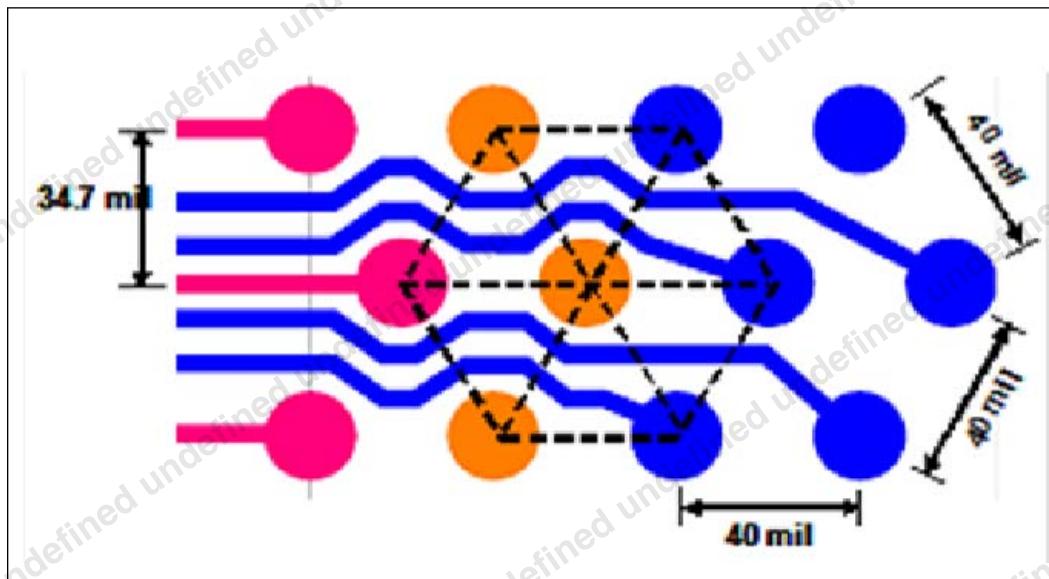
This section describes a surface mount, LGA (Land Grid Array) socket intended for the Intel® Xeon® processor E5-1600 and E5-2600 v3 product families processor-based platform. The socket provides I/O, power and ground contacts for processor operation. The socket contains 2011 contacts arrayed about a cavity in the center of the socket with lead-free solder balls for surface mounting on the motherboard.

The LGA2011-3 uses a hexagonal area array ball-out which provides many benefits:

- Socket contact density increased by 12% while maintaining 40 mil minimum via pitch requirements, as compared to a linear array
- Corresponding square pitch array's would require a 38mil via pitch for the same package size.

LGA2011-3 has 1.016 mm (40 mil) hexagonal pitch in a 58x43 grid array with 24x16 grid depopulation in the center of the array and selective depopulation elsewhere.

**Figure 1.** Hexagonal Array in LGA2011-3



**Table 2.** LGA2011-3 Socket Attributes

LGA2011-3 Socket	Attributes
Component Size	58.5 mm (L) X 51 mm (W)
Pitch	1.016 mm (Hex Array)
Ball Count	2011



The socket must be compatible with the package (processor) and the Independent Loading Mechanism (ILM). Internal keying posts ensure socket processor compatibility. An external socket key ensures ILM and socket compatibility. The ILM reference design includes a back plate; an integral feature for uniform loading on the socket solder joints and contacts.

## 2.1

## Socket Components

The socket has two main components, the socket body: composed of a housing solder balls, and processor contacts, and Pick and Place (PnP) cover. The socket is delivered as a single integral assembly. Below are descriptions of the integral parts of the socket.

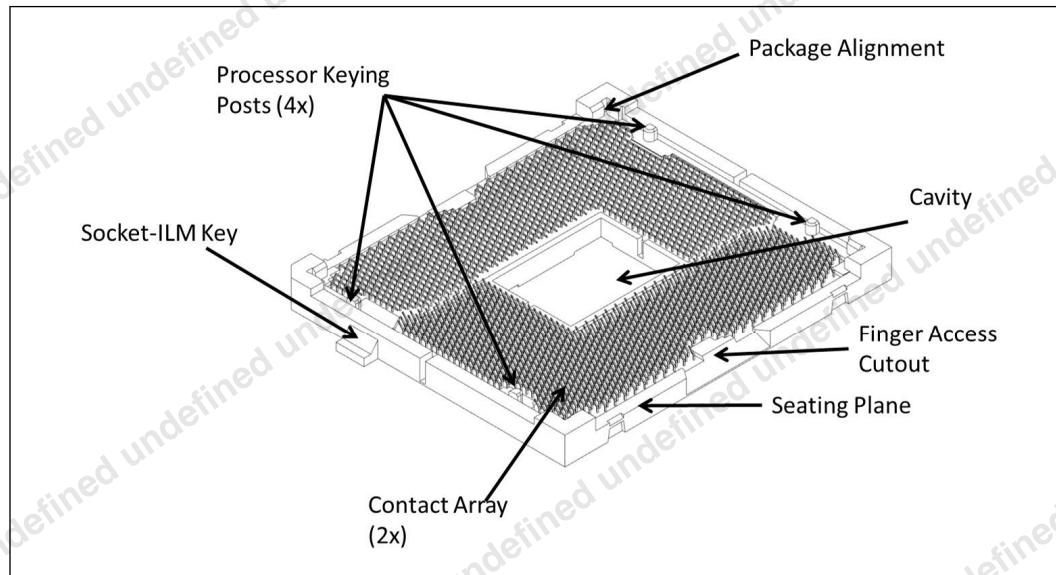
### Socket Body Housing

The housing material is thermoplastic or equivalent with UL 94 V-0 flame rating capable of withstanding 260°C for 40 seconds (typical reflow/rework). The socket coefficient of thermal expansion (in the XY plane), and creep properties, are such that the integrity of the socket is maintained for the environmental conditions listed in the TMSDG.

The color of the housing will be dark as compared to the solder balls to provide the contrast needed for pick and place vision systems. A labeled representation of the socket can be seen in the figure below.

Figure 2.

### Socket with Labeled Features



### Solder Balls

A total of 2011 solder balls corresponding to the contacts are on the bottom of the socket for surface mounting with the motherboard.

The socket has the following solder ball material:

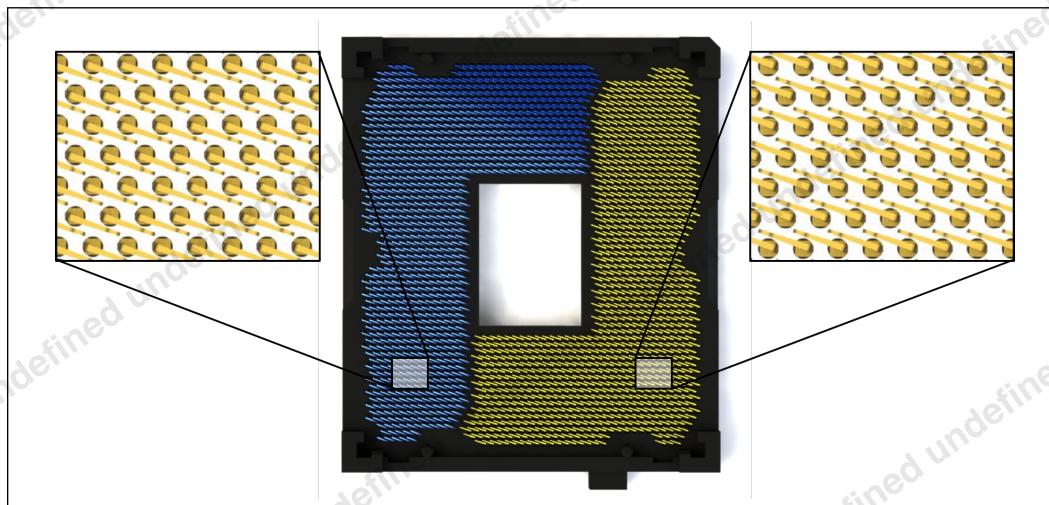
- Lead free SAC305 (SnAgCu) solder alloy with a silver (Ag) content 3%, copper (Cu) 0.5%, tin (Sn) 96.5% and a melting temperature of approximately 217°C. The immersion silver (ImAg) motherboard surface finish and solder paste alloy must be compatible with the SAC305 alloy solder paste.

### Contacts

The base material for the contacts is high strength copper alloy. For the area on socket contacts where processor lands will mate, there is a 0.381 mm [0.015 inches] minimum gold plating over 1.27 mm [0.05 inches] minimum nickel underplate. No contamination by solder in the contact area is allowed during solder reflow. All socket contacts are designed such that the contact tip lands within the substrate pad boundary before any actuation load is applied and remain within the pad boundary at final installation, after actuation load is applied.

The contacts are laid out in two L-shaped arrays as shown in the figure below. The detailed view of the contacts indicate the wiping orientation of the contacts in the two regions to be 29.6°.

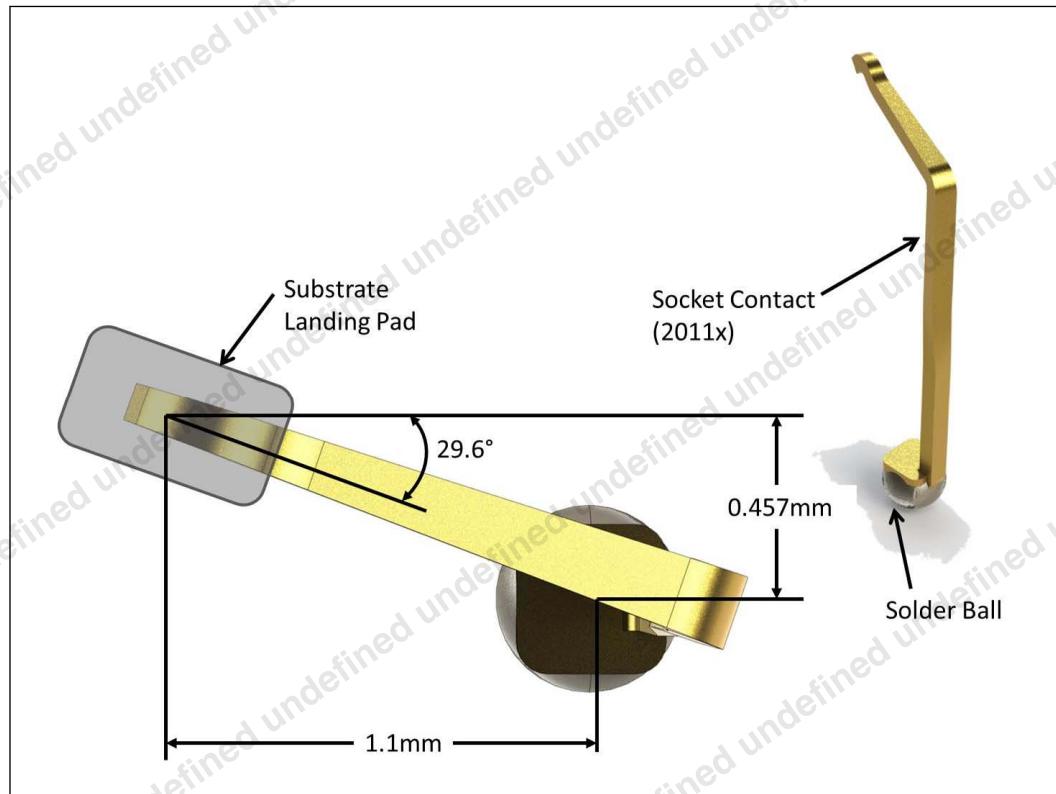
**Figure 3.** Contact Wiping Direction



The contact between substrate land and socket contact are offset. The following diagram shows contact offset from solder ball location and orientation of contact tip.



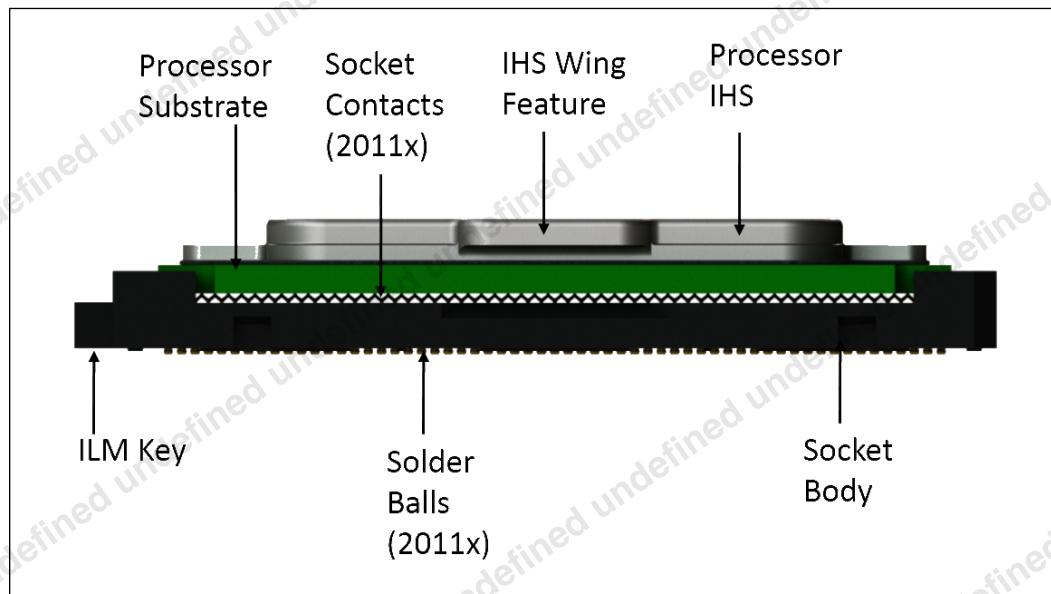
**Figure 4. Contact Tip Offset with Respect to Solder Ball**



#### Socket Standoffs

Standoffs on the bottom of the socket base establish the minimum socket height after solder reflow. The following diagram highlights each feature of the socket-processor stack up.

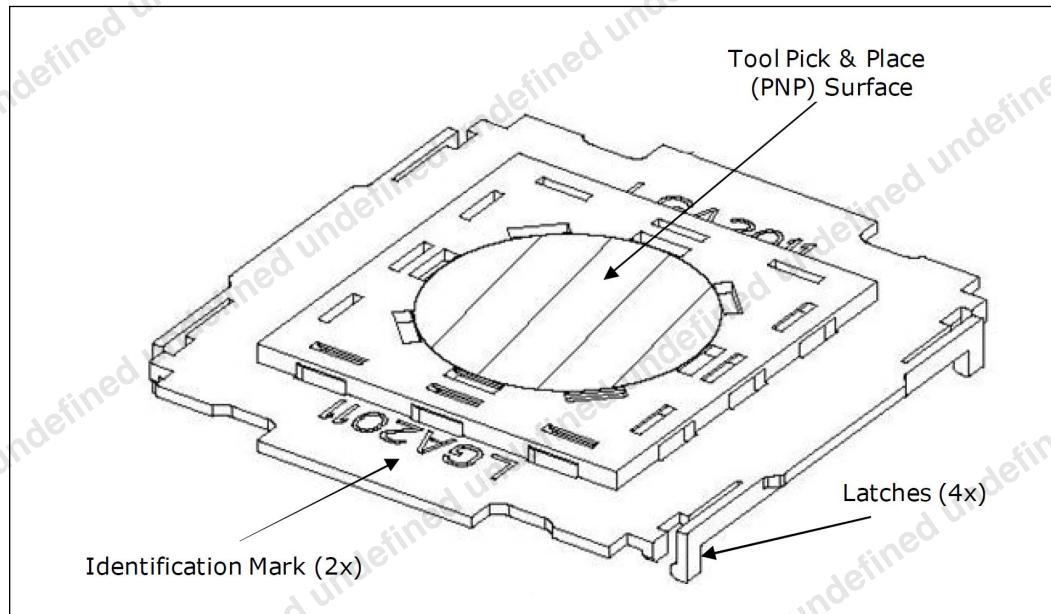
**Figure 5. Processor Socket Stack Up**



#### Pick and Place Cover

The cover provides a planar surface for vacuum pick up used to place components in the Surface Mount Technology (SMT) manufacturing line. The proceeding diagram labels key features of the Pick and Place cover.

**Figure 6. Pick and Place Cover with Labeled Features**

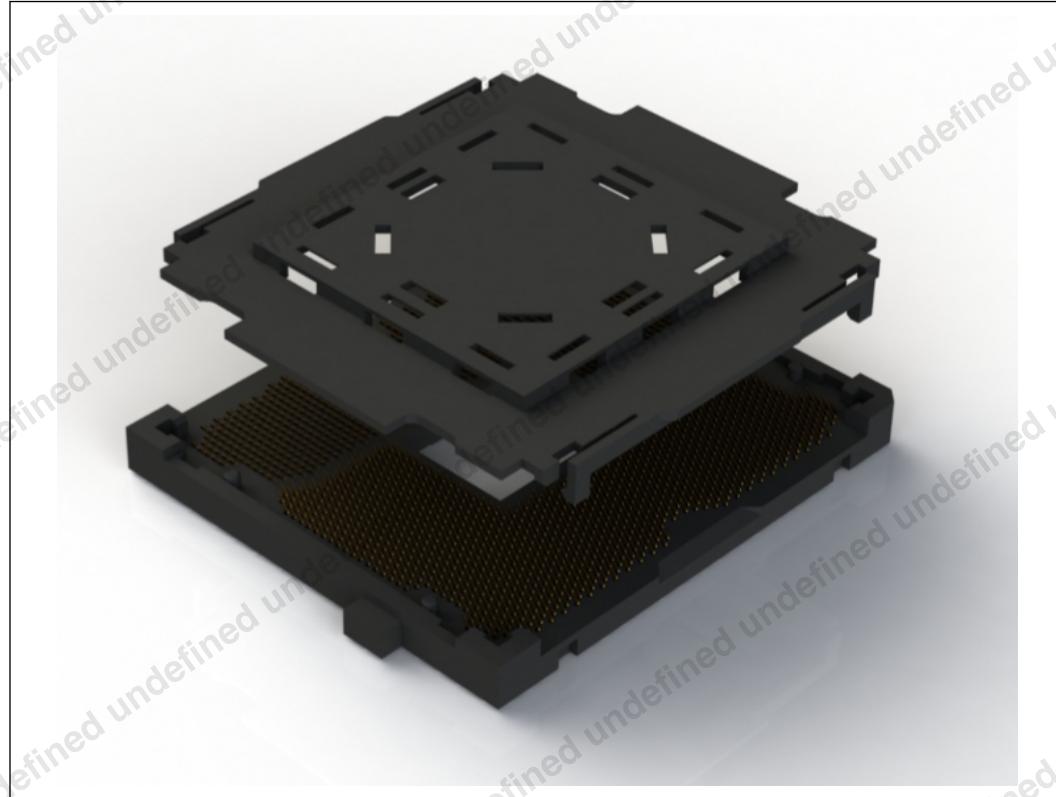


The cover remains on the socket during reflow to help prevent contamination during reflow. The cover can withstand 260°C for 40 seconds (typical reflow/rework profile) and the environmental conditions listed in the TMSDG.



The following figure diagrams the PnP and socket assembly. To reduce risk of damage to socket contacts the pick and place (PnP) cover remains on the socket during ILM installation.

**Figure 7. PnP Cover and Socket Assembly**



Once the ILM with its cover is installed Intel is recommending the PnP cover be removed to help prevent damage to the socket contacts. To reduce the risk of bent contacts the PnP Cover and ILM Cover were designed to not be compatible. Covers can be removed without tools.

The pick and place covers are designed to be interchangeable between socket suppliers.

## 2.2

### Socket Land Pattern Guidance

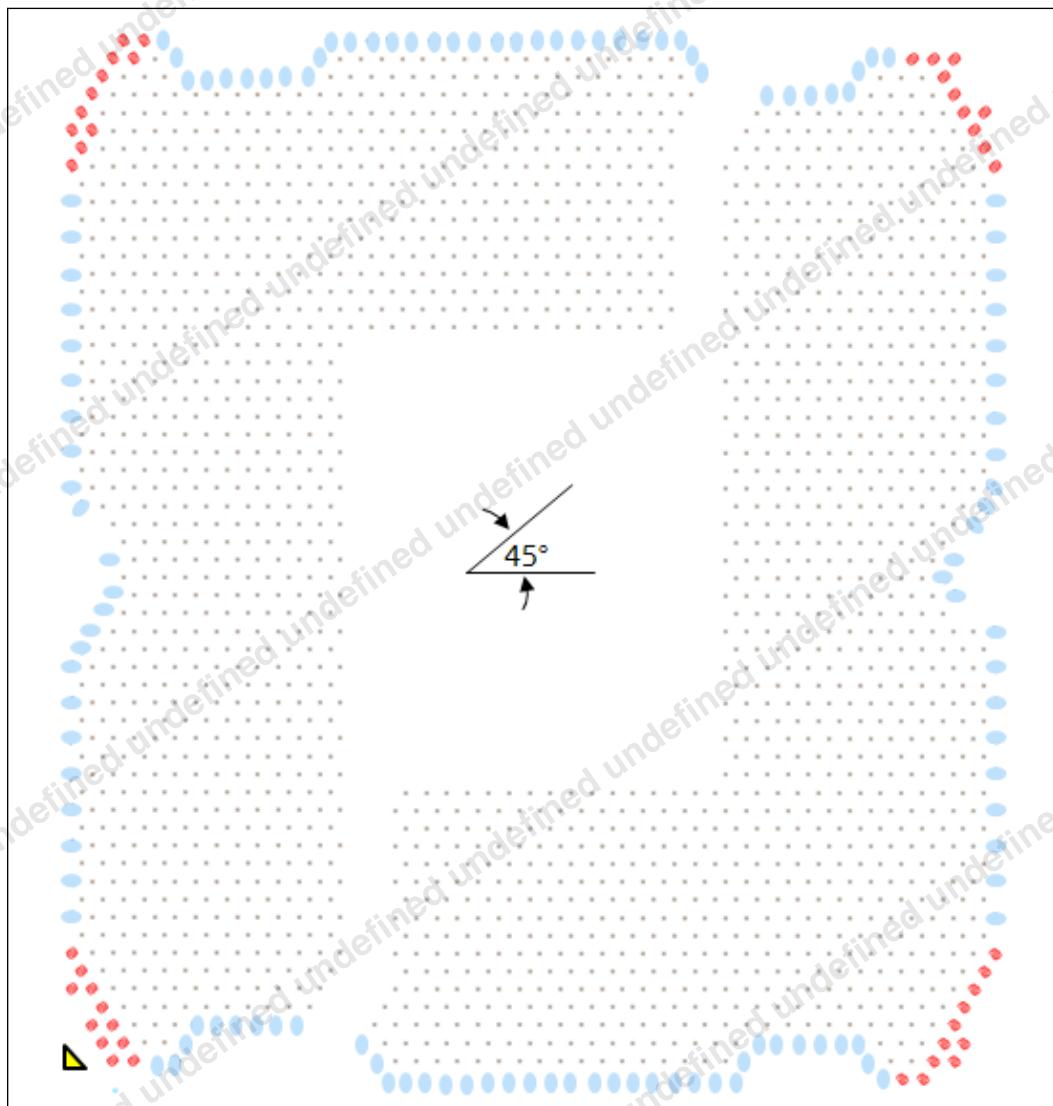
The land pattern guidance provided in this section applies to printed circuit board design. Recommendation for Printed Circuit Board (PCB) Land Patterns is to ensure solder joint reliability during dynamic stresses, often encountered during shipping and handling and hence to increase socket reliability.

#### LGA 2011-3 Land Pattern

The land pattern for the LGA2011-3 socket is 40 mils hexagonal array see the following figure for detailed location and land pattern type.

**Note:** There is no round-off (conversion) error between socket pitch (1.016 mm) and board pitch (40 mil) as these values are equivalent.

**Figure 8.** **Socket 2011-3 Land Pattern**



**Table 3.** PIN Count By Pad Definition

Pad Definition / Padstack	Color	Quantity
20 X 17 Oblong Partially SMD / O17X20	<b>RED Pins</b>	43
20 X 17 Oblong Partially SMD / O17X20	<b>LIGHT BLUE Pins</b>	123
17 mil Ø MD / C17	<b>GREY Pins</b>	1845

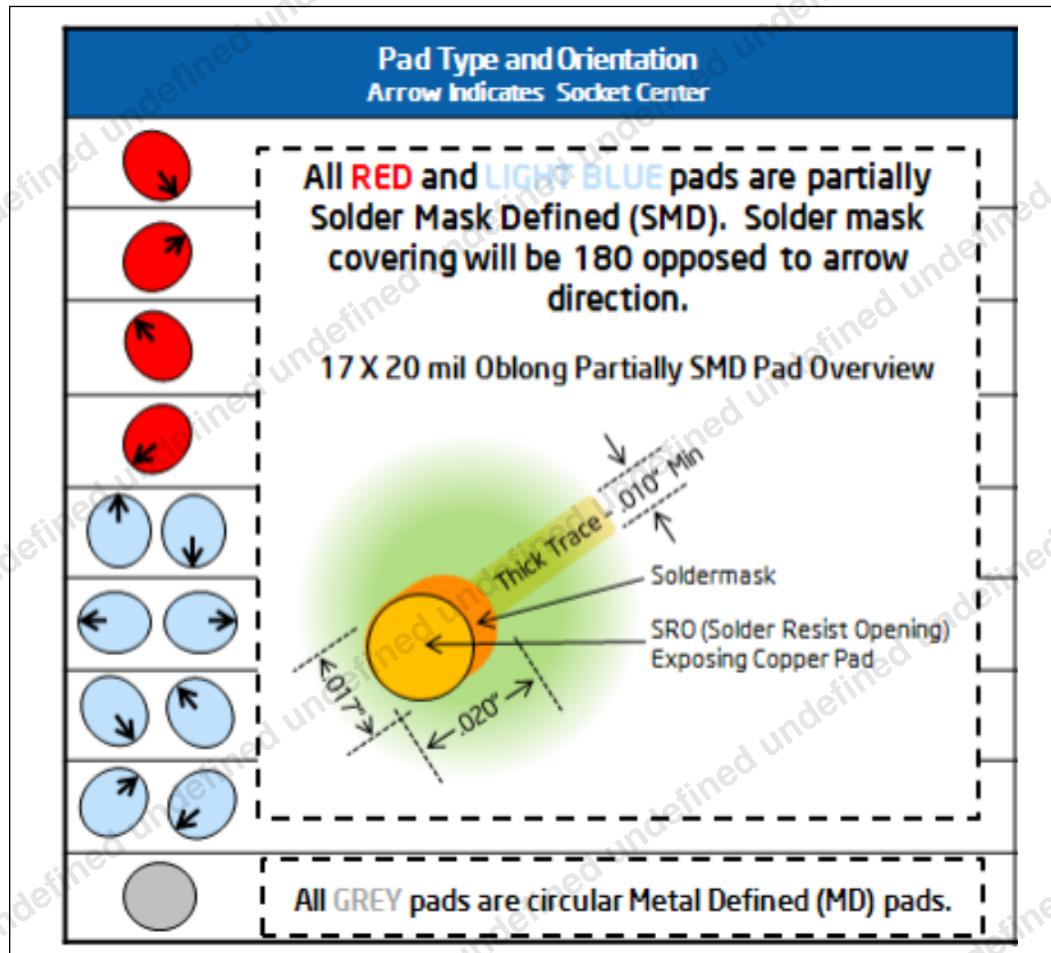
Notes: 1. **RED Pins:** Corner nCTF pads (43 total) are all designed as 20 X 17 mil oblong partially soldermask defined pads with an SRO of  $17 \pm 1$  mil Ø (shown below). The long axis of the pad is oriented at 45° from the center of the socket. All nCTF pads require thick traces ideally oriented at 45° toward the package corner.  
 2. **LIGHT BLUE Pins:** Edge CTF pads (total) are all designed as 20 X 17 mil oblong partially soldermask defined pads with an SRO of  $17 \pm 1$  mil Ø (shown below). The long axis of the pad is oriented at 90° to the socket edge.  
 3. **GREY Pins:** Critical to function pins are all designed as 17 mil circular MD (Metal Defined) pads.

### Pad Type Recommendations

Intel defines two types of pad types based on how they are constructed. A metal defined (MD) pad is one where a pad is individually etched into the PCB with a minimum width trace exiting it. The solder mask defined (SMD) pad is typically a pad in a flood plane where the solder mask opening defines the pad size for soldering to the component. In thermal cycling a MD pad is more robust than a SMD pad type. The solder mask that defines the SMD pad can create a sharp edge on the solder joint as the solder ball / paste conforms to the window created by the solder mask. For certain failure modes the MD pad may not be as robust in shock and vibration (S&V). During S&V, the predominant failure mode for a MD pad in the corner of the BGA layout is pad craters and solder joint cracks. A corner MD pad can be made more robust and behave like a SMD pad by having a wide trace enter the pad. This trace should be 10 mil minimum wide but not to exceed the pad diameter and exit the pad at a 45 degree angle (parallel to the diagonal of the socket). During board flexure that results from shock & vibration, a SMD pad is less susceptible to a crack initiating due to the larger surface area. Intel has defined selected solder joints of the socket as non-critical to function (NCTF) when evaluating package solder joints post environmental testing. The signals at NCTF locations are typically redundant ground or non-critical reserved, so the loss of the solder joint continuity at end of life conditions will not affect the overall product functionality.

The following figure diagrams shape and location of solder pad types for socket 2011-3.

**Figure 9.** **Socket 2011-3 Pad Types and Locations**



**Notes:**

- When ordering PCBs with the Socket R (LGA2011) footprint, it is important to specify the following verbiage on the FAB drawing as well as within the purchase requisition: *All BGA pads, Soldermask or Metal defined, min/max size tolerance, should comply with Intel PCB specification, current revision. Nominal BGA pad size, Soldermask or Metal defined, is Ø +/− 1 mil. This pad size is critical to function on socket locations.*
- The solder paste stencil aperture recommendation for Socket R (LGA2011) is: 24 mil Ø circular aperture opening with a stencil thickness of 5 mils.

## 2.3

### Socket Loading Requirements

The socket must meet the mechanical loading and strain requirements outlined in the table below. All dynamic requirements are under room temperature conditions while all static requirements are under product use condition temperature. Specifically, ILM and HS load range may vary for different LGA 2011 derivatives (e.g. 2011-0, 2011-1) due to the package form factor, and the design of loading mechanism and thermal solution (e.g., HS mass).



### 2.3.1      **Socket Loading Specifications**

The table below provides load specifications for the socket. These mechanical limits should not be exceeded during component assembly, mechanical stress testing, or standard drop and shipping conditions. All dynamic requirements are under room temperature conditions while all static requirements are under 100 °C conditions.

**Table 4.      **Socket Load Values****

<b>Parameter</b>	<b>Load Limits, SI Units</b>		<b>Load Limits, Imperial Units</b>		<b>Definition</b>
	<b>Min</b>	<b>Max</b>	<b>Min</b>	<b>Max</b>	
Static Compressive per Contact	15 (gf)	38 (gf)	0.53 (ozf)	1.34 (ozf)	The compressive load applied by the package on the LGA contacts to meet electrical performance. This condition must be satisfied throughout the life of the product
Static Compressive (ILM)	445 (N)	712 (N)	100 (lbf)	160 (lbf)	The total load applied by the enabling mechanism onto the socket as transferred through the package, contacts and socket seating plane.
Static Compressive Beginning of Life (HS)	222 (N)	400 (N)	50 (lbf)	90 (lbf)	The total load applied by the heatsink mechanism onto the socket as transferred through the package, contacts and socket seating plane. Measured at Beginning of Life
Static Compressive End of Life (HS)	178 (N)	400 (N)	40 (lbf)	90 (lbf)	The total load applied by the heatsink mechanism onto the socket as transferred through the package, contacts and socket seating plane. Measured at End of Life
Static Total Compressive	667 (N)	1068 (N)	150 (lbf)	240 (lbf)	The total load applied by enabling mechanism and heat sink onto the socket as transferred through the package, contacts and socket seating plane.
Dynamic Compressive	NA	588 (N)	NA	132 (lbf)	Quasi-static equivalent compressive load applied during the mechanical shock from heatsink, calculated using a reference 600g heatsink with a 25G shock input and an amplification factor of 3 ( $600\text{g} \times 25\text{G} \times 3 = 441\text{N} = 99\text{lbf}$ ). This specification can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this value. Intel reference system shock requirement for this product family is 25G input as measured at the chassis mounting location.
Board Transient Bend Strain	NA	500 (ue) for 62 (mil); 400 (ue) for 100 (mil)	NA	500 (ue) for 62 (mil); 400 (ue) for 100 (mil)	This is the strain on boards near to socket BGA corners during transient loading events through manufacturing flow or testing. The test guidance can be found in Board Flexure Initiative (BFI) strain guidance from your local CQE.

### 2.4      **Socket Maximum temperature**

The power dissipated within the socket is a function of the current at the pin level and the effective pin resistance. To ensure socket long term reliability, Intel defines socket maximum temperature using a via on the underside of the motherboard. Exceeding the temperature guidance may result in socket body deformation, or increases in thermal and electrical resistance which can cause a thermal runaway and eventual electrical failure. The guidance for socket maximum temperature is listed below:

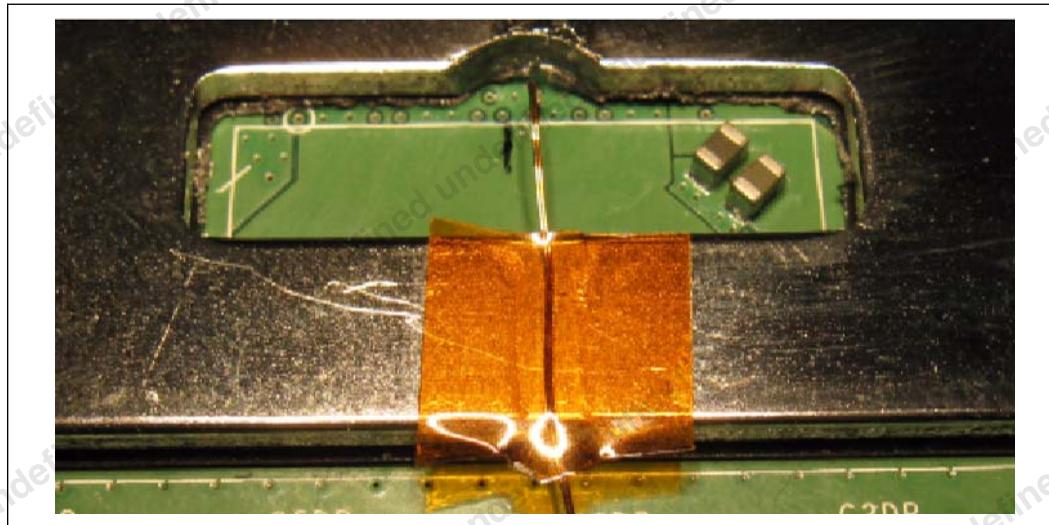
- Via temperature under socket <78 °C

- The specific via used for temperature measurement is located on the bottom of the motherboard between pins BC1 and BE1.
- The socket maximum temperature is defined at Thermal Design Current (TDC). In addition, the heatsink performance targets and boundary conditions must be met to limit power dissipation through the socket.

To measure via temperature:

1. Drill a hole through the back plate corresponding to the location of pins BC1 and BE1.
2. Thread a T-type thermocouple (36 - 40 gauge) through the hole and glue it into the specific measurement via on the underside of the motherboard.
3. Once the glue dries, reinstall the back plate and measure the temperature

**Figure 10. Socket Temperature Measurement**



## 2.5

### Strain Guidance for Socket

Intel provides manufacturing strain guidance commonly referred to as Board Flexure Initiative or BFI Strain Guidance. The BFI strain guidance apply only to transient bend conditions seen in board manufacturing assembly environment with no ILM, for example during In Circuit Test. BFI strain guidance limits do not apply once ILM is installed. It should be noted that any strain metrology is sensitive to boundary conditions. Intel recommends the use of BFI to prevent solder joint defects from occurring in the test process. For additional guidance on BFI, see Manufacturing With Intel® Components - Strain Measurement for Circuit Board Assembly, also referred as BFI MAS ( Manufacturing Advantage Services) and BFI STRAIN GUIDANCE SHEET (LGA2011-3 socket). Consult your Intel Customer Quality Engineer for additional guidance in setting up a BFI program in your factory.

#### Note:

When the ILM is attached to the board, the boundary conditions change and the BFI strain limits are not applicable. The ILM, by design, increases stiffness in and around the socket and places the solder joints in compression. Intel does not support strain metrology with the ILM assembled.

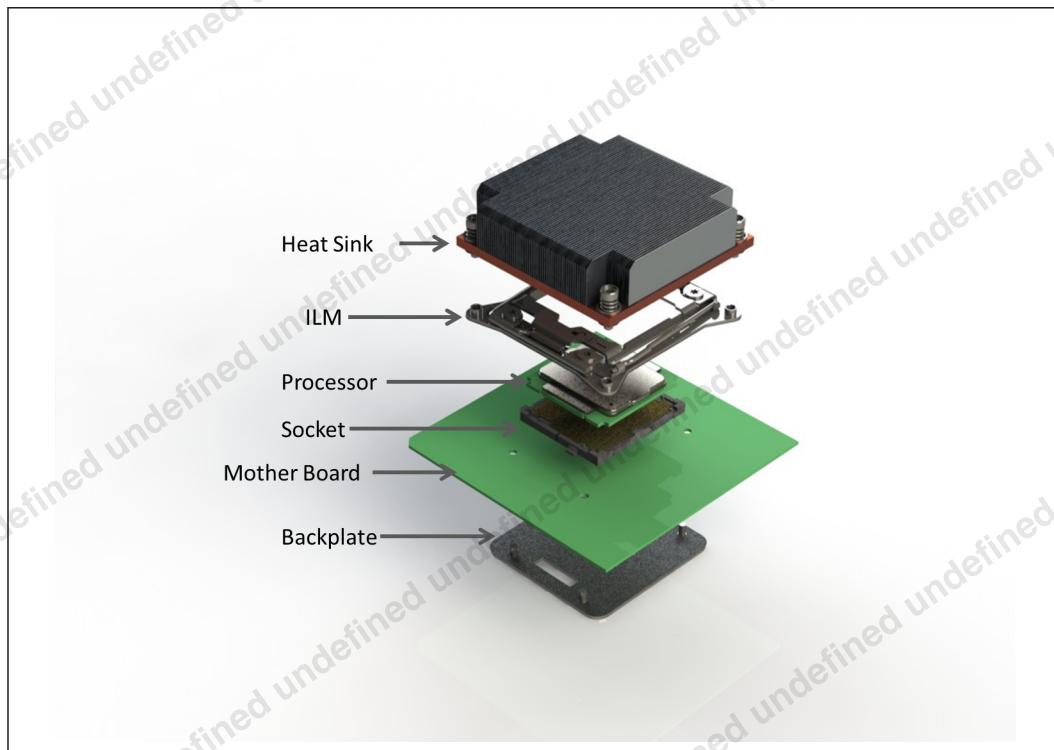


### 3.0

## Independent Loading Mechanism (ILM) Specifications

The Independent Loading Mechanism (ILM) provides the force needed to seat the land LGA package onto the socket contacts. See image below for total processor stack consisting of all relevant mechanical components.

**Figure 11. Processor Stack**



The ILM is physically separate from the socket body. The assembly of the ILM is expected to occur after attaching the socket to the board. The exact assembly location is dependent on manufacturing preference and test flow.

The mechanical design of the ILM is a key contributor to the overall functionality of the socket. Intel performs detailed studies on integration of processor package, socket and ILM as a system. These studies directly impact the design of the ILM. The Intel reference ILM will be "built to print" from Intel controlled drawings. Intel recommends using the Intel Reference ILM. Custom non-Intel ILM designs do not benefit from Intel's detailed studies and may not incorporate critical design parameters.



The ILM has two critical functions: evenly deliver and distribute the force to seat the processor onto the socket contacts and ultimately through the socket solder joints. Another purpose of ILM is to ensure electrical integrity/performance of the socket and package.

Socket LGA2011-3 has two POR (Plan of Record) ILMs:

1. Square ILM - This ILM has 80x80mm heatsink mounting hole pattern.
2. Narrow ILM - This ILM has 56x94mm heatsink mounting hole pattern.

### 3.1

## ILM Load Specifications

The Independent Loading Mechanism (ILM) provides the force needed to seat the package onto the socket contacts.

### Maximum Allowable Loads

The table below provides load specifications for the processor package. These maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure or other damage to the system. The processor substrate should not be used as a mechanical reference or load bearing surface for thermal solutions.

**Table 5.**

### LGA 2011-3 Maximum Allowable Loads

Item	Maximum
Static Pre-Load Compressive (ILM load)	712N (160 lbf)
Static Pre-Load Compressive (HS load)	400N (90 lbf)
Total Socket Static Compressive (ILM+HS=Socket)	1068N (240 lbf)

### Minimum Allowable Loads

The ILM is designed to achieve the minimum Socket Static Pre-Load Compressive load specification. The thermal solution (heatsink) should apply additional load. The combination of an ILM and HS will be used to achieve the load targets shown in the table below.

**Table 6.**

### LGA 2011-3 Minimum Allowable Loads

Item	Minimum
Static Pre-Load Compressive (ILM load)	445N (100 lbf)
Static Pre-Load Compressive (HS load)	222N (50 lbf)
Total Socket Static Compressive (ILM+HS=Socket)	667N (150 lbf)

### End of Life Load Targets

The ILM is designed to achieve the minimum end of life loads for the socket. The thermal solution (heatsink) should apply a portion of the end of life load. The combination of an ILM and HS will be used to achieve the load targets shown in the table below.



**Table 7. LGA 2011-3 Minimum End of Life Loads**

Item	End of Life Minimum
Static Pre-Load Compressive (ILM load)	311N (70 lbf)
Static Pre-Load Compressive (HS load)	178N (40 lbf)
Total Socket Static Compressive (ILM+HS=Socket)	490N (110 lbf)

### 3.2

### ILM Keepout Zones (KOZ)

The table below lists envelope dimensions for ILM KOZ , both topside and backplate. For detailed views, refer to dimensioned drawings in [Mechanical Drawings](#) on page 78.

**Table 8. LGA 2011-3 ILM General Keepout Dimensions**

Keepout Type	Square ILM	Narrow ILM
Topside envelope	93x93 mm (3.6x3.7in)	80x107.5 mm (3.15x4.2in)
ILM Hole Location		46x69.2 mm (1.8x2.7 in)
Backplate Envelope		78x84 mm (3.1x3.3 in)

### 3.3

### Independent Loading Mechanism (ILM)

The Independent Loading Mechanism (ILM) provides the force needed to seat the package onto the socket contacts. The ILM is a mechanical assembly that is physically separate from the socket body. The assembly of the ILM to the motherboard is expected to occur after attaching the socket to the board. The exact assembly location is dependent on manufacturing preference and test flow.

The mechanical design of the ILM is a key contributor to the overall functionality of the socket. Intel performs detailed studies on integration of processor package, socket and ILM as a system. These studies directly impact the design of the ILM. The Intel reference ILM will be "built to print" from Intel controlled drawings. Intel recommends using the Intel Reference ILM. Custom non-Intel ILM designs do not benefit from Intel's detailed studies and may not incorporate critical design parameters.

The ILM has two critical functions: deliver the force to seat the processor onto the socket contacts resulting in even load transfer through the socket solder joints. Another purpose of ILM is to ensure electrical integrity/performance of the socket and package.

### 3.4

### ILM Mechanical Design Considerations and Recommendations

An retention/loading mechanism must be designed to support the processor heatsink and to ensure processor interface with the socket contact is maintained since there are no features on the socket for direct attachment of the heatsink or retaining the processor. In addition to supporting the processor heatsink over the processor, this mechanism plays a significant role in the robustness of the system in which it is implemented, in particular:



- Ensuring that thermal performance of the TIM applied between the IHS and the heatsink is achievable. TIMs, especially those based on phase change materials, are very sensitive to applied pressure: the higher the pressure, the better the initial performance. TIMs such as thermal greases are not as sensitive to applied pressure. Designs should consider the impact of shock and vibration events on TIM performance as well as possible decrease in applied pressure over time due to potential structural relaxation in enabled components.
- Ensuring that system electrical, thermal, and structural integrity is maintained under shock and vibration events. The mechanical requirements of the attach mechanism depend on the weight of the heatsink, as well as the level of shock and vibration that the system must support. The overall structural design of the baseboard and system must be considered when designing the heatsink and ILM attach mechanism. Their design should provide a means for protecting the socket solder joints as well as preventing package pullout from the socket.
- The load applied by the attachment mechanism and the heatsink must comply with the package specifications, along with the dynamic load added by the mechanical shock and vibration requirements of the package and socket.
- Load induced onto the package and socket by the ILM may be influenced with heatsink installed. Determining the performance for any thermal/mechanical solution is the responsibility of the customer.

A potential mechanical solution for heavy heatsink is the use of a supporting mechanism such as a backer plate or the utilization of a direct attachment of the heatsink to the chassis pan. In these cases, the strength of the supporting component can be utilized rather than solely relying on the baseboard strength. In addition to the general guidelines given above, contact with the baseboard surfaces should be minimized during installation in order to avoid any damage to the baseboard.

Placement of board-to-chassis mounting holes also impacts board deflection and resultant socket solder ball stress. Customers need to assess the shock for their designs as heatsink retention (back plate), heatsink mass and chassis mounting holes may vary.

### 3.5 ILM Features

The ILM is defined by four basic features

- ILM Loadplate: Formed sheet metal that when closed applies four point loads onto the IHS seating the processor into the socket
- ILM Frame: Single piece or assembly that mounts to PCB board and provides the hinge locations for the levers the ILM frame also contains captive mounts for heatsink attach. An insulator is pre applied by the vendor to the bottom side of the ILM frame.
- ILM Actuation levers: Formed loading levers designed to place equal force on both ends of the ILM load plate. Some of the load is passed through the socket body to the board inducing a slight compression on the solder joints
- ILM Backplate: A flat steel back plate with threaded studs to attach to the ILM frame. A clearance hole is located at the center of the plate to allow access to test points and backside capacitors. Two additional cut-outs on the backplate provide clearance for backside voltage regulator components. An insulator is pre applied by the vendor to the side with the threaded studs.

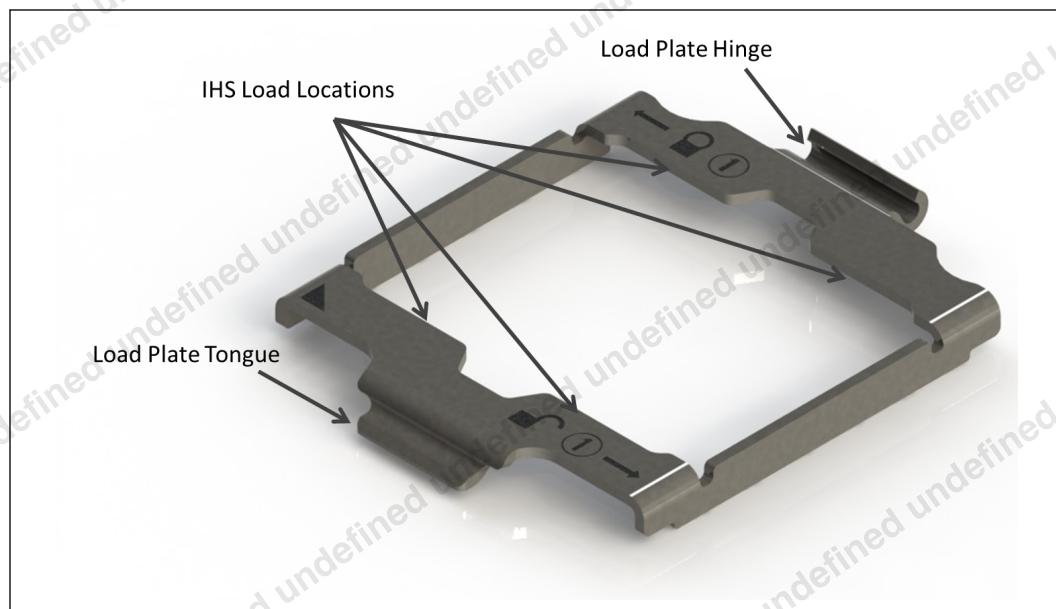


Heatsink mounting studs on ILM frame allow for topside thermal solution attach to a rigid structure. This eliminates the motherboard thickness dependency from the heatsink mechanical stackup. ILM assembly provides a clamping force between the ILM frame, backplate and board, resulting in reduced board bending leading to higher solder joint reliability. ILM lever design provides an interlocking mechanism to ensure proper opening or closing sequence for the operator. This has been implemented in both square and narrow ILM.

### ILM Load Plate Design

Four point loading contributes to minimizing package and socket warpage under non uniformly distributed load. The reaction force from closing the load plate is transmitted to the frame and through the captive fasteners to the back plate. Some of the load is passed through the socket body to the board inducing a slight compression on the solder joints. The load plate design is common between the two POR ILMS and is shown in the figure below.

**Figure 12. ILM Load Plate**



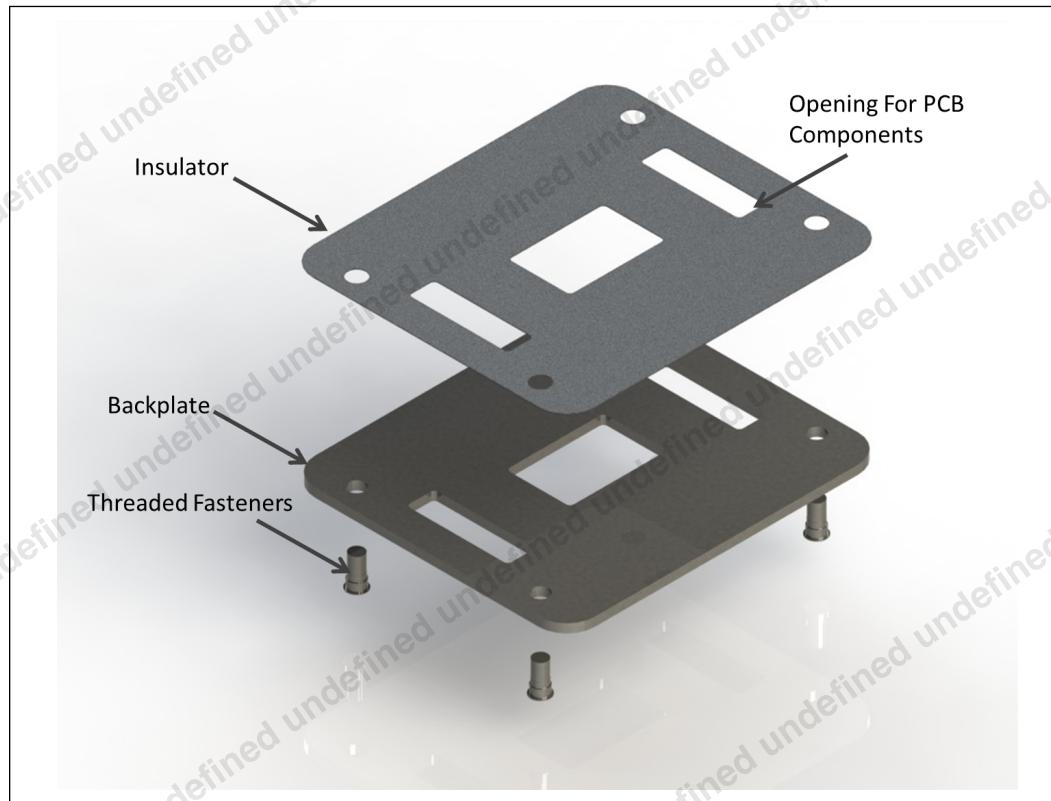
### Lever Actuation/Release Forces

Maximum allowable force to actuate the levers not to exceed 4.7 lbf (21 N) at the point of typical finger placement.

### ILM Back Plate Design

The backplate assembly consists of a supporting plate and captive standoffs. It provides rigidity to the system to ensure minimal board and socket deflection. Four externally threaded (male) inserts which are press fit into the back plate are for ILM attachment. Three cavities are located at the center of the plate to allow access to the baseboard test points and backside capacitors. An insulator is pre-applied to prevent shorting the board.

**Figure 13. ILM Backplate**



## 3.6 Intel® ILM Reference Designs

Intel has designed and validated two ILMs compatible with Socket LGA2011-3 :

1. Square ILM - 80x80 mm heat sink mounting hole pattern.
2. Narrow ILM - 56x94 mm heat sink mounting hole pattern.

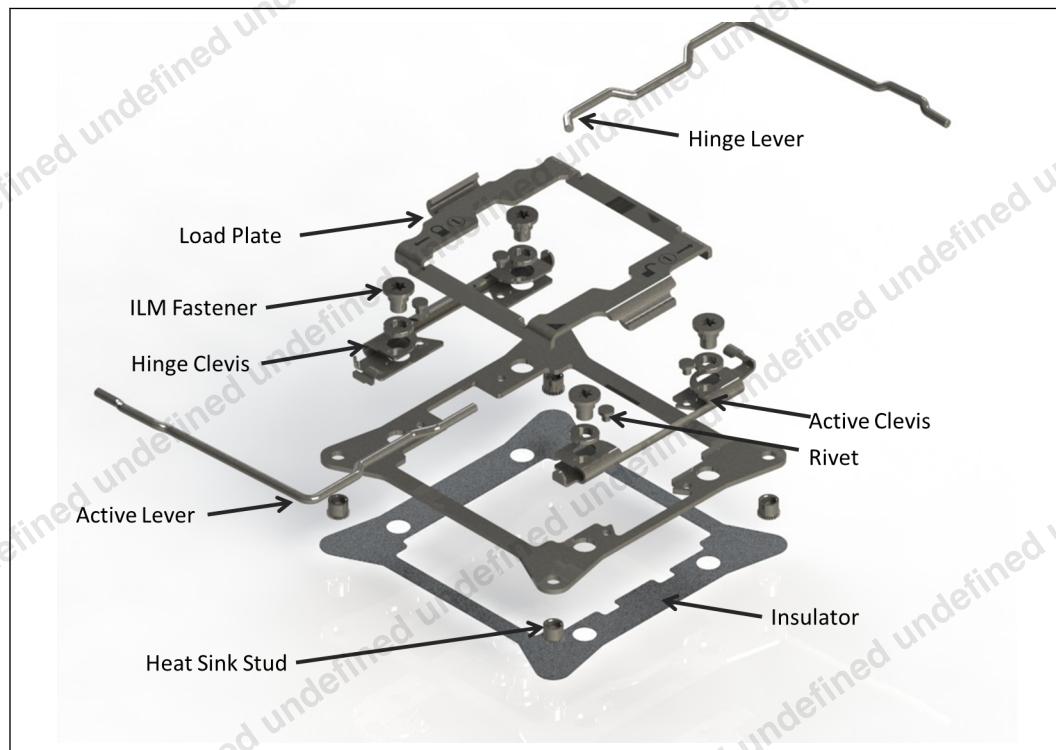
The two POR ILMs share most components, only the top plate and active lever differ between the two assemblies.

### 3.6.1 Square ILM

The square ILM consists of two sub assemblies that will be procured as a set from the enabled vendors. These two components are the ILM assembly and back plate. The square ILM assembly consists of several pieces as shown and labeled in the following diagram. The hinge lever, active lever, load plate, top plate, clevises, and the captive fasteners. For clarity the ILM cover is not shown in this view.



**Figure 14. Exploded Square ILM**



An assembled view is shown in the following figure.

**Figure 15.** Assembled Square ILM**Table 9.****Square ILM Component Thickness and materials**

Component	Thickness	Material
ILM Frame	1.20 mm	310 Stainless Steel
ILM Load Plate	1.50 mm	310 Stainless Steel
ILM Back Plate	2.20 mm	S50C low Carbon Steel

The square ILM supports the legacy 80x80 mm heat sink mounting patterns used in some form factors.

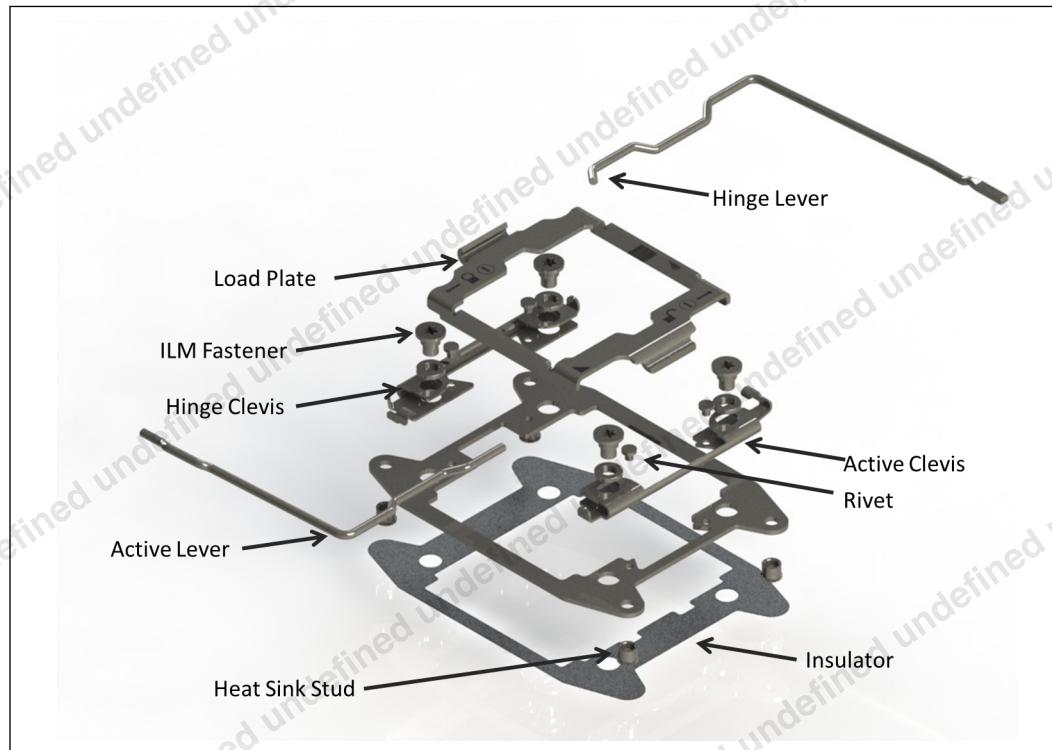
### 3.6.2

### Narrow ILM

The narrow ILM consists of two sub assemblies that will be procured as a set from the enabled vendors. These two components are the ILM assembly and back plate. The ILM assembly is shown in the following figure.



Figure 16. Exploded Narrow ILM



The narrow ILM assembly consists of several pieces as shown and labeled above. The hinge lever, active lever, load plate, top plate, clevises, ILM cover, and the captive fasteners. For clarity the ILM cover is not shown in this view. An assembled view is shown in the following figure. The Narrow ILM maintains the structure and function of the square ILM but utilizes separate clevises riveted onto the ILM frame.

**Figure 17.** Assembled Narrow ILM**Table 10.** Narrow ILM Component Thickness and materials

Component	Thickness	Material
ILM Frame	1.50 mm	310 Stainless Steel
ILM Clevis	0.80 mm	301 Stainless Steel
ILM Load Plate	1.50 mm	310 Stainless Steel
ILM Back Plate	2.20 mm	S50C low Carbon Steel

The narrow ILM supports a smaller east west dimension constraint conducive for use in space constrained form factors.

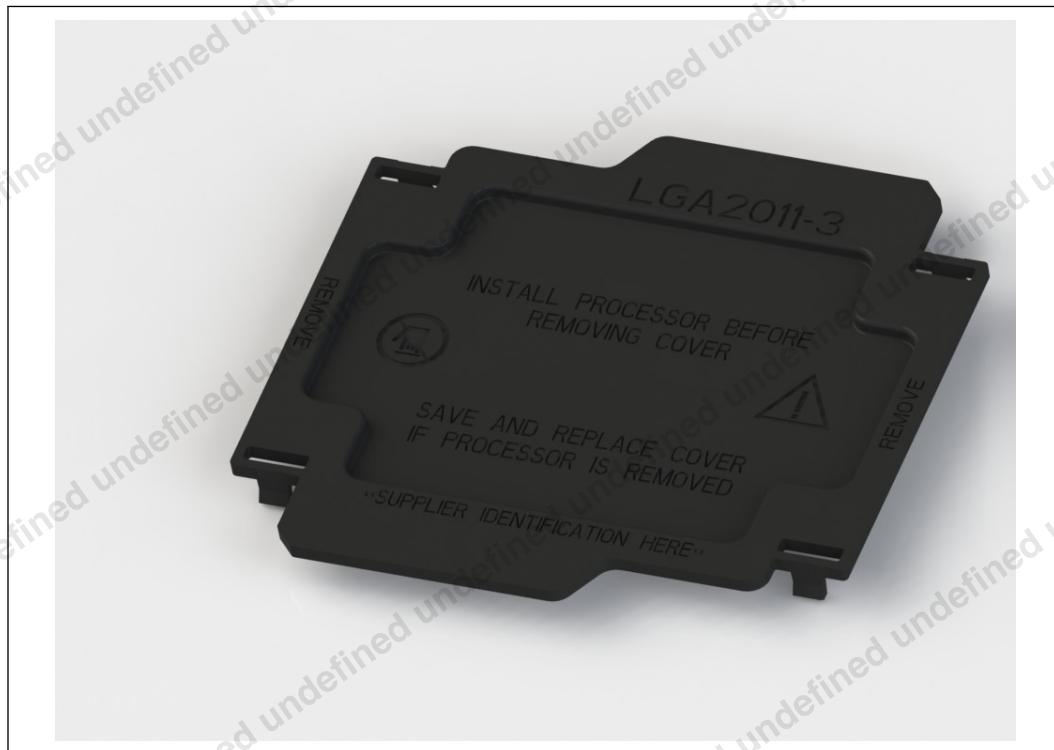
### 3.7 ILM Cover

Intel has developed a cover that will snap on to the ILM for the LGA2011 socket family.

The ILM cover is intended to reduce the potential for socket contact damage from the operator / customer fingers being close to the socket contacts to remove or install the pick and place cover. By design the ILM cover and pick and place covers can not be installed simultaneously. This cover is intended to be used in place of the pick and place cover once the ILM is assembled to the board. The ILM will be offered with the ILM cover pre assembled as well as a discrete part.



**Figure 18. ILM cover**



- Pre-assembled by the ILM vendors to the ILM load plate. It will also be offered as a discrete component.
- The ILM cover will pop off if a processor is installed in the socket.
- Maintain inter-changeability between validated ILM vendors for LGA2011-3 socket.
- The ILM cover for the LGA2011-3 socket will have a flammability rating of V-0 per UL 60950-1.

**Note:**

Intel recommends removing the Pick and Place cover (PnP) of the socket body in manufacturing as soon as possible at the time when ILM is being installed.

#### **ILM Cover Attach/Removal Force**

The required force to remove the ILM cover shall not exceed 7.6 N when the load is applied by finger at the center of cover.

### **3.8**

#### **ILM Allowable Board Thickness**

The ILM components described in this document will support board thickness in the range of 1.5748 - 2.54 mm (0.062" - 0.100"). Boards (PCBs) not within this range may require modifications to the back plate or other ILM components retention. Contact the component suppliers ([Component Suppliers](#) on page 76) for modifications.



## 4.0 Processor Thermal Specifications and Features

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### 4.1 **T<sub>case</sub> and DTS-Based Thermal Specification Implementation**

Thermal solutions should be sized such that the processor complies to the T<sub>CASE</sub> thermal profile all the way up to TDP, because, when all cores are active, a thermal solution sized as such will have the capacity to meet the DTS thermal profile, by design. When all cores are not active or when Intel Turbo Boost Technology is active, attempting to comply with the DTS thermal profile may drive system fans to speeds higher than the fan speed required to comply with the T<sub>CASE</sub> thermal profile at TDP.

In cases where thermal solutions are undersized, and the processor does not comply with the T<sub>CASE</sub> thermal profile at TDP, compliance can occur when the processor power is kept lower than TDP, **AND** the actual T<sub>CASE</sub> is below the T<sub>CASE</sub> thermal profile at that lower power.

In most situations, implementation of DTS thermal profile can reduce average fan power and improve acoustics, as compared to T<sub>CONTROL</sub>-based fan speed control. When DTS < T<sub>CONTROL</sub>, the processor is compliant, and T<sub>CASE</sub> and DTS thermal profiles can be ignored.

#### 4.1.1 Margin to Thermal Specification (M)

To simplify processor thermal specification compliance, the processor calculates and reports margin to DTS thermal profile (M) using the following method.

Processor reads firmware programmable values:

1. TCC\_OFFSET: In-band: TEMPERATURE\_TARGET[27:24]. BIOS must write in a value before CPL3.

Processor gathers information about itself:

1. Processor stores the intercept and slope terms (T<sub>LA</sub> and Ψ<sub>PA</sub>) from the DTS Thermal Profile for that particular SKU (one-time read only)
2. Processor reads its own energy consumption and calculates power, P
3. Processor reads its own temperature, DTS

Finally, processor calculates the margin value (M) to the specification (solid black line in the graph below). The PECI command for reading margin (M) is RdPkgConfig(), Index 10.

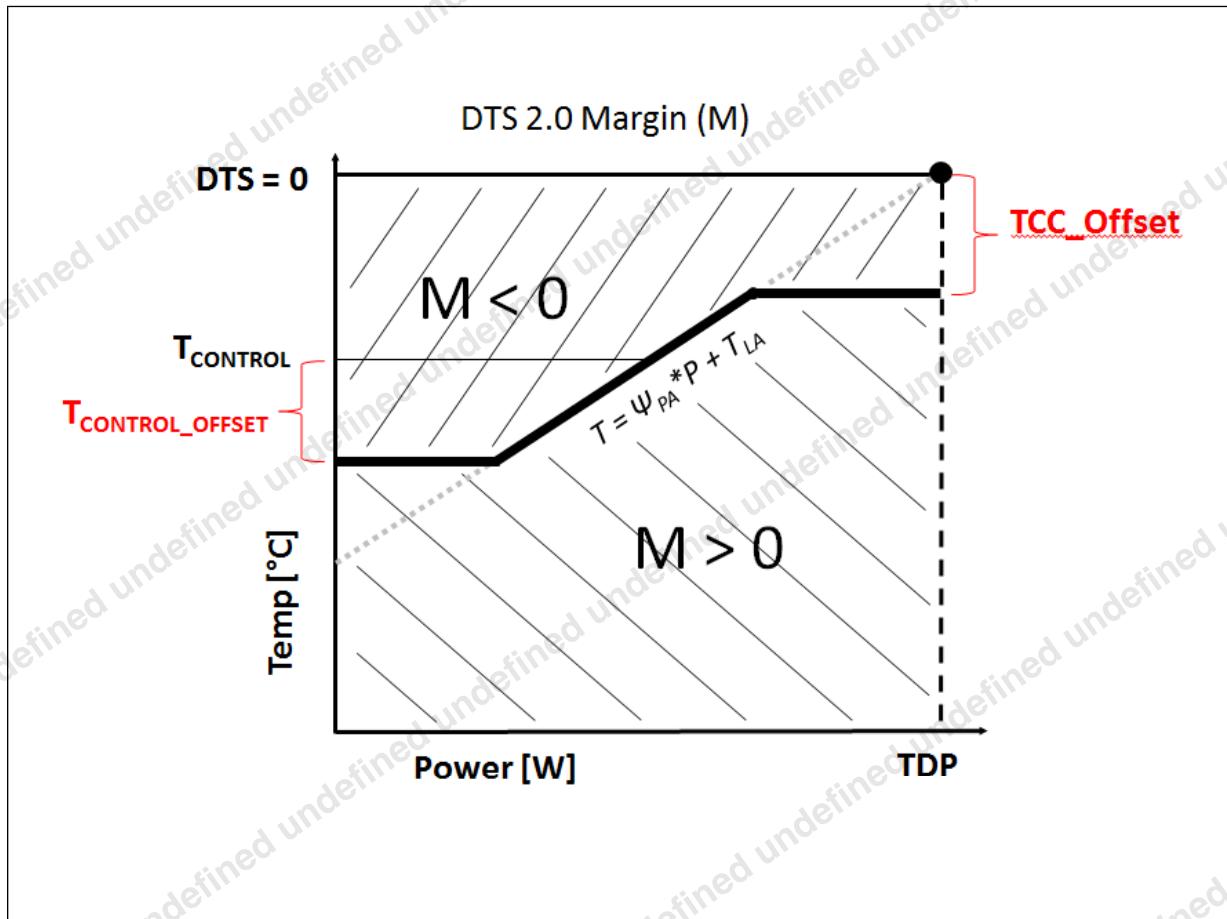
M < 0 indicates gap to spec, processor needs more cooling (for example, increase fan speed)

M > 0 this indicates margin to spec, processor is sufficiently cooled

Graphically, this is represented below. T<sub>CONTROL\_OFFSET</sub> is not writable to a register.



**Figure 19. Margin to Thermal Spec (M)**



DTS 2.0 processor Margin values can be obtained via PECI or Processor register see documentation below as well as *Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families, Volume 2 of 2, Registers Datasheet* and *Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families, Volume 1 of 2, Electrical Datasheet*

**Table 11. DTS 2.0 Margin From PECI**

Service	Index Value (IV) (decimal)	Parameter Value (word)	RdPkgConfig() Data (dword)	WrPkgConfig() Data (dword)	Description
Thermal Margin	10	0x0000	15:0--Package Temperature margin in 8.8 format, 32:16--Reserved	N/A	Package temperature margin with regards to DTS Thermal Profile. Positive indicates thermal margin, and package is less than DTS thermal profile

*Note: Refer to Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families, Volume 2 of 2, Registers Datasheet and Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families, Volume 1 of 2, Electrical Datasheet for further details*



**Table 12. DTS 2.0 Margin From Processor Register: CSR for PACKAGE\_THERM\_MARGIN**

Bus:1		Device:30	Function:0	Offset:E0
Bit	Attr	Default	Description	
31:16	RSVD-P	0000h	Reserved--Protected	
15:0	R0-V	0000h	THERM_MARGIN--This field provides Platform Firmware with running average of the instantaneous temperature margin above Tspec in 2's complement 8.8 format. This is the recommended field for Platform firmware to use for fan control. When this value is negative, it indicates a firmware must increase the fan speed. With a positive value, firmware may decrease the speed of the fan	

**Note:** • Refer to *Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families, Volume 2 of 2, Registers Datasheet* and *Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families, Volume 1 of 2, Electrical Datasheet* for full documentation of registers and field descriptions

## 4.2 Processor Thermal Features

### 4.2.1 Absolute Processor Temperature

The processor has a software readable field in the TEMPERATURE\_TARGET register that contains the minimum temperature at which the Thermal Control Circuit (TCC) will be activated and PROCHOT\_N will be asserted.

Intel does not test any third party software that reports absolute processor temperature. As such, Intel cannot recommend the use of software that claims this capability. Since there is part-to-part variation in the TCC (thermal control circuit) activation temperature, use of software that reports absolute temperature could be misleading.

### 4.2.2 Short Duration TCC Activation

Systems designed to meet thermal capacity may encounter short durations of throttling, also known as TCC activation, especially when running nonsteady processor stress applications. This is acceptable and is functionally within the intended temperature control parameters of the processor. Such short duration TCC activation is not expected to provide noticeable reductions in application performance, and is typically within the normal range of processor to processor performance variation.

## 4.3 Processor Thermal Specifications

The processor requires a thermal solution to maintain temperatures within operating limits. Any attempt to operate the processor outside these limits may result in permanent damage to the processor and potentially other components within the system. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete solution includes both component and system level thermal management features. Component level thermal solutions can include active or passive heatsinks attached to the processor integrated heat spreader (IHS). Typical system level thermal solutions may consist of system fans combined with ducting and venting.



For more information on designing a component level thermal solution, refer to [Processor Thermal Solutions](#) on page 47.

#### 4.3.1

### Thermal Specifications

To allow optimal operation and long-term reliability of Intel processor-based systems, the processor must remain between the minimum and maximum case temperature ( $T_{CASE}$ ) specifications as defined in the tables in the following sub-sections. Thermal solutions that do not provide sufficient thermal cooling may affect the long-term reliability of the processor and system.

Thermal profiles ensure adherence to Intel reliability requirements.

Intel assumes specific system boundary conditions (system ambient, airflow, heatsink performance / pressure drop, preheat, etc.) for each processor SKU to develop  $T_{case}$  and DTS thermal specifications. For servers each processor will be aligned to either 1U or 2U system boundary conditions. Customers can use other boundary conditions (for example a better thermal solution with higher ambient) providing they are compliant to those specifications. Furthermore, implementing a thermal solution that violates the thermal profile for extended periods of time may result in permanent damage to the processor or reduced life. The upper point of the thermal profile consists of the Thermal Design Power (TDP) and the corresponding  $T_{CASE\_MAX}$  value ( $x = TDP$  and  $y = T_{CASE\_MAX}$ ) represents a thermal solution design point.

For embedded servers, communications and storage markets, Intel has SKUs that support thermal profiles with nominal and short-term conditions designed to meet NEBS level 3 compliance. For these SKUs, operation at either the nominal or short-term thermal profiles should result in virtually no TCC activation. Thermal profiles for these SKUs are found in this chapter as well.

Intel recommends that thermal solution designs target the Thermal Design Power (TDP). The Adaptive Thermal Monitor feature is intended to help protect the processor in the event that an application exceeds the TDP recommendation for a sustained time period. The Adaptive Thermal Monitor feature must be enabled for the processor to remain within its specifications.

#### 4.3.2

### $T_{CASE}$ and DTS Based Thermal Specifications

To simplify compliance to thermal specifications at processor run time, the processor has a Digital Thermal Sensor (DTS) based thermal specification. Digital Thermal Sensor outputs a relative die temperature from TCC activation temperature.  $T_{CASE}$ -based specifications are used for heatsink sizing while DTS-based specs are used for acoustic and fan speed optimizations while the server is operating. Some SKUs may share the same  $T_{CASE}$  thermal profiles but have distinct DTS thermal profiles.

All thermal profiles, whether based on  $T_{CASE}$  or DTS, follow the straight-line equation format namely,  $y = mx + b$ . Where,

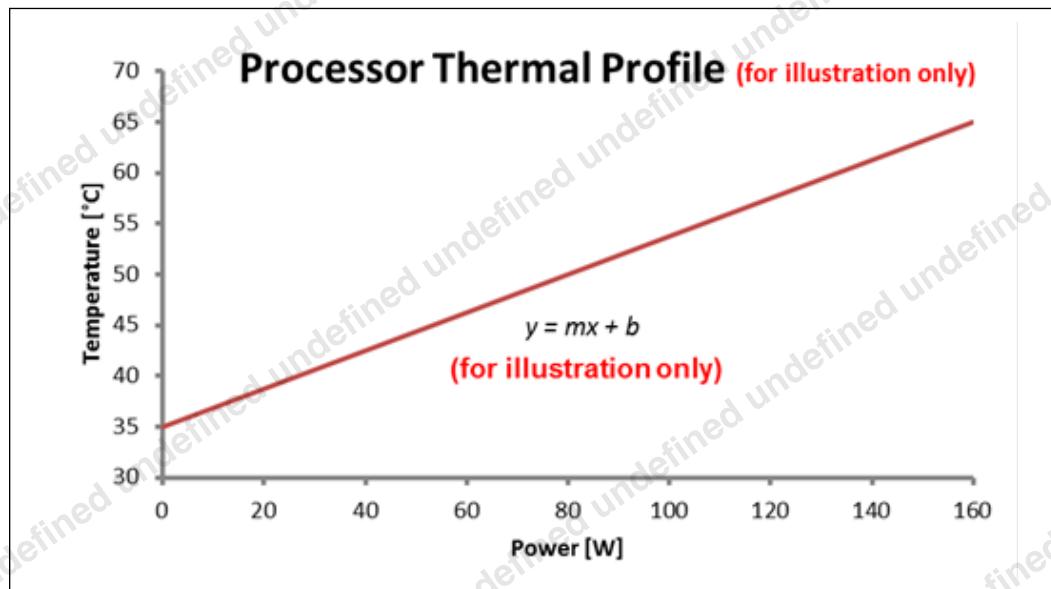
$y$  = temperature ( $T$ ) in °C

$m$  = slope ( $\Psi$ )

$x$  = power ( $P$ ) in Watts

$b$  =  $y$ -intercept ( $T_{LA}$ ) ( $LA$  = local ambient)

**Figure 20. Typical Thermal Profile Graph (Illustration Only)**



### 4.3.3 Server Processor Thermal Profiles and Form Factors

**Table 13.** Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families Stack  $T_{case}$  and DTS Thermal Profiles and Correction Factors

Category	Processor Number	Package Form Factor (die)	TDP (W)	Core Count	Assumed Heatsink Form Factor	C1E Disable Offset (°C)	$T_{control}$	Thermal Profiles		
								$T_{CASE}$ (°C)	DTS (°C)	DTS max at TDP Note: 5
Advanced	E5-2690 v3	Small (MCC)	135	12	1U Square	0	18	$T_c=[0.235*P]+58.2$	$T_{DTS}=[0.299*P]+58.2$	99
	E5-2680 v3	Small (MCC)	120	12	1U Square	0	10	$T_c=[0.235*P]+56.3$	$T_{DTS}=[0.311*P]+56.3$	95
	E5-2670 v3	Small (MCC)	120	12	1U Square	0	10	$T_c=[0.235*P]+56.3$	$T_{DTS}=[0.310*P]+56.3$	95
	E5-2660 v3	Small (MCC)	105	10	1U Square	0	10	$T_c=[0.236*P]+54.2$	$T_{DTS}=[0.329*P]+54.2$	90
	E5-2650 v3	Small (MCC)	105	10	1U Square	0	10	$T_c=[0.235*P]+54.2$	$T_{DTS}=[0.324*P]+54.2$	90
Standard	E5-2640 v3	Small (LCC)	90	8	1U Square	0	10	$T_c=[0.246*P]+52.2$	$T_{DTS}=[0.363*P]+52.2$	86
	E5-2630 v3	Small (LCC)	85	8	1U Square	0	10	$T_c=[0.243*P]+51.4$	$T_{DTS}=[0.392*P]+51.4$	86
	E5-2620 v3	Small (LCC)	85	6	1U Square	0	10	$T_c=[0.248*P]+51.5$	$T_{DTS}=[0.371*P]+51.5$	85

*continued...*



Category	Processor Number	Package Form Factor (die)	TDP (W)	Core Count	Assumed Heatsink Form Factor	C1E Disable Offset (°C)	Tcontrol	Thermal Profiles		
								Tcase (°C)	DTS (°C)	DTS max at TDP Note: 5
Basic	E5-2609 v3	Small (MCC)	85	6	1U Square	2	10	$T_c=[0.231*P]+51.3$	$T_{DTS}=[0.325*P]+51.3$	80
	E5-2603 v3	Small (LCC)	85	6	1U Square	0	10	$T_c=[0.250*P]+51.5$	$T_{DTS}=[0.353*P]+51.5$	83
Segment Optimized	E5-2699 v3	Large (HCC)	145	18	2U Square	0	18	$T_c=[0.175*P]+51.0$	$T_{DTS}=[0.243*P]+51.0$	88
	E5-2698 v3	Large (HCC)	135	16	1U Square	4	18	$T_c=[0.221*P]+58.2$	$T_{DTS}=[0.277*P]+58.2$	97
	E5-2697 v3	Large (HCC)	145	14	2U Square	0	18	$T_c=[0.177*P]+51.0$	$T_{DTS}=[0.276*P]+51.0$	93
	E5-2695 v3	Large (HCC)	120	14	1U Square	0	10	$T_c=[0.221*P]+56.1$	$T_{DTS}=[0.314*P]+56.1$	95
	E5-2683 v3	Large (HCC)	120	14	1U Square	0	10	$T_c=[0.220*P]+56.1$	$T_{DTS}=[0.285*P]+56.1$	92
	E5-2685 v3	Small (MCC)	120	12	1U Square	0	10	$T_c=[0.235*P]+56.3$	$T_{DTS}=[0.304*P]+56.3$	94
Frequency Optimized	E5-2667 v3	Small (LCC)	135	8	2U Square	3	18	$T_c=[0.202*P]+50.5$	$T_{DTS}=[0.336*P]+50.5$	97
	E5-2643 v3	Small (LCC)	135	6	2U Square	2	18	$T_c=[0.205*P]+49.6$	$T_{DTS}=[0.369*P]+49.6$	97
	E5-2637 v3	Small (LCC)	135	4	2U Square	2	18	$T_c=[0.205*P]+48.9$	$T_{DTS}=[0.402*P]+48.9$	97
	E5-2623 v3	Small (LCC)	105	4	1U Square	0	10	$T_c=[0.250*P]+53.9$	$T_{DTS}=[0.433*P]+53.9$	101
Low Power Workstation Only	E5-2687W v3 Note: 3	Small (MCC)	160	10	WS Passive Tower	0	10	$T_c=[0.190*P]+44.3$	$T_{DTS}=[0.299*P]+44.3$	94
Low Power	E5-2650L v3	Small (MCC)	65	12	1U Square	0	10	$T_c=[0.232*P]+48.5$	$T_{DTS}=[0.320*P]+48.5$	71
	E5-2630L v3	Small	55	8	1U Square	0	10	$T_c=[0.240*P]+47.2$	$T_{DTS}=[0.372*P]+47.2$	69

continued...



Category	Processor Number	Package Form Factor (die)	TDP (W)	Core Count	Assumed Heatsink Form Factor	C1E Disable Offset (°C)	T <sub>control</sub>	Thermal Profiles		
								T <sub>CASE</sub> (°C)	DTS (°C)	DTS max at TDP Note: 5
	(LCC)									

Notes: 1. These values are specified at VccIN\_MAX for all processor frequencies. Systems must be designed to ensure the processor is not subjected to any static Vcc and Icc combination wherein VccIN exceeds VccIN\_MAX at a specified Icc. Please refer to the electrical loadline specifications.  
 2. Thermal Design Power (TDP) should be used as a target for processor thermal solution design. Processor power may exceed TDP for short durations. Please see [Intel® Turbo Boost Technology](#) on page 50  
 3. This SKU is intended for dual processor workstations only and uses workstation specific use conditions for reliability assumptions.  
 4. Disabling C1E will result in an automatic reduction of DTSmax so that reliability is still protected. DTSmax will be reduced by the value shown 'C1E Disable Offset'. If thermal design has not been optimized to the reduced DTSmax value, throttling may result. Tcontrol is already an offset to DTSmax, therefore the absolute temp at which the Tcontrol threshold is reached will shift by the same amount.  
 5. DTS max at TDP is 2°C greater than DTS thermal profile at TDP, but applies only when part is operating at thermal design power and is installed in a system using microcode update 0x25 or later.  
 6. Tcase Minimum is 0°C

#### 4.3.4 Server 4S Processor Thermal Profiles and Form Factors

**Table 14. Intel® Xeon® Processor E5-4600 v3 Product Families Stack Product Family T<sub>case</sub> and DTS Thermal Profiles and Correction Factors**

Category	Processor Number	Package Form Factor (Die)	TDP (W)	Core Count	Assumed Heatsink Form Factor	C1E Disable Offset (°C)	T <sub>control</sub>	Thermal Profiles		DTS max at TDP Note: 5	Correction Factors
								T <sub>CASE</sub> (°C)	DTS (°C)		
High Performance Dense 4S Glueless	E5-4669 v3	Large (HCC)	135	18	1U Square	0	10	T <sub>C</sub> =[0.219*P]+58.1	T <sub>DTS</sub> =[0.280*P]+58.1	97	-0.007 -0.014
	E5-4667 v3	Large (HCC)	135	16	1U Square	0	10	T <sub>C</sub> =[0.219*P]+58.1	T <sub>DTS</sub> =[0.276*P]+58.1	97	-0.007 -0.014
Frequency Optimized Dense 4S Glueless	E5-4655 v3	Small (MCC)	135	6	1U Square	0	10	T <sub>C</sub> =[0.233*P]+56.3	T <sub>DTS</sub> =[0.352*P]+56.3	100	0.009 0.002
	E5-4627 v3	Small (MCC)	135	10	1U Square	0	10	T <sub>C</sub> =[0.237*P]+56.9	T <sub>DTS</sub> =[0.332*P]+56.9	100	0.013 0.006

*continued...*



Category	Processor Number	Package Form Factor (Die)	TDP (W)	Core Count	Assumed Heatsink Form Factor	C1E Disable Offset (°C)	T <sub>control</sub>	Thermal Profiles		DTS max at TDP Note: 5	Correction Factors	
								T <sub>CASE</sub> (°C)	DTS (°C)		Lukeville TTV	Looneyville TTV
Advanced	E5-4660 v3	Large (HCC)	120	14	1U Square	0	10	T <sub>C</sub> =[0.221*P]+56.1	T <sub>DTS</sub> =[0.312*P]+56.1	95	-0.005	-0.012
	E5-4650 v3	Large (HCC)	105	12	1U Square	0	10	T <sub>C</sub> =[0.224*P]+54.0	T <sub>DTS</sub> =[0.288*P]+54.0	86	-0.001	-0.008
Standard	E5-4640 v3	Large (HCC)	105	12	1U Square	0	10	T <sub>C</sub> =[0.224*P]+54.0	T <sub>DTS</sub> =[0.280*P]+54.0	85	-0.001	-0.008
	E5-4620 v3	Large (HCC)	105	10	1U Square	0	10	T <sub>C</sub> =[0.225*P]+54.0	T <sub>DTS</sub> =[0.289*P]+54.0	86	0.000	-0.007
Basic	E5-4610 v3	Large (HCC)	105	10	1U Square	0	10	T <sub>C</sub> =[0.224*P]+54.0	T <sub>DTS</sub> =[0.283*P]+54.0	85	0.000	-0.007
<p><b>Notes:</b></p> <ol style="list-style-type: none"> <li>These values are specified at VccIN_MAX for all processor frequencies. Systems must be designed to ensure the processor is not subjected to any static Vcc and Icc combination wherein VccIN exceeds VccIN_MAX at a specified Icc. Please refer to the electrical loadline specifications.</li> <li>Thermal Design Power (TDP) should be used as a target for processor thermal solution design. Processor power may exceed TDP for short durations. Please see <a href="#">Intel® Turbo Boost Technology</a> on page 50</li> <li>These specifications may be updated as further characterization data becomes available.</li> <li>Minimum T<sub>case</sub> Specification is 0°C</li> <li>DTS max at TDP is 2°C greater than DTS thermal profile at TDP, but applies only when part is operating at thermal design power and is installed in a system using microcode update 0x25 or later. See doc 550666 for further details</li> </ol>												

### 4.3.5 Workstation Processor Thermal Profiles and Form Factors

**Table 15. Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families 1S Workstation Stack T<sub>case</sub> and DTS Thermal Profiles and Correction Factors**

Category	Processor Number	Package Form Factor (Die Size)	TDP (W)	Core Count	Assumed Heatsink Form Factor	C1E Disable Offset (°C)	T <sub>control</sub>	Thermal Profiles		DTS max at TDP Note: 5
								T <sub>CASE</sub> (°C)	DTS (°C)	
1S Workstation	E5-1680 v3	Small (LCC)	140	8	WS Active Tower	3	10	T <sub>C</sub> =[0.175*P]+41.7	T <sub>DTS</sub> =[0.321*P]+41.7	88
	E5-1660 v3	Small (LCC)	140	8	WS Active Tower	0	10	T <sub>C</sub> =[0.173*P]+41.7	T <sub>DTS</sub> =[0.352*P]+41.7	92
	E5-1650 v3	Small (LCC)	140	6	WS Active Tower	2	10	T <sub>C</sub> =[0.178*P]+41.8	T <sub>DTS</sub> =[0.364*P]+41.8	94
	E5-1630 v3	Small (LCC)	140	4	WS Active Tower	5	10	T <sub>C</sub> =[0.177*P]+41.4	T <sub>DTS</sub> =[0.428*P]+41.4	103

*continued...*



Category	Processor Number	Package Form Factor (Die Size)	TDP (W)	Core Count	Assumed Heatsink Form Factor	C1E Disable Offset (°C)	T <sub>control</sub>	Thermal Profiles		DTS max at TDP Note: 5
								T <sub>CASE</sub> (°C)	DTS (°C)	
	E5-1620 v3	Small (LCC)	140	4	WS Active Tower	5	10	T <sub>C</sub> =[0.177*P]+41.4	T <sub>DTS</sub> =[0.428*P]+41.4	103
	E5-1607 v3	Small (LCC)	140	4	WS Active Tower	2	10	T <sub>C</sub> =[0.176*P]+41.4	T <sub>DTS</sub> =[0.423*P]+41.4	102
	E5-1603 v3	Small (LCC)	140	4	WS Active Tower	0	10	T <sub>C</sub> =[0.181*P]+41.8	T <sub>DTS</sub> =[0.336*P]+41.8	90

Notes:

1. These values are specified at VccIN\_MAX for all processor frequencies. Systems must be designed to ensure the processor is not subjected to any static Vcc and Icc combination wherein VccIN exceeds VccIN\_MAX at a specified Icc. Please refer to the electrical loadline specifications.
2. Thermal Design Power (TDP) should be used as a target for processor thermal solution design. Processor power may exceed TDP for short durations. Please see [Intel® Turbo Boost Technology](#) on page 50
3. This SKU is intended for single processor workstations only and uses workstation specific use conditions for reliability assumptions.
4. Minimum T<sub>case</sub> Specification is 0°C
5. DTS max at TDP is 2°C greater than DTS thermal profile at TDP, but applies only when part is operating at thermal design power and is installed in a system using microcode update 0x25 or later.

#### 4.3.6 Embedded Server Processor Thermal Profiles

Embedded Server processor SKUs target higher case temperatures and/or Network Equipment Building System (NEBS) thermal profiles for embedded communications server and storage form factors. The following thermal profiles pertain only to those specific SKUs. Network Equipment Building System is the most common set of environmental design guidelines applied to telecommunications equipment in the United States.



**Table 16. Embedded Server Processor Thermal Profiles**

Category	Processor Number	Package Form Factor	TDP (W)	Core Count	C1E Disable Offset (°C)	T <sub>Control</sub>	Maximum T <sub>CASE</sub> (°C)	T <sub>CASE</sub> Thermal Profile		DTS Thermal Profile			
								T <sub>CASE</sub> (°C) (Nominal)	T <sub>CASE</sub> (°C) (Short Term)	T <sub>DTS</sub> (°C) (Nominal)	DTS max at TDP (nominal) Note: 7	T <sub>DTS</sub> (°C) (Short Term)	DTS max at TDP (Short Term) Note: 7
Advanced	E5-2658A v3	Small	105	12	0	18	91	T <sub>C</sub> =[0.228 *P] + 52.0	T <sub>C</sub> =[0.228 *P] + 67.0	T <sub>DTS</sub> =[0.296 *P] + 52.0	85	T <sub>DTS</sub> =[0.296 *P] + 67.0	100
	E5-2658 v3	Small	105	12	0	18	87	T <sub>C</sub> =[0.190 * P] + 52.0	T <sub>C</sub> =[0.190 * P] + 67.0	T <sub>DTS</sub> =[0.258 * P] + 52.0	81	T <sub>DTS</sub> =[0.258 * P] + 67.0	96
Standard	E5-2648L v3	Small	75	12	0	18	87	T <sub>C</sub> =[0.267 * P] + 52.0	T <sub>C</sub> =[0.267 * P] + 67.0	T <sub>DTS</sub> =[0.350 * P] + 52.0	80	T <sub>DTS</sub> =[0.350 * P] + 67.0	95
	E5-2628L v3	Small	75	10	0	18	87	T <sub>C</sub> =[0.267 * P] + 52.0	T <sub>C</sub> =[0.267 * P] + 67.0	T <sub>DTS</sub> =[0.352 * P] + 52.0	80	T <sub>DTS</sub> =[0.352 * P] + 67.0	95

*continued...*



Category	Processor Number	Package Form Factor	TDP (W)	Core Count	C1E Disable Offset (°C)	T <sub>control</sub>	Maximum T <sub>CASE</sub> (°C)	T <sub>CASE</sub> Thermal Profile		DTS Thermal Profile			
								T <sub>CASE</sub> (°C) (Nominal)	T <sub>CASE</sub> (°C) (Short Term)	T <sub>DTS</sub> (°C) (Nominal)	DTS max at TDP (nominal)	T <sub>DTS</sub> (°C) (Short Term)	DTS max at TDP (Short Term)
Basic	E5-2618L v3	Small	75	8	0	18	87	T <sub>C</sub> = [0.267 * P] + 52.0	T <sub>C</sub> = [0.267 * P] + 67.0	T <sub>DTS</sub> = [0.378 * P] + 52.0	82	T <sub>DTS</sub> = [0.378 * P] + 67.0	97
Basic	E5-2608L v3	Small	52	6	0	18	88	T <sub>C</sub> = [0.404 * P] + 52.0	T <sub>C</sub> = [0.404 * P] + 67.0	T <sub>DTS</sub> = [0.509 * P] + 52.0	81	T <sub>DTS</sub> = [0.509 * P] + 67.0	96

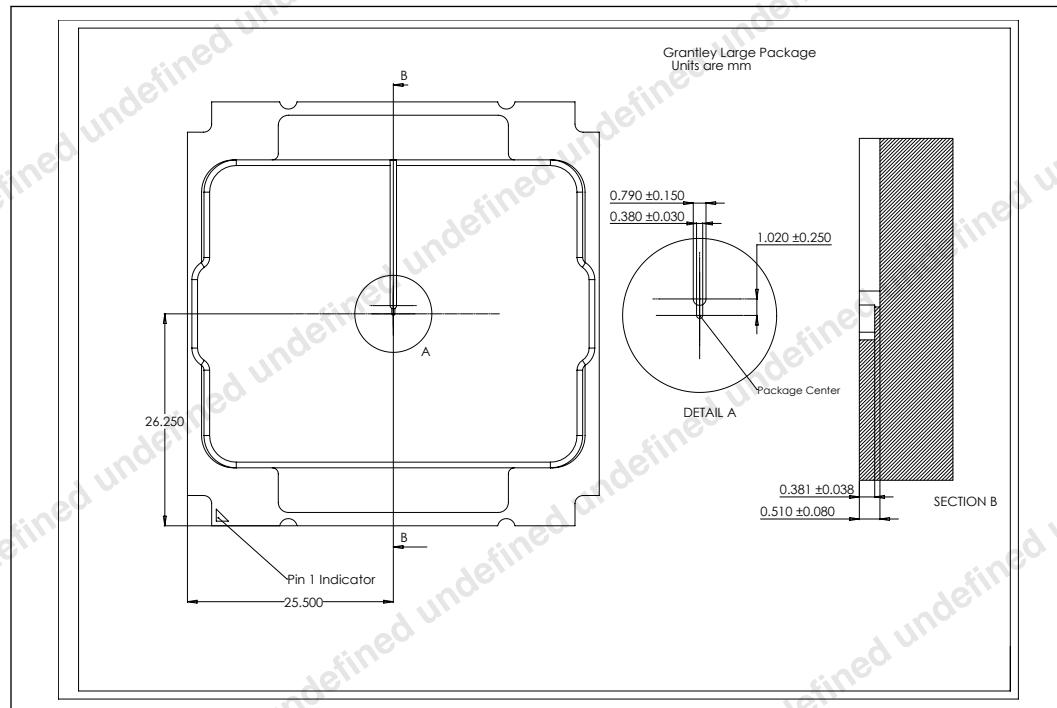
- Notes:
1. These values are specified at VccIN\_MAX for all processor frequencies. Systems must be designed to ensure the processor is not subjected to any static Vcc and Icc combination wherein VccIN exceeds VccIN\_MAX at a specified Icc. Please refer to the electrical lineout specifications.
  2. Thermal Design Power (TDP) should be used as a target for processor thermal solution design at maximum T<sub>CASE</sub>. Processor power may exceed TDP for short durations. Please see [Intel® Turbo Boost Technology](#) on page 50.
  3. Power specifications are defined at all VIDs found in the *Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families, Volume 2 of 2, Registers Datasheet* and *Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families, Volume 1 of 2, Electrical Datasheet*. Processors may be delivered under multiple VIDs for each frequency.
  4. The Nominal Thermal Profile must be used for all normal operating conditions or for products that do not require NEBS Level 3 compliance.
  5. The Short-Term Thermal Profile may only be used for short-term excursions to higher ambient operating temperatures, not to exceed 96 hours per instance, 360 hours per year, and a maximum of 15 instances per year, as compliant with NEBS Level 3. Operation at the Short-Term Thermal Profile for durations exceeding 360 hours per year violate the processor thermal specifications and may result in permanent damage to the processor.
  6. Minimum T<sub>case</sub> Specification is 0°C
  7. DTS max at TDP is 2°C greater than DTS thermal profile at TDP, but applies only when part is operating at thermal design power and is installed in a system using microcode update 0x25 or later.

#### 4.3.7 Thermal Metrology

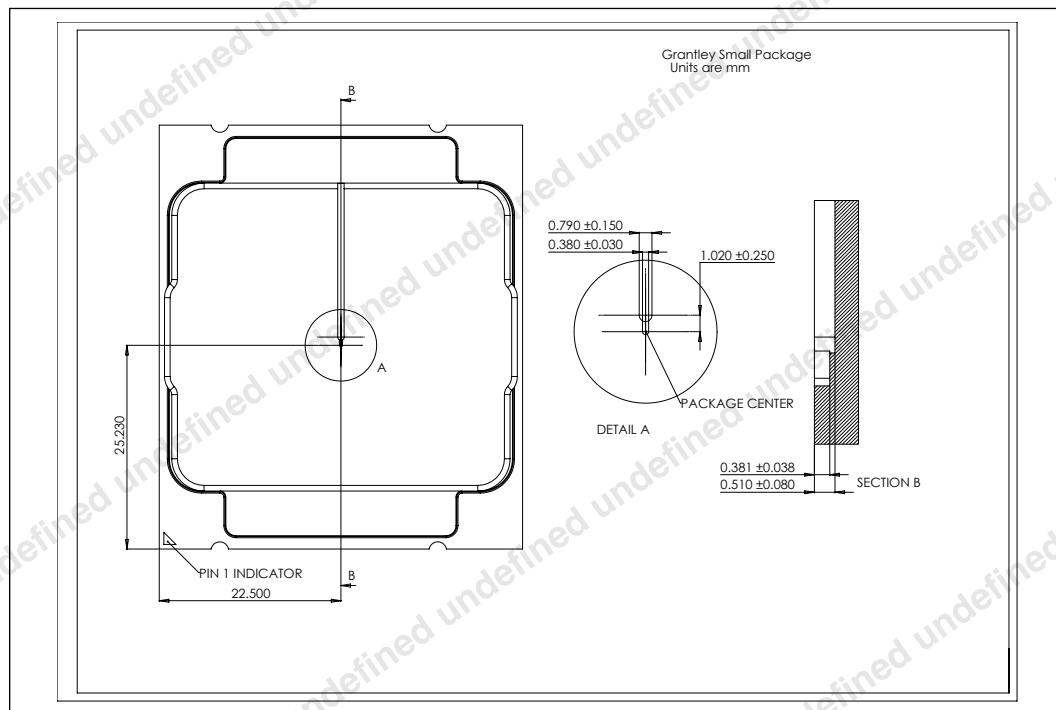
The minimum and maximum case temperatures (T<sub>CASE</sub>) specified are measured at the geometric top center of the processor integrated heat spreader (IHS). The following figures illustrate the location where T<sub>CASE</sub> temperature measurements should be made. The figures also include geometry guidance for modifying the IHS to accept a thermocouple probe.



**Figure 21. Case Temperature ( $T_{CASE}$ ) Measurement Location for Large Package**



**Note:** Figure is not to scale and is for reference only.

**Figure 22. Case Temperature ( $T_{CASE}$ ) Measurement Location for Small Package**

**Note:** Figure is not to scale and is for reference only.

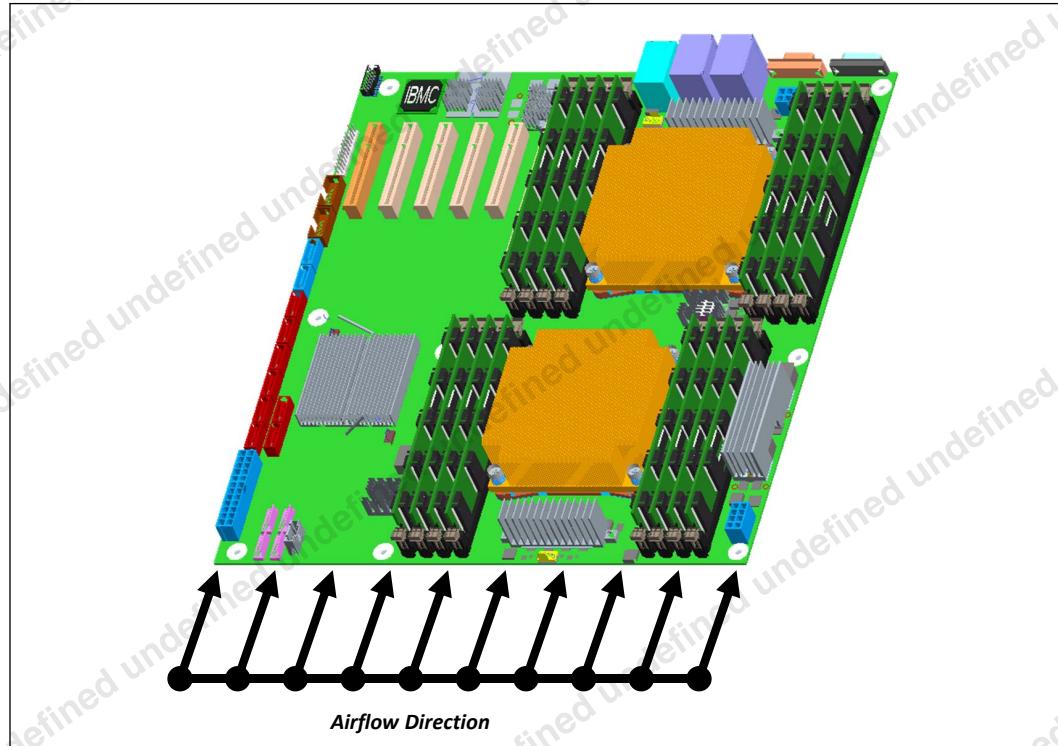


## 5.0 Processor Thermal Solutions

### 5.1 Processor Boundary Conditions for Shadowed and Spread Core Layouts

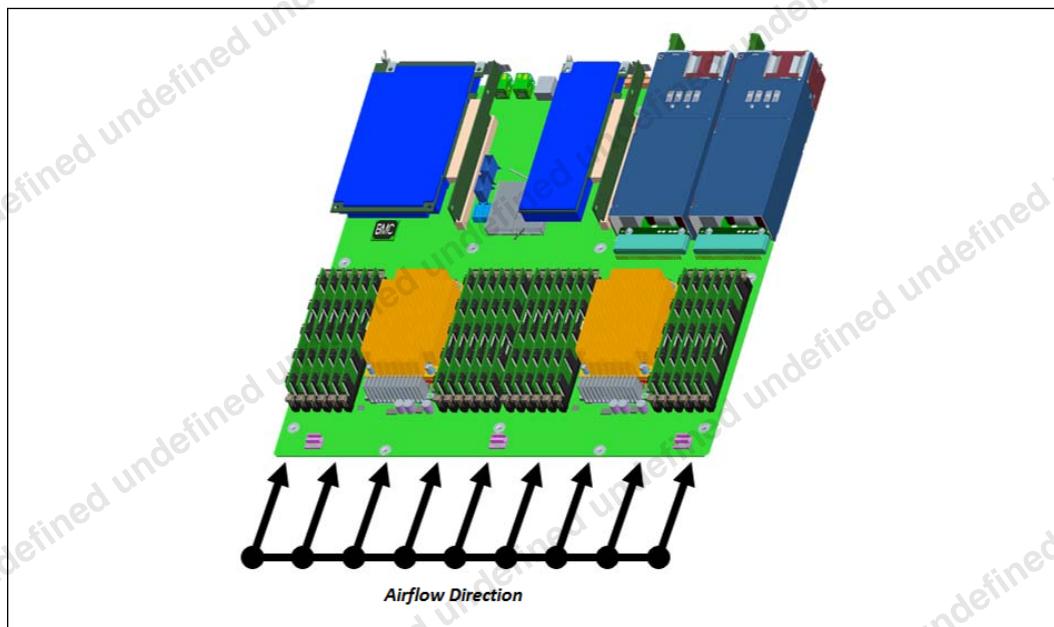
Intel's processors go into a variety of board layouts and form factors. Boundary conditions for the SSI EEB layout (sometimes referred to as "shadowed layout") are included in the table below for 1U, 2U and Workstation systems. A typical shadowed layout with a 1U heat sink is shown below.

**Figure 23. Typical Shadowed Layout**



Another approach is the "spread core" layout, where neither processor is "shadowed" by the other, as shown below.

**Figure 24. Typical Spread Core Layout**



**Table 17. Processor Boundary Conditions for Shadowed and Spread Core Layouts**

System <sup>1</sup>	Board Layout <sup>2</sup>	Heatsink Form Factor <sup>3</sup>	Heatsink Description	Airflow <sup>4</sup> (CFM) / RPM	$\Delta P$ <sup>4</sup> (in H <sub>2</sub> O)	$\Psi_{CA,TV}^{LA}$ (°C/W) <sup>5</sup>	T <sub>LA</sub> for each TDP SKU (°C) <sup>6</sup>								
							70W	80W	85W	105W	120W	135W	140W	145W	160W
1U	Spread core, 24 DIMMs	70 x 106 x 25.5mm (Narrow) [STS200PNR]	Copper base Aluminum fin (Passive)	10.2	0.233	0.256	41.5	41.5	41.5	41.5	41.5	41.5	N/A	N/A	N/A
1U	SSI EEB, 16 DIMMs	91.5 x 91.5 x 25.5mm (Square) [STS200P]	Copper base Aluminum fin (Passive)	15.2	0.382	0.250	47.4	48.6	49.1	51.4	53.1	54.8	N/A	N/A	N/A
2U	SSI EEB, 16 DIMMs	91.5 x 91.5 x 64mm (Square) [STS200C]	Copper base Aluminum fin with Heatpipe (Passive)	26.0	0.138	0.201	42.8	43.5	43.9	45.3	46.4	47.5	47.9	48.2	N/A
WS	SSI EEB, 16 DIMMs	100 x 70 x 123.2mm (Tower)	Copper base Aluminum fin with Heatpipe (Active)	2600 RPM	Not meaningful for Active Heatsink	0.197	38.2	38.5	38.7	39.3	39.7	40.1	40.3	40.5	40.9

**Note:**

- 1U = 1.75" which is the outside-to-outside dimension of the server enclosure.
- SSI Specification is found at <https://ssiforum.org/>.

*continued...*



System <sup>1</sup>	Board Layout <sup>2</sup>	Heatsink Form Factor <sup>3</sup>	Heatsink Description	Airflow <sup>4</sup> (CFM) / RPM	ΔP <sup>4</sup> (in H <sub>2</sub> O)	Ψ <sup>CA-TTV</sup> (°C/W) <sup>5</sup>	T <sub>LA</sub> for each TDP SKU (°C) <sup>6</sup>								
							70W	80W	85W	105W	120W	135W	140W	145W	160W
3. Refer to Intel Reference Design Heat Sink on page 55. Dimensions of heat sink do not include socket or processor. 4. Airflow through the heat sink fins with zero bypass. Max target for pressure drop ( $\Delta P$ ) measured in inches H <sub>2</sub> O. 5. Mean + 3σ performance for a heat sink on top of the Thermal Test Vehicle (TTV). These estimates are <b>not</b> necessarily the thermal performance targets needed to meet processor thermal specifications. Includes thermal performance of Honeywell* PCM45F. 6. System ambient $T_{SA} = 35^{\circ}\text{C}$ . Increase in air temperature inside the chassis (from the front grill to the downstream, or shadowed, processor heatsink). Includes preheat from hard drives, VRs, front processor, etc. as shown below.															

  
 $T_{RISE}$   
(shown for illustration only)

## 5.2

## Heatsink Design Considerations

To remove the heat from the processor, three basic parameters should be considered:

- The area of the surface on which the heat transfer takes place - Without any enhancements, this is the surface of the processor package IHS. One method used to improve thermal performance is to attach a heatsink to the IHS. A heatsink can increase the effective heat transfer surface area by conducting heat out of the IHS and into the surrounding air through fins attached to the heatsink base.
- The conduction path from the heat source to the heatsink fins - Providing a direct conduction path from the heat source to the heatsink fins and selecting materials with higher thermal conductivity typically improves heatsink performance. The length, thickness, and conductivity of the conduction path from the heat source to the fins directly impact the thermal performance of the heatsink. In particular, the quality of the contact between the package IHS and the heatsink base has a higher impact on the overall thermal solution performance as processor cooling requirements become strict. Thermal interface material (TIM) is used to fill in the gap between the IHS and the bottom surface of the heatsink, and thereby improves the overall performance of the thermal stackup (IHS-TIM-Heatsink). With extremely poor heatsink interface flatness or roughness, TIM may not adequately fill the gap. The TIM thermal performance depends on its thermal conductivity as well as the pressure load applied to it.
- The heat transfer conditions on the surface upon which heat transfer takes place - Convective heat transfer occurs between the airflow and the surface exposed to the flow. It is characterized by the local ambient temperature of the air, TLA, and the local air velocity over the surface. The higher the air velocity over the surface, the more efficient the resulting cooling. The nature of the airflow can also enhance heat transfer via convection. Turbulent flow can provide improvement over laminar flow. In the case of a heatsink, the surface exposed to the flow includes the fin faces and the heatsink base.



An active heatsink typically incorporates a fan that helps manage the airflow through the heatsink.

Passive heatsink solutions require in-depth knowledge of the airflow in the chassis. Typically, passive heatsinks see slower air speed. Therefore, these heatsinks are typically larger (and heavier) than active heatsinks due to the increase in fin surface necessary to meet a required performance. As the heatsink fin density (the number of fins in a given cross-section) increases, the resistance to the airflow increases; it is more likely that the air will travel around the heatsink instead of through it, unless air bypass is carefully managed. Using air-ducting techniques to manage bypass area is an effective method for maximizing airflow through the heatsink fins.

## 5.3

## Thermal Design Guidelines

### 5.3.1

### Intel® Turbo Boost Technology

Intel® Turbo Boost Technology is a feature available on certain Intel® Xeon® processor E5-1600 and E5-2600 v3 product families SKUs that opportunistically, and automatically allows the processor to run faster than the marked frequency if the part is operating below certain power and temperature limits. With Turbo Boost enabled, the instantaneous processor power *can exceed TDP for short durations* resulting in increased performance.

System thermal design should consider the following important parameters (set via BIOS):

- POWER\_LIMIT\_1 (PL1) = average processor power over a long time window (default setting is TDP)
- POWER\_LIMIT\_2 (PL2) = average processor power over a short time window above TDP (short excursions). Maximum allowed by the processor is 20% above TDP for all SKUs ( $1.2 * \text{TDP}$ ). Note that actual power will include IMON inaccuracy.
- POWER\_LIMIT\_1\_TIME (Tau) = time constant for the exponential weighted moving average (EWMA) which optimizes performance while reducing thermal risk. (dictates how quickly power decays from its peak)

Please note that although the processor can exceed PL1 (default TDP) for a certain amount of time, the *exponential weighted moving average (EWMA) power will never exceed PL1*.

A properly designed processor thermal solution is important to maximizing Turbo Boost performance. However, heatsink performance (thermal resistance,  $\Psi_{CA}$ ) is only one of several factors that can impact the amount of benefit. Other factors are operating environment, workload and system design. With Turbo Mode enabled, the processor may run more consistently at higher power levels, and be more likely to operate above TCONTROL, as compared to when Turbo Mode is disabled. This may result in higher acoustics.

### 5.3.2

### Thermal Excursion Power

Under fan failure or other anomalous thermal excursions, processor temperature (either  $T_{CASE}$  or DTS) may exceed the thermal profile for a duration totaling less than 360 hours per year without affecting long term reliability (life) of the processor. For



more typical thermal excursions, Thermal Monitor is expected to control the processor power level as long as conditions do not allow the processor to exceed the temperature at which Thermal Control Circuit (TCC) activation initially occurred.

Under more severe anomalous thermal excursions when the processor temperature cannot be controlled at or below thermal profile by TCC activation, then data integrity is not assured. At some higher thresholds, THERMTRIP\_N will enable a shut down in an attempt to prevent permanent damage to the processor.

A designer can check anomalous power ratio of an individual part by reading register PWR\_LIMIT\_MISC\_INFO and dividing the value of PN\_POWER\_OF\_SKU by the sku TDP. Please refer to *Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families, Volume 2 of 2, Registers Datasheet* and *Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families, Volume 1 of 2, Electrical Datasheet*

### 5.3.3

### Thermal Characterization Parameters

The case-to-local ambient Thermal Characterization Parameter ( $\Psi_{CA}$ ) is defined by:

$$\Psi_{CA} = (T_{case} - T_{LA}) / TDP$$

Where:

$T_{CASE}$  = Processor case temperature (°C)

$T_{LA}$  = Local ambient temperature before the air enters the processor heatsink (°C)

TDP = TDP (W) assumes all power dissipates through the integrated heat spreader. This inexact assumption is convenient for heatsink design.

$$\Psi_{CA} = \Psi_{CS} + \Psi_{SA}$$

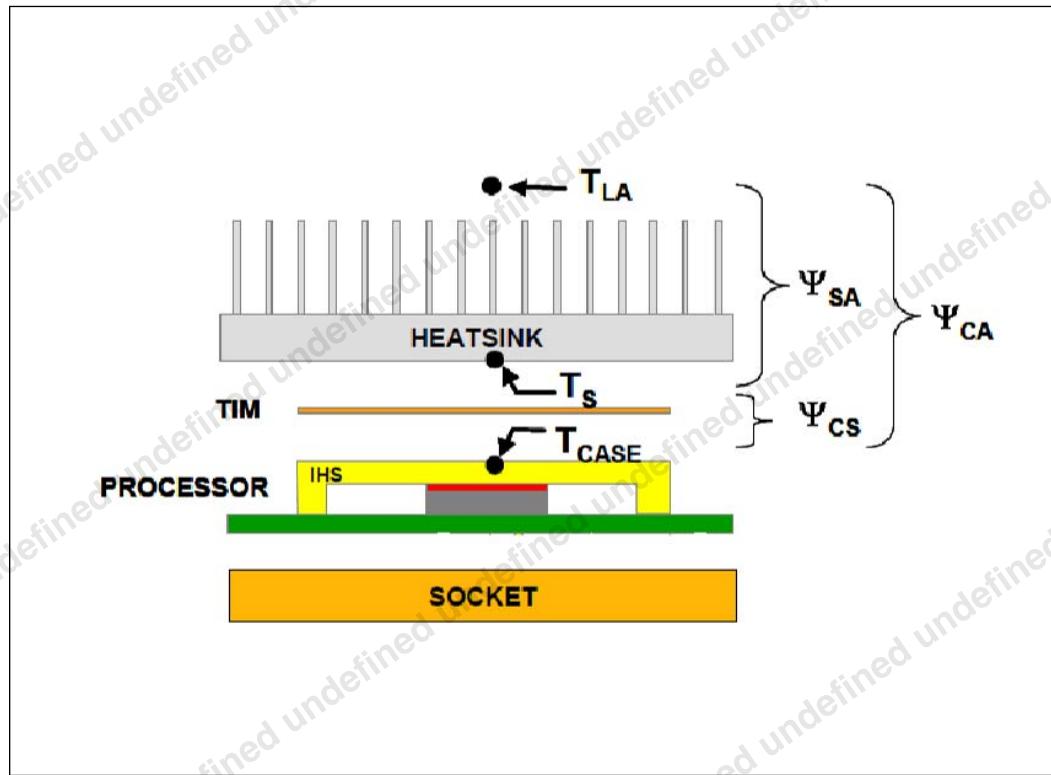
Where:

$\Psi_{CS}$  = Thermal characterization parameter of the TIM (°C/W) is dependent on the thermal conductivity and thickness of the TIM.

$\Psi_{SA}$  = Thermal characterization parameter from heatsink-to-local ambient (°C/W) is dependent on the thermal conductivity and geometry of the heatsink and dependent on the air velocity through the heatsink fins.

The following figure illustrates the thermal characterization parameters.

**Figure 25. Thermal Characterization Parameters**



## 5.4

### Thermal Interface Material (TIM) Considerations

Thermal Interface Material between the processor IHS and the heatsink base is necessary to improve thermal conduction from the IHS to the heatsink. Many thermal interface materials can be pre-applied to the heatsink base prior to shipment from the heatsink supplier without the need for a separate TIM dispense or attachment process in the final assembly factory.

All thermal interface materials should be sized and positioned on the heatsink base in a way that ensures that the entire area is covered. It is important to compensate for heatsink-to-processor positional alignment when selecting the proper TIM size.

When pre-applied material is used, it is recommended to have a protective cover. Protective tape is not recommended as the TIM could be damaged during its removal step.

Thermal performance usually degrades over the life of the assembly and this degradation needs to be accounted for in the thermal performance. Degradation can be caused by shipping and handling, environmental temperature, humidity conditions, load relaxation over time, temperature cycling or material changes (most notably in the TIM) over time. For this reason, the measured  $T_{CASE}$  value of a given processor may increase over time, depending on the type of TIM material.



## 5.5

## Mechanical Recommendations and Targets

Thermal solutions should be designed to meet the mechanical requirements described in this section.

Keep in mind that the heatsink retention will need to apply additional load in order to achieve the minimum Socket Static Total Compressive load. This load should be distributed over the IHS (Integrated Heat Spreader). The dual-loading approach is represented by the following equation.

$$F_{ILM} + F_{HEATSINK} = F_{SOCKET}$$

### 5.5.1

### Processor / Socket Stackup Height

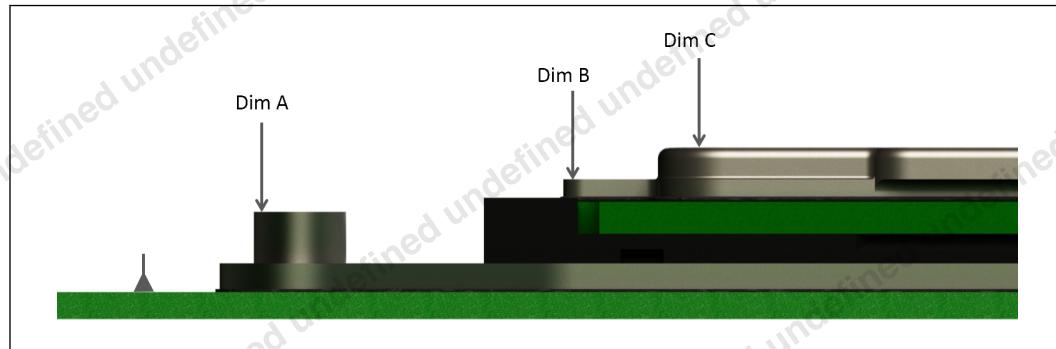
The table below provides the stackup height of a processor and LGA2011-3 socket with processor fully seated. This value is the root sum of squares summation of: (a) the height of the socket seating plane above the motherboard after reflow, (b) the height of the package, from the package seating plane to the top of the IHS, and accounting for its nominal variation and tolerances given in the processor, socket and ILM drawings

**Table 18. Target Stackup Heights From Top of Board to Top of IHS**

	Intel® Xeon® Processor E5-1600 and E5-2600 v3 Product Families <sup>1,2,4</sup>
Integrated Stackup Height From Top of Board to Top of ILM Stud (Dimension A)	4.678 (+0.367)/(-0.231mm)
Integrated Stackup Height From Top of Board to Top of IHS Load Lip (Dimension B)	6.581±0.289
Integrated Stackup Height From Top of Board to Top of IHS (Dimension C)	8.481±0.279

*Notes:* 1. Tolerance Stackups are a Root Sum of Squares (RSS) of all components in stack calculation using mother board surface as the reference point  
 2. Intel® Xeon® processor E5-1600 and E5-2600 v3 product families Stackup targets are inclusive of all package sizes (large and small)  
 3. All packages are compatible with reference retention solutions and will meet mechanical specifications

**Figure 26. Integrated Stack Up Height**



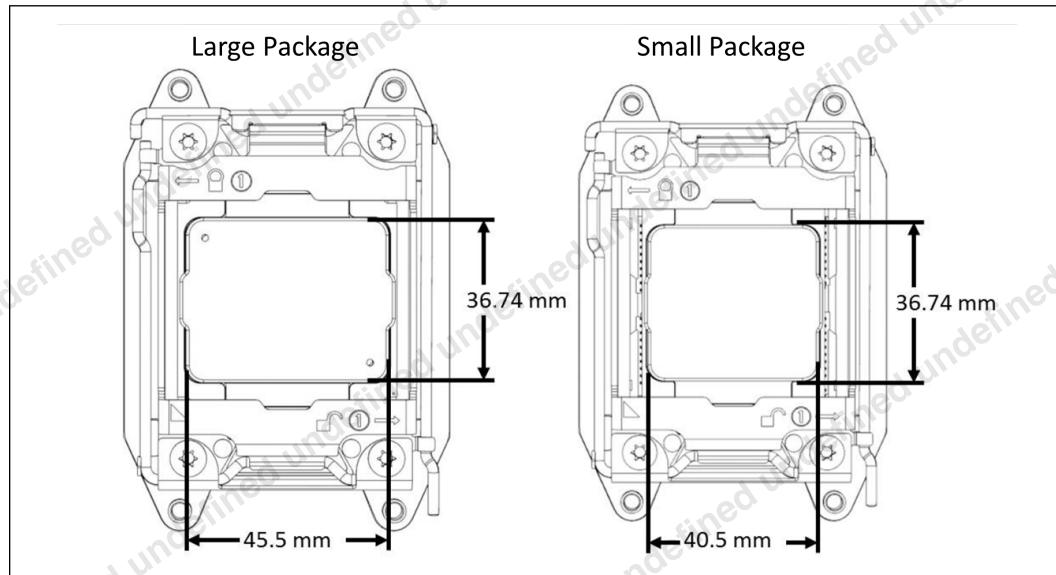
*Note:* ILM components removed for clarity

The table below provides the available surface dimensions for cooling the processor when fully seated in LGA2011-3 socket. This value is the X and Y dimensions for the flat top of the IHS.

**Table 19. Available Cooling Area for Large and Small IHS**

Available Area	Large package	45.5 mm x 36.74 mm (1.791 in x 1.446 in)
	Small package	40.5 mm x 36.74 mm (1.594 in x 1.446 in)

**Figure 27. Available Cooling Area for Top of Large and Small IHS**



## 5.5.2 Processor Heatsink Mechanical Targets

**Table 20. Heatsink Mechanical Targets**

Parameter	Min	Max	Notes
Heatsink Mass (includes retention)		600 g (1.32 lbf)	3
Heatsink Applied Static Compressive Load	222 N (50 lbf)	400 N (90 lbf)	1,2
Heatsink Applied Dynamic only Compressive load		445 N (100 lbf)	1,4,5

**Notes:**

- 1. These specifications apply to uniform compressive loading in a direction perpendicular to the processor top surface (IHS).
- 2. This is the minimum and maximum static force that can be applied by the heatsink retention to the processor top surface (IHS).
- 3. This specification prevents excessive baseboard deflection during dynamic events.
- 4. Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement.
- 5. An experimentally validated test condition used a heatsink mass of 1.32 lbf (600g) with 25 G acceleration measured on a shock table with a dynamic amplification factor of 3. This specification can have flexibility in specific values, but the ultimate product of mass times acceleration should not exceed this validated dynamic load (1.32 lbf x 25 G x 3 = 100 lbf).



## 5.6

## Heatsink Mechanical and Structural Considerations

An attachment mechanism must be designed to support the heatsink because there are no features on the socket on which to directly attach a heatsink. In addition to holding the heatsink in place on top of the IHS, this mechanism plays a significant role in the performance of the system, in particular:

- Ensuring thermal performance of the TIM applied between the IHS and the heatsink. TIMs, especially those based on phase change materials, are very sensitive to applied pressure: the higher the pressure, the better the initial performance. TIMs such as thermal greases are not as sensitive to applied pressure. Designs should consider the possible decrease in applied pressure over time due to potential structural relaxation in enabled components.
- Ensuring system electrical, thermal, and structural integrity under shock and vibration events, particularly the socket solder joints. The mechanical requirements of the attachment mechanism depend on the weight of the heatsink and the level of shock and vibration that the system must support. The overall structural design of the baseboard and system must be considered when designing the heatsink attachment mechanism. Their design should provide a means for protecting socket solder joints, as well as preventing package pullout from the socket.

Please note that the load applied by the attachment mechanism must comply with the processor mechanical specifications, along with the dynamic load added by the mechanical shock and vibration requirements, as discussed in [Package Loading Specifications](#) on page 63.

A potential mechanical solution for heavy heatsinks is the use of a supporting mechanism such as a backer plate or the utilization of a direct attachment of the heatsink to the chassis pan. In these cases, the strength of the supporting component can be utilized rather than solely relying on the baseboard strength. In addition to the general guidelines given above, contact with the baseboard surfaces should be minimized during installation in order to avoid any damage to the baseboard.

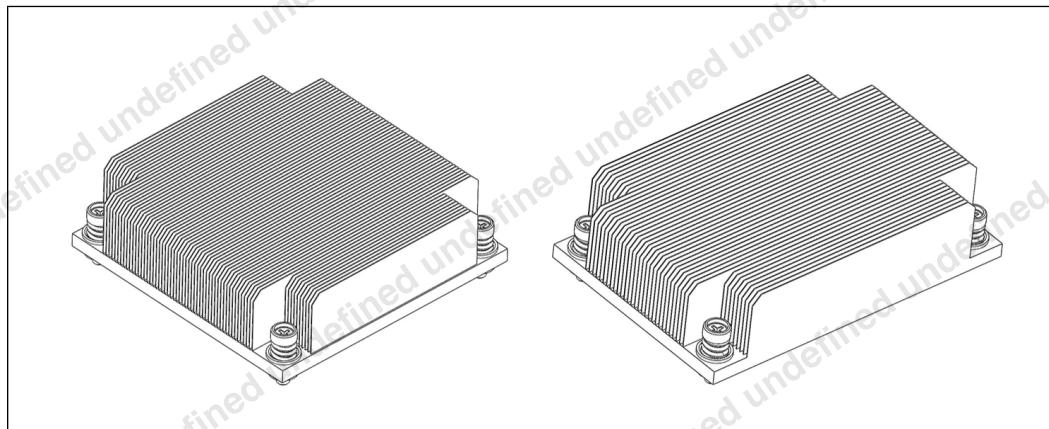
## 5.7

## Intel Reference Design Heat Sink

Intel has several reference heat sinks for the Grantley platform. This section details the design targets and performance of each. These heat sinks are also productized as part of Intel's Boxed Processors retail program (product codes shown in parentheses). For more information please goto [Boxed Processor Specifications](#) on page 67.

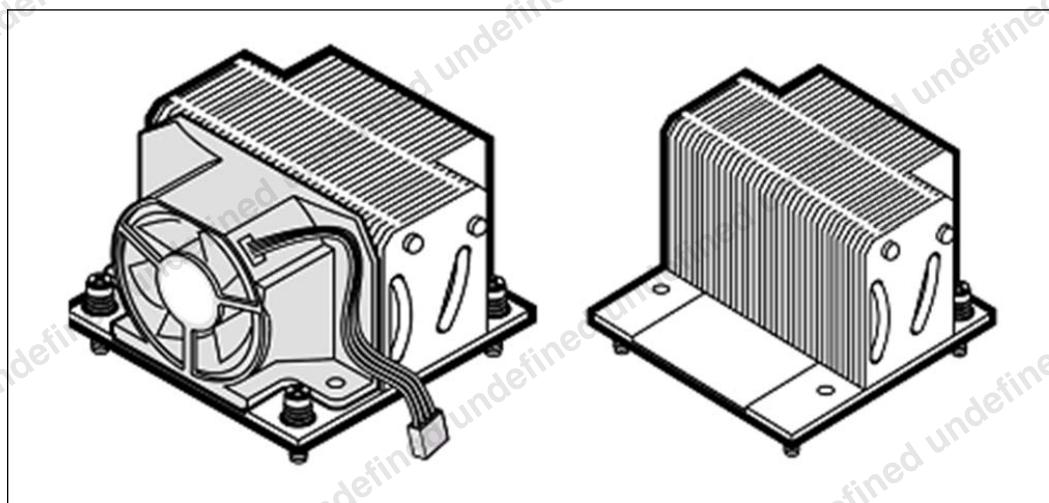
Below are the 1U Square and 1U Narrow heatsinks (STS200P and STS200PNRW respectively).

**Figure 28.** 1U Form Factor Heat Sinks



Below are the 2U Square active and passive heatsinks (STS200C).

**Figure 29.** 2U Form Factor Heat Sinks



Below is the Tower Active heatsink.



**Figure 30. Workstation Form Factor Heat Sink**



### Heat Sink Performance

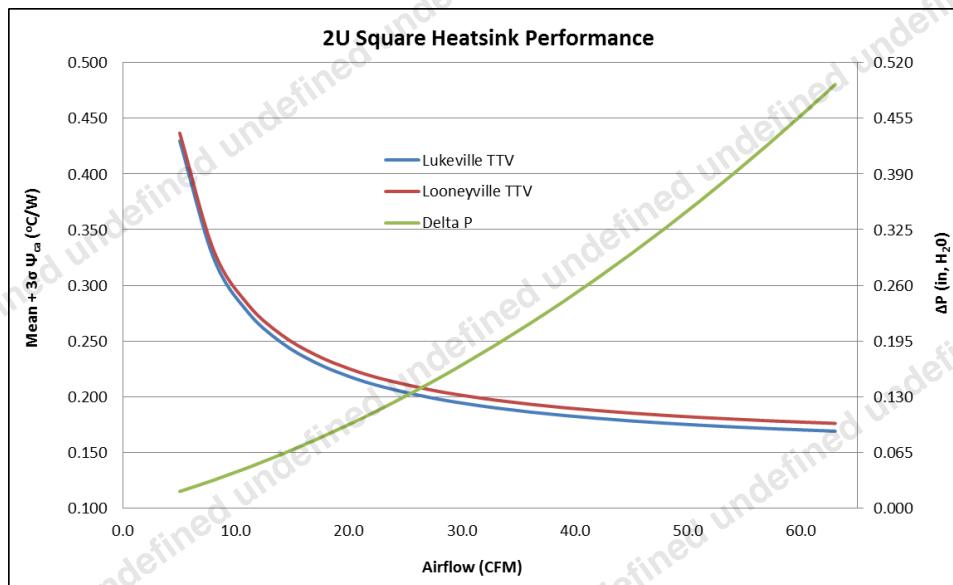
The graphs below show mean thermal resistance ( $\Psi_{CA}$ ) and pressure drop ( $\Delta P$ ) as a function of airflow. Best-fit equations are also provided. The sample calculations match the boundary conditions given in the [Processor Boundary Conditions for Shadowed and Spread Core Layouts](#) on page 47.

#### 5.7.1

### 2U Square Heatsink Performance

The following performance curves are based on the Intel® Xeon® processor E5-1600 and E5-2600 v3 product families Lukeville and Looneyville thermal test vehicle (TTV). Refer to *Lukeville FCLGA12 Package Thermal/Mechanical Test Vehicle Application Note* for details.

- $\Psi_{CA}(\text{mean})$ ,  $\mu = 0.127 + (1.3901) \cdot (\text{CFM})^{-0.9862}$  ( $^{\circ}\text{C}/\text{W}$ ). This is based on Lukeville TTV
- $\Psi_{CA}(\text{mean})$ ,  $\mu = 0.134 + (1.3901) \cdot (\text{CFM})^{-0.9862}$  ( $^{\circ}\text{C}/\text{W}$ ). This is based on Looneyville TTV
- $\Psi_{CA}(\text{variance})$ ,  $\sigma = 0.0062$  ( $^{\circ}\text{C}/\text{W}$ )
- $\Delta P = (6.91E-05) \cdot (\text{CFM})^2 + (3.50E-3) \cdot (\text{CFM})$  (in.  $\text{H}_2\text{O}$ )



Sample calculation when airflow = 26 CFM

- **Ψ<sub>CA</sub> Based on Lukeville TTV**
  - $\Psi_{CA}(\mu) = 0.127 + (1.3901) \cdot (26)^{-0.9862} = 0.183$  ( $^{\circ}\text{C}/\text{W}$ )
  - $\Psi_{CA}(\mu + 3\sigma) = 0.183 + 3 * (0.0062) = \mathbf{0.202}$  ( $^{\circ}\text{C}/\text{W}$ )
- **Ψ<sub>CA</sub> Based on Looneyville TTV**
  - $\Psi_{CA}(\mu) = 0.134 + (1.3901) \cdot (26)^{-0.9862} = 0.190$  ( $^{\circ}\text{C}/\text{W}$ )
  - $\Psi_{CA}(\mu + 3\sigma) = 0.190 + 3 * (0.0062) = \mathbf{0.209}$  ( $^{\circ}\text{C}/\text{W}$ )
- $\Delta P = (6.91E-05) \cdot (26)^2 + (3.50E-3) \cdot (26) = \mathbf{0.138}$  (in.  $\text{H}_2\text{O}$ )

## 5.7.2

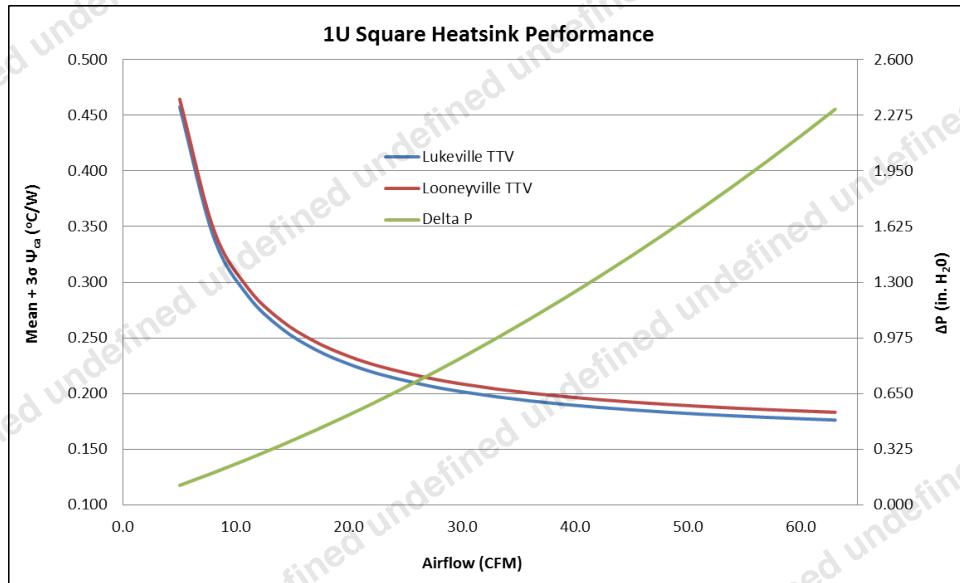
### 1U Square Heatsink Performance

The following performance curves are based on the Intel® Xeon® processor E5-1600 and E5-2600 v3 product families Lukeville and Looneyville thermal test vehicle (TTV). Refer to *Lukeville FCLGA12 Package Thermal/Mechanical Test Vehicle Application Note* for details.

- $\Psi_{CA}(\text{mean})$ ,  $\mu = 0.147 + (1.60914) \cdot (\text{CFM})^{-1.03664}$  ( $^{\circ}\text{C}/\text{W}$ ). This is based on Lukeville TTV
- $\Psi_{CA}(\text{mean})$ ,  $\mu = 0.154 + (1.60914) \cdot (\text{CFM})^{-1.03664}$  ( $^{\circ}\text{C}/\text{W}$ ). This is based on Looneyville TTV



- $\Psi_{CA}$ (variance),  $\sigma = 0.0024$  ( $^{\circ}\text{C}/\text{W}$ )
- $\Delta P = (2.41\text{E}-04) * (\text{CFM})^2 + (2.15\text{E}-02) * (\text{CFM})$  (in.  $\text{H}_2\text{O}$ )



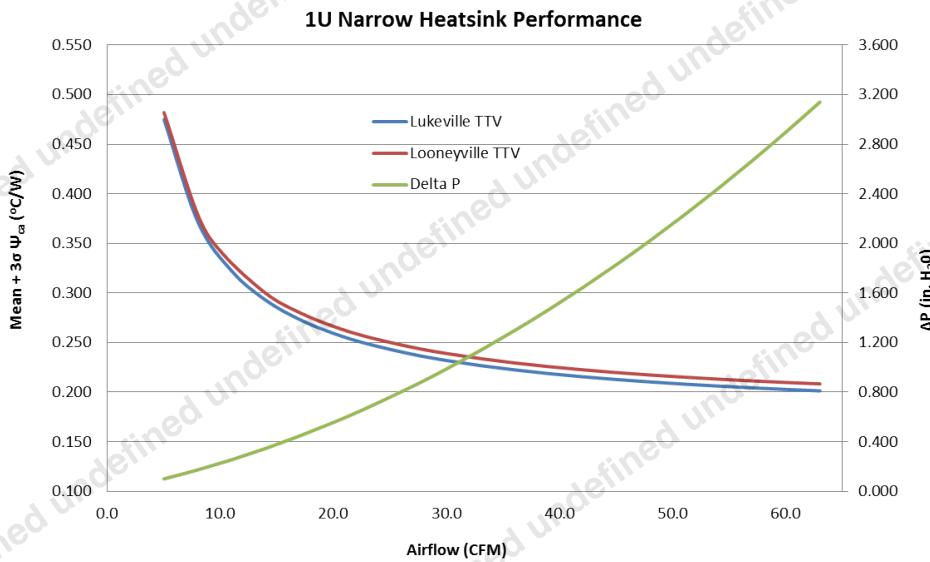
Sample calculation when airflow = 15.2 CFM.

- **$\Psi_{CA}$  Based on Lukeville TTV**
  - $\Psi_{CA}(\mu) = 0.147 + (1.60914) * (15.2)^{-1.03664} = 0.243$  ( $^{\circ}\text{C}/\text{W}$ )
  - $\Psi_{CA}(\mu + 3\sigma) = 0.243 + 3 (0.0024) = \mathbf{0.250}$  ( $^{\circ}\text{C}/\text{W}$ )
- **$\Psi_{CA}$  Based on Looneyville TTV**
  - $\Psi_{CA}(\mu) = 0.154 + (1.60914) * (15.2)^{-1.03664} = 0.250$  ( $^{\circ}\text{C}/\text{W}$ )
  - $\Psi_{CA}(\mu + 3\sigma) = 0.250 + 3 (0.0024) = \mathbf{0.257}$  ( $^{\circ}\text{C}/\text{W}$ )
- **$\Delta P = (2.41\text{E}-04) * (15.2)^2 + (2.15\text{E}-02) * (15.2) = 0.382$  (in.  $\text{H}_2\text{O}$ )**

### 5.7.3 1U Narrow Heatsink Performance

The following performance curves are based on the Intel® Xeon® processor E5-1600 and E5-2600 v3 product families Lukeville and Looneyville thermal test vehicle (TTV). Refer to *Lukeville FCLGA12 Package Thermal/Mechanical Test Vehicle Application Note* for details.

- $\Psi_{CA}$ (mean),  $\mu = 0.151 + (1.254) * (\text{CFM})^{-0.874}$  ( $^{\circ}\text{C}/\text{W}$ ). This is based on Lukeville TTV
- $\Psi_{CA}$ (mean),  $\mu = 0.158 + (1.254) * (\text{CFM})^{-0.874}$  ( $^{\circ}\text{C}/\text{W}$ ). This is based on Looneyville TTV
- $\Psi_{CA}$ (variance),  $\sigma = 0.0056$  ( $^{\circ}\text{C}/\text{W}$ )
- $\Delta P = (5.12\text{E}-04) * (\text{CFM})^2 + (1.76\text{E}-02) * (\text{CFM})$  (in.  $\text{H}_2\text{O}$ )



Sample calculation when airflow = 10.2 CFM.

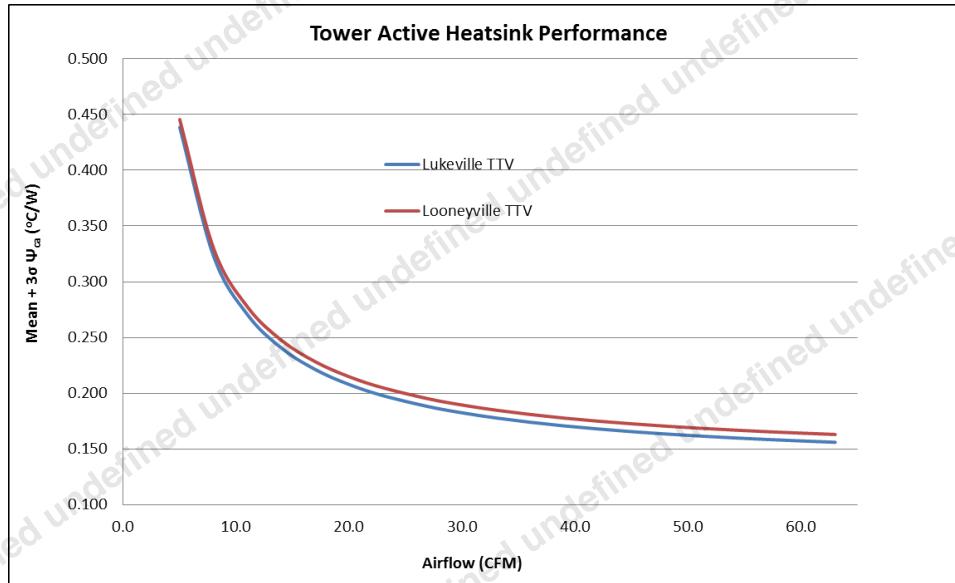
- **Ψ<sub>CA</sub> Based on Lukeville TTV**
  - $\Psi_{CA}(\mu) = 0.151 + (1.254)*(10.2)^{-0.874} = 0.316 \text{ } (\text{°C/W})$
  - $\Psi_{CA}(\mu + 3\sigma) = 0.316 + 3 (0.0056) = \mathbf{0.333 \text{ } (\text{°C/W})}$
- **Ψ<sub>CA</sub> Based on Looneyville TTV**
  - $\Psi_{CA}(\mu) = 0.158 + (1.254)*(10.2)^{-0.874} = 0.323 \text{ } (\text{°C/W})$
  - $\Psi_{CA}(\mu + 3\sigma) = 0.323 + 3 (0.0056) = \mathbf{0.340 \text{ } (\text{°C/W})}$
- **ΔP** =  $(5.12E-04)*(10.2)^2 + (1.76E-02)*(10.2) = \mathbf{0.233 \text{ } (\text{in. H}_2\text{O})}$

## 5.7.4

### Workstation Tower Active Heatsink Performance

The following performance curves are based on the Intel® Xeon® processor E5-1600 and E5-2600 v3 product families Lukeville and Looneyville thermal test vehicle (TTV). Refer to *Lukeville FCLGA12 Package Thermal/Mechanical Test Vehicle Application Note* for details.

- $\Psi_{CA}(\text{mean}), \mu = 0.102 + (1.559)*(CFM)^{-1.011} \text{ } (\text{°C/W})$ . This is based on Lukeville TTV
- $\Psi_{CA}(\text{mean}), \mu = 0.109 + (1.559)*(CFM)^{-1.011} \text{ } (\text{°C/W})$ . This is based on Looneyville TTV
- $\Psi_{CA}(\text{variance}), \sigma = 0.0101 \text{ } (\text{°C/W})$



Sample calculation when airflow = 23.2 CFM.

- **Ψ<sub>CA</sub> Based on Lukeville TTV**
  - $\Psi_{CA}(\mu) = 0.102 + (1.559)*(23.2)^{-1.011} = 0.167 \text{ } (\text{°C/W})$
  - $\Psi_{CA}(\mu + 3\sigma) = 0.167 + 3 (0.0101) = \mathbf{0.197 \text{ } (\text{°C/W})}$
- **Ψ<sub>CA</sub> Based on Looneyville TTV**
  - $\Psi_{CA}(\mu) = 0.109 + (1.254)*(23.2)^{-0.874} = 0.174 \text{ } (\text{°C/W})$
  - $\Psi_{CA}(\mu + 3\sigma) = 0.174 + 3 (0.0101) = \mathbf{0.204 \text{ } (\text{°C/W})}$

## 5.7.5 Mechanical Load Range

Intel's reference heat sinks are thermally validated for the load range described in the [Processor Heatsink Mechanical Targets](#) on page 54.

## 5.7.6 Thermal Interface Material (TIM)

Honeywell PCM45F material was chosen as the interface material for analyzing boundary conditions and processor specifications. The recommended minimum activation load for PCM45F is ~15 PSI [103 kPa]. Meeting the minimum heat sink load targets described in [Processor Heatsink Mechanical Targets](#) on page 54 ensures that this is accomplished. The largest package has a usable area of ~ 2.6 in<sup>2</sup> which translates to a pressure of 19 PSI [131 kPa] at minimum load of 50 lbf [222 N].

Please refer to [Thermal Interface Material \(TIM\)](#) on page 68 which outlines the TIM for Boxed Heat Sinks which may be different.

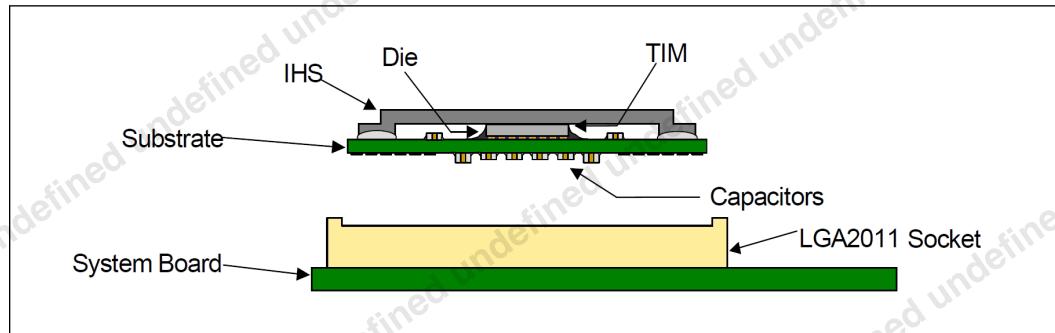
## 6.0 Processor Mechanical Specifications

The processor is packaged in a Flip-Chip Land Grid Array (FCLGA10) package that interfaces with the baseboard via an LGA2011-3 socket. The package consists of a processor mounted on a substrate land-carrier. An integrated heat spreader (IHS) is attached to the package substrate and core and serves as the mating surface for processor component thermal solutions, such as a heatsink. Diagram below shows a sketch of the processor package components and how they are assembled together.

The package components shown below include the following:

1. Integrated Heat Spreader (IHS)
2. Thermal Interface Material (TIM)
3. Processor core (die)
4. Package substrate
5. Capacitors

**Figure 31. Processor Package Assembly Sketch**



**Notes:**

- Socket and baseboard are included for reference and are not part of processor package.
- Processor package land count may be greater than socket contact count

## 6.1 Package Size

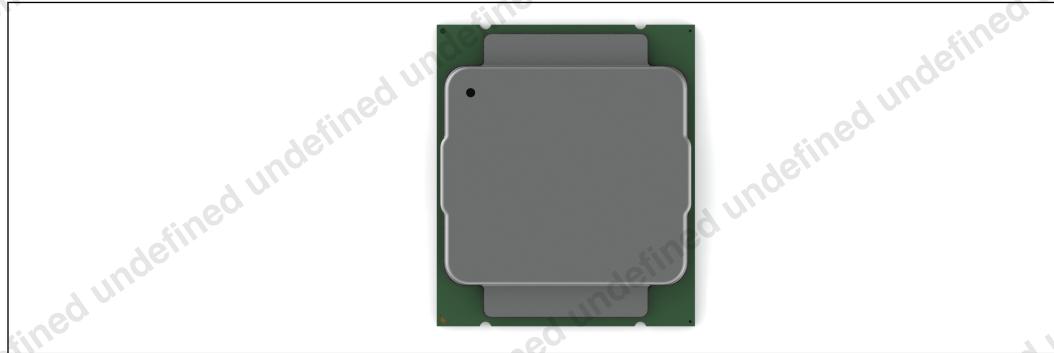
The processor has two different form factors Small and Large. Both form factors are compatible with socket 2011-3 (R3) and the reference ILMs. Size of IHS and dimensions of package substrate vary between the two form factors. For detailed drawings see [Mechanical Drawings](#) on page 78. For Sku specific identification of package for factors see [Processor Thermal Specifications](#) on page 36. All Low Core Count (LCC) and Mid Core Count (MCC) SKUs are Intel® Xeon® processor E5-1600 and E5-2600 v3 product families Small form factor. All High Core Count (HCC) SKUs are Intel® Xeon® processor E5-1600 and E5-2600 v3 product families Large form factor.

Substrate X-Y geometries for each package are:



- Intel® Xeon® processor E5-1600 and E5-2600 v3 product families Small: 52.5mm x 45mm
- Intel® Xeon® processor E5-1600 and E5-2600 v3 product families Large: 52.5mm x 51mm

**Figure 32. Rendering of Intel® Xeon® processor E5-1600 and E5-2600 v3 product families Small Form Factor**



**Figure 33. Rendering of Intel® Xeon® processor E5-1600 and E5-2600 v3 product families Large Form Factor**



## 6.2 Package Loading Specifications

The following table provides load specifications for the processor package. These maximum limits should not be exceeded during heatsink assembly, shipping conditions, or standard use condition. Exceeding these limits during test may result in component failure. The processor substrate should not be used as a mechanical reference or load bearing surface for thermal solutions.



**Table 21.** Processor Loading Specifications

Parameter	Maximum	Notes
Static Compressive Load	1068 N (240 lbf)	This is the maximum static force that can be applied by the heatsink and Independent Loading Mechanism (ILM).
Dynamic Load	540 N (121 lbf)	Dynamic loading is defined as an 11 ms duration average load superimposed on the static load requirement. This load will be a function of the geometry and mass of the enabling components used.
<i>Note:</i> • These specifications apply to uniform compressive loading in a direction normal to the processor IHS.		

## 6.3 Processor Mass Specification

The typical mass of the processor is currently 45 grams. This mass [weight] includes all the components that are included in the package.

## 6.4 Processor Materials

The table below lists some of the package components and associated materials.

**Table 22.**

Processor Materials

Component	Material
Integrated heat Spreader	Nickel Plated Copper
Substrate	Halogen Free, Fiber Reinforced Resin
Substrate lands	Gold Plated Copper

## 6.5 Processor Markings

Labeling locations and information are shown for Intel® Xeon® processor v3 product families Small and Large packages in the diagrams below.



**Figure 34. Small Package Labeling**



**Figure 35.** Large Package Labeling

## 6.6

### Package Handling Guidelines

The processor can be inserted into and removed from a socket 15 times. The following table includes a list of guidelines on package handling in terms of recommended maximum loading on the processor IHS relative to a fixed substrate. These package handling loads may be experienced during heatsink removal.

**Table 23.****Load Limits for Package Handling**

Parameter	Maximum Recommended
Shear	356 N (80 lbf)
Tensile	156 N (35 lbf)
Torque	3.6 N·m (31.5 in-lbf)



## **7.0 Boxed Processor Specifications**

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Intel boxed processors are intended for system integrators who build systems from components available through distribution channels. The Intel® Xeon® processor E5-1600 and E5-2600 v3 product families will be offered as Intel boxed processors. Thermal solutions, however, will be sold separately.

### **7.1 Boxed Processor Thermal Solutions**

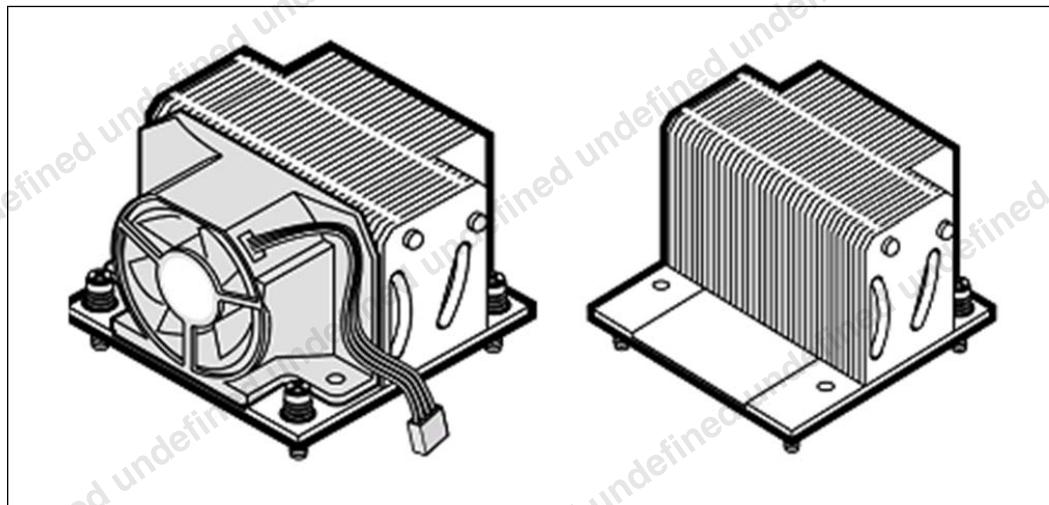
#### **7.1.1 Available Boxed Thermal Solution Configurations**

Intel will offer three different Boxed Heat Sink solutions to support LGA2011-3 Boxed Processors

1. Boxed Intel Thermal Solution STS200C (Order Code BXSTS200C): A Passive / Active Combination Heat Sink Solution that is intended for processors with a 160W TDP or lower in a pedestal or 145W in 2U+ chassis with appropriate ducting.
2. Boxed Intel Thermal Solution STS200P (Order Code BXSTS100P): A 25.5 mm Tall Passive Heat Sink Solution that is intended for processors with a 135W TDP or lower in 1U, or 2U chassis with appropriate ducting. This heat sink is compatible with the square integrated load mechanism (Square ILM). Check with Blade manufacturer for compatibility.
3. Boxed Intel Thermal Solution STS200PNRW (Order Code BXSTS200PNRW): A 25.5 mm Tall Passive Heat Sink Solution that is intended for processors with a 135W TDP or lower in 1U, or 2U chassis with appropriate ducting. This heat sink is compatible with the narrow integrated load mechanism (Narrow ILM). Check with Blade manufacturer for compatibility.

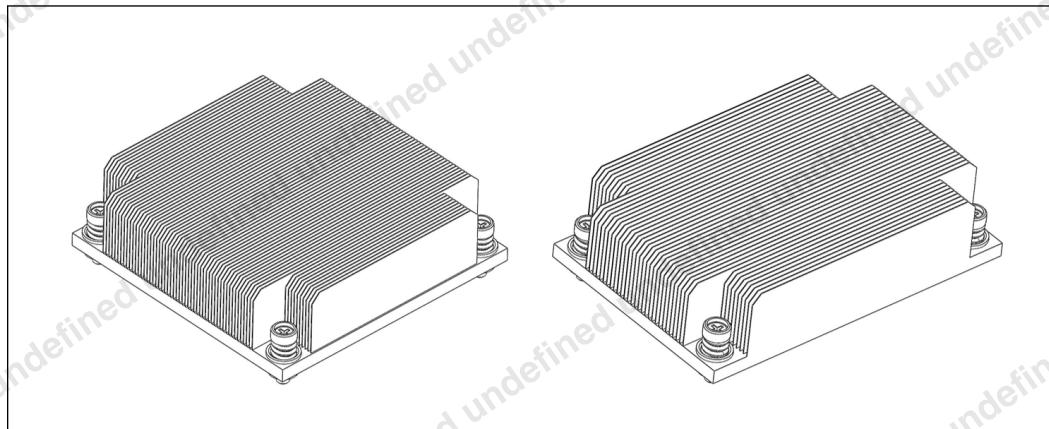
#### **7.1.2 Intel® Thermal Solution STS200C (Passive/Active Combination Heat Sink Solution)**

The STS200C, based on a 2U passive heat sink with a removable fan, is intended for a 160W TDP or lower in active configuration and 145W TDP in passive configuration. This heat pipe-based solution is intended to be used as either a passive heat sink in a 2U or larger chassis, or as an active heat sink for pedestal chassis. Although the active combination solution with the fan installed mechanically fits into a 2U keepout, its use has not been validated in that configuration. The active fan configuration is primarily designed to be used in a pedestal chassis where sufficient air inlet space is present. The STS200C with the fan removed, as with any passive thermal solution, will require the use of chassis ducting and is targeted for use in rack mount or ducted-pedestal servers. The recommended retention for these heat sinks is the Square ILM. Refer to [Intel® ILM Reference Designs](#) on page 28 for more info.

**Figure 36. STS200C Active / Passive Combination Heat Sink (with Removable Fan)**

### 7.1.3 Intel® Thermal Solution STS200P and STS200PNRW (Boxed 25.5 mm Tall Passive Heat Sink Solutions)

The STS200P and STS200PNRW are available for use with boxed processors that have a 135W TDP and lower. These 25.5 mm tall passive solutions are designed to be used in SSI Blades, 1U, and 2U chassis where ducting is present. The use of a 25.5 mm tall heatsink in a 2U chassis is recommended to achieve a lower heatsink  $T_{LA}$  and more flexibility in system design optimization. The recommended retention for the STS200P is the Square ILM. The recommended retention for the STS200PNRW is the Narrow ILM. Refer to [Intel® ILM Reference Designs](#) on page 28 for more info.

**Figure 37. STS200P and STS200PNRW 25.5 mm Tall Passive Heat Sinks**

### 7.1.4 Thermal Interface Material (TIM)

These heat sinks will come pre-applied with Dow Corning TC-1996. Please consult your Intel representative or Dow Corning for more information.



## 7.2

## Boxed Processor Cooling Requirements

Meeting the processor's temperature specifications is a function of the thermal design of the entire system. The processor temperature specifications are found in [Processor Thermal Specifications](#) on page 36 of this document. Meeting the processor's temperature specification is the responsibility of the system integrator.

### STS200C (Passive/Active Combination Heat Sink Solution)

The active configuration should help meet the thermal processor requirements particularly for pedestal chassis designs. Some form of ducting is recommended to meet memory cooling and processor  $T_{LA}$  temperature requirements. Use of the active configuration in a 2U rack mount chassis is not recommended, however.

In the passive configuration a chassis duct should be implemented.

The active solution can be used with a 160W TDP or lower. The passive solution can be used with a 145W TDP or lower.

### STS200P and STS200PNRW (25.5 mm Tall Passive Heat Sink Solution)

These passive solutions are intended for use in SSI Blade, 1U or 2U rack configurations. It is assumed that a chassis duct will be implemented in all configurations.

These thermal solutions should be used with a 135W TDP or lower.

For a list of processor and thermal solution boundary conditions for common layouts, such as  $\Psi_{ca}$ ,  $T_{LA}$ , airflow, flow impedance, please refer to the section on [Processor Boundary Conditions for Shadowed and Spread Core Layouts](#) on page 47.

## 7.3

## Mechanical Specifications

### Boxed Processor Heat Sink Dimensions and Baseboard Keepout Zones

The boxed heat sink (thermal solution) is sold separately from the boxed processor. Clearance is required around the thermal solution to ensure unimpeded airflow for proper cooling. Baseboard keepout zones are shown in [Mechanical Drawings](#) on page 78 which detail the physical space requirements for each of the boxed heat sinks.

None of the heat sink solutions exceed a mass of 550 grams. See [Package Loading Specifications](#) on page 63 for processor loading specifications.

### Boxed Heat Sink Support with ILM

Baseboards designed for Intel® Xeon® processor E5-1600 and E5-2600 v3 product families processors should include holes that are aligned with the ILM. Please refer to [Independent Loading Mechanism \(ILM\) Specifications](#) on page 23 chapter for more information.

Boxed heat sinks will require a #2 Phillips screwdriver to attach to the ILM. The screws should be tightened until they no longer turn easily. This is approximately 8 inch-pounds [0.90 N·m]. Exceeding this recommendation may damage the screw or other components.

Please refer the Grantley Manufacturing Advantage Service Document.



## 7.4

### Fan Power Supply [STS200C]

The 4-pin PWM controlled thermal solution is offered to help provide better control over pedestal chassis acoustics. Fan RPM is modulated through the use of an ASIC located on the baseboard that sends out a PWM control signal to the 4th pin of the connector labeled as Control. This thermal solution requires a constant +12 V supplied to pin 2 of the active thermal solution and does not support variable voltage control or 3-pin PWM control.

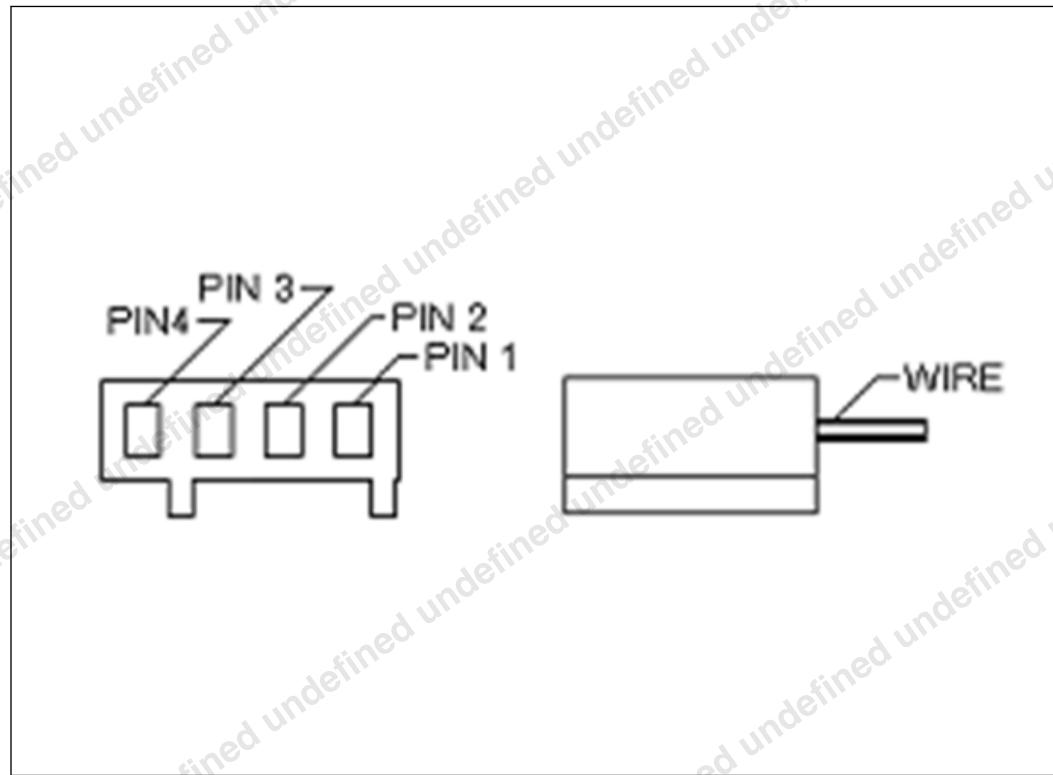
The fan power header on the baseboard must be positioned to allow the fan heat sink power cable to reach it. The fan power header identification and location must be documented in the suppliers platform documentation, or on the baseboard itself. The baseboard fan power header should be positioned within 7 in. [177.8 mm] from the center of the processor socket.

Description	Min Frequency	Nominal Frequency	Max Frequency	Unit
PWM Control Frequency Range	21,000	25,000	28,000	Hz

Description	Min	Typical Steady	Max Steady	Max Startup	Unit
+12 V: 12 volt fan power supply	10.8	12	12	13.2	V
IC: Fan Current Draw	N/A	1.25	1.5	2.2	A
SENSE: SENSE frequency	2	2	2	2	Pulses per fan revolution



Figure 38. Fan Cable Connector Pin Out for 4-Pin Active Thermal Solution



Pin Number	Signal	Color
1	Ground	Black
2	<b>Power: (+12 V)</b>	Yellow
3	<b>SENSE:</b> 2 pulses per revolution	Green
4	<b>Control:</b> 21 - 28 KHz	Blue

## 7.5

### Boxed Processor Contents

The Boxed Processor and Boxed Thermal Solution contents are outlined below.

#### Boxed Processor

- Intel® Xeon® processor E5-1600 and E5-2600 v3 product families
- Installation and warranty manual
- Intel Inside® Logo

#### Boxed Thermal Solution

- Thermal solution assembly
- Thermal interface material (pre-applied)
- Installation and warranty manual



## 8.0 Quality Reliability and Ecological Requirements

### 8.1 Use Conditions

Intel evaluates reliability performance based on the use conditions (operating environment) of the end product by using acceleration models.

The use condition environment definitions provided in the tables below are based on speculative use condition assumptions, and are provided as examples only.

Based on the system enabling boundary condition, the solder ball temperature can vary and needs to be comprehended for reliability assessment.

Use Environment	Speculative Stress Condition	Example Use Condition	Example 7 yr. Stress Equivalent	Example 10 yr. Stress Equivalent
Slow small internal gradient changes due to external ambient (temperature cycle or externally heated) Fast, large gradient on/off to max operating temp. (power cycle or internally heated including power save features)	Temperature Cycle	D T = 35 - 44°C (solder joint)	550-930 cycles Temp Cycle (-25°C to 100°C)	780-1345 cycles Temp Cycle (-25°C to 100°C)
High ambient moisture during low-power state (operating voltage)	THB/HAST	T = 25 -30°C 85%RH (ambient)	110-220 hrs at 110°C 85%RH	145-240 hrs at 110°C 85%RH
High Operating temperature and short duration high temperature exposures	Bake	T = 95 - 105°C (contact)	700 - 2500 hrs at 125°C	800 - 3300 hrs at 125°C

Use Environment	Speculative Stress Condition		Example Use Condition
Shipping and Handling	<u>Mechanical Shock</u> <ul style="list-style-type: none"><li>• System-level</li><li>• Unpackaged</li><li>• Trapezoidal</li><li>• 25 g</li><li>• velocity change is based on packaged weight</li></ul>		Total of 12 drops per system: <ul style="list-style-type: none"><li>• 2 drops per axis</li><li>• ± direction</li></ul>
	Product Weight (lbs) < 20 lbs 20 to > 40 40 to > 80 80 to < 100 100 to < 120 ≥120	Non-palletized Product Velocity Change (in/sec) 250 225 205 175 145 125	
Change in velocity is based upon a 0.5 coefficient of restitution.			
Shipping and	<u>Random Vibration</u> <ul style="list-style-type: none"><li>• System Level</li></ul>	Total per system: <ul style="list-style-type: none"><li>• 10 minutes per axis</li></ul>	

*continued...*



Use Environment	Speculative Stress Condition		Example Use Condition
Handling	<ul style="list-style-type: none"> <li>• Unpackaged</li> <li>• 5 Hz to 500 Hz</li> <li>• 2.20 g RMS random</li> <li>• 5 Hz @ 0.001 g<sup>2</sup>/Hz to 20 Hz @ 0.01 g<sup>2</sup>/Hz (slope up)</li> <li>• 20 Hz to 500 Hz @ 0.01 g<sup>2</sup>/Hz (flat)</li> <li>• Random control limit tolerance is ± 3 dB</li> </ul>	<ul style="list-style-type: none"> <li>• 3 axes</li> </ul>	

## 8.2

## Intel® Reference Component Validation

Intel tests reference components individually and as an assembly on mechanical test boards and assesses performance to the envelopes specified in previous sections by varying boundary conditions.

While component validation shows a reference design is tenable for a limited range of conditions, customers need to assess their specific boundary conditions and perform reliability testing based on their use conditions.

Intel reference components are also used in board functional tests to assess performance for specific conditions.

### 8.2.1

### Board Functional Test Sequence

Each test sequence should start with components (baseboard, heatsink assembly, and so on) that have not previously endured any reliability testing.

Prior to the mechanical shock and vibration test, the units under test should be preconditioned for 72 hours at 45°C. The purpose is to account for load relaxation during burn-in stage.

The test sequence should always start with a visual inspection after assembly, and BIOS/processor/memory test. The stress test should be then followed by a visual inspection and then BIOS/processor/memory test.

### 8.2.2

### Post-Test Pass Criteria Examples

The post-test pass criteria examples are:

1. No significant physical damage to the heatsink and retention hardware.
2. Heatsink remains seated and its bottom remains mated flat against the IHS surface. No visible gap between the heatsink base and processor IHS. No visible tilt of the heatsink with respect to the retention hardware.
3. No signs of physical damage on baseboard surface due to impact of heatsink.
4. No visible physical damage to the processor package.
5. Successful BIOS/Processor/memory test of post-test samples.
6. Thermal compliance testing to demonstrate that the case temperature specification can be met.



### 8.2.3

### Recommended BIOS/Processor/Memory Test Procedures

This test is to ensure proper operation of the product before and after environmental stresses, with the thermal mechanical enabling components assembled. The test shall be conducted on a fully operational baseboard that has not been exposed to any battery of tests prior to the test being considered.

Testing setup should include the following components, properly assembled and/or connected:

- Appropriate system baseboard,
- Processor and memory,
- All enabling components, including socket and thermal solution parts.

The pass criterion is that the system under test shall successfully complete the checking of BIOS, basic processor functions and memory, without any errors. Intel PC Diags is an example of software that can be utilized for this test.

## 8.3

## Material and Recycling Requirements

Material shall be resistant to fungal growth. Examples of non-resistant materials include cellulose materials, animal and vegetable based adhesives, grease, oils, and many hydrocarbons. Synthetic materials such as PVC formulations, certain polyurethane compositions (for example, polyester and some polyethers), plastics which contain organic fillers of laminating materials, paints, and varnishes also are susceptible to fungal growth. If materials are not fungal growth resistant, then MIL-STD-810E, Method 508.4 must be performed to determine material performance. Cadmium shall not be used in the painting or plating of the socket. CFCs and HFCs shall not be used in manufacturing the socket.

Any plastic component exceeding 25 gm should be recyclable per the European Blue Angel recycling standards.

Supplier is responsible for complying with industry standards regarding environmental care as well as with the specific standards required per supplier's region. More specifically, supplier is responsible for compliance with the European regulations related to restrictions on the use of Lead and Bromine containing flame-retardants. Legislation varies by geography, European Union (RoHS/WEEE), China, California, and so forth.

The following definitions apply to the use of the terms lead-free, Pb-free, and RoHS compliant.

**Halogen flame retardant free (HFR-Free) PCB:** Current guidance for the socket pad layout supports FR4 and HFR-Free designs. In future revisions of this document, Intel will be providing guidance on the mechanical impact to using a HFR-free laminate in the PCB. This will be limited to workstations.

**Lead-free and Pb-free:** Lead has not been intentionally added, but lead may still exist as an impurity below 1000 ppm.

**RoHS compliant:** Lead and other materials banned in RoHS Directive are either (1) below all applicable substance thresholds as proposed by the EU or (2) an approved/pending exemption applies.



**Note:** RoHS implementation details are not fully defined and may change.



## Appendix A Component Suppliers

Customers can purchase the Intel reference or collaboration thermal solutions from the suppliers listed in the following table.

**Table 24. Intel® Reference or Collaboration Thermal Solutions**

Item	Intel Part Number	Supplier PN	Delta Supplier Contact Info	Foxconn Supplier Contact Info
1U Square Heatsink Assy with TIM (91.5x91.5x25.5)	E89205-001	contact supplier	Jason Tsai Delta Products Corp Portland, Oregon jtsai@delta-corp.com 971-205-7074	Cary Huang 黃寬裕 Foxconn Technology Co, Inc. 2525 Brockton Dr., Suite 300 Austin, TX 78758 Phone: 512-670-2638 cary.huang@foxconn.com
1U Narrow Heatsink Assy with TIM (70x106x25.5)	G16539-001	contact supplier		
2U Active/Combo Heatsink Assy w/TIM, Fan Guard	E62452-004	contact supplier		
Delrin eRing retainer	G13624-001	FT1008-A	ITW Electronics Business Asia Co., Ltd.	Chak Chakir chak.chakir@itweba.com 512-989-7771
Thermal Interface Material (TIM)	N/A	PCM45F	Honeywell	Judy Oles judy.oles@honeywell.com +1-509-252-8605
		TC-5022	Dow Corning	Ed Benson e.benson@dowcorning.com +1-617-803-6174

Customers can purchase the Intel LGA2011-3 sockets and reference LGA2011-3 ILMs from the suppliers listed in the following table.

**Table 25. LGA2011-3 Socket and ILM Components**

Item	Intel PN	Foxconn (Hon Hai)	Tyco	Lotes	Amtek	Molex
LGA 2011-3 Socket POR	G64443-001	PE201127-435 5-01H	2201838-1	AZIF0001-P004C	NA	NA
LGA 2011-3 Square ILM	G63449-005	PT44L11-4711	2229339-2	AZIF0018-P001C	ITLG63449001	105274-2000
LGA 2011-3 Narrow ILM	G43051-006	PT44L12-4711	2229339-1	AZIF0019-P001C	ITLG43051002	105274-1000
LGA 2011-3 Backplate	E91834-001	PT44P41-4401	2134440-1	DCA-HSK-182-T02	ITLE91834001	105142-7000
Supplier Contact Info		Eric Ling	Alex Yeh	Cathy Yang	Alvin Yap	Edmund Poh

*continued...*



Item	Intel PN	Foxconn (Hon Hai)	Tyco	Lotes	Amtek	Molex
		eric.ling@foxconn.com 503-693-3509 x225	alex.yeh@te.com Tel: +886-2-21715 280	Cathy@lotes.com.cn Tel: +1-86-20-8468 6519 x219	alvinyap@amtek.com.cn Tel +(86)752-2634 562 Cathy Yu cathy_yu@amtek.com.cn Tel +(86)752-2616 809	edmund.poh@molex.com Tel +1-630-718-5416



## Appendix B Mechanical Drawings

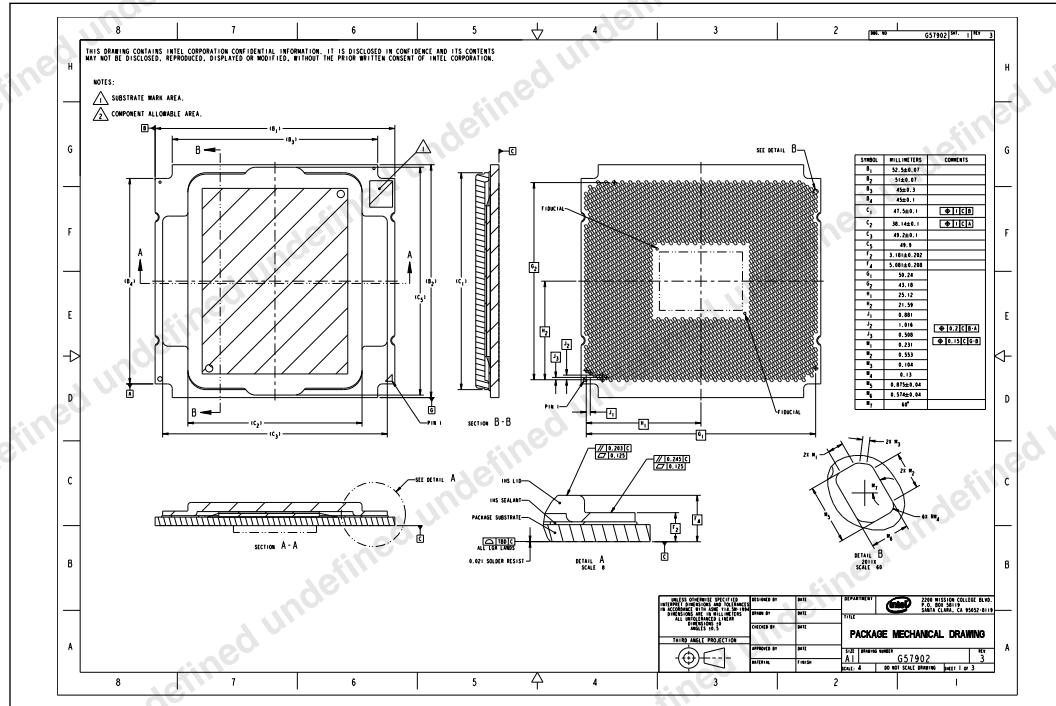
The following sections contain mechanical drawings of reference retention designs, processor package geometry and reference heat sink designs.

**Table 26. List of Mechanical Drawings**

<a href="#">Package Mechanical Drawing Page 1</a> on page 81
<a href="#">Large Package Mechanical Drawing Page 2</a> on page 80
<a href="#">Package Mechanical Drawing Page 1</a> on page 81
<a href="#">Package Mechanical Drawing Page 2</a> on page 82
<a href="#">ILM Backplate Keep Out Zone</a> on page 83
<a href="#">ILM Mounting Hole Keep Out Zone</a> on page 84
<a href="#">Narrow ILM Keep Out Zone</a> on page 85
<a href="#">Narrow ILM 3D Keep Out Zone</a> on page 86
<a href="#">ILM Keep Out Zone</a> on page 87
<a href="#">3D Keep Out Zone</a> on page 88
<a href="#">Heat Sink Retaining Ring</a> on page 89
<a href="#">Heat Sink Spring</a> on page 90
<a href="#">1U Narrow Heat Sink Geometry (Page 1)</a> on page 92
<a href="#">1U Narrow Heat Sink Geometry (Page 2)</a> on page 93
<a href="#">1U Narrow Heat Sink Assembly (Page 1)</a> on page 94
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<a href="#">1U Square Heat Sink Geometry (Page 1)</a> on page 96
<a href="#">1U Square Heat Sink Geometry (Page 2)</a> on page 97
<a href="#">1U Square Heat Sink Assembly (Page 1)</a> on page 98
<a href="#">1U Square Heat Sink Assembly (Page 2)</a> on page 99
<a href="#">2U Square Heat Sink Geometry (Page 1)</a> on page 100
<a href="#">2U Square Heat Sink Geometry (Page 2)</a> on page 101
<a href="#">2U Square Heat Sink Assembly (Page 1)</a> on page 102
<a href="#">2U Square Heat Sink Assembly (Page 2)</a> on page 103

**B.1****Large Package Mechanical Drawing Page 1**

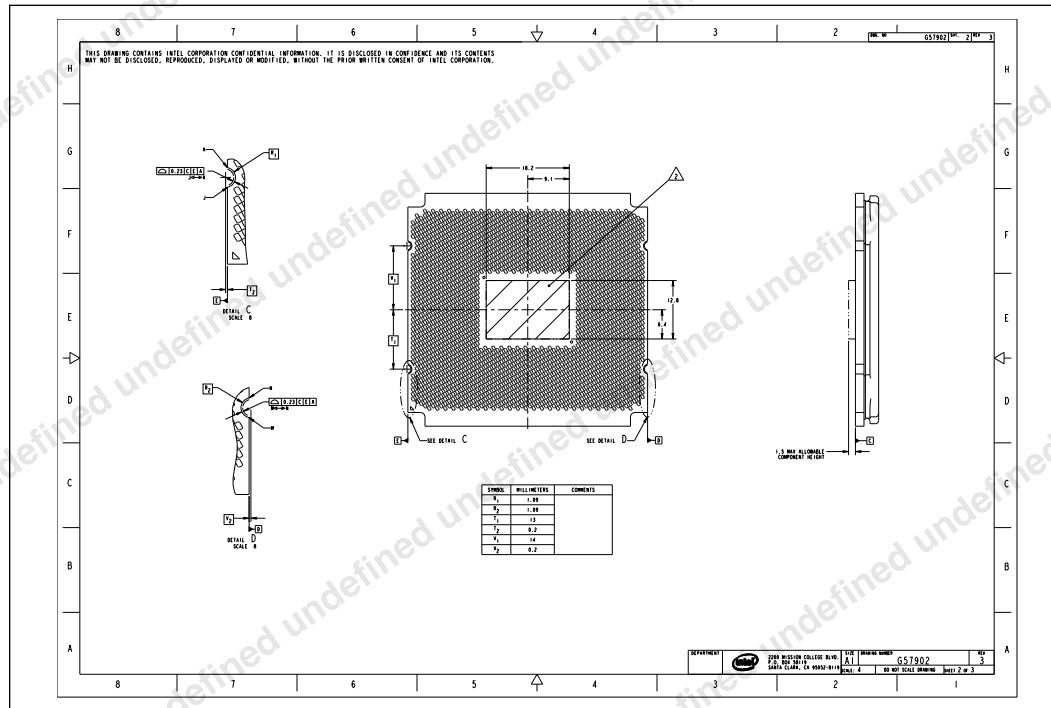
**Figure 39.** Intel® Xeon® Processor v3 Product Families Large Package Mechanical Drawing Page 1





## B.2 Large Package Mechanical Drawing Page 2

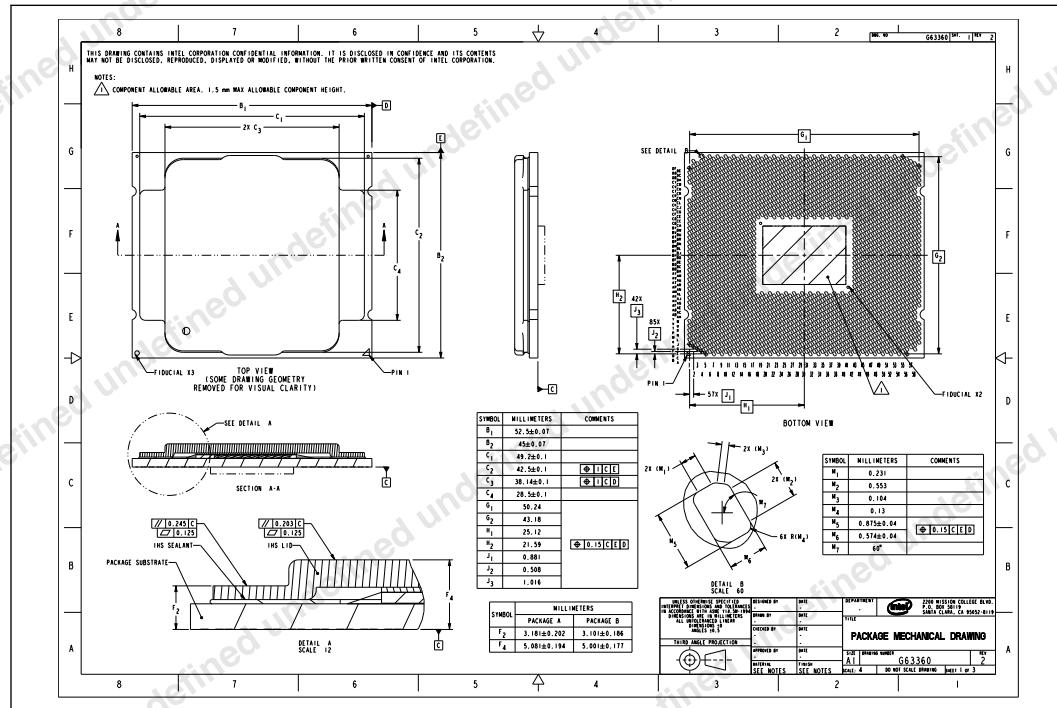
**Figure 40.** Intel® Xeon® Processor v3 Product Families Large Package Mechanical Drawing Page 2





## B.3 Package Mechanical Drawing Page 1

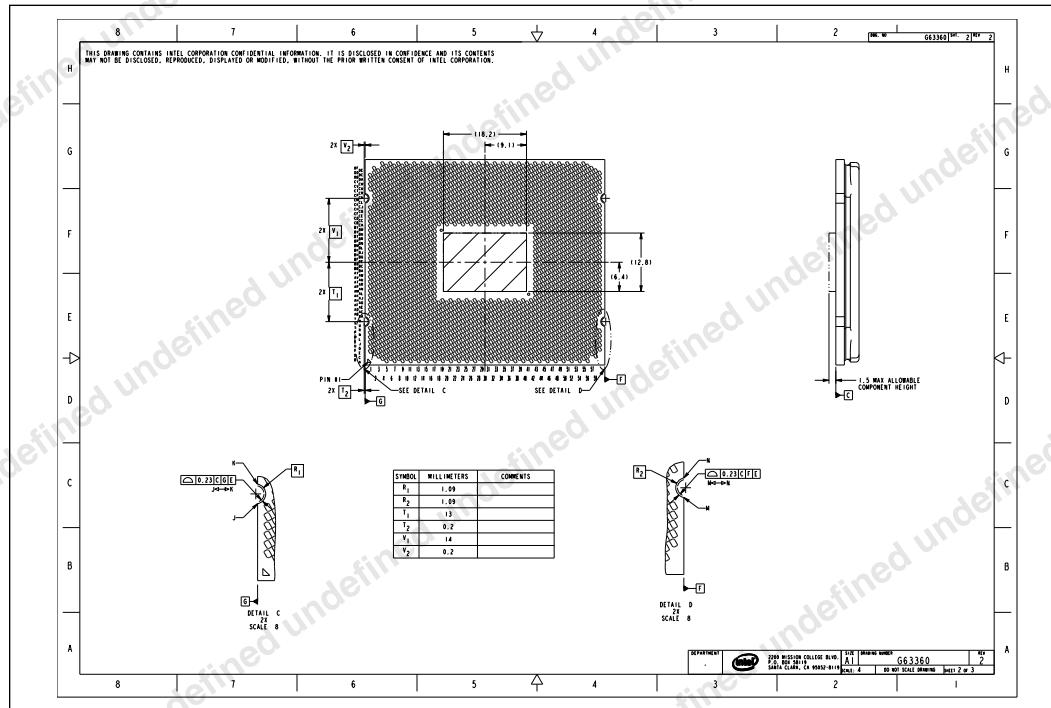
**Figure 41. Intel® Xeon® Processor v3 Product Families Small Package Mechanical Drawing Page 1**





## B.4 Package Mechanical Drawing Page 2

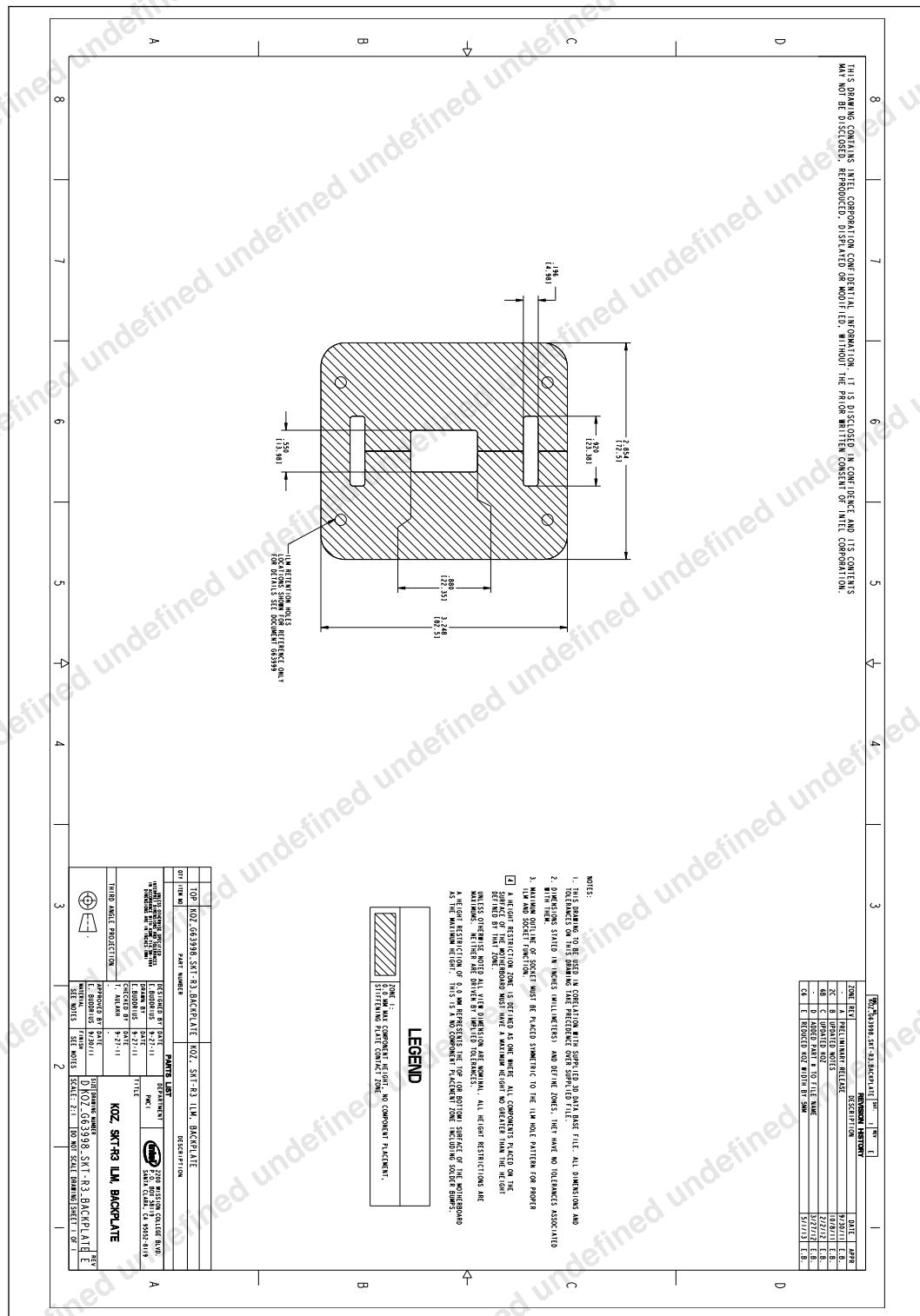
**Figure 42.** Intel® Xeon® Processor v3 Product Families Small Package Mechanical Drawing Page 2





## B.5 ILM Backplate Keep Out Zone

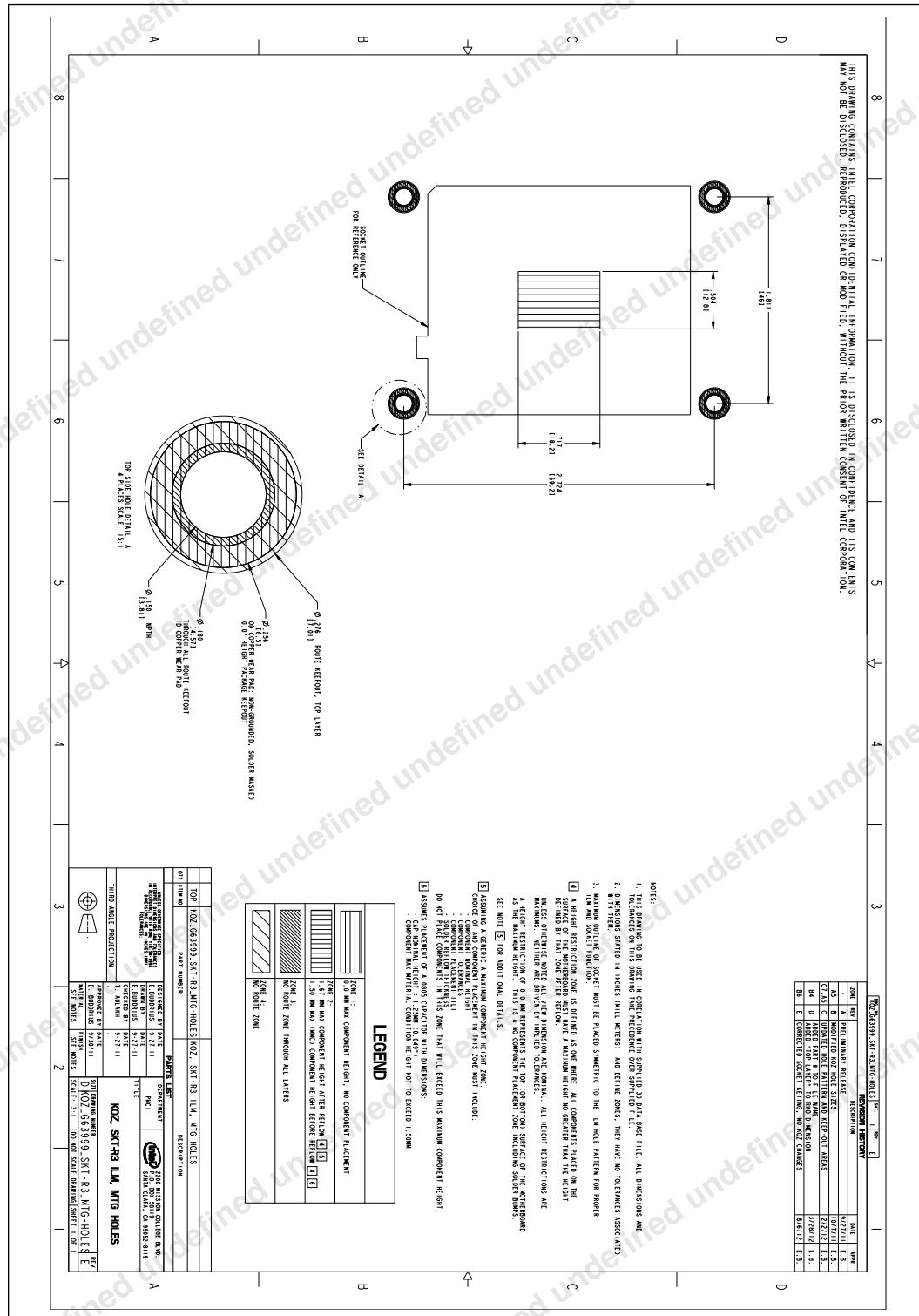
**Figure 43.** ILM Backplate Keep Out Zone





## B.6 ILM Mounting Hole Keep Out Zone

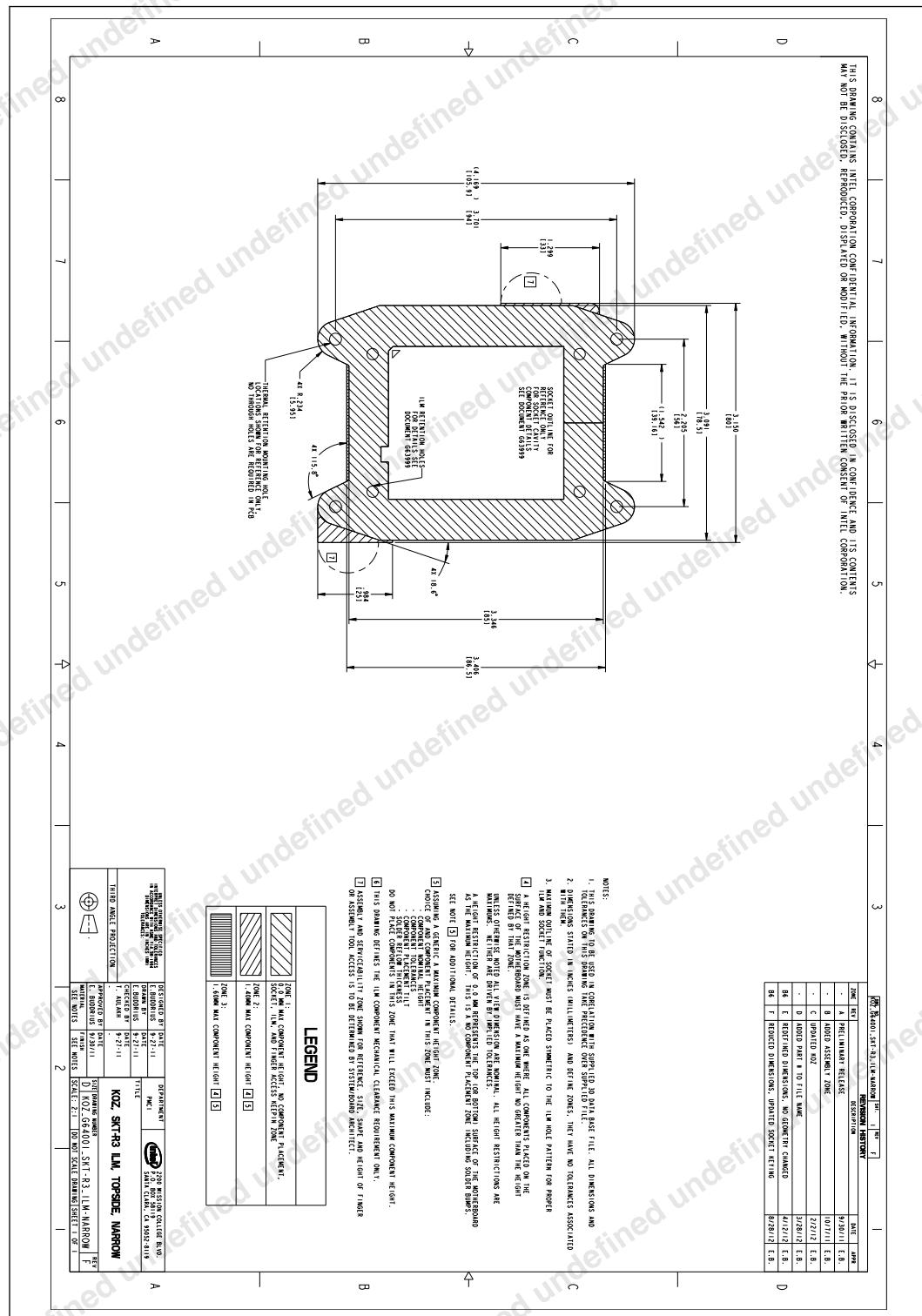
**Figure 44. ILM Mounting Hole Keep Out Zone**





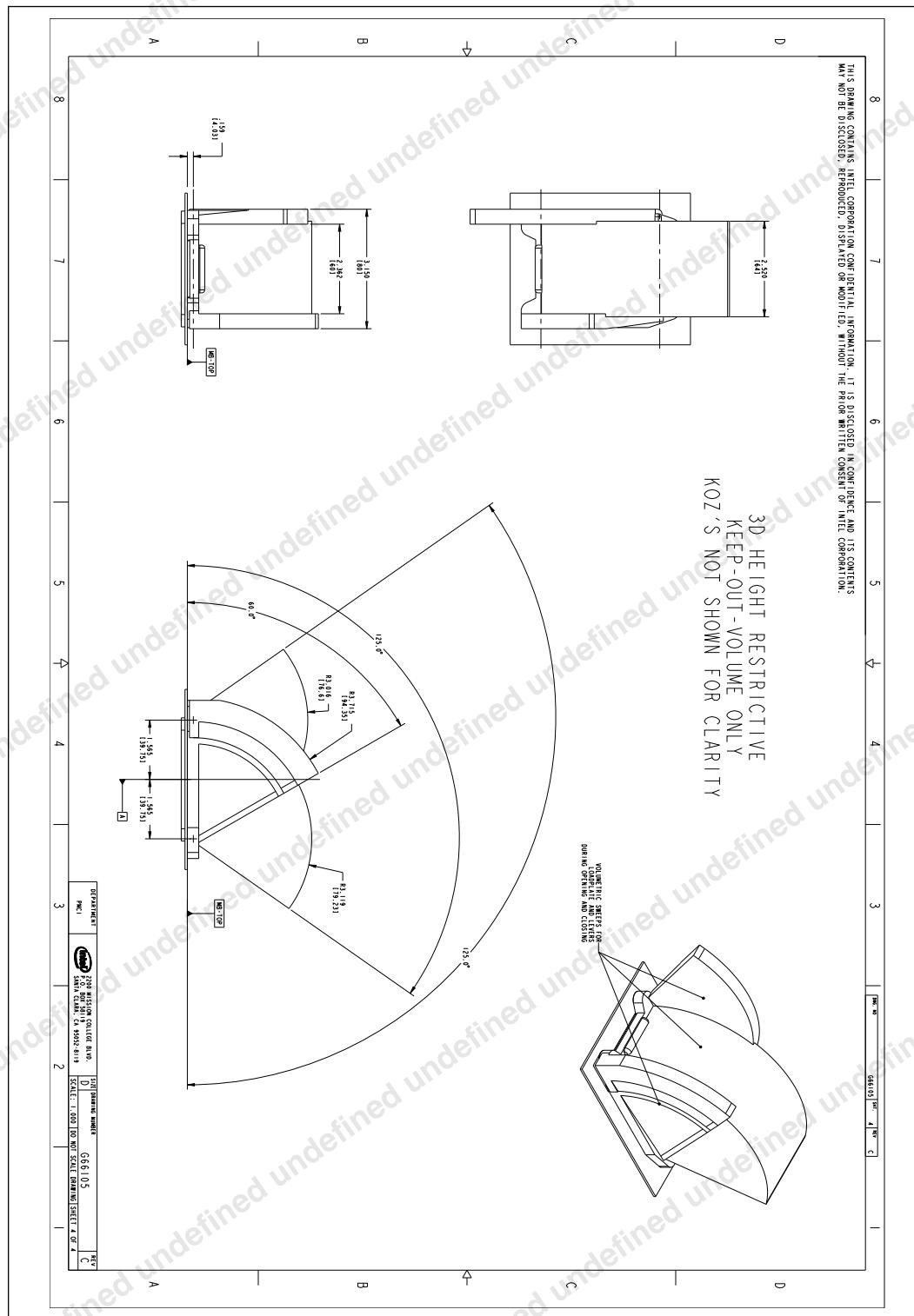
## B.7 Narrow ILM Keep Out Zone

**Figure 45. Narrow ILM Keep Out Zone**



## B.8 Narrow ILM 3D Keep Out Zone

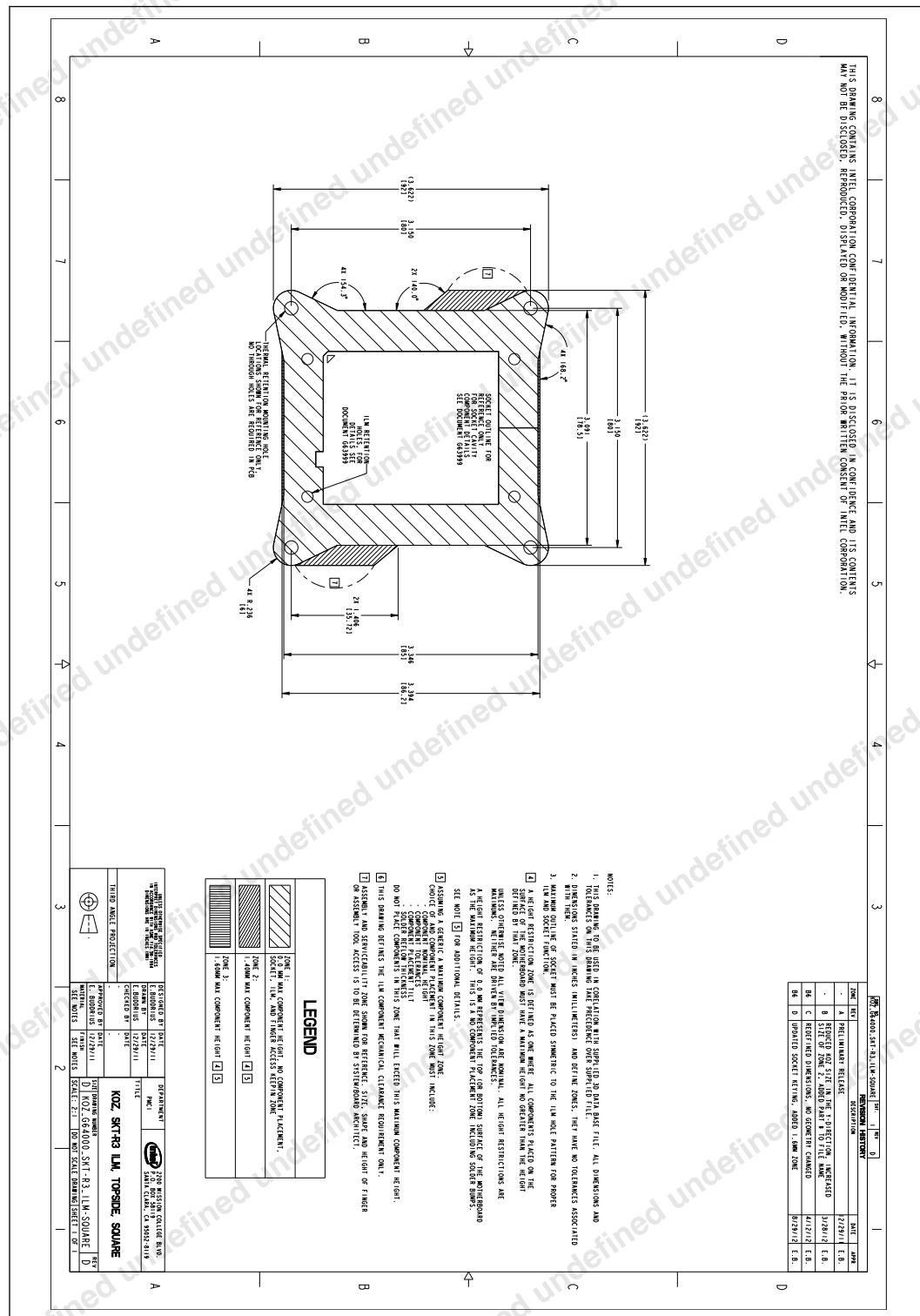
**Figure 46.** **Narrow ILM 3D Keep Out Zone**





## B.9 ILM Keep Out Zone

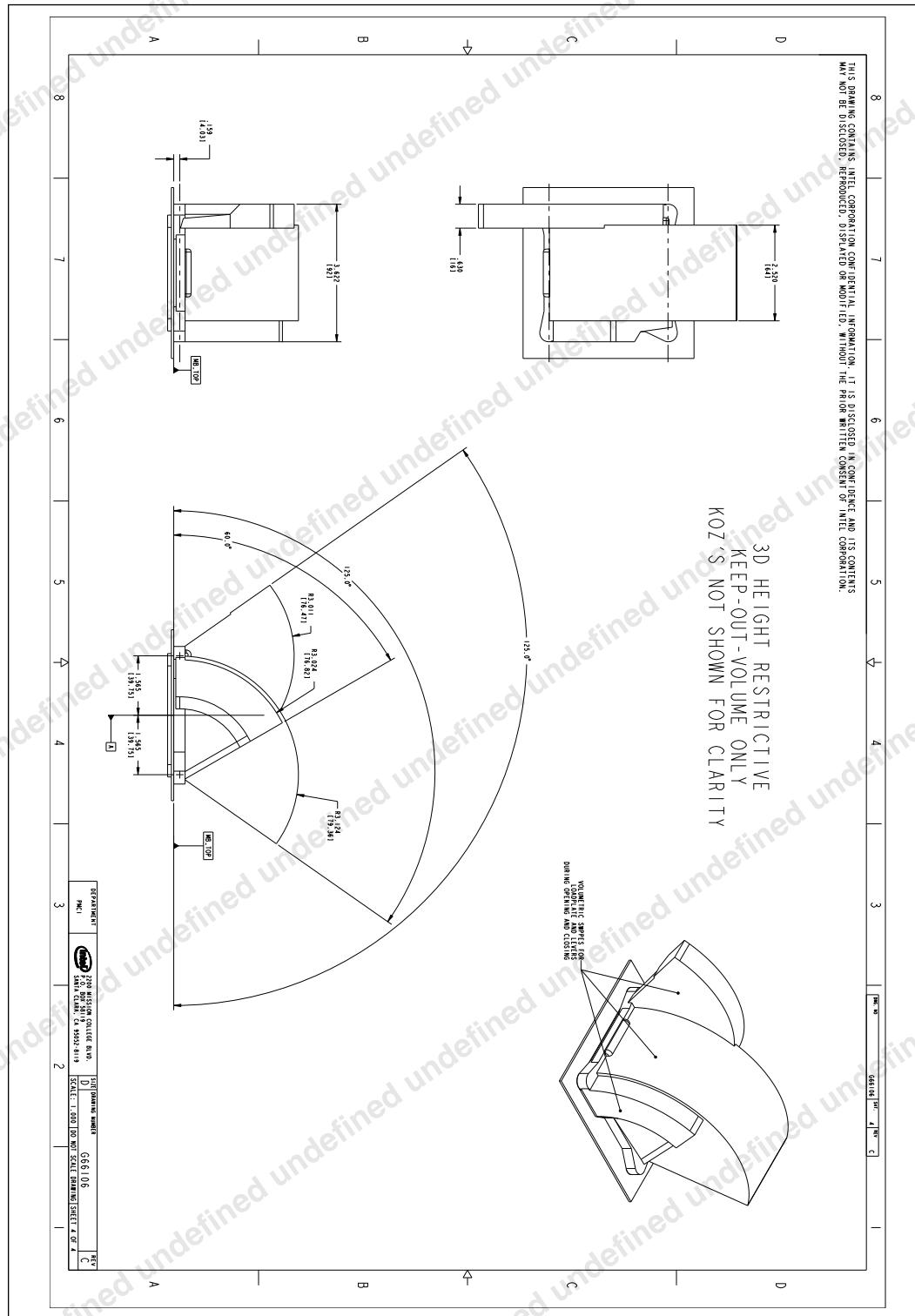
**Figure 47.** Square ILM Keep Out Zone





## B.10 3D Keep Out Zone

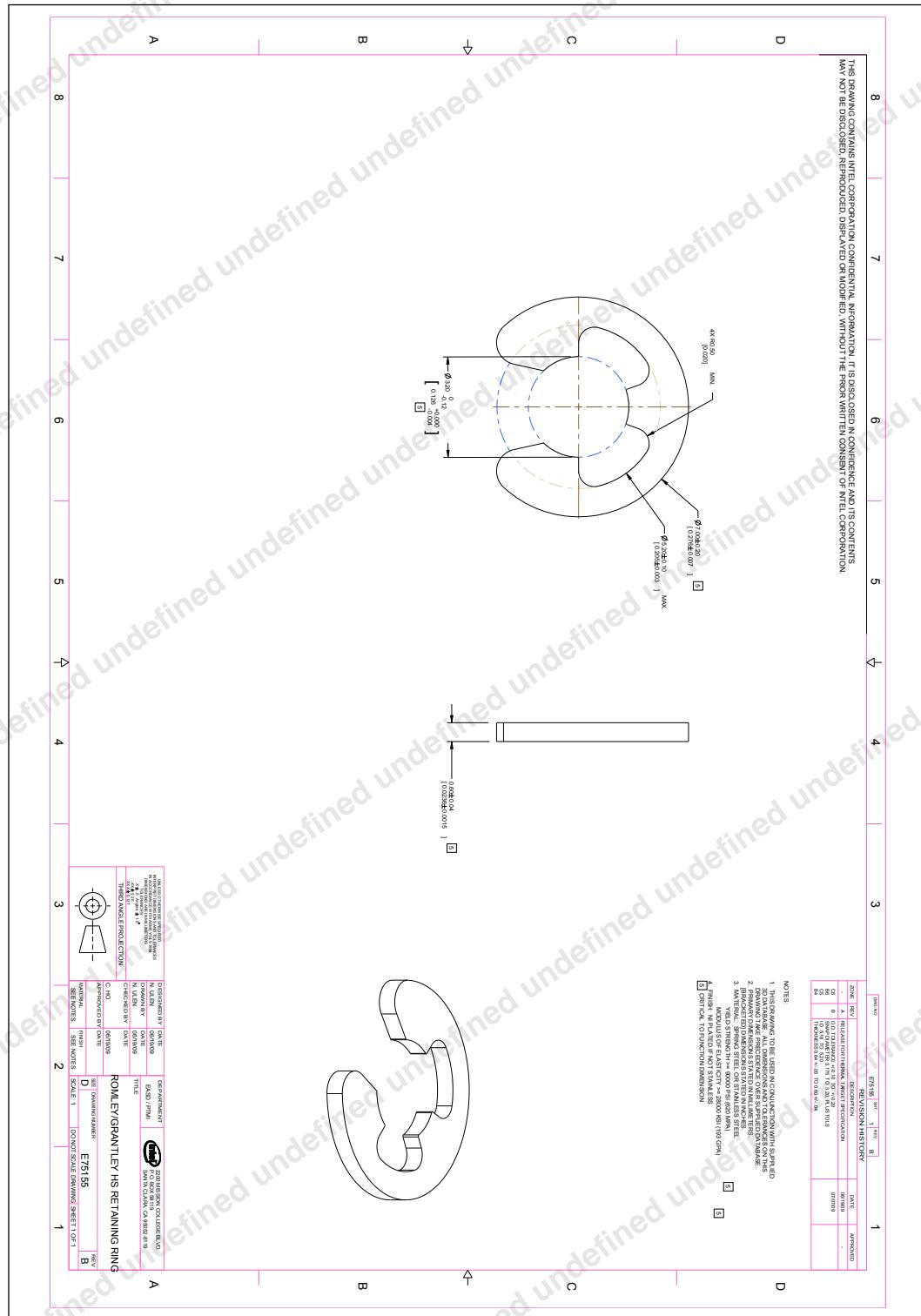
Figure 48. Square 3D Keep Out Zone





## B.11 Heat Sink Retaining Ring

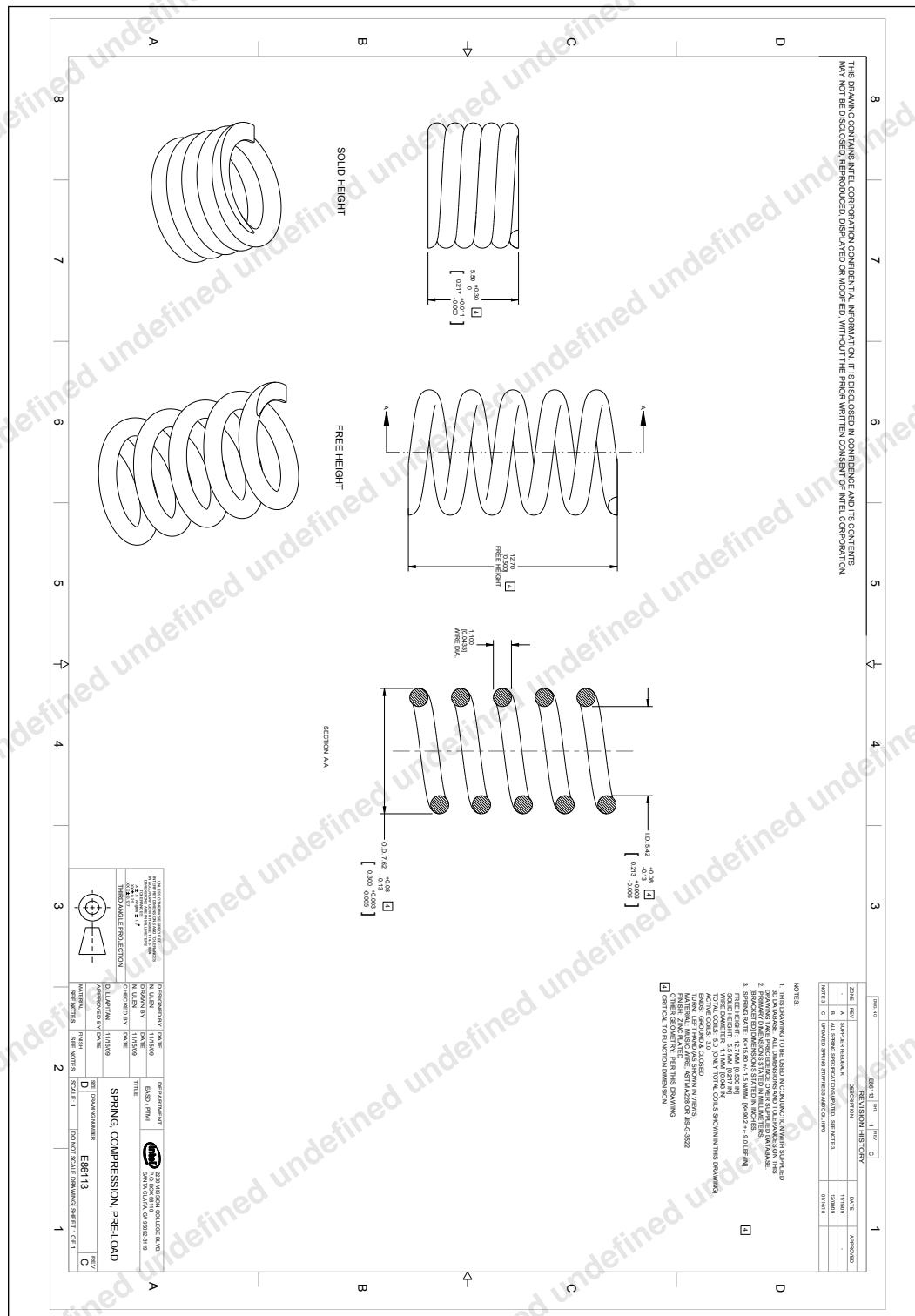
**Figure 49.** Heat Sink Retaining Ring





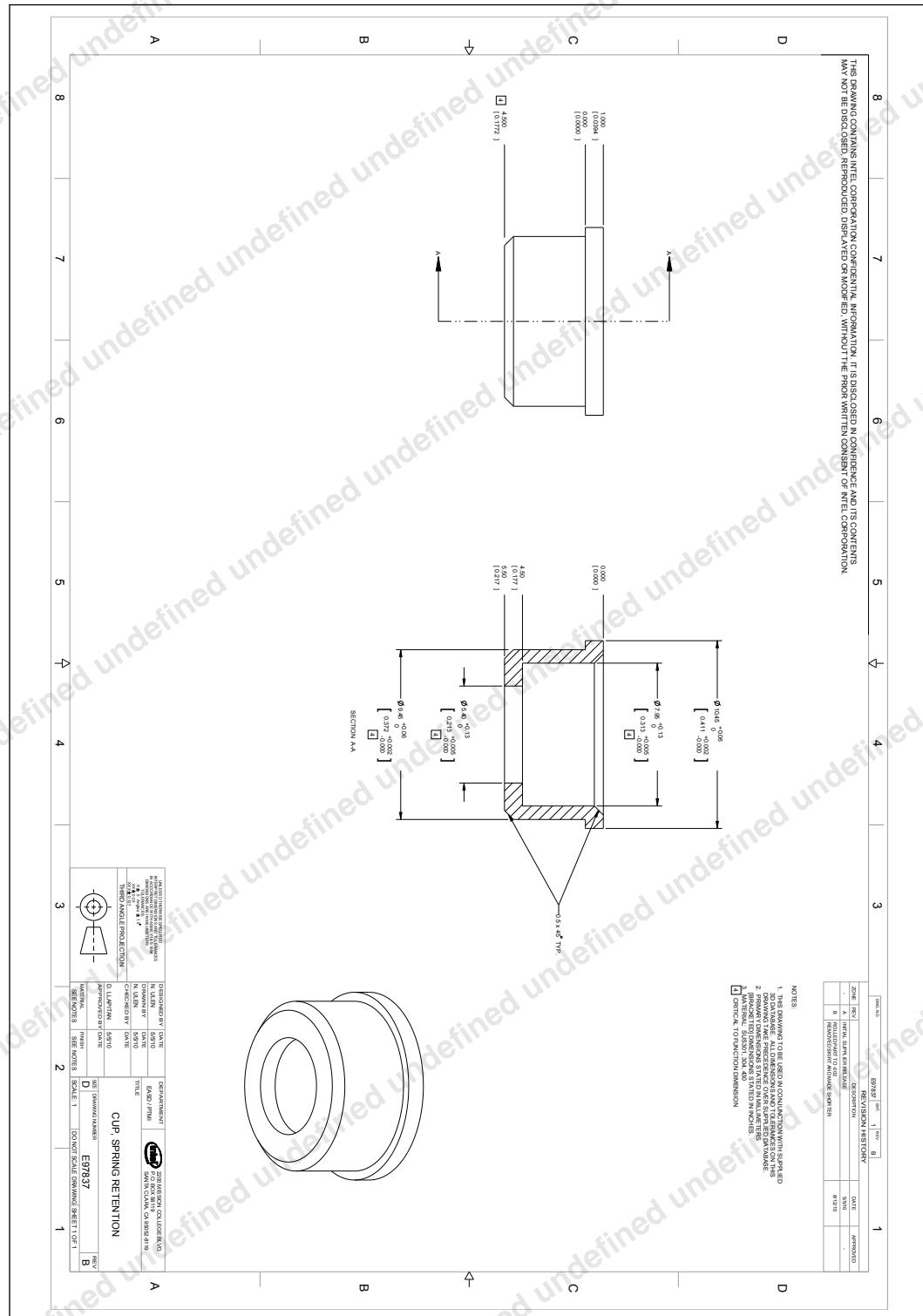
## B.12 Heat Sink Spring

Figure 50. Heat Sink Spring



## B.13 Heat Sink Spring Cup

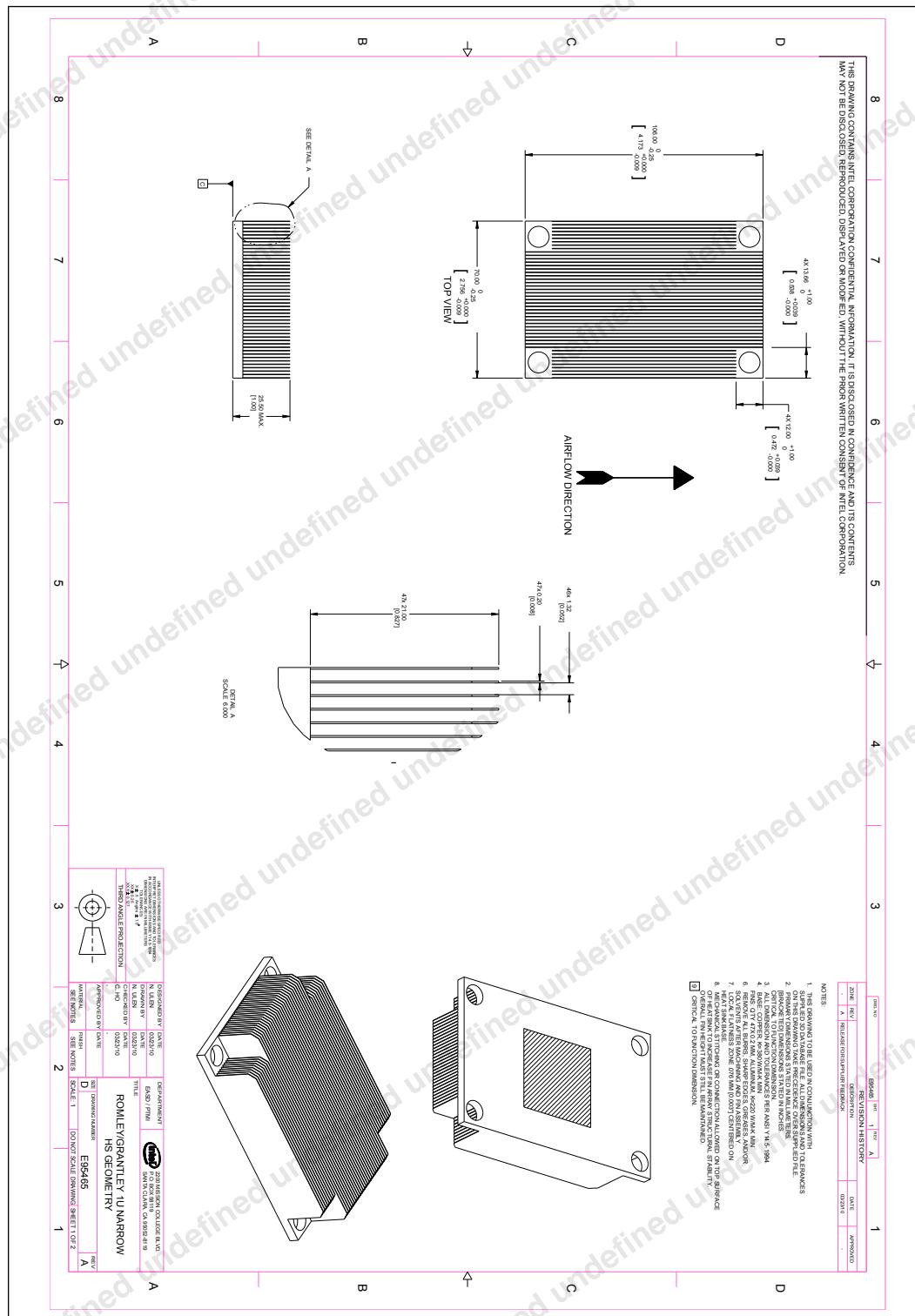
**Figure 51. Heat Sink Spring Cup**

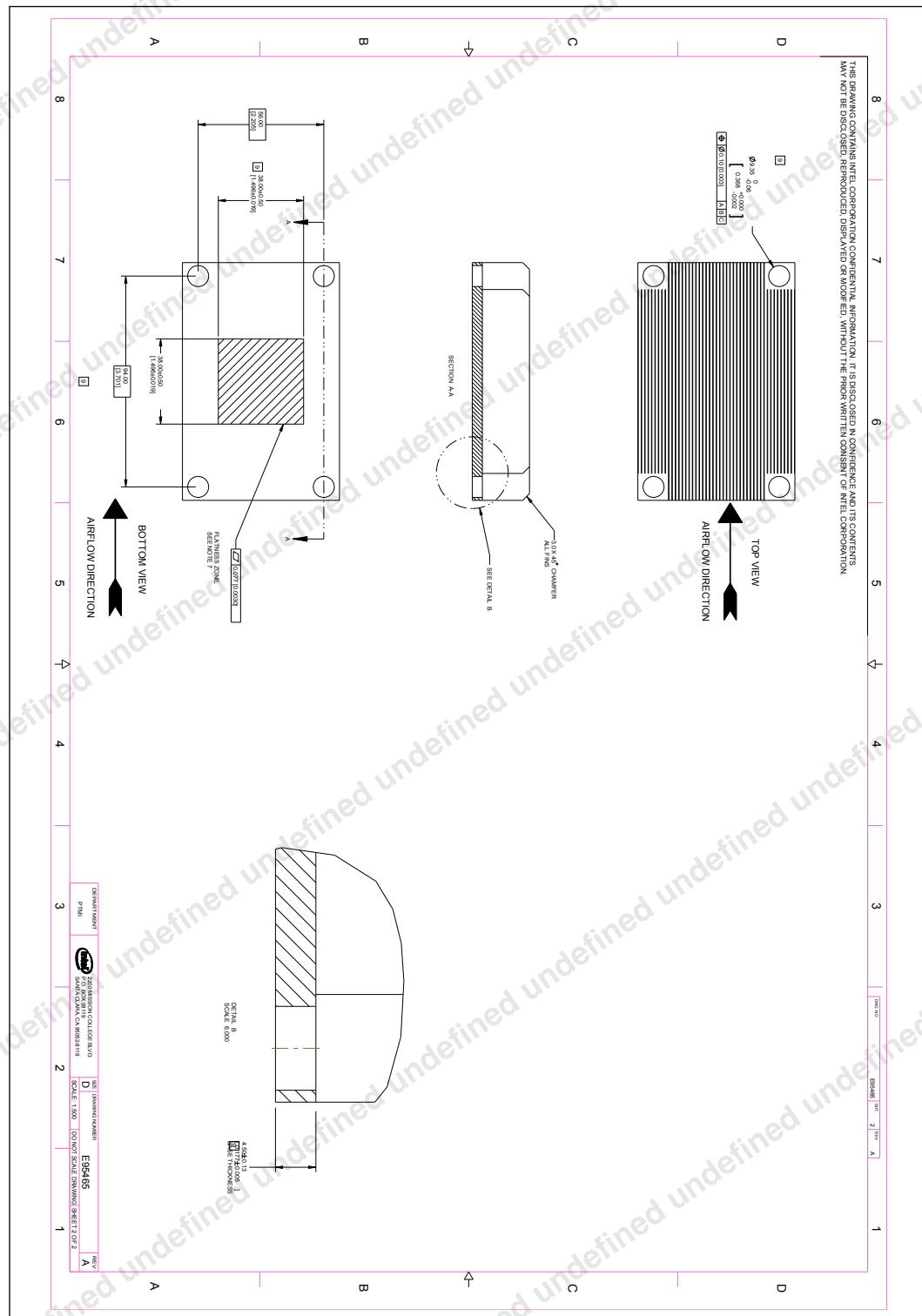




## B.14 1U Narrow Heat Sink Geometry (Page 1)

Figure 52. 1U Narrow Heat Sink Geometry (Page 1)

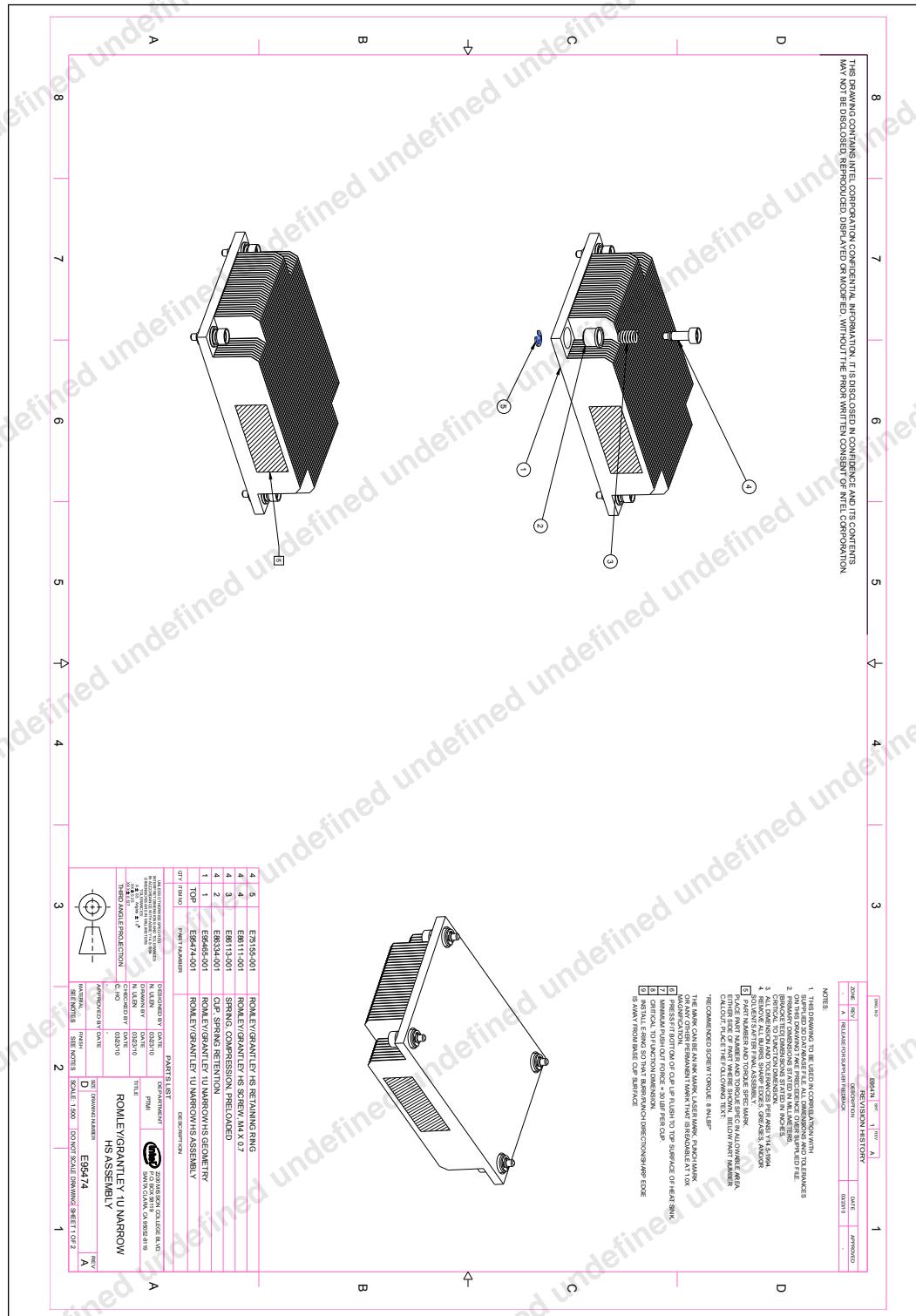


**B.15****1U Narrow Heat Sink Geometry (Page 2)****Figure 53.** 1U Narrow Heat Sink Geometry (Page 2)



## B.16 1U Narrow Heat Sink Assembly (Page 1)

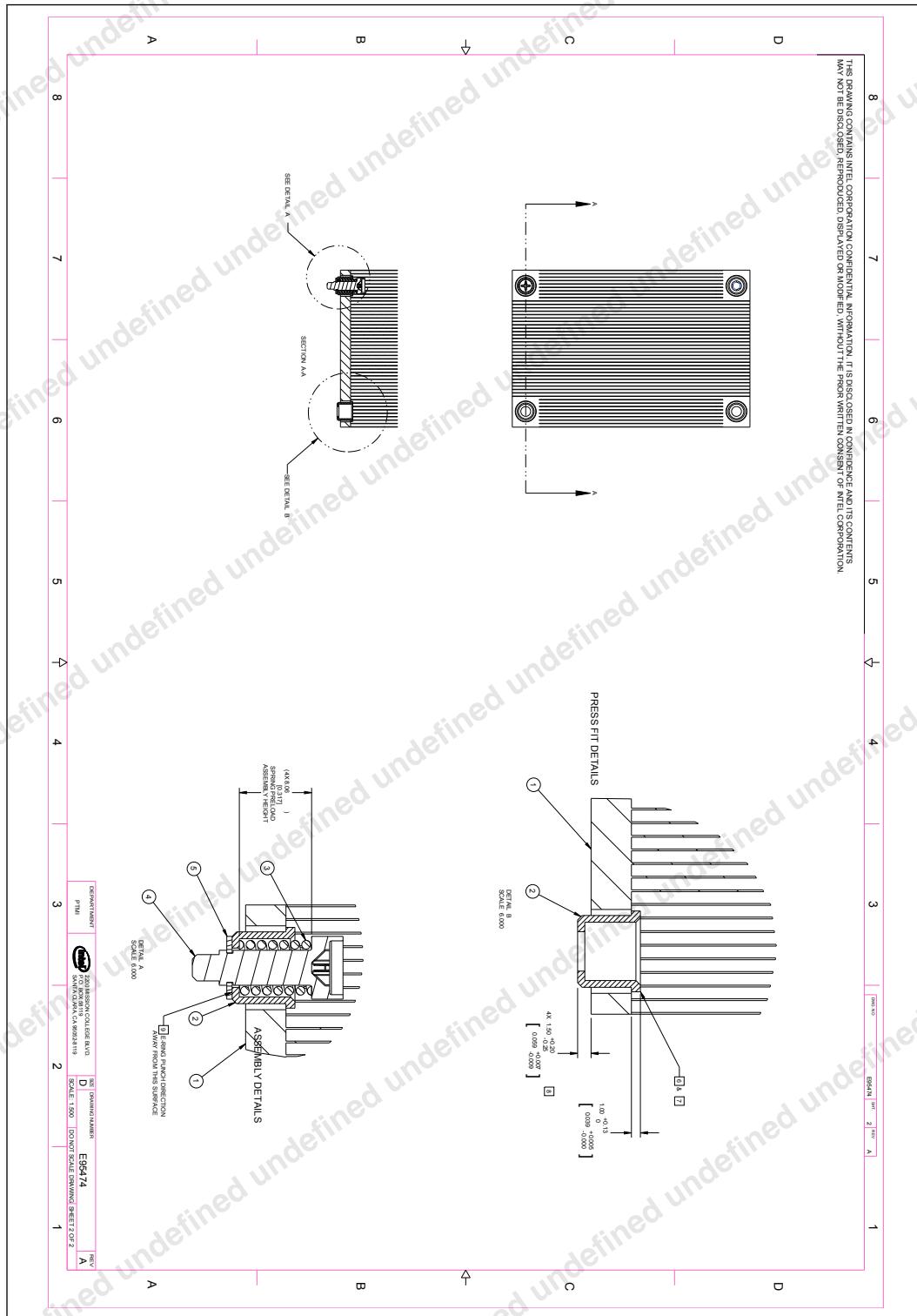
Figure 54. 1U Narrow Heat Sink Assembly (Page 1)





## B.17 1U Narrow Heat Sink Assembly (Page 2)

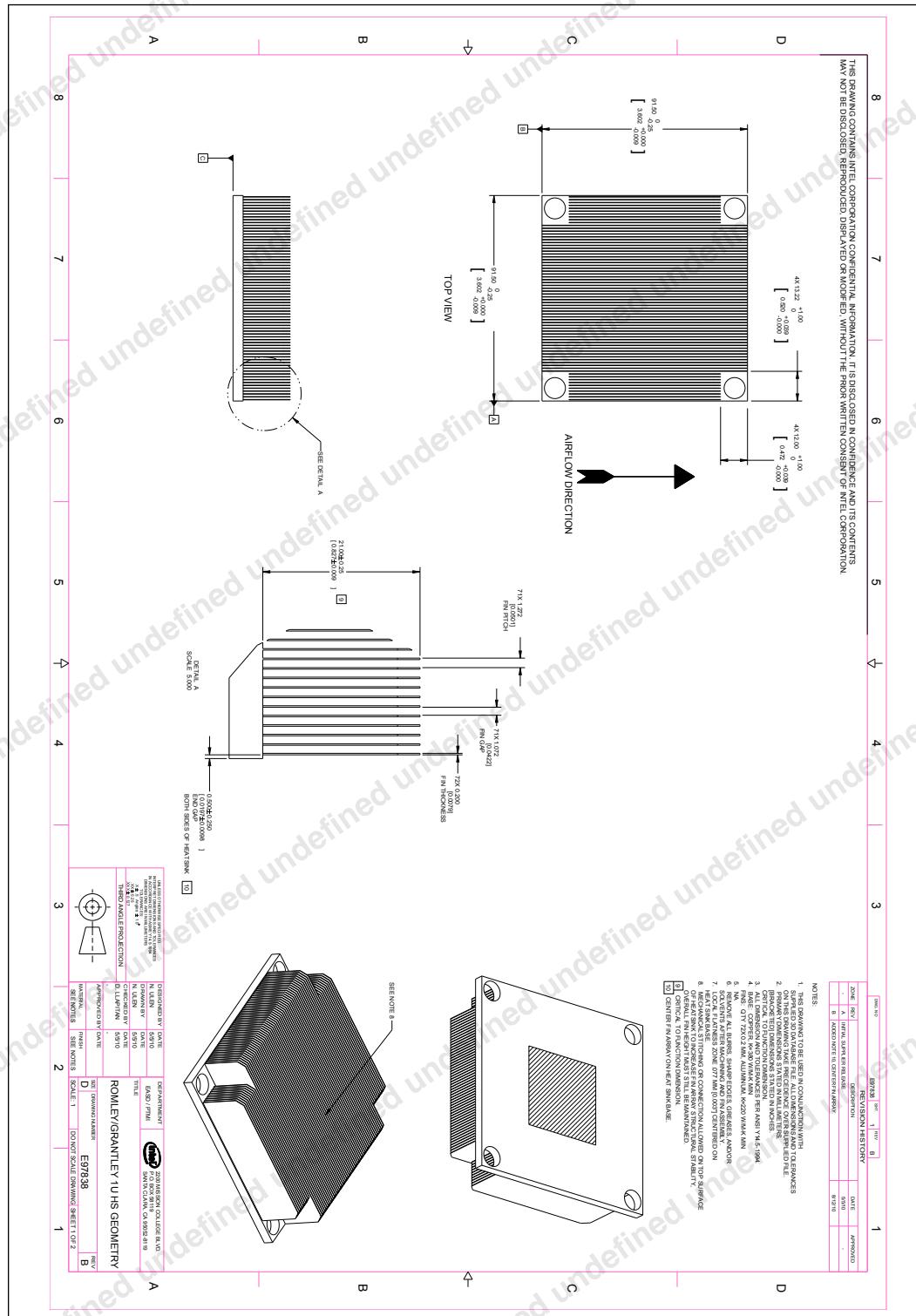
**Figure 55.** 1U Narrow Heat Sink Assembly (Page 2)

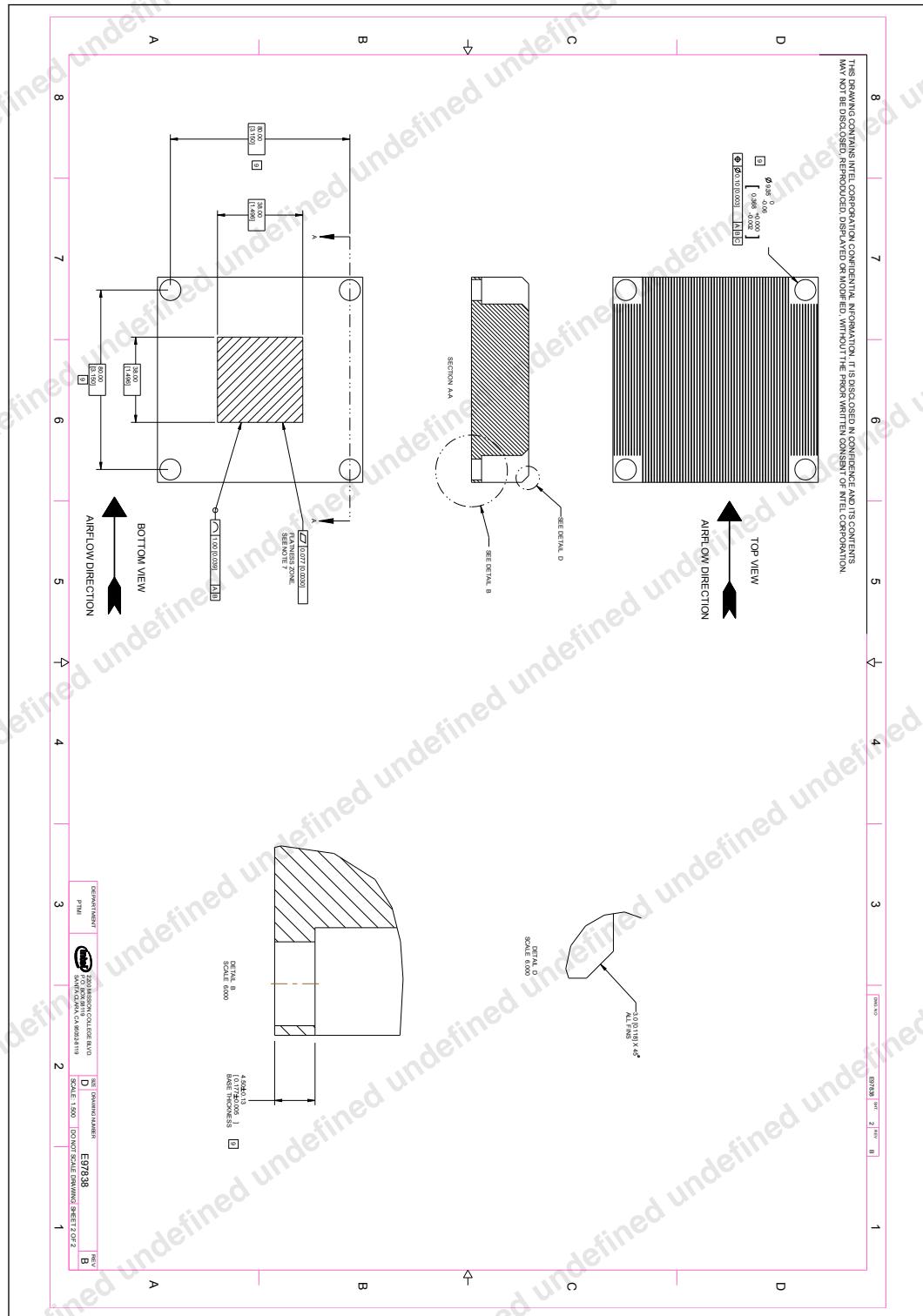




## B.18 1U Square Heat Sink Geometry (Page 1)

Figure 56. 1U Square Heat Sink Geometry (Page 1)

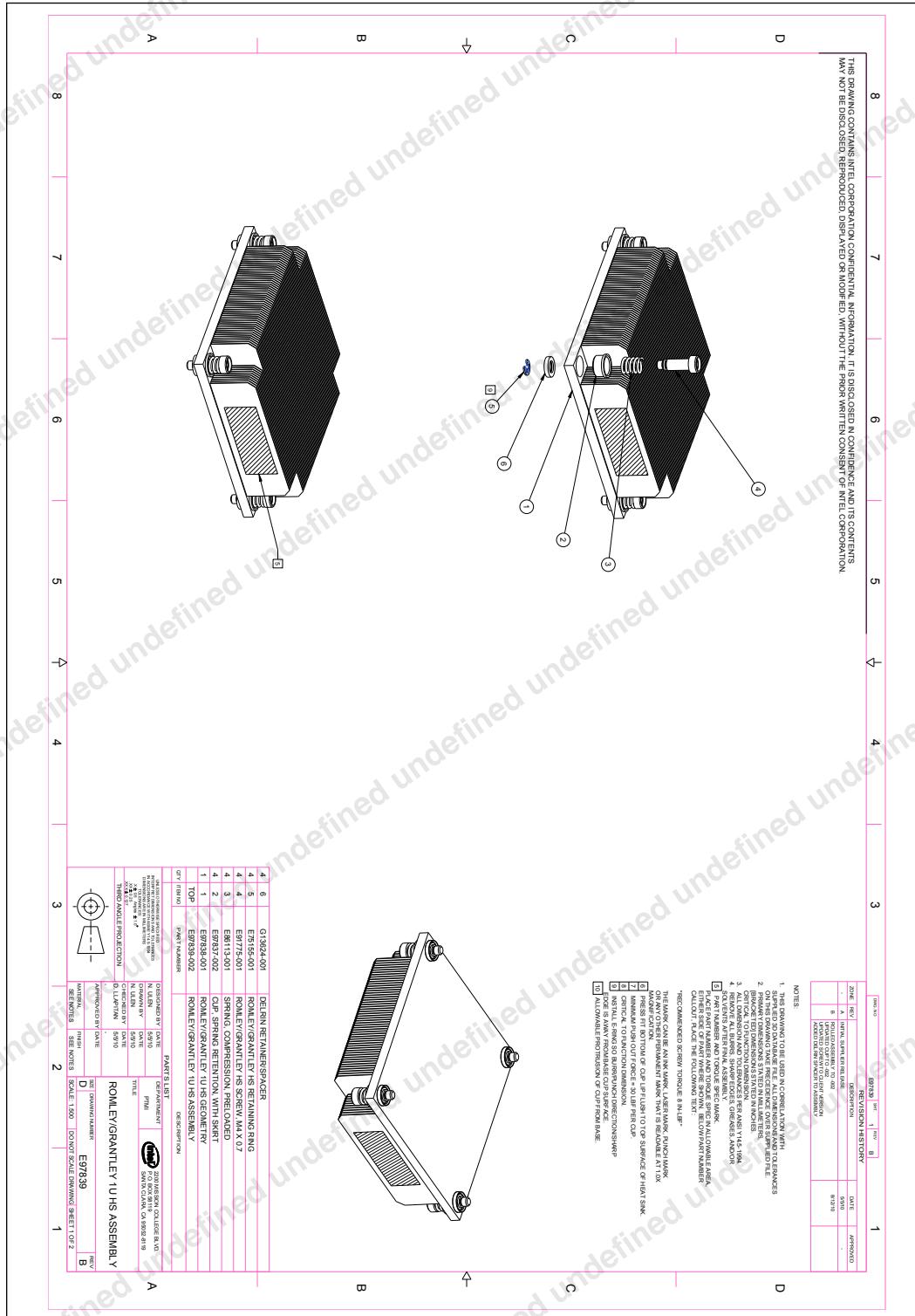


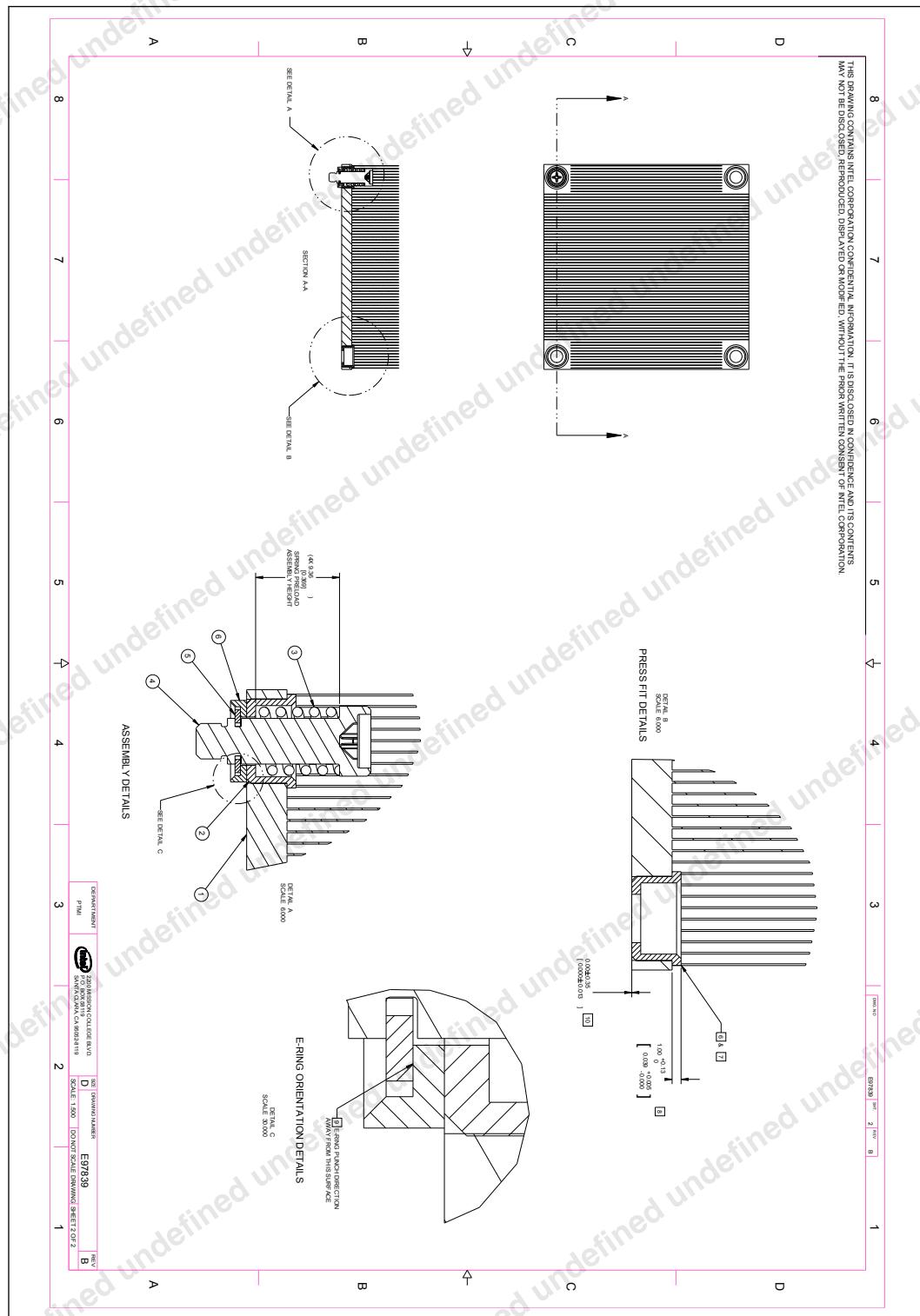
**B.19****1U Square Heat Sink Geometry (Page 2)****Figure 57.** **1U Square Heat Sink Geometry (Page 2)**



## B.20 1U Square Heat Sink Assembly (Page 1)

Figure 58. 1U Square Heat Sink Assembly (Page 1)

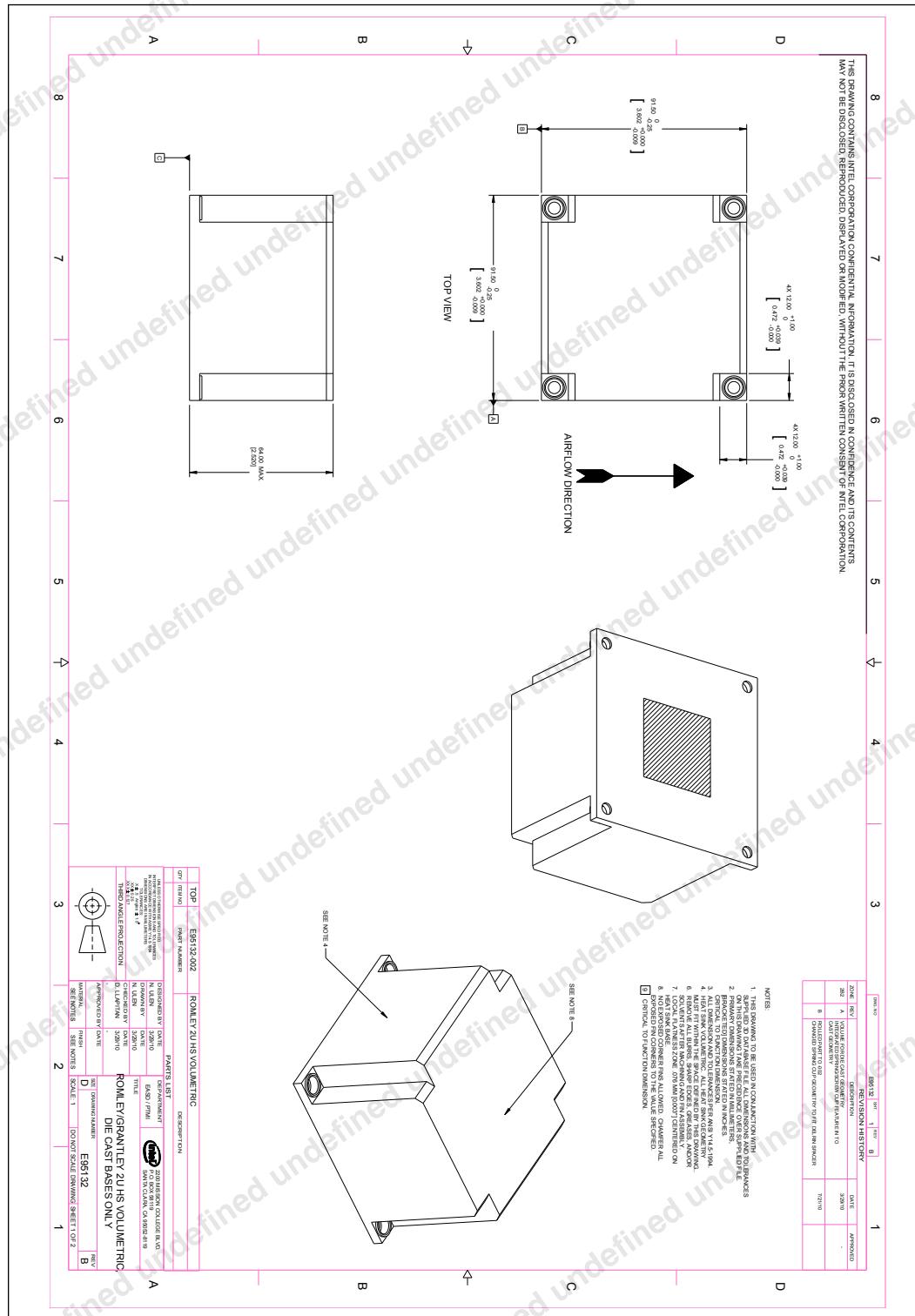


**B.21****1U Square Heat Sink Assembly (Page 2)****Figure 59.** **1U Square Heat Sink Assembly (Page 2)**



## B.22 2U Square Heat Sink Geometry (Page 1)

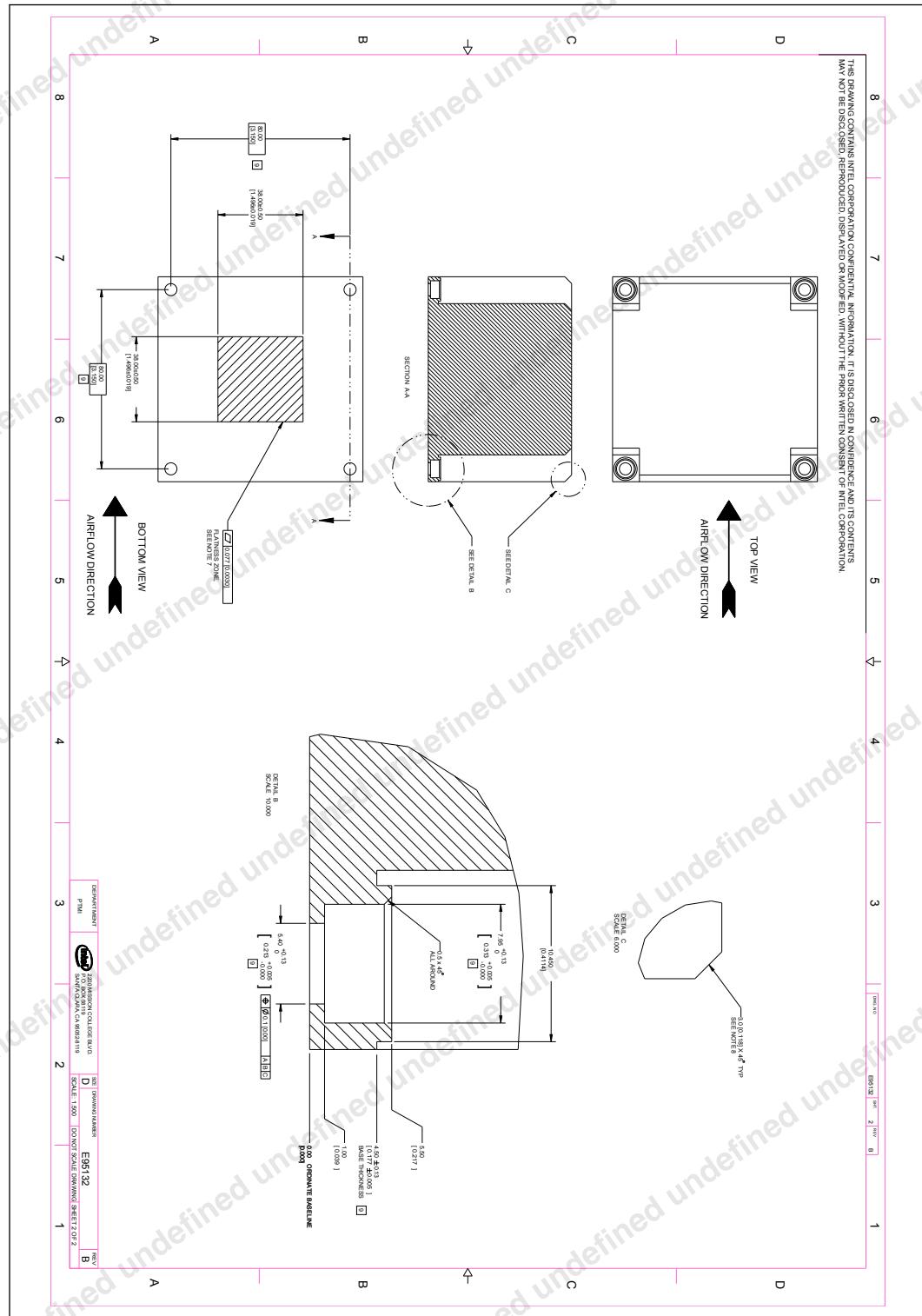
Figure 60. 2U Square Heat Sink Geometry (Page 1)





## B.23 2U Square Heat Sink Geometry (Page 2)

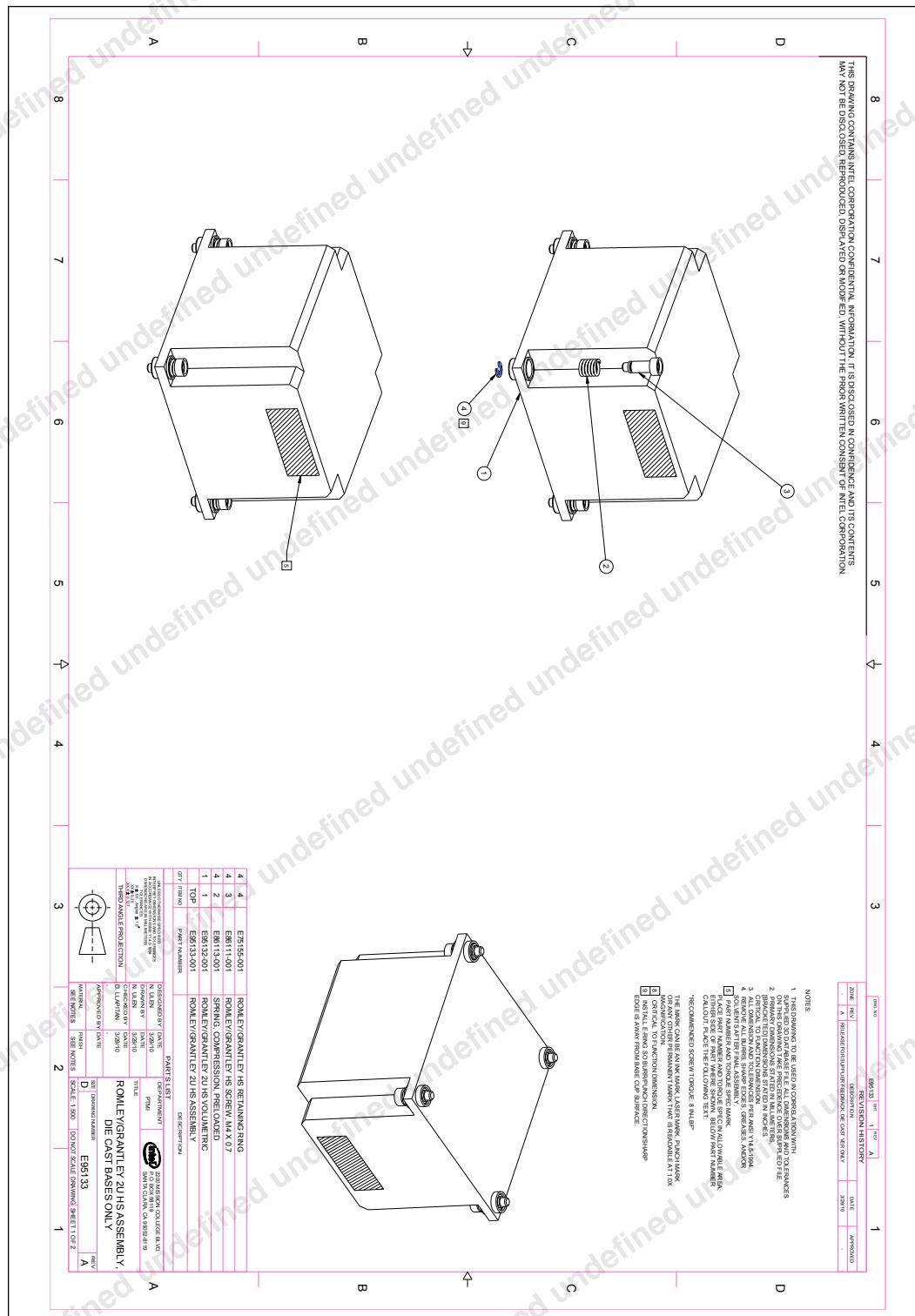
**Figure 61.** 2U Square Heat Sink Geometry (Page 2)





## B.24 2U Square Heat Sink Assembly (Page 1)

Figure 62. 2U Square Heat Sink Assembly (Page 1)





## B.25 2U Square Heat Sink Assembly (Page 2)

**Figure 63.** 2U Square Heat Sink Assembly (Page 2)

