ASSIGNMENT – 1

CIS – 580 INTRO TO COMPUTER ARCHEITECTURE SECTION 50

GROUP #8 ANIL PAVULURU

HASSAN AHMED

UNIT – 1

Q 1) The gadgets which are developed in a sequence of micro instructions and satisfy the user coherence are nothing but embedded CPU. Inside these gadgets' microprocessor are placed in order to control the function and behave like a minicomputer. There is a huge scope in different areas such as communication, Weapon Equipment's, Medical and daily electrical equipment's etc.

Applications:

1) Micro oven

2) Washing Machine

3) Telecommunication

Q 2) Moore's law predicted that every year a 60% annual increase in the number of transistors that are placed on the chip.

According to Moore's the next generation chip will have 1.6times transistors are increased.

So, for the area of one transistor is 1/1.6=0.625 as respectively to previous chip.

Area of transistor increased as square of the diameter
$0.1/\sqrt{1.625}=0.07905$microns.

Diameter of transistor next year is 0.07905microns

UNIT – 2

Q 3) System 1 takes up to 10nsec to get executed. Now, system 1 connected to pipe line (fetch, decode, execute, memory access, and write back) it executes 500million instructions per second.

System 2 cannot connect to pipeline it can execute maximum of 200million instruction and cannot do better than thus which is less and it highly unpredictable to judge which is faster one and slower one.

Q 4) Computer take binary instruction in the form of 0's and 1's and more over each cell is power of 2.

1,024 is rounded as 1000 in computer terminology. Memory capacity is always multiples of 1,024=1byte, and 1, 07, 37,41, 824=1GigaByte (2^{30} =1,07,37,41,824bytes)

Q 5) 1010101

11	10	9	8	7	6	5	4	3	2	1
1	0	1	*	0	1	0	*	1	*	*
1	0	1	0	0	1	0	1	1	1	1

11 –	1	0	1	1
9 -	1	0	0	1
6 -	0	1	1	0
3 -	0	0	1	1
	0	1	1	1 (Module -2 arithmetic)

Transmitted code: 10100101111

Receiver:

11 –	1	0	1	1
9-	1	0	0	1
6-	0	1	1	0
4-	0	1	0	0
3-	0	0	1	1
2-	0	0	1	0
1-	0	0	0	1
	0	0	0	0 (no error)

Error in 9 th position

11 – 1 0 1 1

6- 0 1 1 0

4- 0 1 0 0

3- 0 0 1 1

2- 0 0 1 0

1- 0 0 0 1

1 0 0 1 (error in 9th position)

Q 6) code word is nothing but (m) useful data bits and (r) additional check bits

N=m+r

2^m bits are legal for 2^n bits and 2^r is the check bits. It doesn't contain error detection for compilation because there is no data in the bit. So, considered as wasted bits.

Percentage of wasted bits for the message of the length is $(r/2^r-1)*100$

For check bit(r=3) = $(3/2^3-1)*100$ =42.85%

Respectively,

For check bit(r=4) = $(4/2^4-1)*100$ =26.67%

For check bit(r=5) = $(5/2^5-1)*100$ =16.1%

For check bit(r=6) = $(6/2^6-1)*100$ =9.5%

For check bit(r=7) = $(7/2^7-1)*100$ =5.5%

For check bit(r=8) = $(8/2^8-1)*100$ =3.1%

For check bit(r=9) = $(9/2^9-1)*100$ =1.8%

For check bit(r=10) = $(10/2^{10}-1)*100$ =1.0%

Q 7) disk consist of 1024 sectors/track rotation with speed of 7200rpm it contains 4 surfaces that is 4*1024=4096 bits/sector. While each of the tracks thus holds 4,194,304(4,096*1,024) bits each. At 7,200RPM each rotation take 1/120sec. in 1sec it can read 120 tracks for a rate of 503,316,480bits/sec 0r 62,914,560 bytes/sec.