PANKAJAN THURAIRATNAM

+94(76)2519997 ⋄ Jaffna, Sri Lanka

STATEMENT

Passionate Electronic & Telecommunication Engineering graduate with hands-on experience in **Accelerators, FPGAs, Digital Design, DSP, VLSI, RF, Neuromorphic computing, Quantum Computing, AI/Machine Learning, Mathematics, and Embedded Systems**, with a strong aptitude for creative, technical, and problem-solving skills. Proven ability to drive R&D projects from concept to hardware deployment. Actively seeking a PhD to advance cutting-edge research, with a keen interest in learning new frontiers, tackling complex problems, and adapting to new technologies, with the ability to work both independently and in a team.

EDUCATION

University of Moratuwa Sri Lanka
BSc (Hons) in Engineering (Electronic & Telecommunication) 2020 - July, 2024
CGPA : 3.71/4.0 (First Class), Dean's list semesters : 1,2,5,6,7,8.

St. John's College Jaffna, Sri Lanka
G.C.E Advanced Level - 3A 2012 - 2018

WORK EXPERIENCE

Team Lead - FPGA/DSP 2024/06–2025/11(Eng.) 2025/12–Current (TL.)
Thakshana Technologies (Pvt) Ltd

- Research and development role focused on **defensive communication** over **SATCOM**, with an emphasis on modem & SDR designs. Collaborated with international teams to develop and integrate complex **DSP algorithms**, from basic modules such as modulators, demodulators, DFE components, and synchronizers to full-scale hardware implementations. Experienced in the entire **FPGA design flow, including integration of high-end IPs, embedded Linux development, and protocols such as JESD and Aurora**. Gained hands-on exposure to supporting hardware, including **AFEs** and **microcontrollers**, while working with a wide range of **SoC, FPGA, and embedded platforms**. Additionally, I lead a team of engineers and trained new recruits, ensuring successful project execution and knowledge transfer.

Trainee Electronic Engineer 2023/01–2023/06
Paraqum Technologies (Pvt) Ltd

- R&D project to develop a long-range **RF communication** link with high throughput, ensuring quality and low-latency communication. Gained experience with **ZYNQ-7000** based FPGA devices, designing and programming FPGAs using **MATLAB/Simulink**. Was given full freedom to tackle challenges and self-learn. Worked on tasks involving model generation for different schemes from a base design and integrating ECC algorithms into the model. During this time, I developed the critical skill of identifying, dissecting, and solving problems arising from very complex designs.

Visiting instructor & Project supervisor 2023/09–2023/11
University of Moratuwa

- Worked with second-year undergraduates during their labs and practical sessions, specifically assisting with digital circuits, basic processor and memory concepts, and introductory FPGA programming. Supervised groups of students on their semester major projects on electronics, digital design and computer architecture.

RESEARCHS AND PROJECTS

[1] Systolic-Array based AI-Adaptable Digital Polyphase Filter Banks - FYT (collaboration with FIU)

- Our project addressed the growing challenges of dynamic interference in wireless communication by presenting an innovative solution using Deep Reinforcement Learning to develop adaptive filters that enhance the performance of communication systems. We trained and tested the filters on audio signals, designing low-pass and band-pass filters capable of canceling interference while maintaining high SINR values. A systolic array architecture was built on FPGA, successfully deploying the learned filter coefficients for real-time processing. We effectively mitigated both static and dynamic interference. The system demonstrated real-time cancellation of interference signals with varying carrier frequencies using the learned IIR filters. Currently being developed into a journal publication.

[2] CSI-based Video Compression and Localization in Hardware (Collaboration with IIT Madras) (Ongoing)

- This project explores a novel approach to video compression that leverages Channel State Information (CSI) rather than conventional image-based features, which are typically power-intensive. By utilizing CSI, the system identifies and localizes key regions of interest (ROI) within each frame, enabling selective compression that removes redundant data outside the ROI. The hardware implementation focuses on accelerating both the AI-based localization and the video compression pipeline to achieve high throughput and low latency while maintaining strict power efficiency constraints.

[3] SIMD design : Scalable Matrix Multiplication Accelerator

- This project focuses on the design and implementation of a custom SoC for efficient matrix-based computations. Data is initially transferred from DDR to BRAM via a DMA engine, enabling high-throughput access. A multi-PE (Processing Element) architecture processes the data in parallel, computing the output matrix over time. The system is scalable, optimized for integer-based operations, and supports matrix dimensions up to 64×64, ensuring efficient resource utilization and extensibility for larger workloads.

[4] RISC-V : Single-cycle processor

- This is a complete RTL design of a single-cycle RISC-V processor implemented in RTL, supporting the 32-bit RV32I base instruction set. All architectural components were independently designed using SystemVerilog and integrated into a unified pipeline. The processor executes one instruction per clock cycle and supports essential control flow mechanisms such as branches and jumps. The design was functionally verified through extensive testbench simulation and waveform analysis using ModelSim, and was successfully synthesized and deployed on a Xilinx FPGA board. This project demonstrates a full digital design workflow, from architectural modeling to RTL coding, simulation, synthesis, and hardware validation. It serves as a foundational platform for further extension toward pipelined or multi-cycle architectures and custom instruction-set enhancements.

[5] Yadkai: Robot Design

- This project involves the implementation of a feature-rich active robot in a fully simulation-based environment due to global constraints. Despite the lack of physical prototyping, the design strictly adheres to real-world parameters, from robotic components to sensor specifications. The robot's mechanical structure was modeled in SolidWorks, where all physical properties were verified. Both the robot and its environment were simulated using the Webots platform. The robot includes image recognition, line following, wall following, and a robotic arm, and was evaluated in a custom-designed arena to validate its integrated functionalities.

ACHIEVEMENTS

Undergrad Thesis Project Competition - Runners up 2024
IEEE Signal Processing Society

Sri Lanka Robotics Competition, University Category - Finalist 2021
University of Moratuwa

Robofest Competition, University Category - Semi finalist 2021
Sri Lanka Institute of Information Technology

SKILLS

Engineering	Accelerators, Micro-architecture, NoC, VLSI, FPGA, DSP, HLS design, Baremetal, RF Design, Petalinux, RISC-V, SoC, Kernal driver, PCB design, 3D modeling, Embedded
Machine Learning	Deep Neural Network paradigms, Deep Reinforcement Learning, LSTM, LLM, Data Structures and Algorithms
Languages	Python, C++, Java, System Verilog, VHDL, Shell scripting, LUA, C#, Tensorflow
Tools	Mathematica, Matlab & Simulink , Verilator, OpenRoad, Klayout, Yosys, Vivado Vitis Tools, Quartus, Webots, Altium Designer, Proteus, Unity Engine, Solidworks, make, FINN, ONNYX, Vitis AI, Gem5, Cadence Genus & Innovus, Synopsis Design Compiler
Soft Skills	Industrial Team Lead, Industrial Trainer, Research Adaptability, Team Leadership, Communication, Technical Mentoring, Project Management Problem solving, Adaptability, Team Leadership, Management and Organizing

EXTRA-CURRICULAR ACTIVITIES

IESL Associate Member
Member of Electronics club University of Moratuwa
National Cadet Corps Sri Lanka
Rugby Player St.John's College

REFERENCES

- **Dr. Chamira U. S. Edussooriya**
  Ph.D. (UVic), MIEEE, M.A.Sc., B.Sc.Eng. (UoM)
  Senior Lecturer at Department of Electronic and Telecommunication Engineering, University of Moratuwa
  Mail : chamira@uom.lk **Tel** : +94 71 165 6562

- **Dr. Ranga Rodrigo**
  Ph.D. (WC), M.E.Sc.(WC), B.Sc.Eng. (UoM)
  Senior Lecturer at Department of Electronic and Telecommunication Engineering, University of Moratuwa
  Mail : ranga@uom.lk **Tel** : +94 11 264 0422

- **Dakshina Liyanagama**
  B.Sc.Eng (UoM)
  Lead Engineer- Embedded, Paraqum Technologies
  Mail : shakya@paraqum.com **Tel** : +94 71 926 0387