CHAPTER 4

INTERFACING A/D AND D/A CONVERTERS

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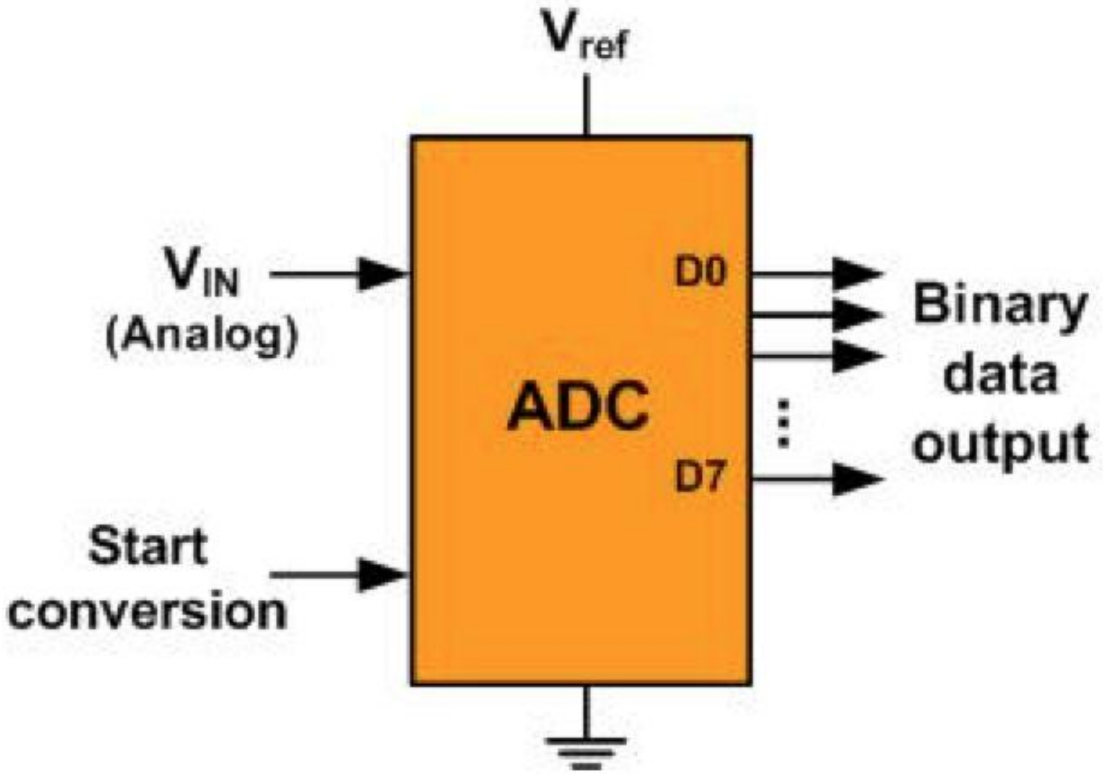
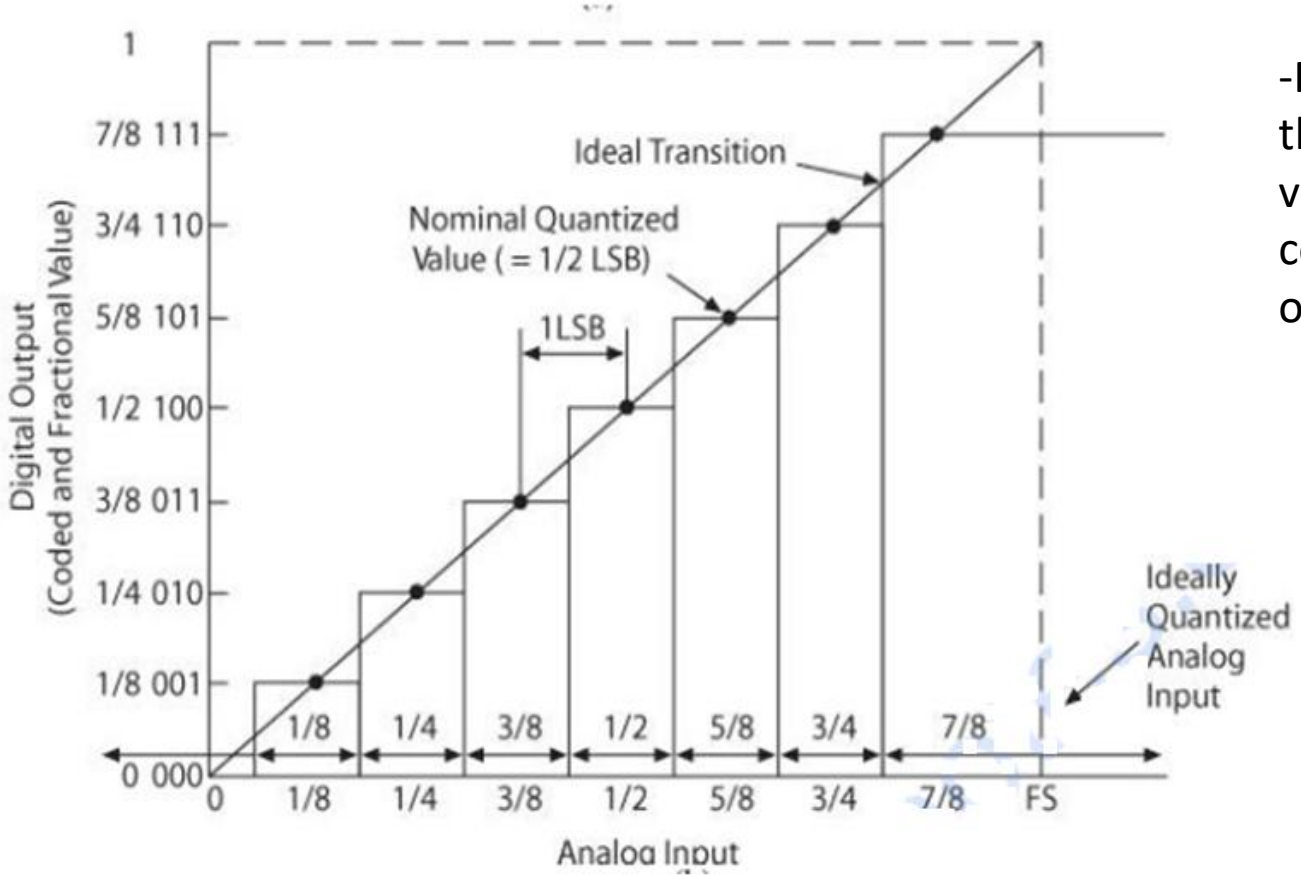
Introduction

- Even though an analog signal may represent a real physical parameter like temperature, pressure etc, it is difficult to process or store the analog signal for later use without introducing a considerable error.
- Therefore, in microprocessor based industrial products, it is necessary to translate an analog signal into digital signal.
- The electronic circuit that translates an analog signal into digital signal is called ADC (Analog to Digital Converter). Similarly a digital signal needs to be translated into an analog signal to represent a physical quantity; this translator is called DAC (Digital to Analog Converter).

General Block Diagram of ADC



Analog input versus digital output



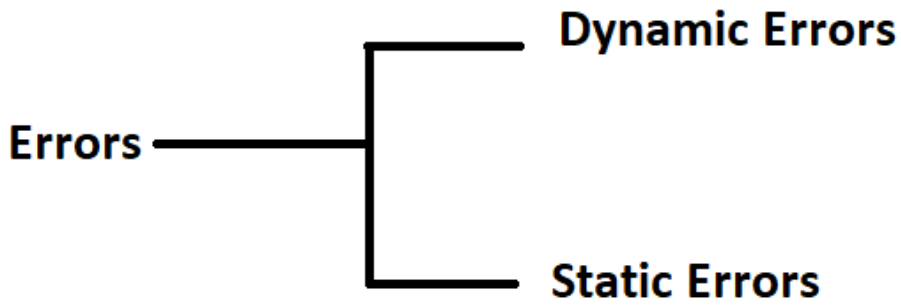
-Fig shows the graph of the analog input voltage (0-1)V and the corresponding digital output signal.

-Fig shows 8(2^3)discrete output states from 000 to 111 each state being 1/8 V apart. This is known as the resolution of the converter

Parameters (Characteristics) of ADC

- **Resolution**
  In ADC, the original analog signal has essentially an infinite resolution as the signal is continuous. The digital representation of this signal would of course reduce this resolution as digital quantities are discrete and vary in equal steps. The resolution of an ADC is smallest change that can be distinguished in the analog input.
  Resolution = FSR (Full Scale Range) / 2^n
- **Conversion Time**
  The A/D conversion another critical parameter is conversion time. This is defined as the total time required converting an analog signal into its digital output.
- **Accuracy**
  It is the comparison of the actual output and the expected output.
- **Linearity**
  The output should be the linear function of input.
- **Full scale output value**
  The maximum bit output achieved from the respective input.

Errors in ADC and DAC



Dynamic Errors

- Conversion time

- Delay time

- Settling time

Errors…

- Static Errors
  - Differential Linearity
  - Monotonicity
  - Integral Linearity
    - Best St. Line Linearity
    - End Point Linearity
    - Absolute Linearity
      - Zero Error
      - Full Scale Error
      - Gain Error

1. Dynamic Errors

A. Conversion Time

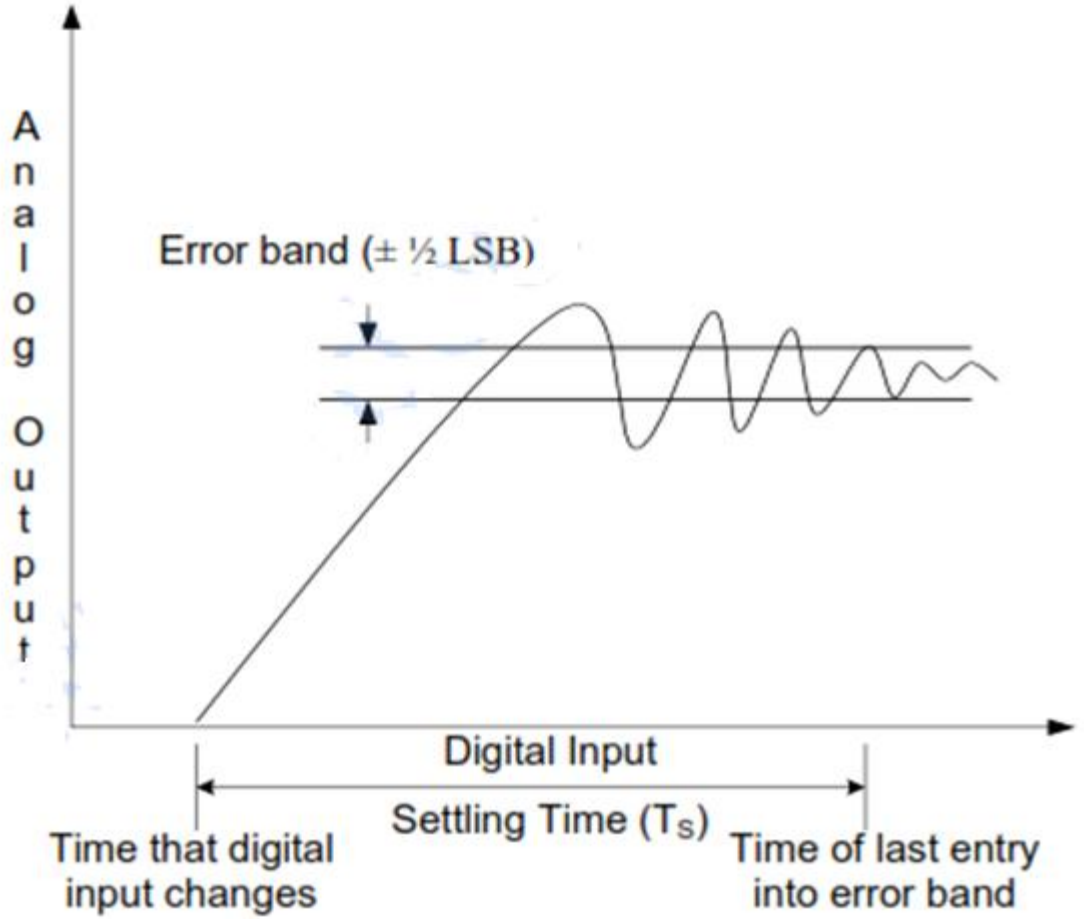
- It is the elapsed time between the command to perform a conversion and the appearance at the converter output of the complete digital representation of the analog input value.

B. Delay Time

- It is the time interval between the instant when the digital input changes and the instant when the analog output passes a specified value that is close to its initial value.

C. Settling Time

- When the output of DAC changes from one value to another, it typically overshoots the new value and may oscillate briefly around that new value before it settles to a constant value.
- It is the time interval between the instant when the analog output passes a specified value and the instant when the analog output enters for a last time a specified error band about its final value.

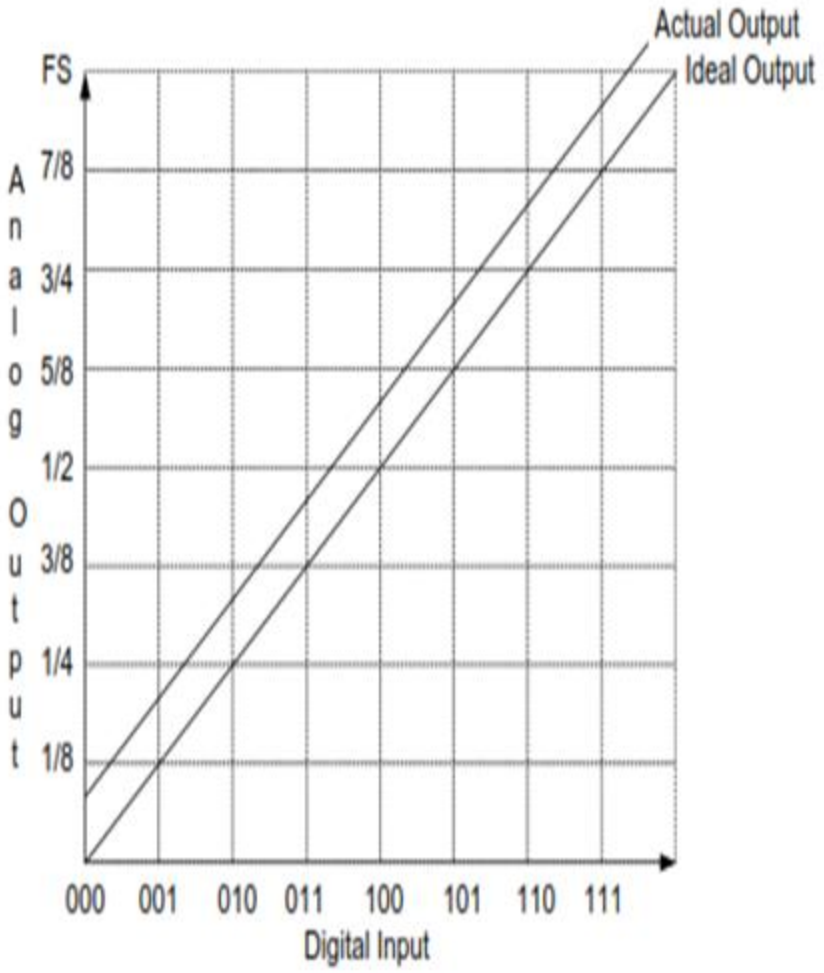

Analog Output
Error band (± ½ LSB)
Digital Input
Settling Time (T_S)
Time that digital input changes
Time of last entry into error band

2. Static Errors

A. Differential Linearity

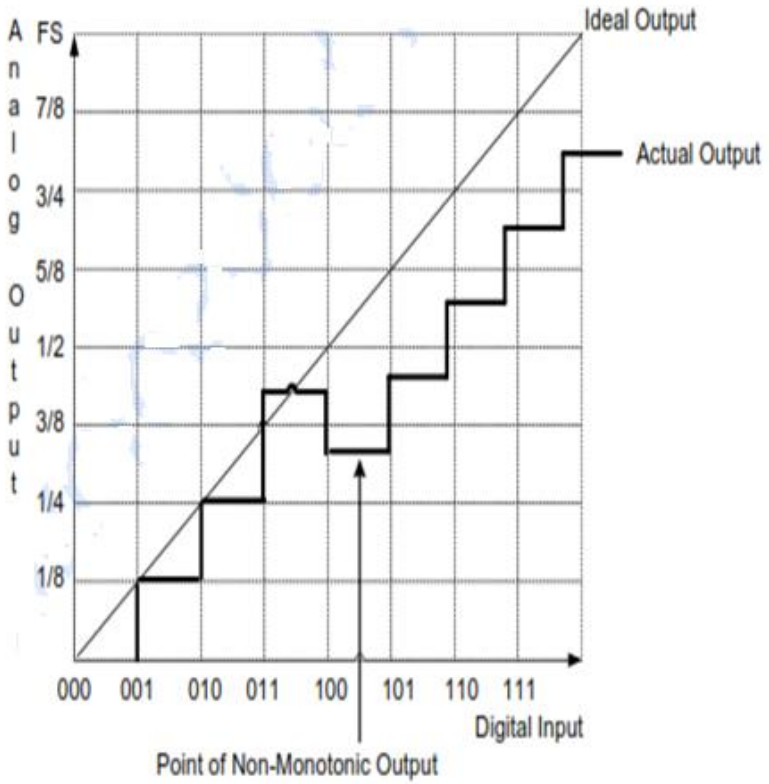
- It is a measure of the separation between adjacent levels.
- Differential linearity measures the bit-to-bit deviations from ideal output steps rather than entire output range.
- If V_s is the ideal change and V_{cx} is the actual change, then the differential linearity can be expressed as:

$$[(V_{CX} - V_S)/V_S]*100\%$$



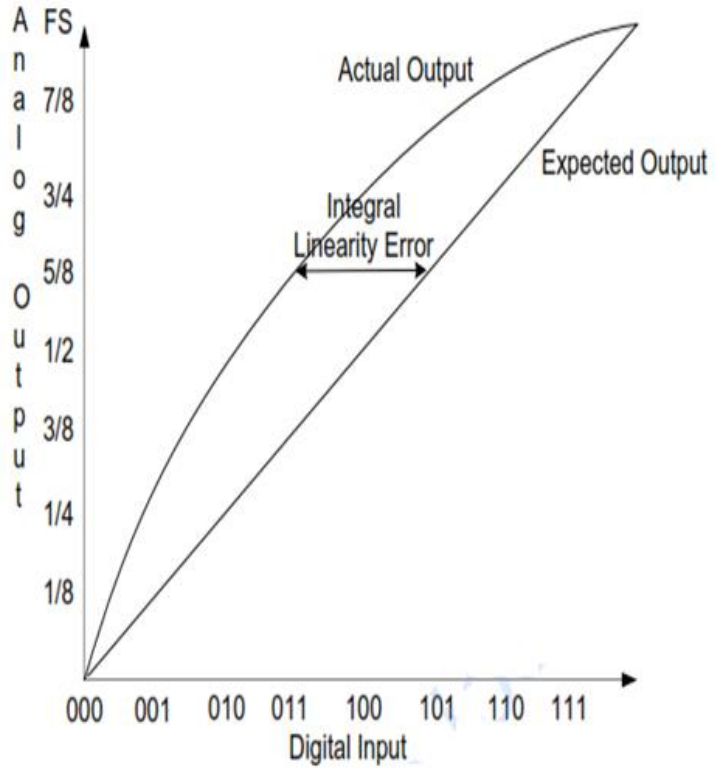
B. Monotonicity

- In a D/A converter; means that as the digital input to the converter increases over its full scale range, the analog output never exhibit a decrease between one conversion step and next.



C. Integral Linearity

- It is the maximum deviation of the output of a D/A for any given input code from a straight line drawn from its ideal minimum to its ideal maximum.



I. Absolute Linearity

- It is measured by assuming that the output of a D/A will begin at zero and end at full scale.
- The actual outputs are compared with a line drawn through these two points.

a. Zero Error

- It is the difference between the actual output and zero when the digital word for a zero output is applied.

b. Full Scale Error

- It is the difference between the actual and the ideal voltage when the digital word for a full scale output is applied.

i. Gain Error (Scale Factor Non-Linearity)

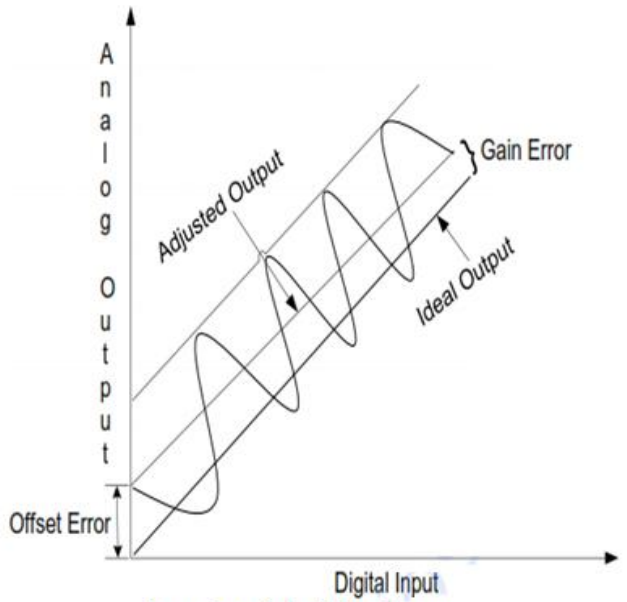
- It is the difference between the gains of the actual static and ideal input output characteristics.

ii. Offset Error

- Offset error adds a constant value to output.

II. Best Straight Line Linearity

It depicts the accuracy of a D/A in terms of the deviation from the ideal output range without regard to zero or full scale errors.



Best Straight Line Error

III. End Point Linearity

It uses a straight line through the actual end points instead of the ideal points.

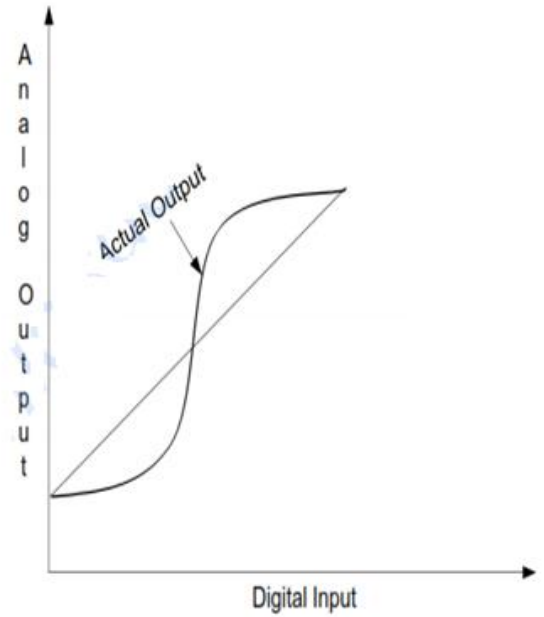
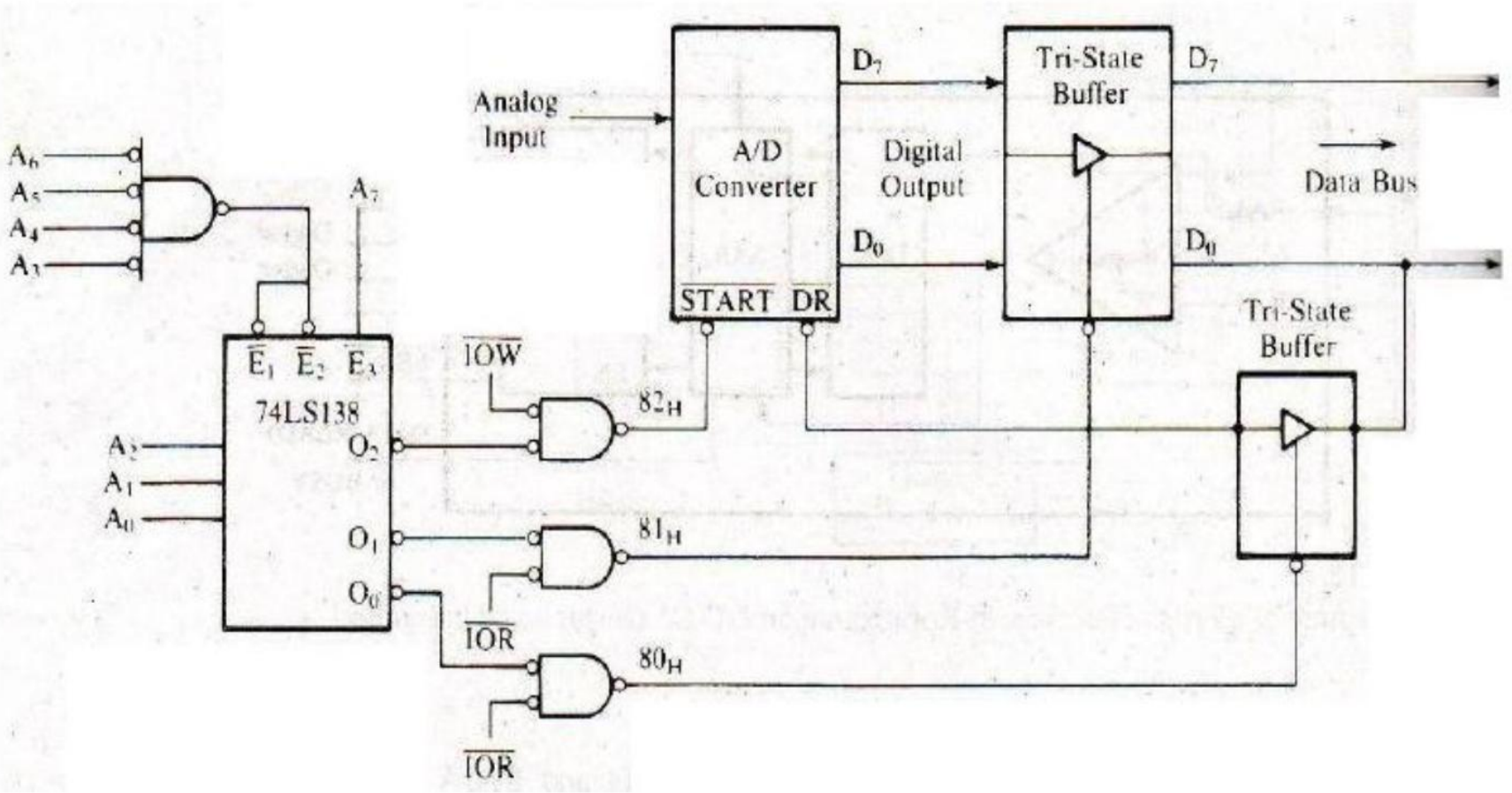


Fig.: End Point Linearity Error

Selection of DAC or ADC (Design Requirements)

- Resolution
- Linearity
- DAC: Settling Time
- ADC: Conversion Time
- Accuracy
- Cost

1. Interfacing an 8-Bit ADC using Status Check

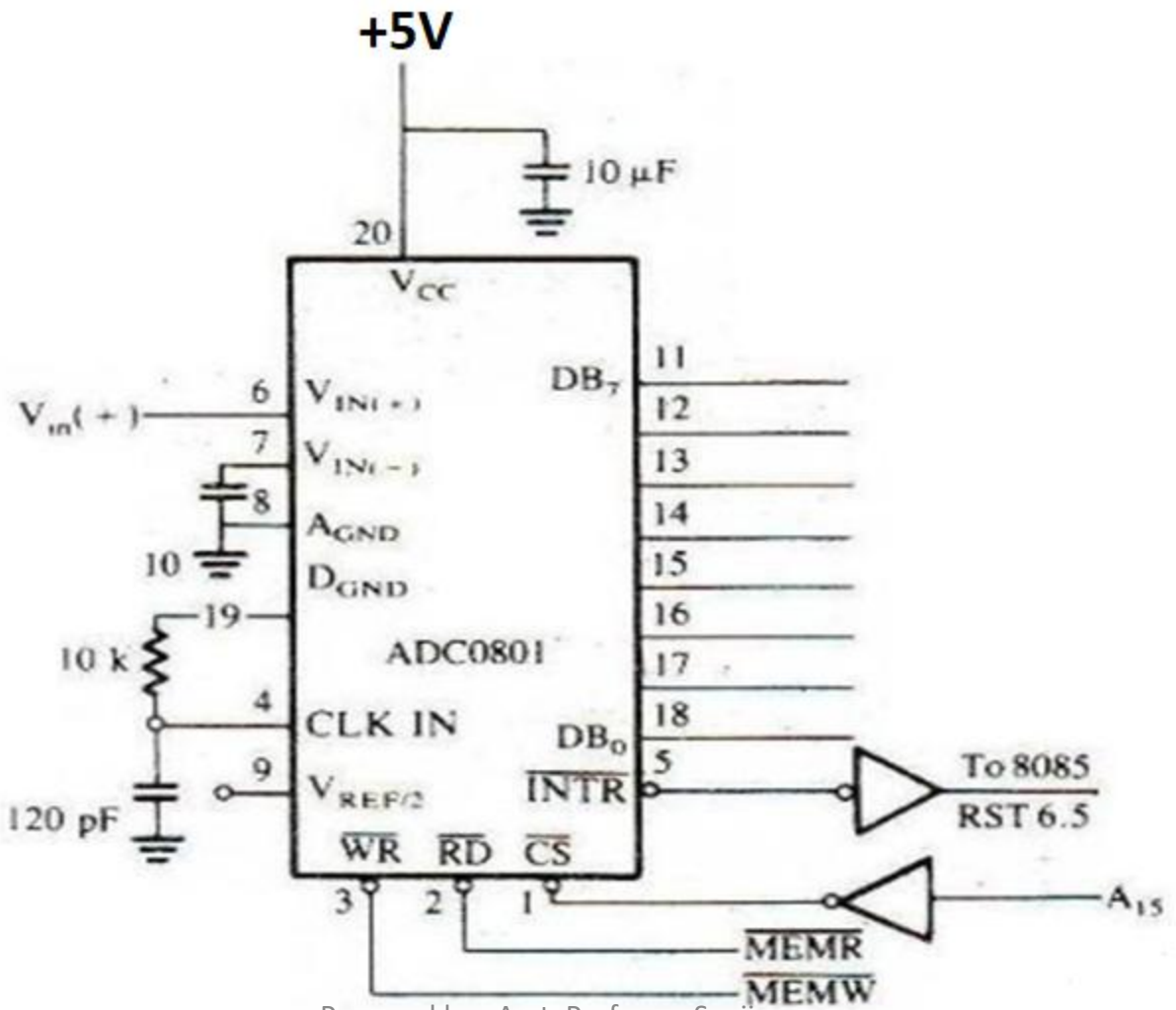


Program

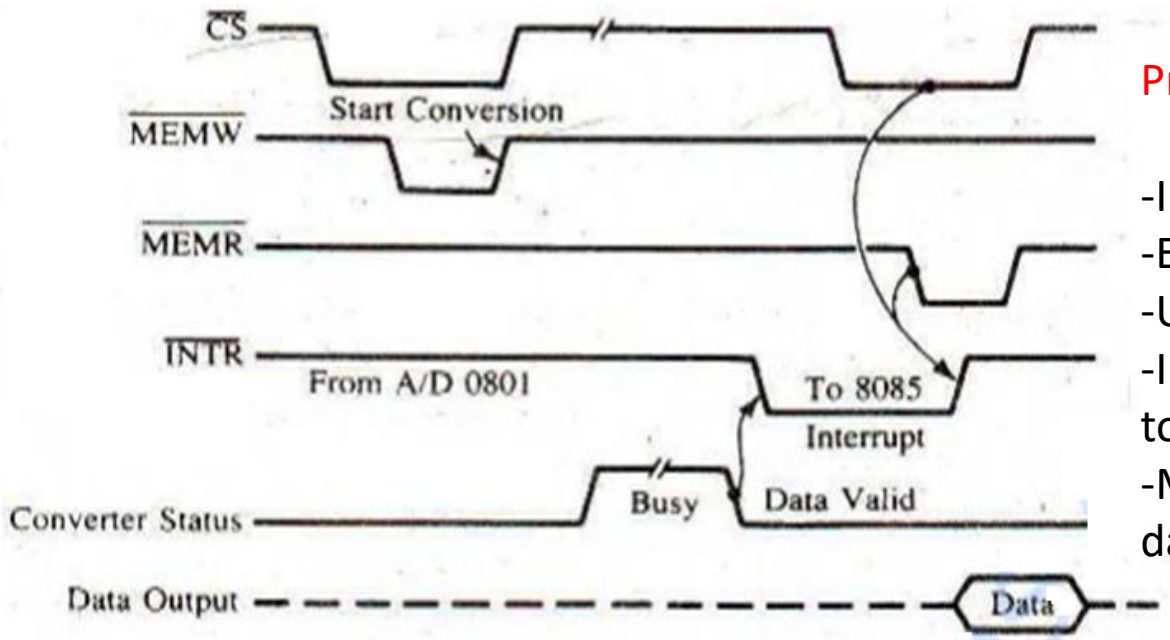
```
        OUT 82H; start Conversion
Test: IN 80H; Read Data Ready Status
        RAR; Rotate Do into carry

        JC TEST: If Do = 1, Conversion is not yet
                                complete go back and check
        IN 81H ; Read Output and save It in accumulator
        RET
```

2. Interfacing an 8-Bit ADC using Interrupt



- The converter requires a clock at CLK IN; the frequency range can be from 100 KHZ to 800 KHZ.
- The user has two options; either to connect an external clock at CLK IN or to use the built in internal clock by connecting a register and a capacitor externally at pins 19 & 4 respectively.
- The frequency is calculated by using the formula F = 1 / 1.1 RC.
- The ADC0801 is designed to be microprocessor compatible. It has three control signals: *WR', CS' and RD' that are used for interfacing.*
- To start conversion, the *WR' and CS' are asserted low.*
- When WR' goes low, the internal SAR is reset and the output lines go into the high impedance state.
- When *WR'* makes transition from low to high, the conversion begins.
- When the conversion is completed, the *INTR* is asserted low and the data are placed on output lines
- INTR signal can be used to interrupt the processor.
- When the processor reads the data by asserting RD', the *INTR* is set.
- When Vcc is +5V, the input voltage can range from 0V to 5V and the corresponding output will be from 00H to FFH.



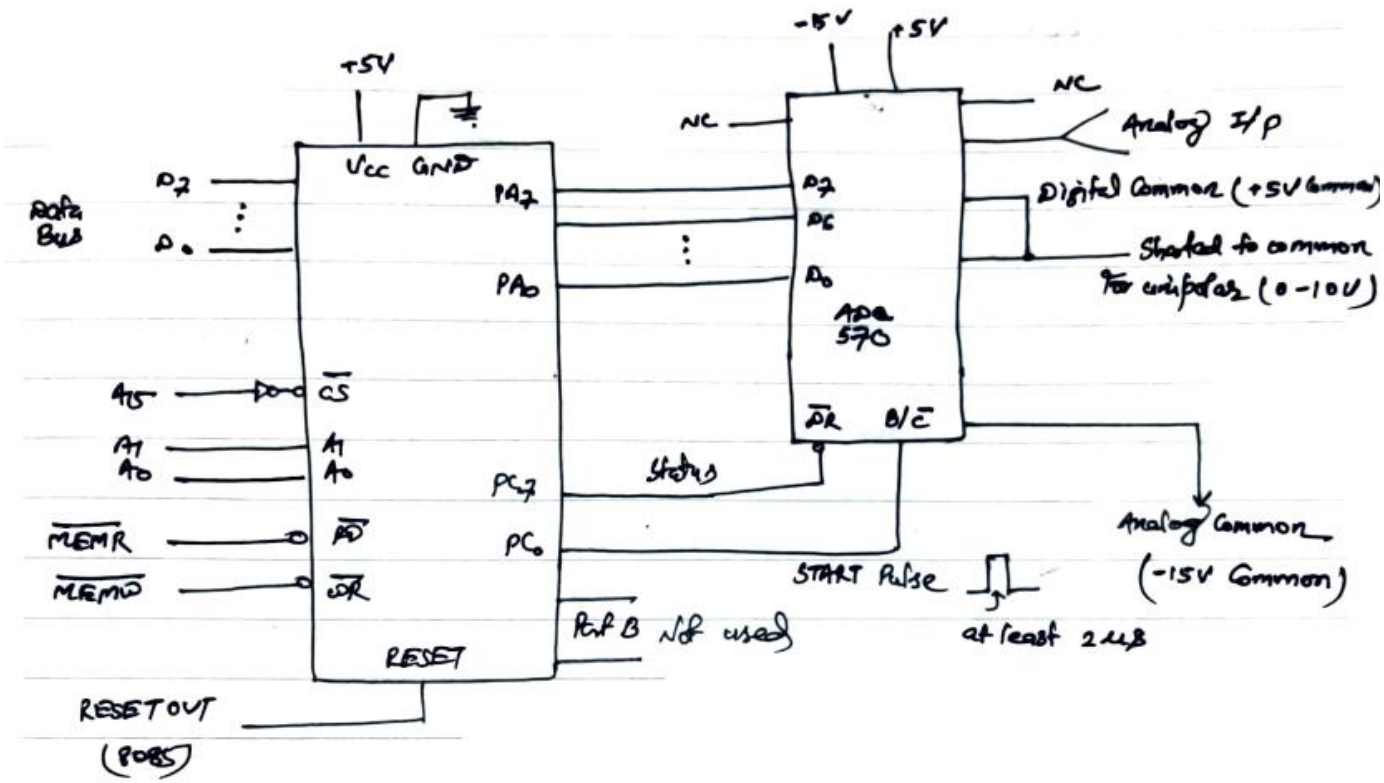
Programming concept:

-Initialize stack
-Enable EI
-Unmask RST 6.5(SIM)
-Initialize a conversion by writing to port 8000H
-Memory-pointer for storing data.

Service Routine:

```
LDA 8000H;   Read data
MOV M, A ;   store data in memory
INX H;       Next  memory location
DCR B;       Next count
STA 8000H;   start next conversion
EI;          Enable interrupt again
RNZ;         Go back to main if counter not equal to zero
HLT
```

- **Given the interfacing circuit to read from an ADC using 8255 in memory – mapped I/0**
  - **Set up Port A to read data**
  - **Set up bit PC0 to start conversion and bit PC7 to read the ready status of the converter**



- Mode 0 Control word : PA = input port, PC_L = output, for start of conversion, PC_U = input, to read status of at PC_7

  $1\ 0011000 = 98H$

- BSR Control word for START Pulse

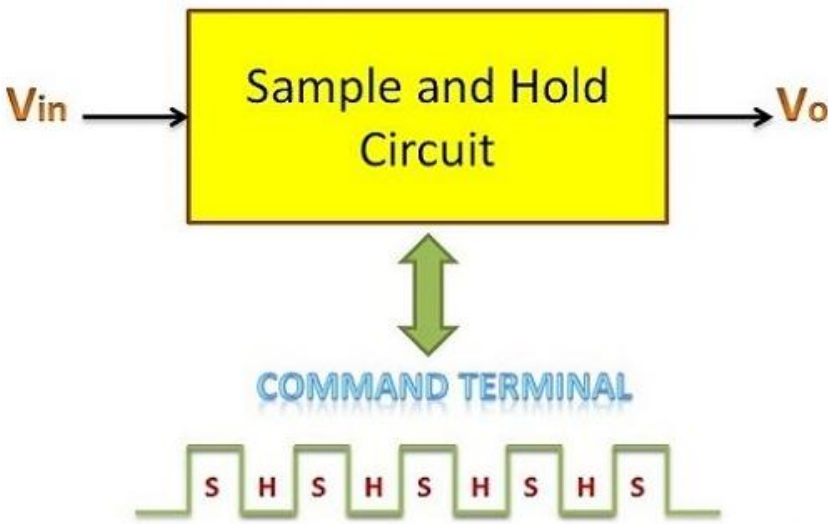
  $0\ 000\ 000\ 0/1 \Rightarrow$ 01H for set, 00H for reset

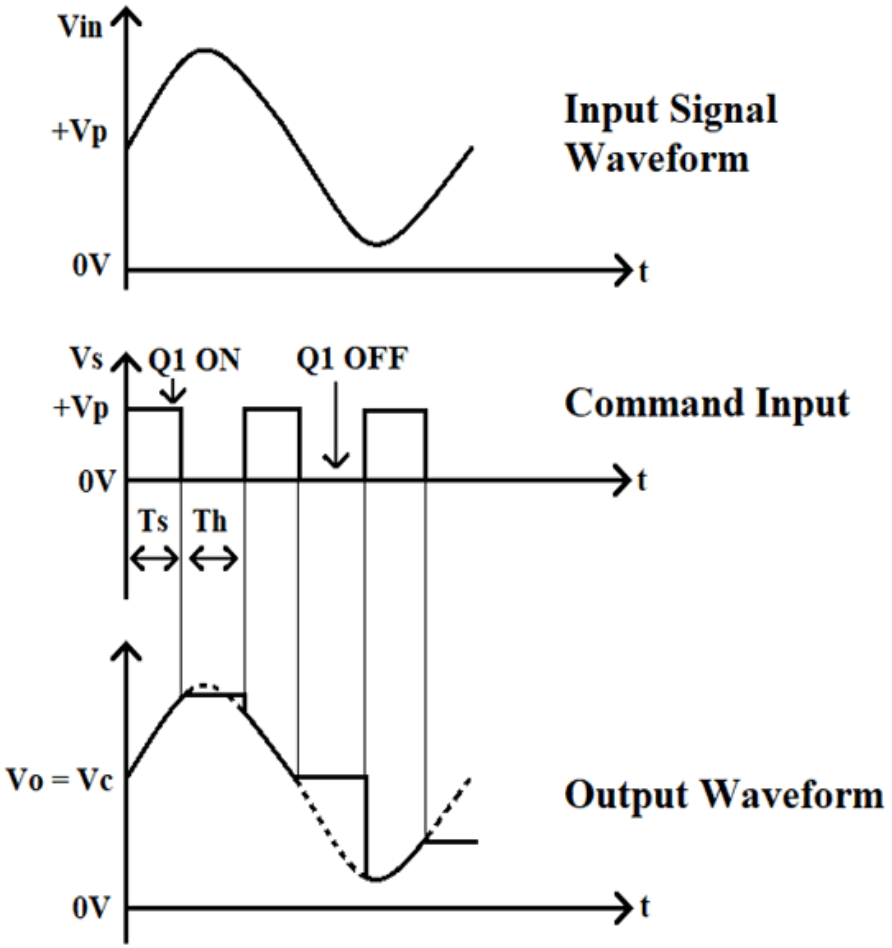
- Port Address : 8000H to 8003H

Sample and Hold Circuit

- **Definition:** The **Sample and Hold circuit** is an electronic circuit which creates the samples of voltage given to it as input, and after that, it holds these samples for the definite time.
- A sample and hold circuit is used before analog signal is fed to ADC, so that the value of analog can be kept constant and conversion can be done with constant value
- The time during which sample and hold circuit generates the sample of the input signal is called **sampling time**.
- Similarly, the time duration of the circuit during which it holds the sampled value is called **holding time**.
- Sampling time is generally between **1μs to 14 μs** while the holding time can assume any value as required in the application

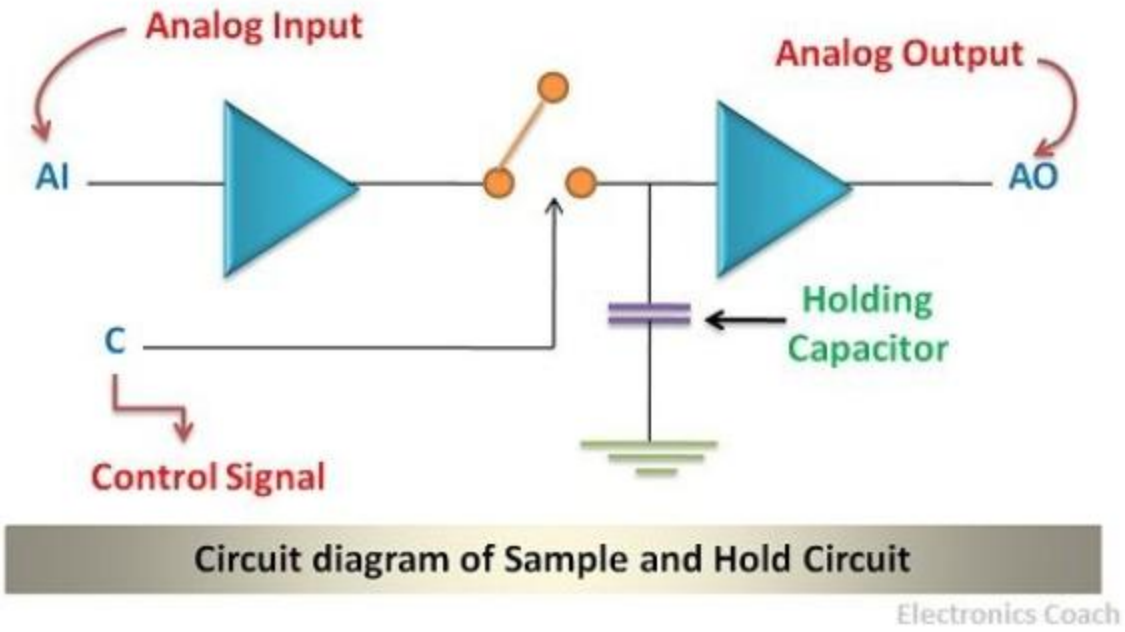
- The capacitor present in circuit charges to its peak value when the switch is opened, i.e. during sampling and holds the sampled voltage when the switch is closed.





Circuit Diagram of Sample and Hold Circuit

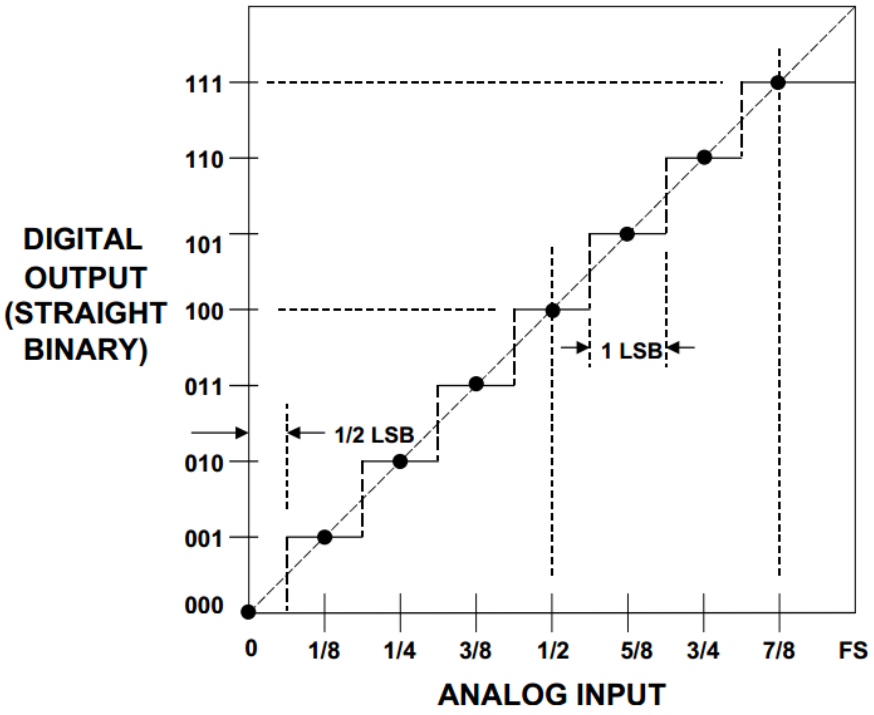
The diagram below shows the circuit of the sample and hold circuit with the help of an Operational Amplifier. It is evident from the circuit diagram that two OP-AMPS are connected via a switch. When the switch is closed sampling process will come into the picture and when the switch is opened holding effect will be there.

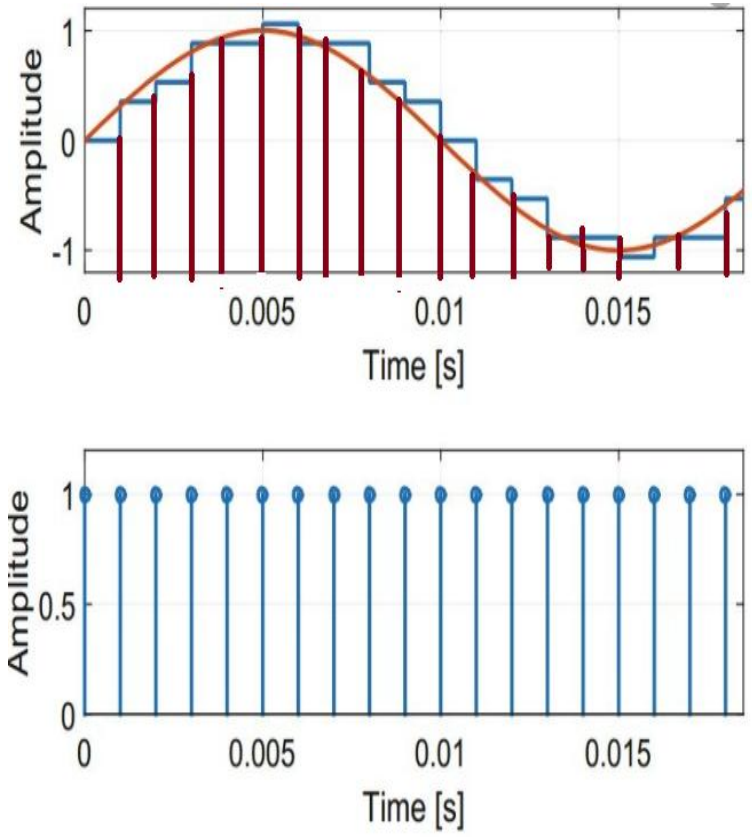


The capacitor connected to the second operational amplifier is nothing but a holding capacitor.

Quantization

- It is the process of converting an input function having continuous values to an output having only discrete values





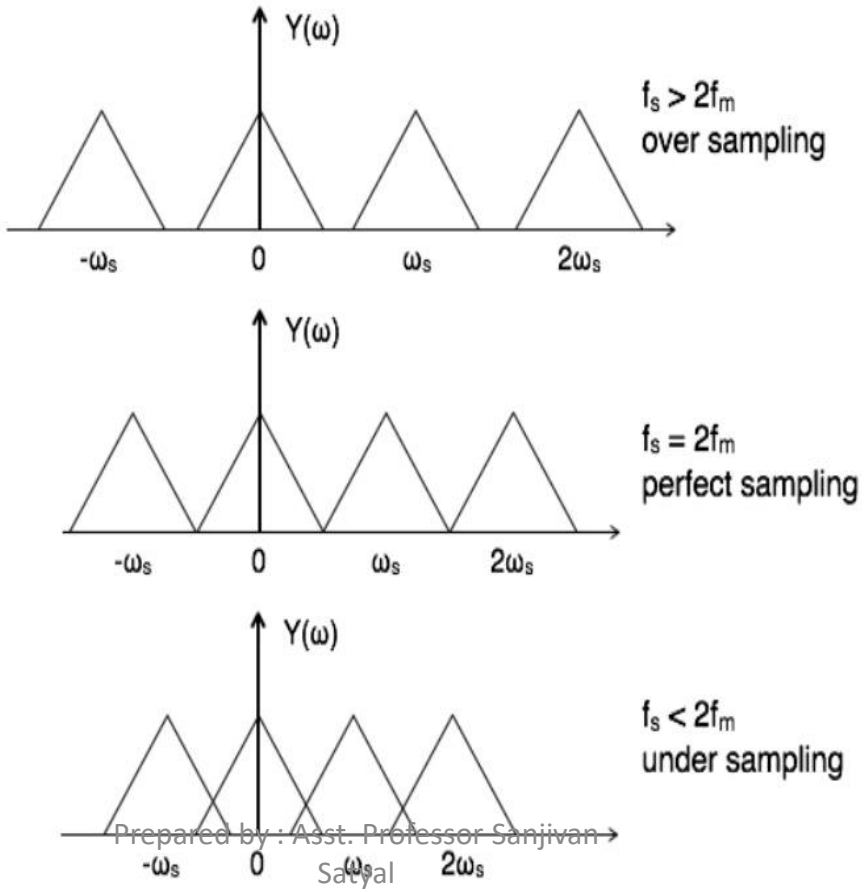
Sampling Rate

- The Analog Signal is continuous in time and it is necessary to convert this to a flow of digital values.
- It is therefore required to define the rate at which new digital values are sampled from the analog signal.
- The rate of new values is called the Sampling Rate or Sampling Frequency of the converter.
- A continuously varying band limited signal can be sampled and then the original signal can be exactly reproduced from the discrete-time values by an interpolation formula.
- The accuracy is limited by quantization error. However, this faithful reproduction is only possible if the sampling rate is higher than twice the highest frequency of the signal.
- This is essentially what is embodied in the Shannon-Nyquist Sampling Theorem.
- Since a practical ADC cannot make an instantaneous conversion, the input value must necessarily be held constant during the time that the converter performs a conversion (called the Conversion Time).
- An input circuit called a Sample and Hold performs this task in most cases by using a capacitor to store the analog voltage at the input, and using an electronic switch or gate to disconnect the capacitor from the input.
- Many ADC integrated circuits include the sample and hold subsystem internally.

Sampling Theorem

Statement: A continuous time signal can be represented in its samples and can be recovered back when sampling frequency f_s is greater than or equal to the twice the highest frequency component of message signal. i. e.

$$f_s \geq 2f_m.$$



Aliasing Effect

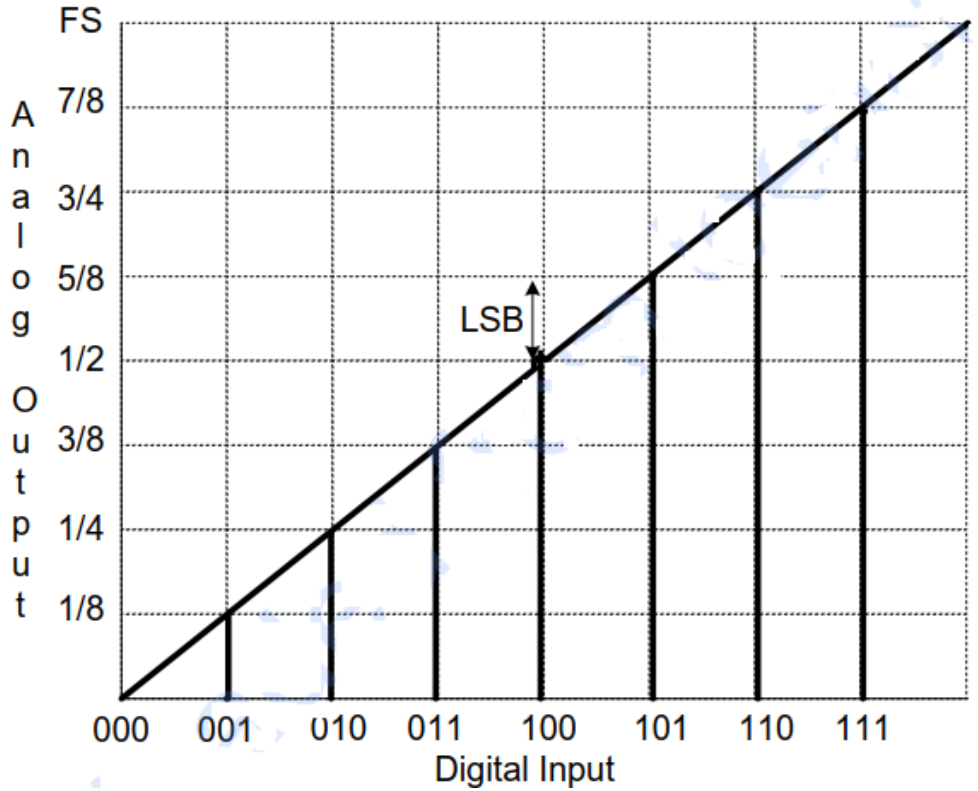
- If the digital values produced by the ADC are converted back to analog values by a DAC, it is desirable that the output of the DAC be an exact replica of the original signal.
- If the input signal is changing much faster than the sample rate, then this will not be the case, and spurious signals (false) called aliases will be produced at the output of the DAC.
- This problem is called aliasing. To avoid aliasing, the input to an ADC must be low-pass filtered to remove frequencies above half the sampling rate.
- This filter is called an Anti-aliasing Filter, and is essential for a practical ADC system that is applied to analog signals with higher frequency content.

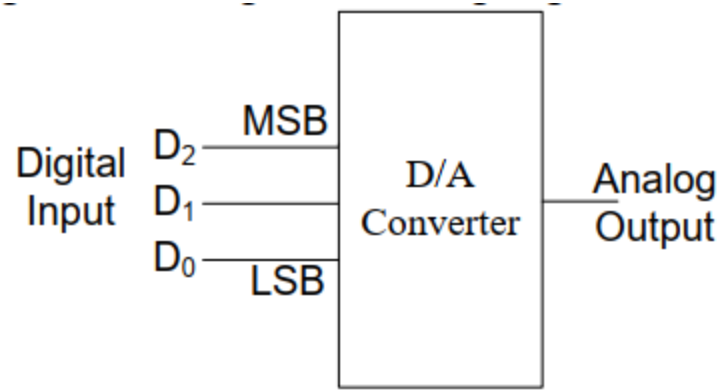
Dither

- In ADC, performance can usually be improved using dither.
- This is a very small amount of random noise (white noise), which is added to the input before conversion.
- The result is an accurate representation of the signal over time.
- A suitable filter at the output of the system can thus recover this small signal variation.
- An audio signal of very low level (with respect to the bit depth of the ADC) sampled without dither sounds extremely distorted and unpleasant.
- Without dither the low level may cause the least significant bit to "stick" at 0 or 1.
- With dithering, the true level of the audio may be calculated by averaging the actual quantized sample with a series of other samples (the dither) that are recorded over time.

DAC(Digital to Analog Converter)

- DAC converts straight binary to analog voltage or current proportional to the digital value.
- DAC can be broadly classified in three categories: Current Output, Voltage Output and Multiplying Type.
- Voltage output DAC is comparatively slower than Current output DAC because of the delay in converting the current signal into voltage signal.

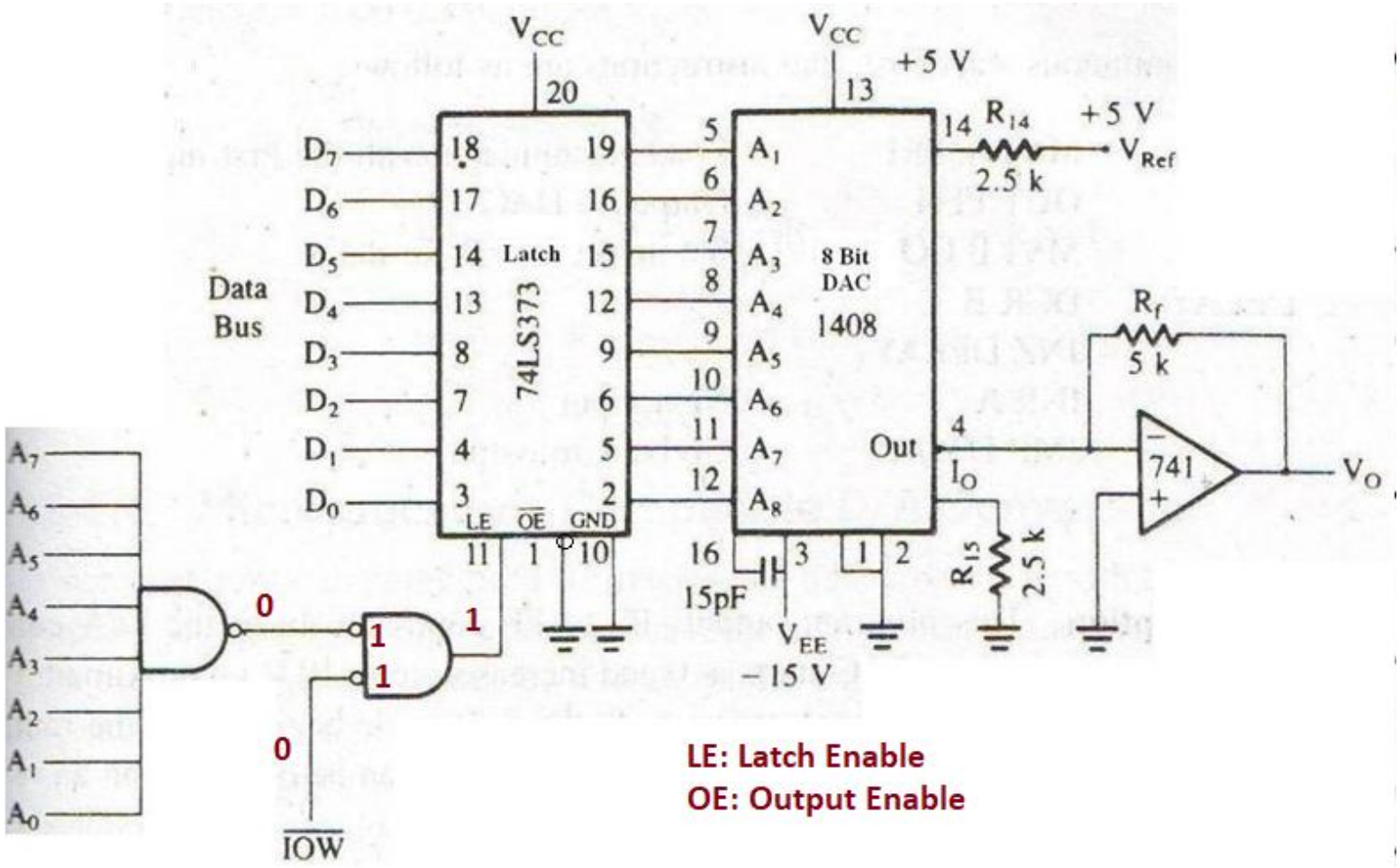




- The three input lines D_2, D_1 and D_0 can assume 8 input combinations from 000 to 111.
- If the full scale analog voltage is 1V, the smallest unit or the LSB (Least Significat Bit) 001_2 is equivalent to $1/2^n$ of 1V. This is defined as resolution. Here, LSB $(001)_2 = 1/8$ V.
- The MSB (Most Significat Bit) represents half of the full scale value. Here, MSB $(100)_2 = 1/2$ V.
- For the maximum input signal $(111)_2$, the output signal is equal to the value of the full scale input signal minus the value of 1 LSB input signal. Here, maximum input signal $(111)_2$ represents $(1 - 1/8) = 7/8$ V.

Interfacing 8-Bit DAC with 8085

Design an output port with the address FFH to interface the 1408 DAC that is calibrated for 0-10V range.



The total reference current source is determined by resistor R_{14} and the voltage V_{ref}. The resistor R_{15} is generally equal to R_{14} to match the impedance of the reference source.

The output $\mathbf{I_0}$ is calculated as

$$I_O = V_{Ref}/R_{14}\,(A_1/2 + A_2/4 + A_3/8 + A_4/16 + A_5/32 + A_6/64 + A_7/128 + A_8/256)$$

Since $I_0 R = \frac{V\text{ref}}{2^n} D$

For full scale input,

$I_O = 5V/2.5K\ (1/2 + ¼ + 1/8 + 1/16 + 1/32 + 1/64 + 1/128 + 1/256)$

$= 2mA\ (255/256)$

$= 1.992mA$

Output voltage,

$V_O = I_O * R_F$

$= 2mA\ (255/256) * 5K$

$= 9.961V$

b. **Write a program to generate a continuous ramp generator.**

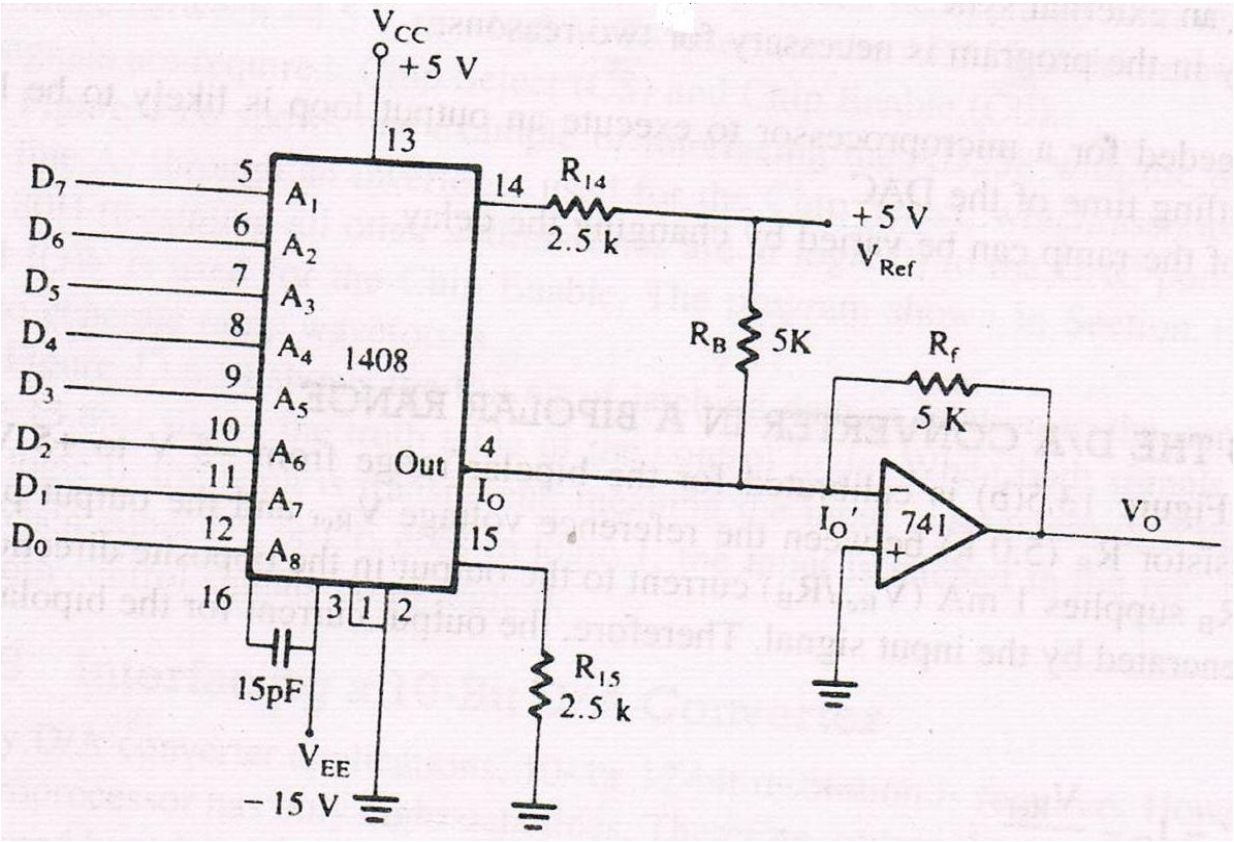
Solution:

```
        MVI A,00H       ; Load accumulator with the first input
DTOA:   OUT FFH         ; Output to DAC (FF is port address)
        MVI B,COUNT     ; Setup register B for delay
DELAY:  DCR B
        JNZ DELAY
        INR A           ; Next input
        JMP DTOA        ; Go back to output
```

- **Program Description:** This program outputs 00 to FF continuously to the DAC. The analog output of the DAC starts at 0 and increases up to 10 V (approx.) as a ramp. When the accumulator contents go to 0, the next cycle begins; thus the ramp signal is generated continuously. The ramp output of the DAC can be observed on an oscilloscope with an external sync.

- The delay in the program is necessary for two reasons;
  - The time needed for a microprocessor to execute an output loop is likely to be less than the settling time of ADC
  - The slope of the ramp can be varied by changing the delay.

Explain the operation of the 1408 which is calibrated for a bipolar range ± 5 V. Calculate output voltage V_0 If the Input is 10000000_2



The 1408 is calibrated for the bipolar range from -5V to +5V by adding the resistor R_B (5.0K) between the reference voltage V_{Ref} and the output pin 4. R_B supplies 1mA (V_{Ref}/R_B) current to the output in the opposite direction of the current generated by input signal.

Here, $I_O' = I_O - V_{Ref}/R_B$

When input signal is zero,

$$V_O = I_O' R_F$$
$$= (IO - V_{Ref}/R_B) R_F$$
$$= (0 - 5V/5K) 5K$$
$$= -5V$$

When the input = 1000 0000, output V_O is

$V_O = I_O' R_F$

$= (I_O - V_{Ref}/R_B) R_F$

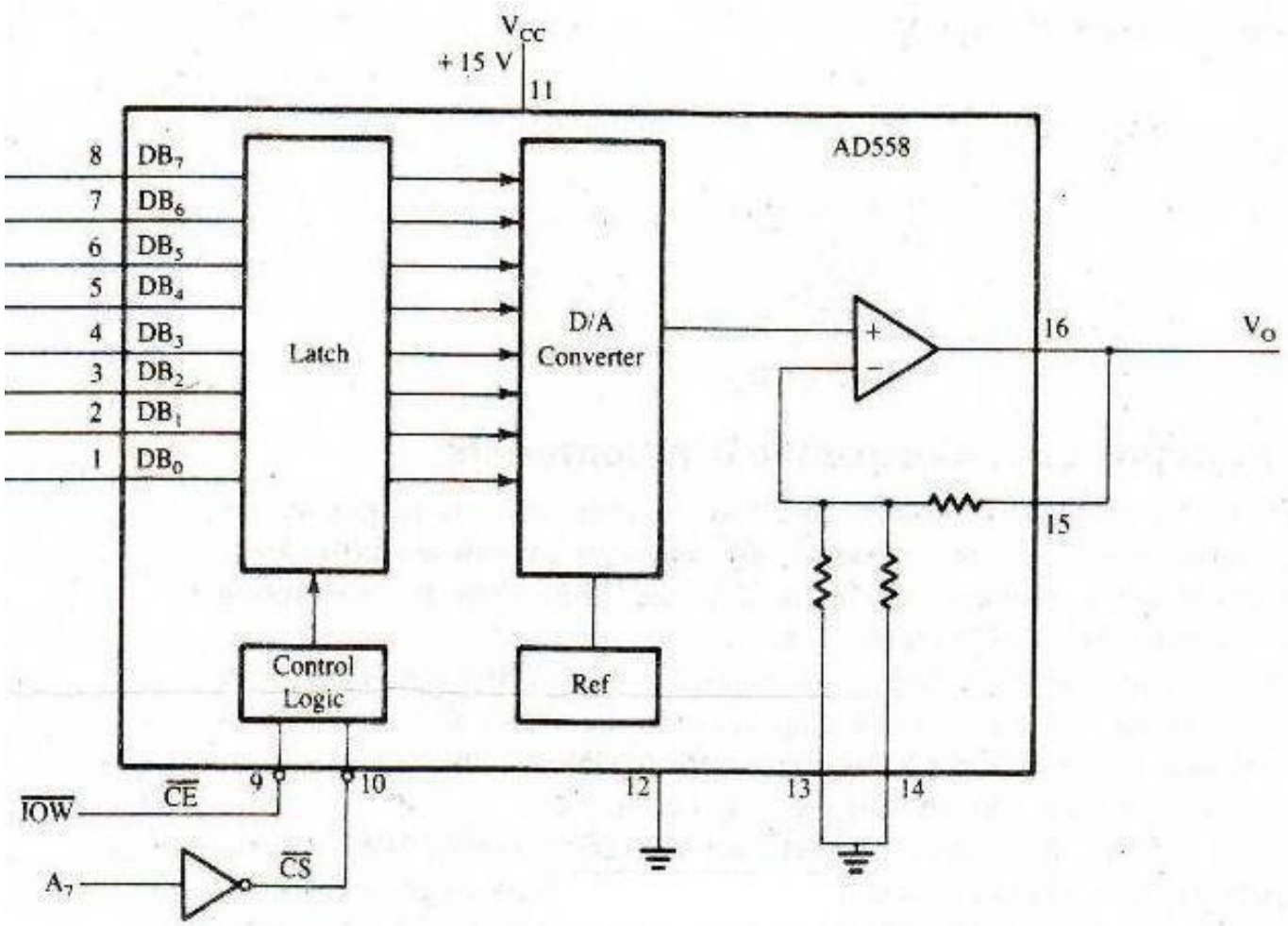
$= (V_{Ref}/R14 * A1/2 - V_{Ref}/R_B) R_F$ [A_8 to $A_2 = 0$]

$= (5V/2.5K * 1/2 - 5V/5K) 5K$

$= (1mA-1mA) 5K$

$= 0V$

Microprocessor Compatible DAC



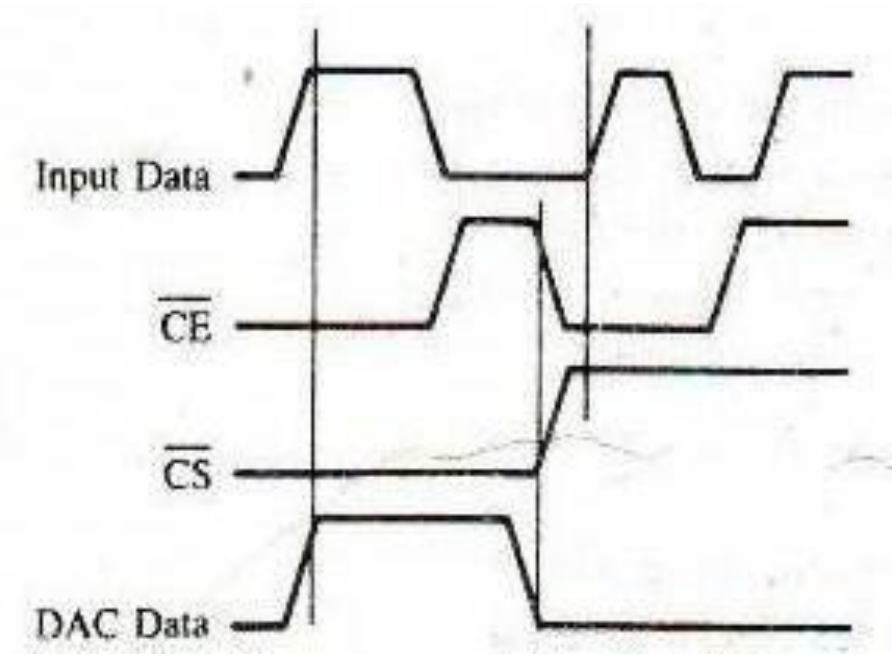
- In response to the growing need for interfacing DAC with the microprocessor, specially designed microprocessor-compatible DAC are available.

- These DAC generally include a latch on the chip, thus eliminating the need for an external latch.

- To interface a device with the microprocessor, two signals are required: Chip Select (*CS'*) and Chip Enable (*CE '*).

- In the figure shown above, the address line A_7 through inverter is used for Chip Select, which assigns port address 80H (assuming all other address lines 0) to the DAC port.

Timing Diagram

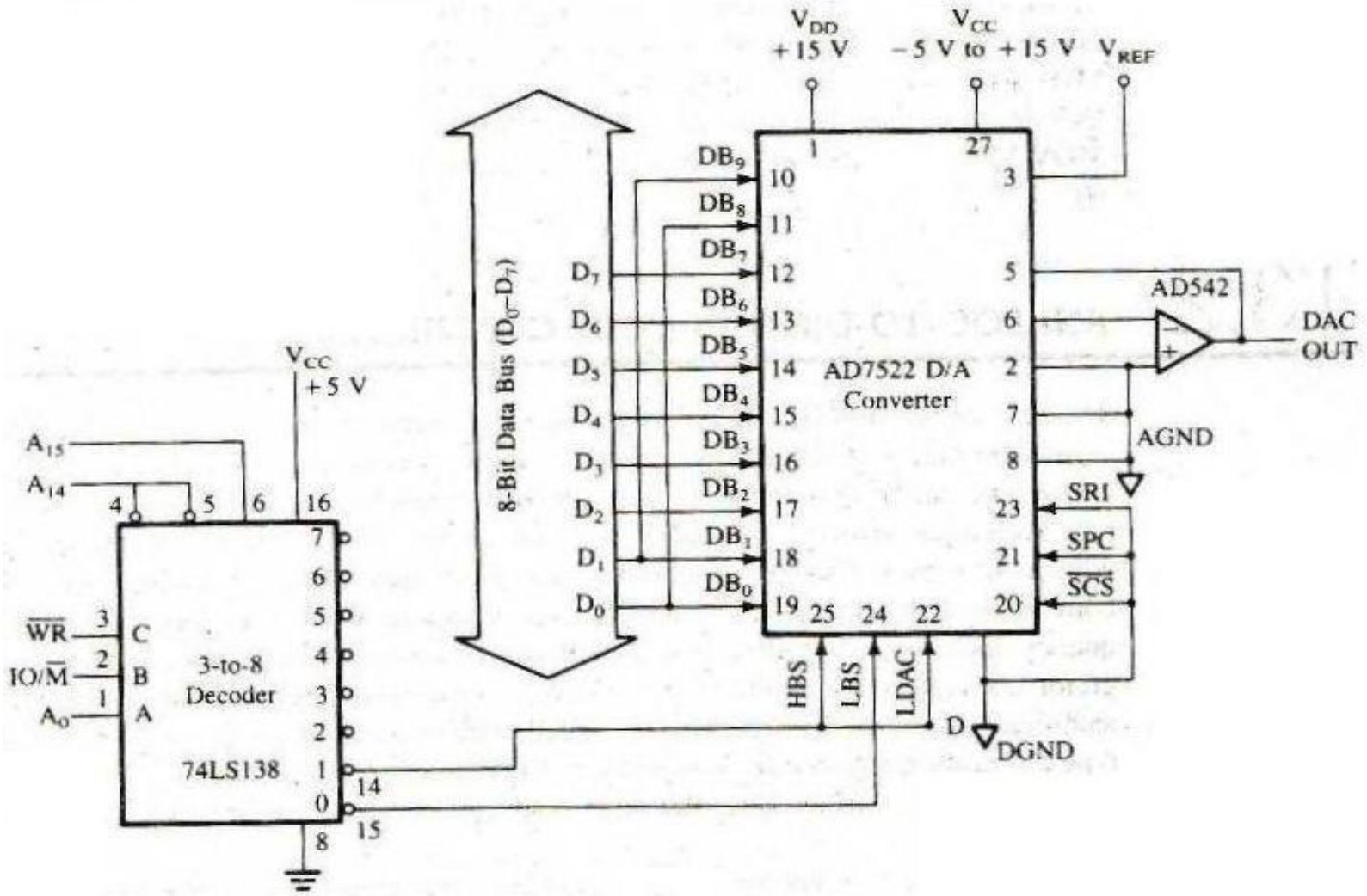


- Figure above shows the timing of latching data in relation to the control signals.

- When both signals *CS'* and *CE'* are at logic 0, the latch is transparent, meaning the input is transferred to the DAC.

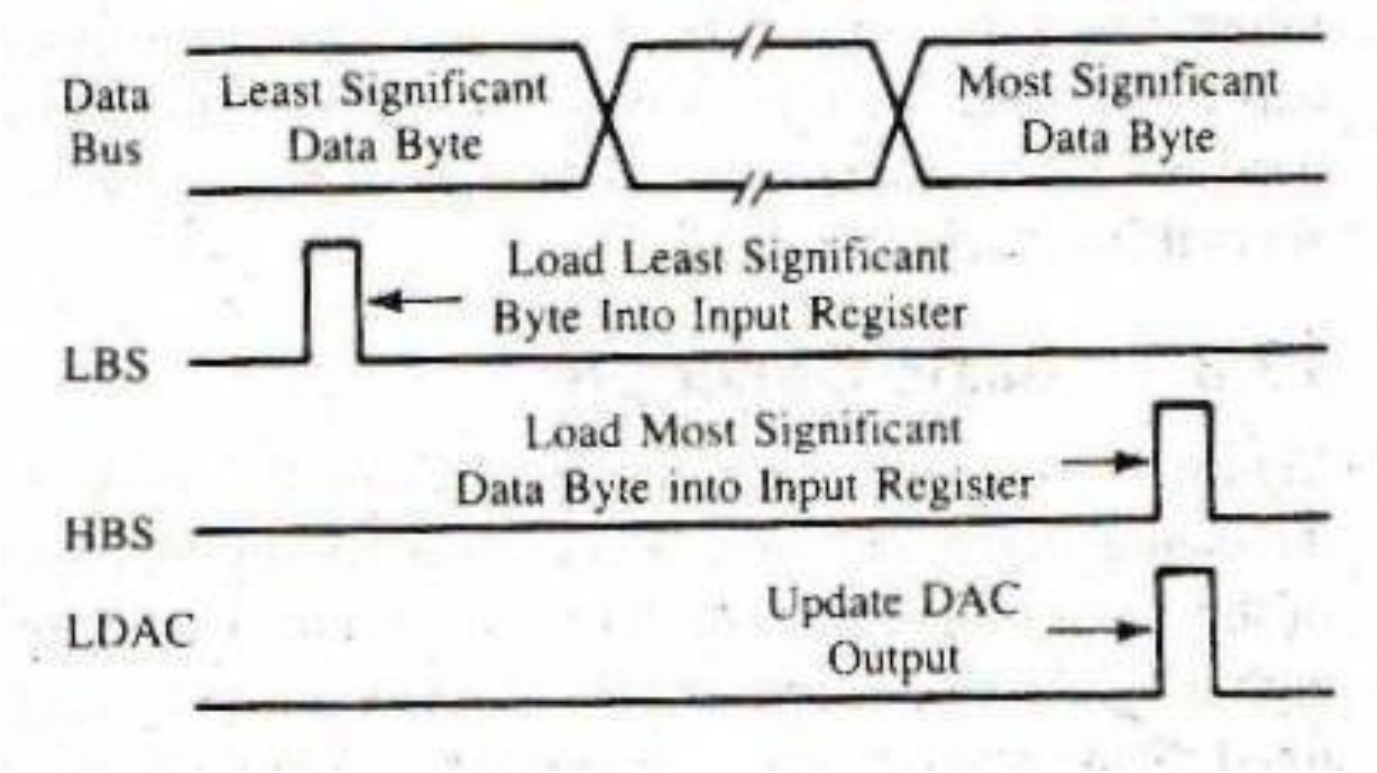
- When either *CS'* or *CE'* goes logic 1, input is latched in the register and held until both control signals go to logic 0.

Interfacing 10-Bit DAC with 8085



- AD7522 is a CMOS 10-bit DAC consists of an input buffer and a holding register.
- 10 bits are loaded into the input register in two steps using two output ports.
- The low-order 8-bits are loaded with the control line LBS and remaining 2-bits are loaded with the control line HBS.
- Then all 10-bits are switched into a holding register for conversion by enabling LDAC line.
- When a data byte is sent to the port address 8000H in a memory map I/O, the *WR'* and IO/*M'* signals go low along with A_0 and the line LBS is enabled.
- Similarly, the address 8001H enables lines HBS and LDAC.

Timing Diagram



Program

LXI B, 03FFH; Load 10-bit at logic 1 in BC register

LXI H, 8000H; Load HL with port address for lower 8-bits

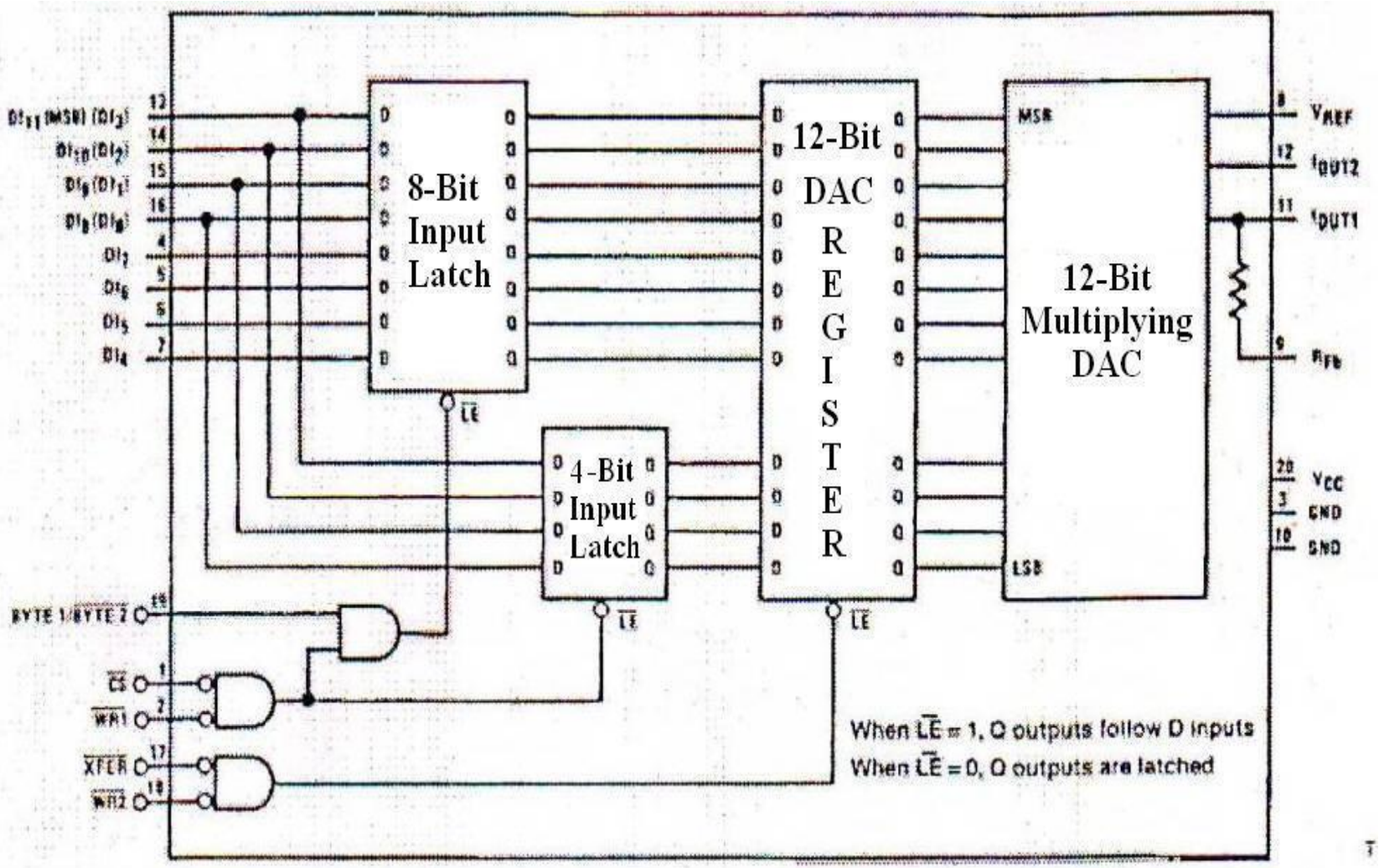
MOV M, C; Load 8-bits D_7-D_0 in the DAC

INX H; Point to port address 8001H

MOV M, B; Load two bits D_9 and D_{10} and switch all ten bits for conversion

HLT

Interfacing 12-bit DAC to 8-bit Data Bus



- The END