AHB_to_APB Bridge Design

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INTRODUCTION

The ARM Advanced Microcontroller Bus Architecture (AMBA) is an open-standard system used to connect and manage different parts of a system-on-chip (SoC) design. AMBA is key in developing multi-processor systems, allowing many controllers and components to communicate through a bus architecture. It is widely implemented in various SoCs, especially in the processors found in today's smartphones and other portable devices.

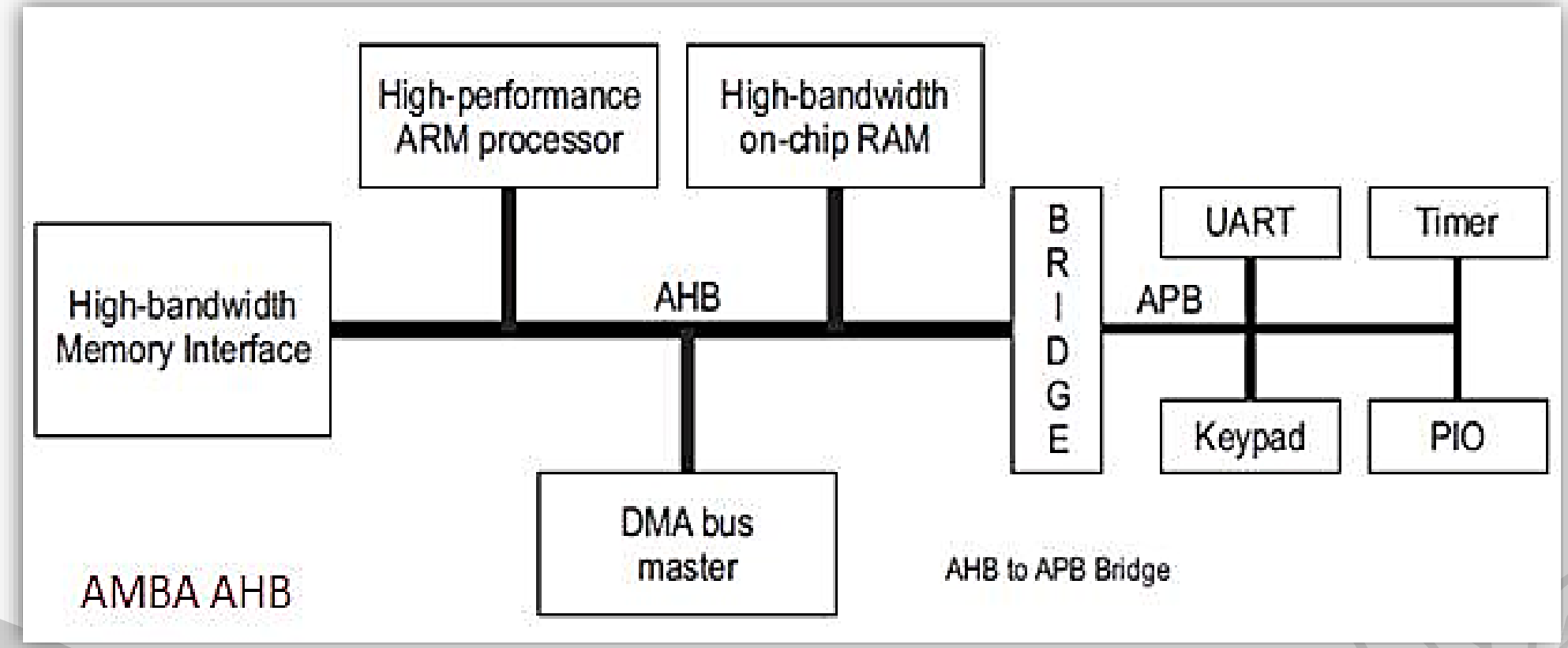
AMBA AHB (Advanced High-performance Bus) is a high-performance bus interface designed to connect key components like masters, interconnects, and slaves within a system. Key features of AMBA AHB include:

- Support for burst data transfers
- Operation on a single clock edge
- A design that does not require tristate signals
- Capability for wide data buses, with options ranging from 64 to 1024 bits

- Typical AHB slave components include internal/external memory interfaces, high-speed peripherals, and bridges to narrower APB buses for lower-speed devices. AHB is frequently used in ARM7, ARM9, and ARM Cortex-M designs. A standard AHB transaction involves two bus cycles: an address phase and a data phase, with no wait states.

- The AMBA APB (Advanced Peripheral Bus) is designed for basic, low-bandwidth tasks such as accessing system peripherals (like Timers, UARTs, and GPIOs). It has a simpler signal set compared to AHB, making it ideal for low-frequency, low-power applications. APB typically uses a 32-bit data width and lacks support for burst transfers.

Architecture



AHB Protocol

- The AMBA AHB bus protocol uses a central multiplexer system where masters issue address and control signals, and an arbiter grants access to the bus.
- A central decoder manages data and response signals, ensuring correct signal selection for the involved slave.
- After receiving access, the bus master starts the transfer by sending address and control signals, which specify the address, transfer direction, width, and whether it's part of a burst operation.
- Data moves from the master to the slave through a write data bus and from the slave back to the master through a read data bus.

Each data transfer involves:

- An address and control phase
- One or more data phases

THE ADDRESS PHASE MUST BE DONE IN A SINGLE CYCLE, MEANING ALL SLAVES MUST CAPTURE THE ADDRESS IMMEDIATELY. HOWEVER, THE DATA PHASE CAN BE EXTENDED USING THE HREADY SIGNAL. WHEN HREADY IS LOW, WAIT STATES ARE ADDED TO THE TRANSFER, GIVING THE SLAVE MORE TIME TO EITHER PROVIDE OR CAPTURE THE DATA.

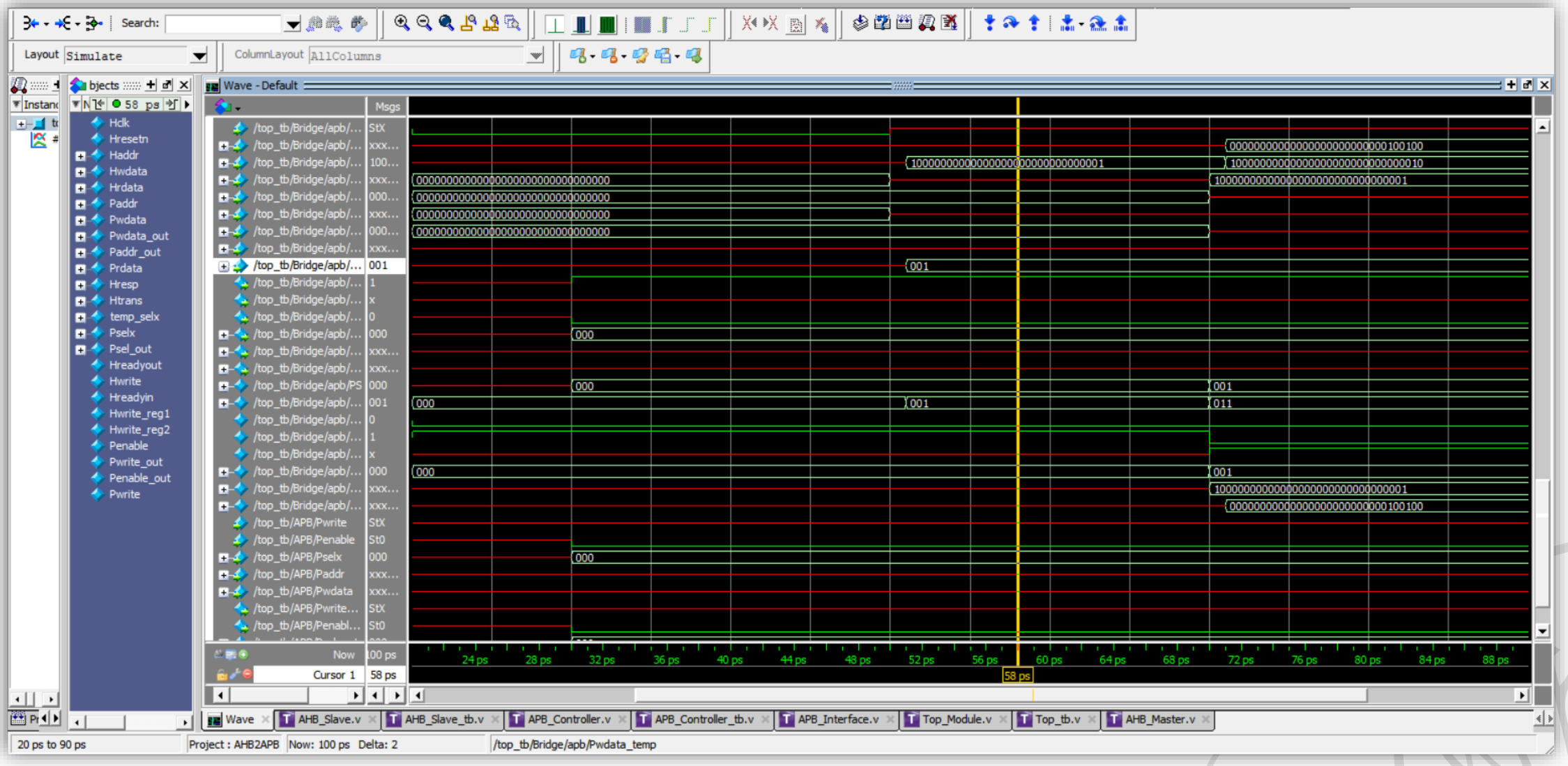
APB Protocol

The AMBA APB (Advanced Peripheral Bus) is designed for economical operation, focusing on low power use and ease of integration. It's suited for peripherals with low data transfer requirements that don't demand the high performance of pipelined interfaces. The APB operates with an unpipelined protocol, where signal transitions align with the rising edge of the clock, simplifying integration into different systems. In the AMBA2 specification, each transaction requires two clock cycles, with newer versions potentially needing more cycles.

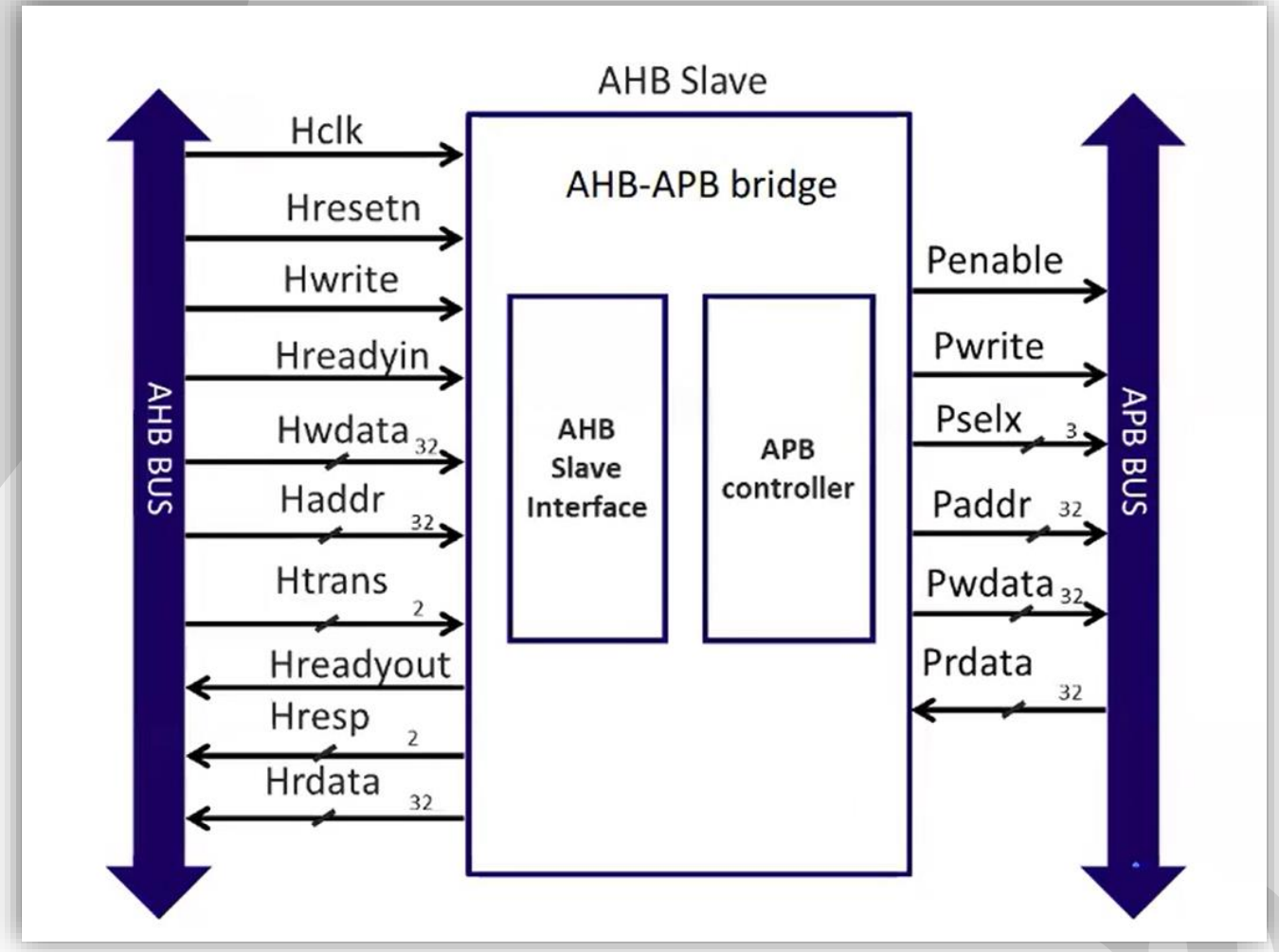
AHB2APB Bridge

- The AHB-to-APB Bridge acts as an AHB slave, converting high-speed AHB operations into lower-speed APB transactions, introducing wait states if the AHB pauses for APB operations.
- It enables communication between high-speed AHB devices and slower APB peripherals by managing signal and protocol conversions, ensuring smooth data transfer between the systems.

Simulation Waveform :



Block Diagram



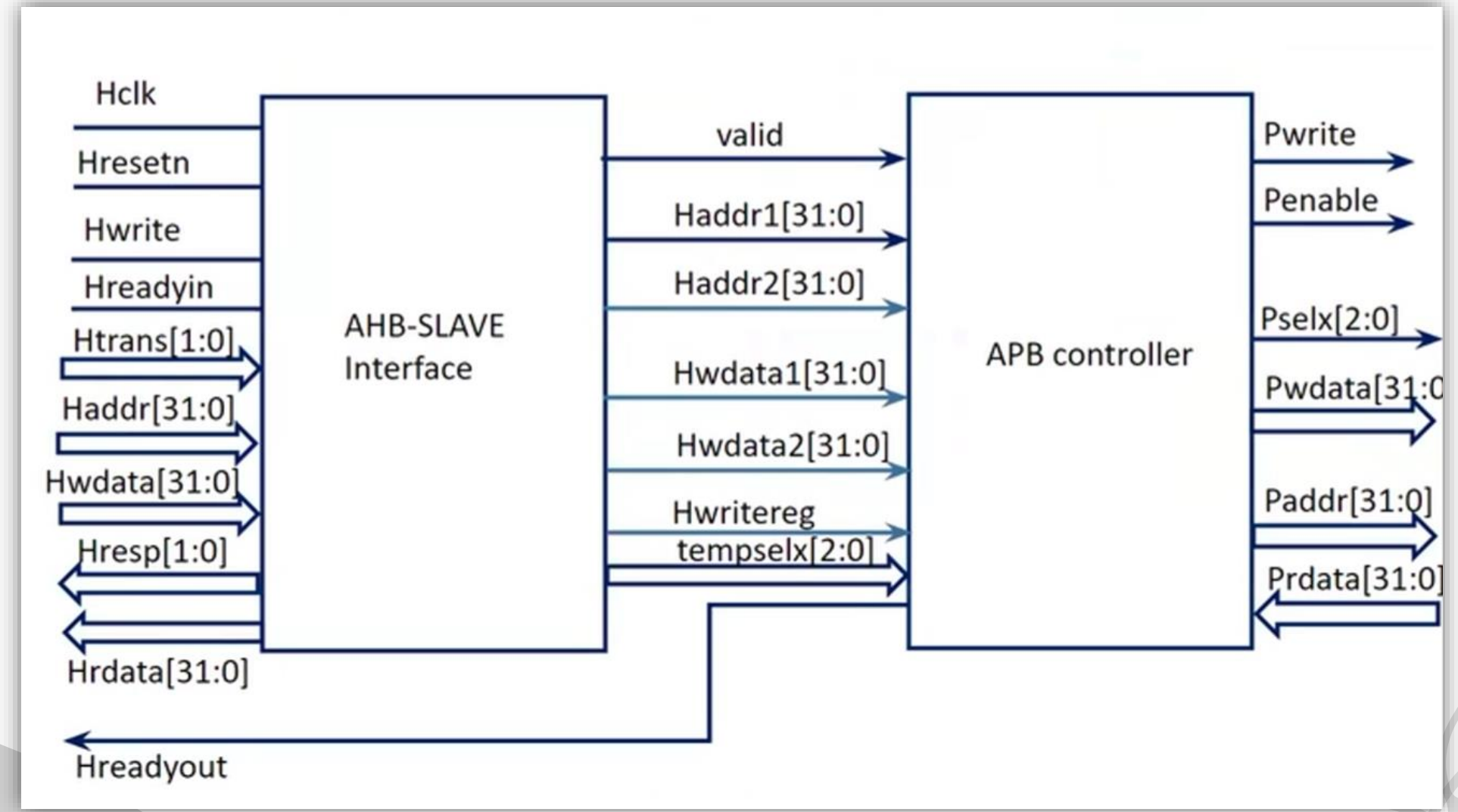
Specifications : AHB Signals

Signal Name	Description
HRESET	The bus reset signal is active LOW and is used to reset the system and the bus. This is the only active LOW signal.
HADDR	The 32-bit system address bus.
HTRANS	Indicates the type of the current transfer, which can be NONSEQUENTIAL, SEQUENTIAL, IDLE or BUSY.
HWRITE	When HIGH this signal indicates a write transfer and when LOW a read transfer.
HRDATA	The write data bus is used to transfer data from the master to the bus slaves during write operations. A minimum data bus width of 32 bits is recommended. However, this may easily be extended to allow for higher bandwidth operation.
HCLK	This clock times all bus transfers. All signal timings are related to the rising edge of HCLK.

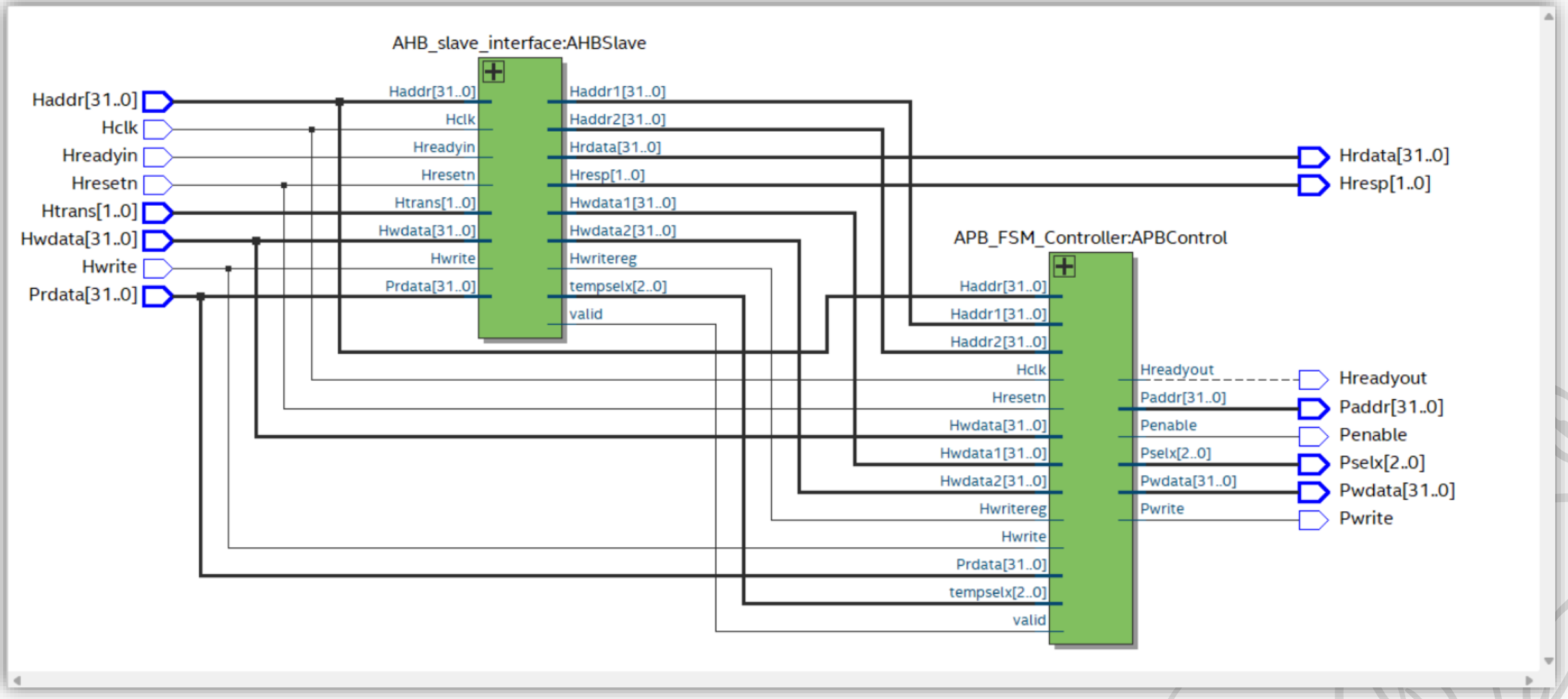
Signal Name	Description
HRDATA	The read data bus is used to transfer data from bus slaves to the bus master during read operations. A minimum data bus width of 32 bits is recommended. However, this may easily be extended to allow for higher bandwidth operation.
HREADY	When HIGH the HREADY signal indicates that a transfer has finished on the bus. This signal may be driven LOW to extend a transfer. Note: Slaves on the bus require HREADY as both an input and an output signal.
HRESP	The transfer response provides additional information on the status of a transfer. Four different responses are provided, OKAY, ERROR, RETRY and SPLIT.

Specifications : APB Signals

Signal Name	Description
PENABLE	This strobe signal is used to time all accesses on the peripheral bus. The enable signal is used to indicate the second cycle of an APB transfer. The rising edge of PENABLE occurs in the middle of the APB transfer.
PADDR	This is the APB address bus, which may be up to 32-bits wide and is driven by the peripheral bus bridge unit.
PWRITE	When HIGH this signal indicates an APB write access and when LOW a read access.
PRDATA	The read data bus is driven by the selected slave during read cycles (when PWRITE is LOW). The read data bus can be up to 32-bits wide.
PWDATA	The write data bus is driven by the peripheral bus bridge unit during write cycles. The write data bus can be up to 32-bits wide.
PSELx	A signal from the secondary decoder, within the peripheral bus bridge unit, to each peripheral bus slave x. This signal indicates that the slave device is selected and a data transfer is required. There is a PSELx signal for each bus slave.


Hclk
Hresetn
Hwrite
Hreadyin
Htrans[1:0]
Haddr[31:0]
Hwdata[31:0]
Hresp[1:0]
Hrdata[31:0]
Hreadyout
AHB-SLAVE
Interface
valid
Haddr1[31:0]
Haddr2[31:0]
Hwdata1[31:0]
Hwdata2[31:0]
Hwritereg
tempselx[2:0]
APB controller
Pwrite
Penable
Pselx[2:0]
Pwdata[31:0]
Paddr[31:0]
Prdata[31:0]

Synthesis of Project



Conclusion :

- The AHB2APB bridge is crucial in VLSI and SoC designs, connecting high-speed AHB subsystems with lower-speed APB components.
- Understanding this bridge involves recognizing the differences between AHB and APB protocols in terms of complexity, speed, and functionality.
- Studying the bridge provides insights into protocol translation, address decoding, and timing alignment, which are essential for optimizing system performance and power efficiency in digital systems.

Thank You