

# The LNMIIT

## Microprocessor and Interface

### Quiz-1

- Note:**
1. Manage the time.
  2. Use the keywords rather than giving general descriptions.
  3. Draw DIA, flowcharts, etc. where ever required.

**Marks: 10**

**Time: 40 Mins**

**Date: 05/Sep/2018**

Q1. Explain the following:

- a) System Bus
- b) Control Unit
- c) Microprocessor

Q2. Discuss Moore's Law.

Q3. Explain the following:

- a) S0 and S1
- b) HOLD and INTA
- c) Reset out and Ready

(16245119)

**The LNM Institute of Information Technology, Jaipur**  
 (Deemed to be University)  
**Supplementary Copy**

Name Vishakha Phaniwani

Roll No 16UEC126

Subject Microprocessor

Date 5/9/18

Signature 

(a) System Bus

System Bus includes Address Bus and Data Bus.  
 Address is of 16 bits and Data of 8 bits in microprocessor 8085

A<sub>0</sub> - A<sub>7</sub> → represent data Bus ✓

A<sub>0</sub> → A<sub>15</sub> → For address Bus ✓

When ALE (Address Latch Enable) is 1 then Pins A<sub>0</sub> → A<sub>7</sub> also act as address Bus. When ALE is 0 then A<sub>0</sub> → A<sub>7</sub> → Data Bus  
 A<sub>8</sub> → A<sub>15</sub> → Address Bus

System Bus is a link of communication between microprocessors or CPU or memory and I/O device.

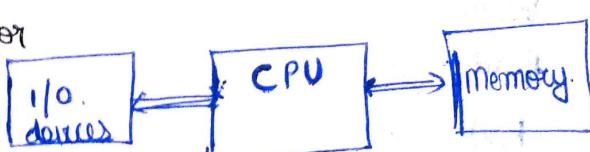
Address Bus is used to location of information.

Data Bus is used to store or receive data from memory or I/O devices

(b) Control Unit

→ It is responsible for control operations like I/O/M, R/W etc.  
 e.g. when ~~process~~ opcode fetch is performed then once CPU gets to the location of data in memory then TCU send instruction for read and only them Data is fetched and send to IR and then to Decoder.

(c) Microprocessor



**Microprocessor:** It is an electronic device which is clock driven and capable of performing decisions / task after taking instructions given to it and capable of storing and extracting information.

Microprocessor is called so because it takes microseconds to perform task. It is a general purpose device used in many applications.

First microprocessor invented was 4004

In 1961

4004, 4008, 8080, 8085, 8086  
↓  
4 bit                  8 bit                  16 bit

### Q2) Moore's Law

In 1965 Moore stated that number of transistors produced will double in every year.

In 1975 Revised moore's law came that stated the number of transistors produced will double in every 18 months.

In 1995 It stated that both microprocessor and memory agree and follow revised moore's law.

371

### Q3 (a) So & S1

		Instruction
S1	S0	
0	0	HLT ✓
0	1	Write ✓
1	0	Read ✓
1	1	Fetch ✓

S0 & S1 are the select lines whose combination specifies which instruction is to be performed i.e. whether Read or Write or Fetch or HLT operation is performed.

(b) HOLD → It is a kind of interrupt which has highest priority among all the interrupts.  
Whenever some other sudden or urgent task is to be performed then HOLD comes.

When CPU acknowledges this HOLD it does HLDA.  
For example when DMA ask CPU to give it control of System bus to perform some sudden tasks. Then HOLD instruction is sent to CPU

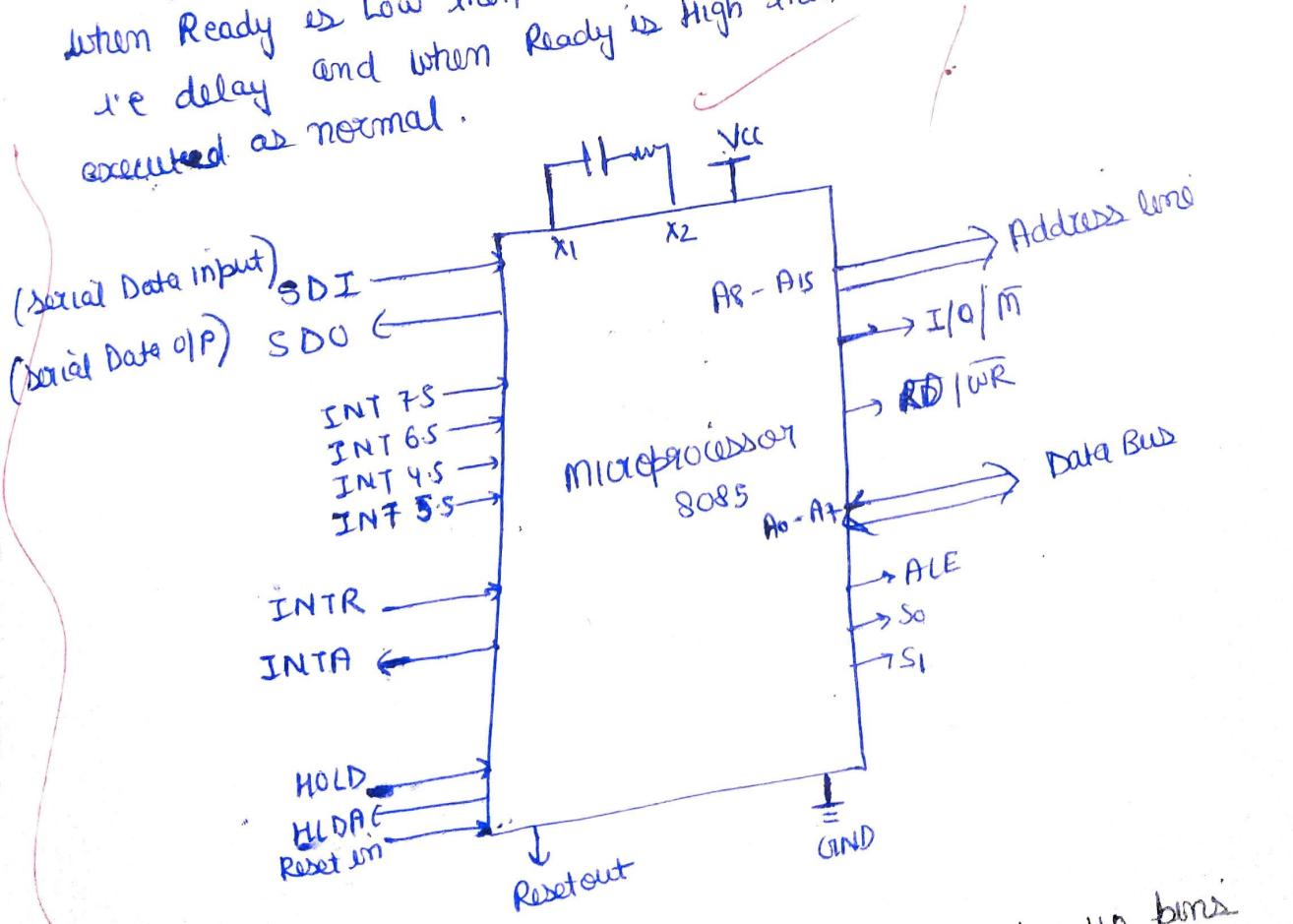
q DMA ~~does~~ does HOLD

INTA → It is Interrupt Acknowledgement.  
Whenever any interrupt comes and if CPU suspends it then it does INTA

(c) Reset Out  
Whenever Reset Out is high then all the devices connected to microprocessor get Reset.

Ready

When Ready is Low then microprocessor is send to a condition of wait i.e. delay and when Ready is High then all instructions are get executed as normal.



Microprocessor 8085 has 40 pins

**The LNMIIT  
Microprocessor and Interface  
Quiz-2**

**Note:** 1. Manage the time.

2. Use the keywords rather than giving general descriptions.
3. Draw DIA, flowcharts, etc. where ever required.

**Marks: 10**

**Time: 40 Mins**

**Date: 17/Sep/2018**

Q1. What is addressing? Explain the advantages and its applications. 2

Q2. Why binary number system<sup>is</sup> most commonly used in computers rather than hexadecimal, BCD etc. 2

Q3. Discuss classification of Instruction format. 1

Q4. Explain the following with respect to 8086. 5

- a) ES
- b) CX
- c) DI
- d) IP
- e) SS

**The LNMIIT**  
**Electronics and Communication Engineering**  
**Midsem Exam**

Marks: 60

Microprocessor and Interface

Duration: 90 Minutes

**Note:** Manage your time  
 Date: 27/09/18

**Q1.** Discuss the evolution of semiconductor technology and classifications of computer architecture.

8

**Q2.** Explain the difference between 8085 and 8086 microprocessors with the help of ISA.

10

**Q3.** What is the function of:

- a) IR
- b) Temp Reg
- c) Opcode fetch cycle
- d) BIU and EU in 8086

(1+2+3+4)

**Q4.** Explain the flag registers in 8086 microprocessor.

5

**Q5.** Explain the following addressing modes with the help of suitable examples:

- a) Relative addressing
- b) Difference between Index and Base addressing
- c) Page Addressing
- d) Register Indirect Addressing

(2+3+3+1)

**Q6.** Explain RIM and SIM instruction in detail. Assuming the microprocessor is completing RST 7.5 interrupt request. Check weather RST 5.5 and 6.5 is pending or not, if pending, enable both without affecting RST 7.5, otherwise return to the main program.

10

**Q7.** Explain the following instructions:

(2+2+2+2)

- a) XTHL and SPHL
- b) DAA and DAD rp
- c) RRC and RAL
- d) RET and JMP addr

The LNMIIT  
Microprocessor and Interface  
ECE331-MICROI  
End Semester Exam

**Note:** 1. Manage the time properly.

2. Use keywords rather than giving general descriptions.
3. Draw diagrams, flowcharts, etc. wherever required.

**Marks:** 100  
**Time:** 3 hours  
**Date:** 28/11/2018

**Q1.** Explain the following with the help of examples 10

- a) Status Manipulation Instructions
- b) Program manipulation Instructions
- c) Miscellaneous Instructions

**Q2.** Draw the timing Diagram of the following Instruction 20

- a) JP 8550
- b) CNZ 9001 (if true)
- c) STAX rp
- d) DAA

**Q3.** Draw the state transition diagram and explain 15

- a) HOLD and HLDA signals
- b)  $T_{hold}$ ,  $T_{wait}$  and  $T_{reset}$
- c) Interrupt handling
- d) HALT

**Q4.** How to eliminate the speed related incompatibilities, explain it with the help of read access and write access diagrams. 10

**Q5.** Explain the following: 20

- a) 16 x 2 LCD display and 7 segment
- b) 8253
- c) 8259
- d) Application of Addressing modes and Relative addressing

**Q6.** Draw and explain: 15

- a) Mode 1 of 8255
- b) Mode 2 of 8255
- c) DMA based Data Transfer
- d) Software and hardware polling

**Q7.** Explain the Hardware interrupt with the help of a diagram. Also discuss how microprocessor executes hardware and software interrupts. 10

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## Instruction to Candidate (for examination)

1. Immediately on receipt of the Test Booklet the candidate will fill in the required particulars on the cover page with Ball Point Pen only.
2. Candidates shall maintain perfect silence and attend to their Question Paper only. Any conversation or gesticulation or disturbance in the Examination Room Hall shall be deemed as misbehaviour. If a candidate is found using unfair means or impersonating, it shall be treated as breach of code of conduct and the matter dealt with accordingly.
3. No candidate, without the special permission of the Invigilator concerned, will leave his her seat or Examination Room until the full duration of the paper is over. Candidate should not leave the room hall without handing over their Answer Sheets to the Invigilator on duty.
4. During the examination time, the invigilator will check ID Card of the candidate to satisfy himself / herself about the identity of each candidate. The invigilator will also put his her signature in the place provided in the Answer Sheet.
5. The Candidate shall fill the number of supplementary sheets attached, on the front page of the main answer sheet.
6. **Bringing cell phones/communication devices in the examination hall is strictly prohibited. Exam conducting authority will not be responsible for the custody of such articles. However, use of scientific calculator is permitted.**

Name of the student: Vishakha Shanwani.....

Roll No. : ...16U.E.C.126.....

Name of Examination : ...3rd Term.....

Subject : ...MICRO-I.....

Day & Date : ...Thursday, 27/9/18.....

No. of Supplementary Sheets Attached: .....

  
Student's Signature

  
Invigilator's Signature

Question No.	Marks Obtained
1	7
2	9
3	10
4	5
5	7
6	10
7	8
8	10
9	
10	
Total Marks	56/60

- (1)
- Q1 Evolution of Semiconductor Technology
- 9m 1947 → First Transistor was invented
  - 1959 → Invention of 1<sup>st</sup> Integrated Circuit
  - 1971 → Invention of First microprocessor (Intel 4004)
  - 1979 → Invention of First Microcontroller (8048)
  - 1965 → Birth of Moore's Law

Year	Invention	Size	Technology
1947	Transistor	1	
1950 - 1960	Discrete Components	1	Tunnel diodes
1960 - 1965	SSI	10 - 100	Logic gates, Flip Flops
1966 - 1970	MSI	100 - 1K	MUX, Adder
1971 - 1979	LSI	1K → 20K	8 bit RAM, ROM
1980 - 1984	VLSI	20K → 50K	DSP, 16 bit, 32 bit mcu, MPU
> 1985	ULSI	> 50K	64 Bit Technology

Elynn's Taxonomy

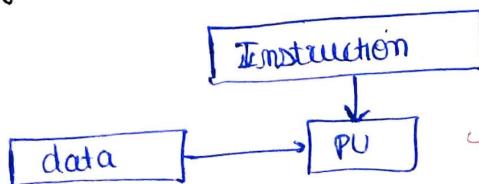
Classification of Computer Architecture

It is based on concurrent instructions and data streams

Based on → Organization

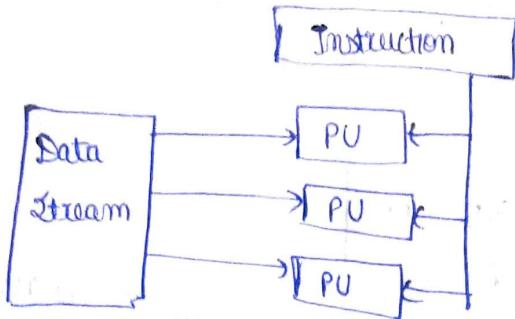
- Functionality
- Implementation of Computer System

SISD (Single Instruction Single Data)



Classical Von-Neumann Architecture

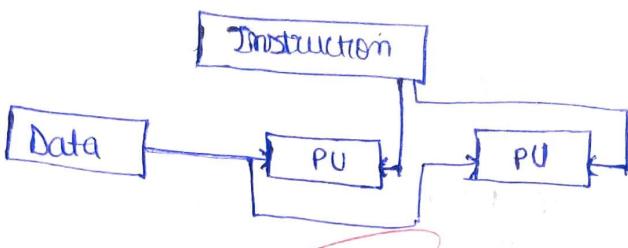
## SIMD (Single Instruction multiple data) (2)



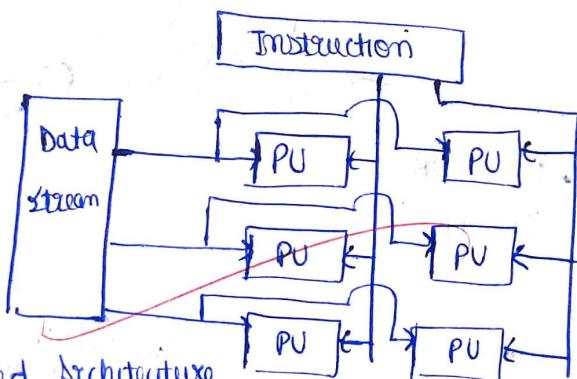
- Array processor
- GPU
- multiple data set
- executed using single instruction
- Parallelized Structure

## MISD (multiple Instruction single Data)

• Not used



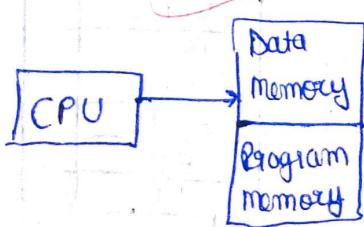
## MIMD (multiple Instruction multiple data)



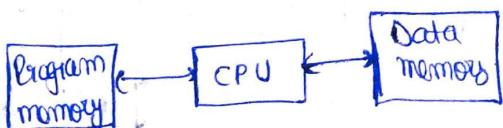
- It is widely used architecture
- Supports multiple processes simultaneously
- Shared memory system
- Distributed memory system
- may send results to control location

(7)

## Von Newman Architecture



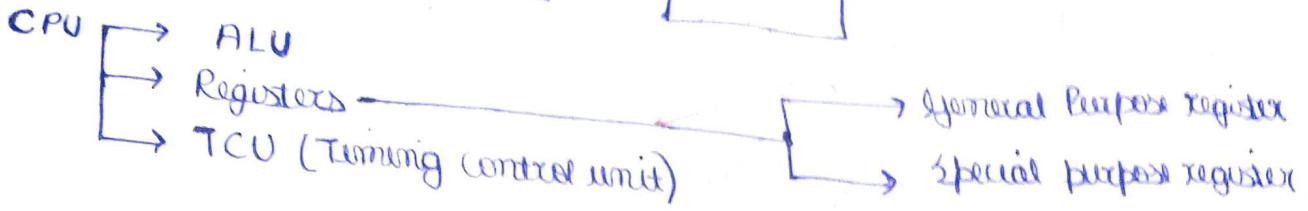
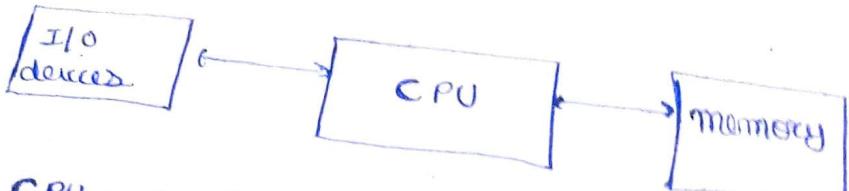
## Harvard Architecture



RISC & CISC.

gr For 8085

(3)



ALU → Performs following operations.

- Arithmetic → Add, Sub, INR, DCR
- Logical → AND, NOT, OR, EXOR
- Branching → JMP, CALL, RET

General Purpose Registers

→ B, C, D, E, H, L

all are 8 bit registers

Special purpose register

→ Accumulator

→ Program Counter

→ Stack Pointer

→ Status Register (S, Z, AC, P, CY)

TCU → Control signals • RD • WR  
→ Status Signals S<sub>0</sub>, S<sub>1</sub>, 101̄m

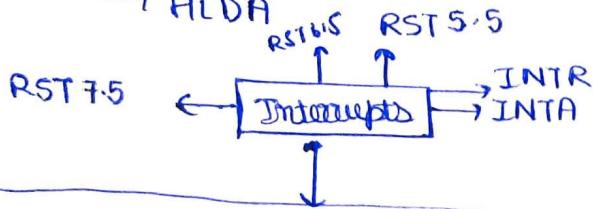
→ ALE

→ READY

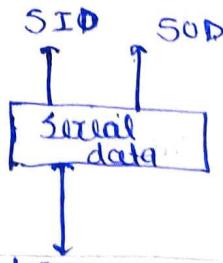
→ RESET IN

→ HOLD

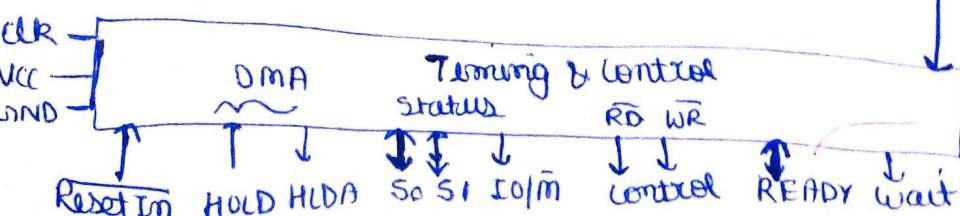
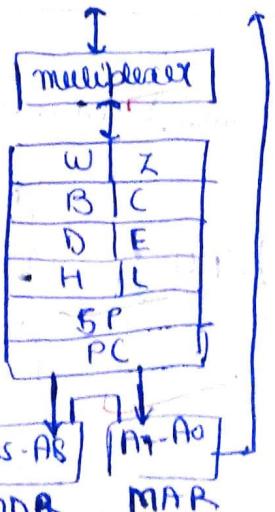
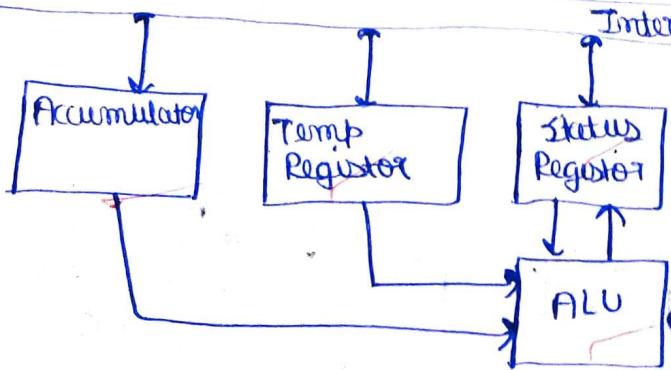
→ HLDA



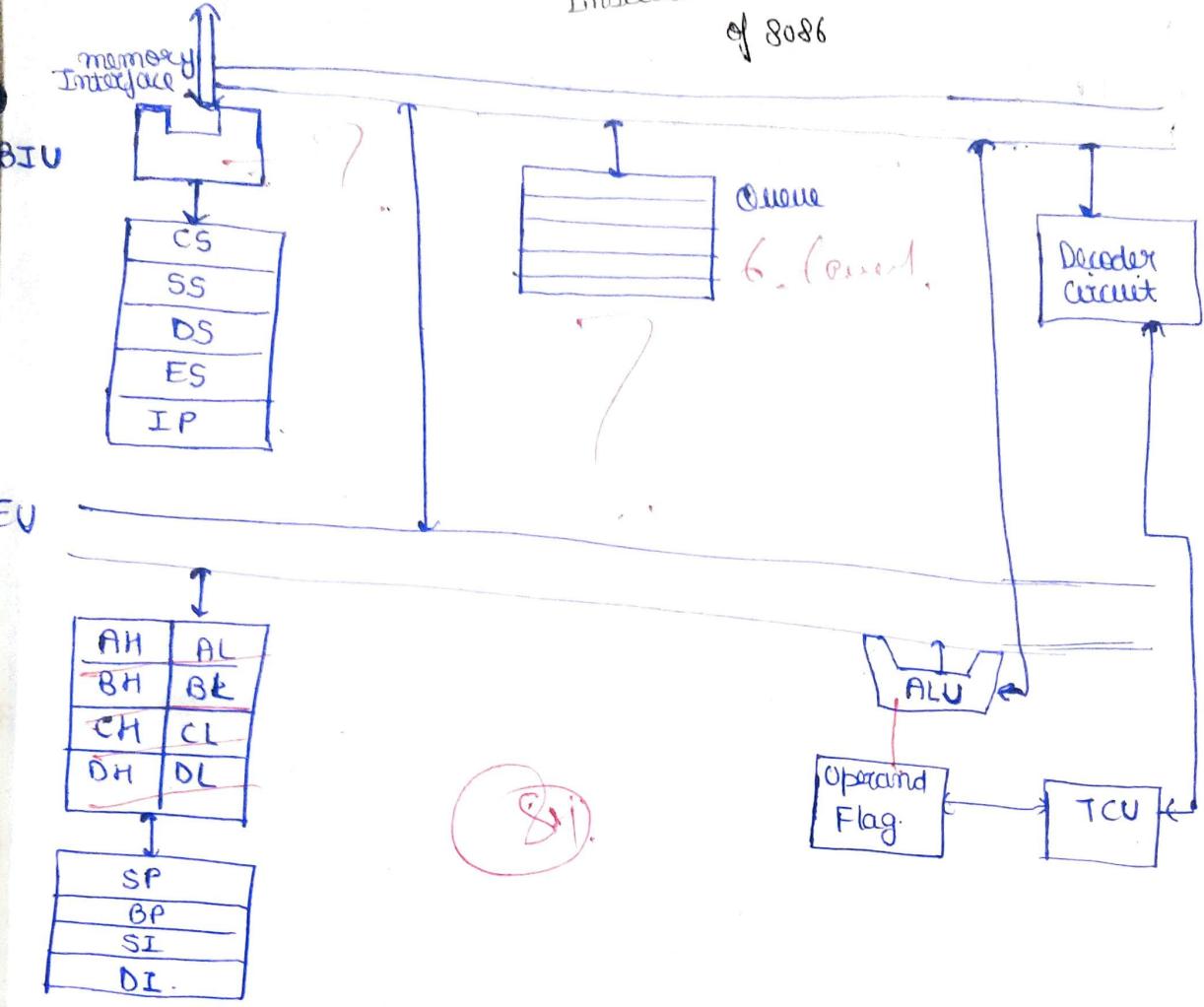
Instruction Set Architecture of 8085



Internal Bus

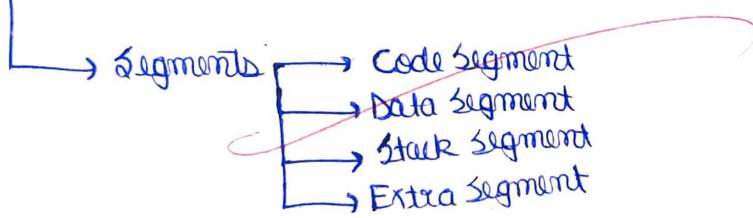


# Instruction Set Architecture of 8086



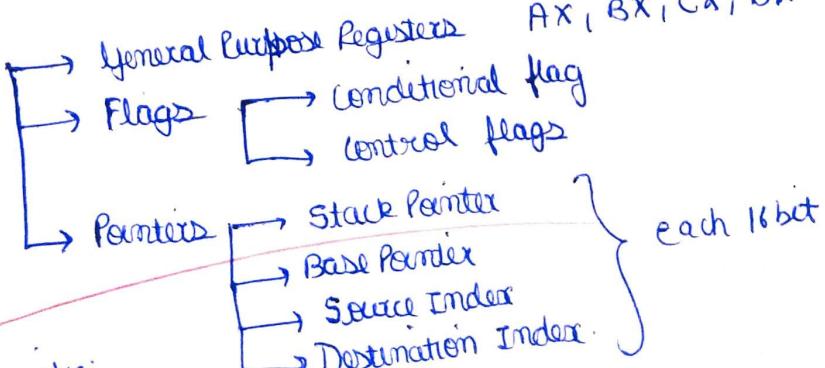
It consists of • BIU (Bus ~~use~~ interface) has control of address bus, data bus & control bus.

BIU → Queue



BIU Fetches the instruction from memory and store it in Queue while EU performs execution.

• EU (Execution Unit)

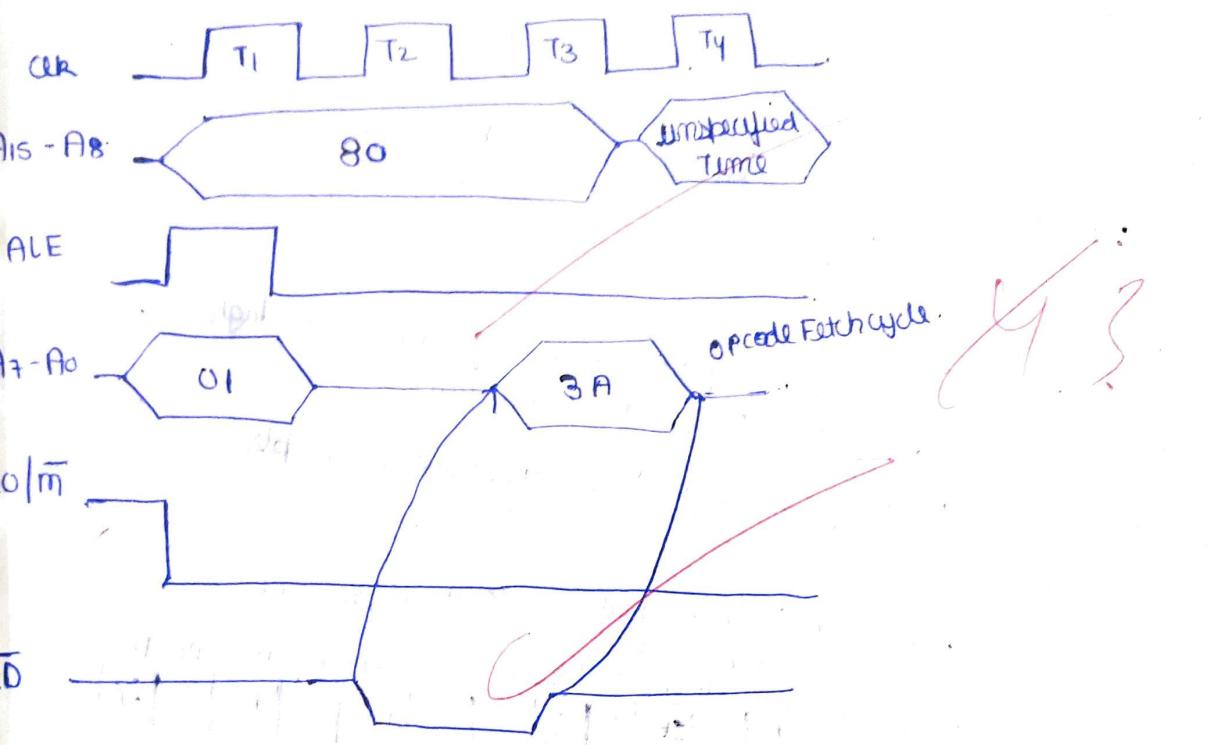


EU performs all Arithmetic & logic operations

Ques 3 (a) IR (Instruction Reader) ⑥  
After fetching instructions from memory IR decodes the instruction and decide it before sending it to ALU for execution.

(b) Temp Register: When execution process is undergoing it holds data temporarily after IR decodes the instruction, the decoded format is send to ALU. ②

c) Opcode fetch cycle: This cycle has 4T states and is used to fetch opcode from instruction which is stored in memory. ③  
8001 → 3A



d) BIU (Bus Interface Unit) ④  
It consists of system bus. While EU perform execution task, BIU fetches the instructions from memory and stores them in queue. It is then taken by EU whenever required.

BIU also consists of various segments.

- Code Segment
- Stack Segment
- Data Segment
- Extra Segment

All these are 16 bit register and contains address of 64 KB segment.

EU (Execution Unit).

It performs all Arithmetic and Logic operations required.  
It consists of

- Flags
- GPR
- Pointers

Ex...  
fetch, decode & execute

Ques (a) Conditional Flags

**Zero Flag :** It indicates whether result of any arithmetic operation is zero or not. Thus it is high i.e. set when result is zero else reset.

**Sign Flag :** This is set when result of addition or subtraction or etc is negative and is Reset when result is positive.

**Parity Flag :** This flag is set if number of high bits are even and reset when number is odd.

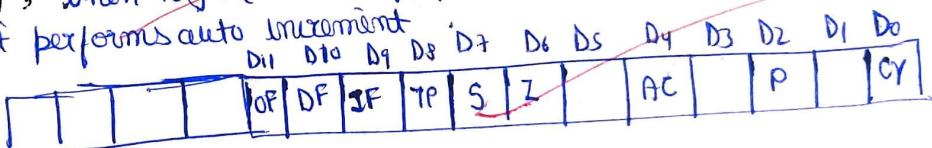
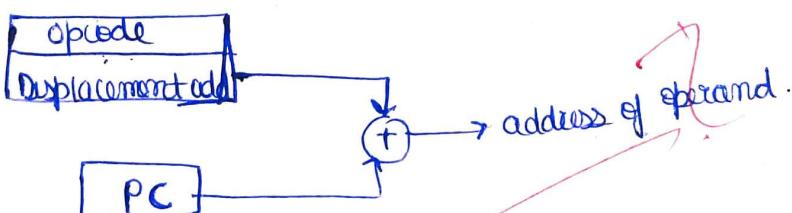
**Auxiliary Carry :** This shows transition from D3 to D4.

**Carry :** This is set when overall carry is generated  
Reset when no carry is generated.

**Overflow :** When result occupies more bits it is set.

(b) Control Flags →

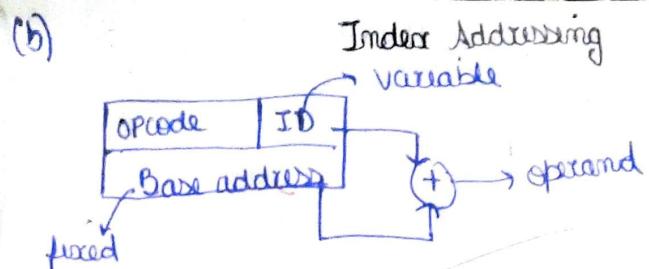
- **Trap Flag :** It is used for step wise debugging when it is high an interrupt occurs after execution of next instruction.
- **Interrupt Flag :** To mask and unmask the maskable interrupts.
- **Direction Flag :** When high (set) it performs auto decrement and when low it performs auto increment.

Ques (a) Relative addressing

It provides position independency.

MOV AX, 5000 [BX]

$$\text{Effective address} = 10H \times DS + BX + 5000$$

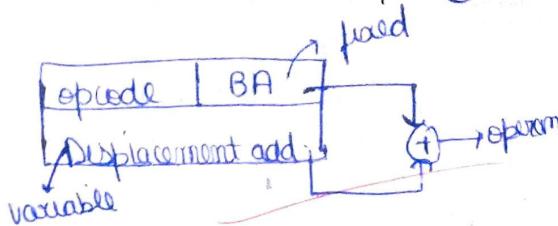


- 3 byte instruction
- used for Increment and decrement

MOV AX, [SI]

$$\text{effective address} = 10H \times DS + SI$$

Base Addressing (8)

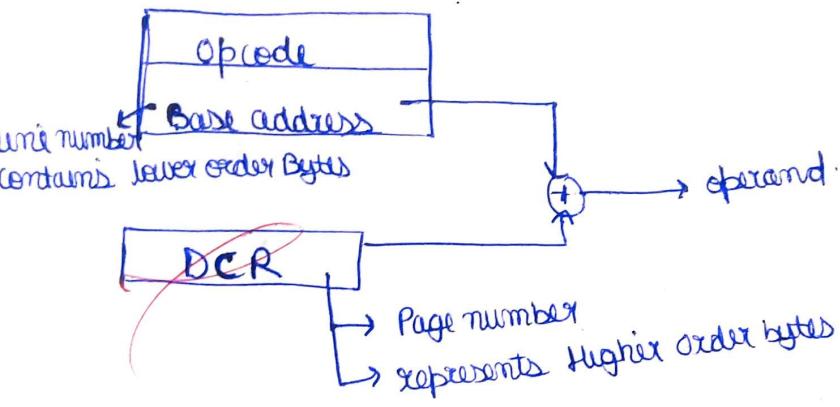


- 3 byte instruction
- used for Reallocation

MOV AX, [BX]

$$\text{effective address} = 10H \times DS + BX$$

## c) Page Addressing

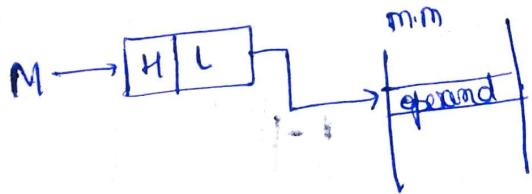


Provides Position independence

## d) Register Indirect Addressing

e.g. MOV A, M

Here address where operand is stored is not provided directly. It points to HL pair register that contains address of operand.



Ques 7 (a)  $XTHL$  : exchange the contents of HL pair and Stack pointer. i.e. content of HL goes to SP & that of SP goes to HL  $HL \leftrightarrow SP$

$XTHL$	Bytes 1	cycles (machine cycles) 5	?
$SPHL$	1	1	

,  $SPHL$  : Store content of HL pair to Stack pointer

$SP \leftarrow HL$

(b)  $DAD RP$

$DAD B \Rightarrow$  add the contents of BC to HL register pair & store address in HL pair only.

Bytes = 1

Cycles = 3

~~DAA (Decimal Adjust accumulator)~~

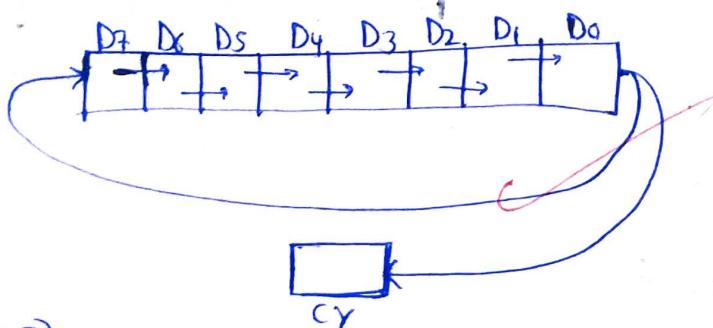
~~It is used to convert binary data to BCD form~~

Bytes = 1

Cycles = 1 (OF)

(c)  $RRC$  (Rotate Right without carry)

This operation is performed in Accumulator.

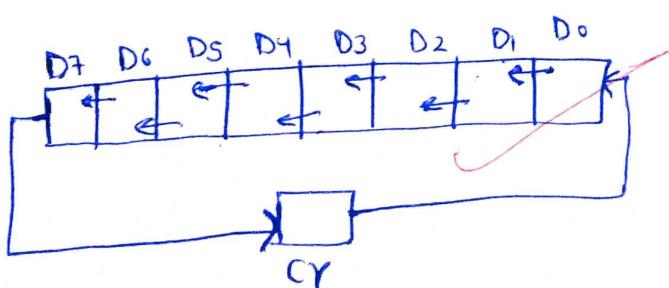


Bytes = 1

Cycles = 1 (OF)

$RAL$  (Rotate Left with carry)

Performed in accumulator.



Bytes = 1

Cycles = 1 (OF)

d) RET → To return back to main program from subroutine

Unconditional Return RET → Bytes = 1  
cycles = 3 (OF+MR+MR)

Conditional Return → Bytes = 1  
cycles = 3 } if condition True

Bytes = 1  
cycles = 1 } if condition False

JMP XXYY → To jump from main program to the given address.  
3 Bytes

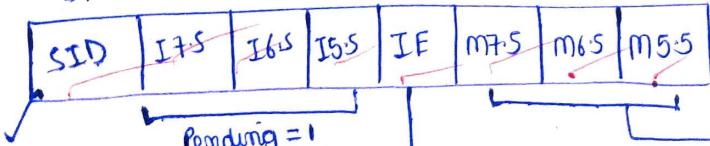
$$\text{Machine Cycles} = \text{OF} + \text{MR} + \text{MR} = 3$$

Conditional Jump  $\begin{cases} \text{True} & \text{Bytes} = 3, \text{cycles} = 3 \\ \text{False} & \text{Bytes} = 3, \text{cycles} = 2 \end{cases}$

	Bytes	Cycles
XTHL	1	5
SPHL	1	1
DAA	1	1
DAD rp	1	3
RRC	1	1
RAL	1	1
RET	1	3
JMP addr	3	3

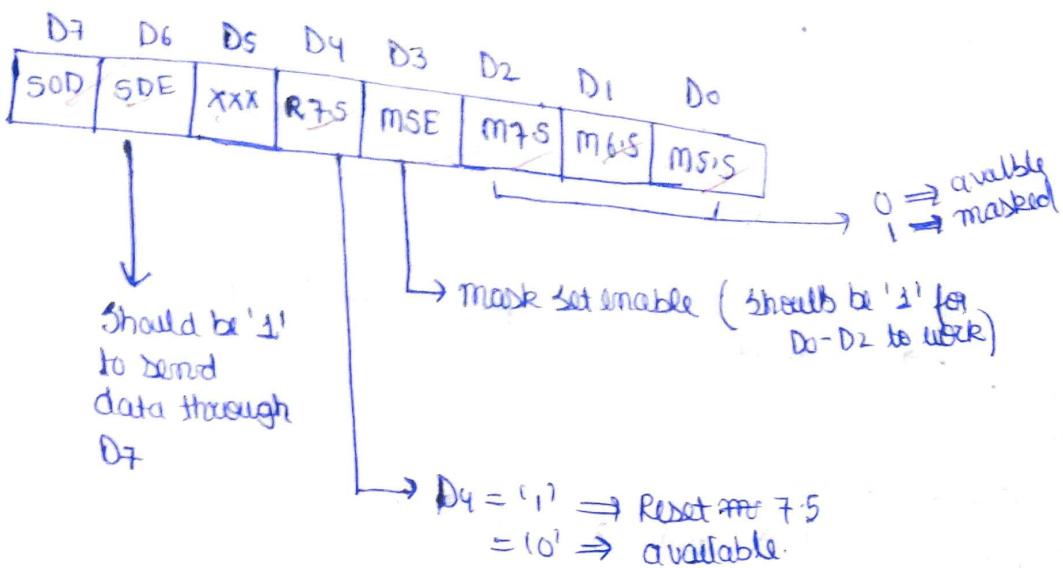
Quest RIM (Read Interrupt mask)  
→ To find if interrupt is pending

D7 D6 D5 D4 D3 D2 D1 D0



Serial input data  
 $\rightarrow \text{mask} = 1, \text{available} = 0$   
 $\text{IE} = 1 \Rightarrow \text{enable}$   
 $\text{IE} = 2 \Rightarrow \text{Disable interrupt}$

- used to set the interrupt mask
- To reset RST 7.5
- For Serial I/O data



Given RST 7.5 = available

Program: To check if RST 6.5 is pending

↑ 5.5

D7	D6	D5	D4	D3	D2	D1	D0
0	0	1	0	0	0	0	0
0	0	0	1				

RIM

MOV B, A

ANI 90H  
JNZ NEXT

EI

RET

NEXT MOV A, B

ANI 0D

ORI 08H

SIM

JMP SERV

1110

1000

12

To check if RST 5.5 is pending

RIM

MOV B, A

ANI 10H

JNZ NENT

EI

RET

NENT MOV A, B

ANI 0EH

ORI 08H

SIM

JMP SERV

To check simultaneously if RST 5.5 & RST 6.5 is pending

(12)

RIM

MOV B, A

ANI 30H

JNZ NEXT

EI  
RET

NEXT: MOV A, B

ANI 0CH

ORI 08H

SIM

JMP SERV

(check if RST 5.5 & RST 6.5 are pending)  
(if pending then move to NEXT)

Completing RST 7.5 request  $\Rightarrow$  Interrupt RST 7.5 is not masked if it is available

