

PMCW Automotive Radar Testing Exploiting Orthogonal Waveforms & Joint Radar & Communication Capabilities

Francesco Biletta, Riccardo Maggiora, Sara Marina Salvador

June 26, 2025

francesco.biletta@polito.it riccardo.maggiora@polito.it sara.salvador@polito.it





Table of contents

- 1. PMCW benefits and ZCZ sequences
- 2. System description
- 3. 2-Tx 4-Rx mmWave board
- 4. Slotted waveguide antennas
- 5. Test and validation

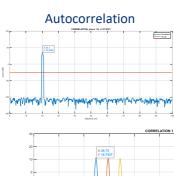


Motivations for PMCW orthogonal waveforms

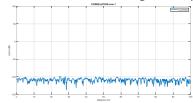
- Binary PMCW radars benefits: better HCR, larger maximum velocity, interference mitigation thanks to code orthogonality, easy integration of communication and sensing, etc.
- FMCW radars use Time Division Multiplexing technique to achieve orthogonality and exploit MIMO advantages. This technique has the main drawback of limiting the maximum unambiguous velocity of the radar.
- Zero Correlation Zone sequences allow to transmit orthogonal signals simultaneously, have no sidelobes inside a determined range and do not require complementary pair.

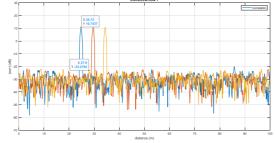


Simulation of ZCZ sequences



Crosscorrelation with orthogonal sequence





Scenario with three orthogonal sequences simultaneously scattered by three targets at different range at 0 dB SNR

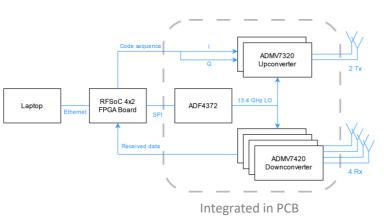


Radar parameters

Bandwidth	250 MHz
T sequence	2 μs
Nchip in a sequence	512
Number of sequences per frame	64
Modulated carrier	250 MHz
Upconverted carrier	80 GHz
Sampling frequency	2 GHz
Frame repetition rate	100 ms
Range resolution	60 cm
Range accuracy	7.5 cm
Max velocity (PRI = 48 μs)	40 m/s
Velocity resolution	0.6 m/s



PMCW radar block diagram





6/13



Real Digital AMD FPGA board



- •Xilinx Gen 3 Zynq UltraScale+ RFSoC ZU48DR
- •Quad core ARM Cortex-A53, Dual core ARM Cortex-R5F
- •Programmable Logic with 930K logic cells, 4272 DSP slices, 38Mb block RAM
- •4x 5GSPS RF ADCs SMA ports
- •2x 9.85GSP RF DACs SMA ports
- •External clock and sync ports
- •4 GB 64-bit 2400MHz Processing System memory
- •4 GB 64-bit 2400MHz Programmable Logic memory
- •10/100/1000 Mbps Ethernet
- •100G Ethernet MAC/PCS w/RS-FEC (QSFP28)



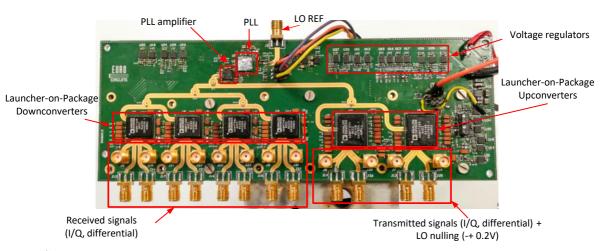
Implemented FPGA firmware

FPGA real-time processing steps:

- Generation of custom digital sequence to be transmitted
- •250 MHz modulated signal generation for radar front-end
- Sampling of received signal from radar front-end
- •Digital demodulation from 250 MHz to baseband
- Correlation with transmitted sequence
- •Doppler FFT calculation and range-doppler map generation
- Data transfer to laptop PC through 1 Gb Ethernet

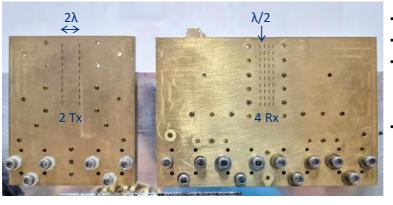


Custom designed MIMO 2-Tx 4-Rx radar front-end





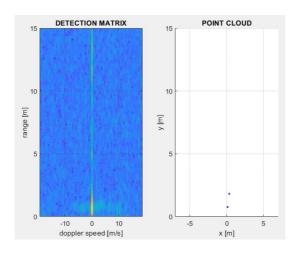
Custom designed MIMO radar high efficiency antennas



- 2 CNC-machined halves
- Tin soldered
- Completely characterized with VNA in anechoic chamber
- Directly connected to chips' Launcher-on-Package

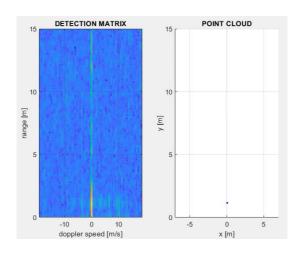


Initial test and validation: walking pedestrian





Initial test and validation: walking pedestrian 2





Conclusions and next steps

Conclusions:

- Full exploitation of PMCW benefits
- High flexibility of the system (sequences and parameters managed via laptop PC)
- Easy integration of communication payload
- Interference mitigation

Next steps:

- Extensive validation of communication and sensing in real-life scenarios
- Advanced antennas configuration for improved MIMO capabilities
- Integration on a single chip



Thank you for your attention

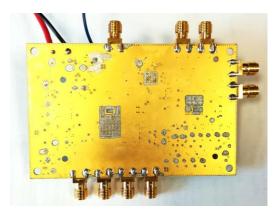
Any questions?

francesco.biletta@polito.it



PMCW radar front-end PCB





Top view

Bottom view