TPS6599xBG Technical Reference Manual

Technical Reference Manual

Literature Number: SLVUCI8
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About This Manual

National Conventions

This document uses the following conventions.

- Hexadecimal numbers may be shown with the suffix h or the prefix 0x. For example, the following number is 40 hexadecimal (decimal 64): 40h or 0x40.
- Registers in this document are shown in figures and described in tables.
  - Each register figure shows a rectangle divided into fields that represent the fields of the register. Each field is labeled with its bit name, its beginning and ending bit numbers above, and its read/write properties with default reset value below. A legend explains the notation used for the properties.
  - Reserved bits in a register figure can have one of multiple meanings:
    - Not implemented on the device
    - Reserved for future device expansion
    - Reserved for TI testing
    - Reserved configurations of the device that are not supported
  - Writing nondefault values to the Reserved bits could cause unexpected behavior and should be avoided.

Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

Related Documents

- USB Power Delivery Specification Revision 3.1 www.usb.org/developers/docs
- USB Type-C Cable and Connector Specification Revision 2.0. www.usb.org/developers/docs

Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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Chapter 1
Introduction

1.1 Introduction

1.1.1 Purpose and Scope

This document describes the Host Interface for the TPS65992EBG, TPS65992SBG, TPS65992DBG, TPS65993BG, and TPS65994BG Type-C Port Switch / Power Delivery (PD) Controller devices.

1.2 PD Controller Host Interface Description

1.2.1 Overview

The PD Controller provides two physical I2C slaves. The I2C_EC slave is meant to be connected to an Embedded Controller (EC). The I2C2s slave is meant to be connected to a secondary controller such as a Thunderbolt controller. For dual-port PD controllers, both of the I2C slaves respond to two slave addresses; one for each Type-C port. Figure 1-1 shows the logical connections for the system for a dual-port PD controller.

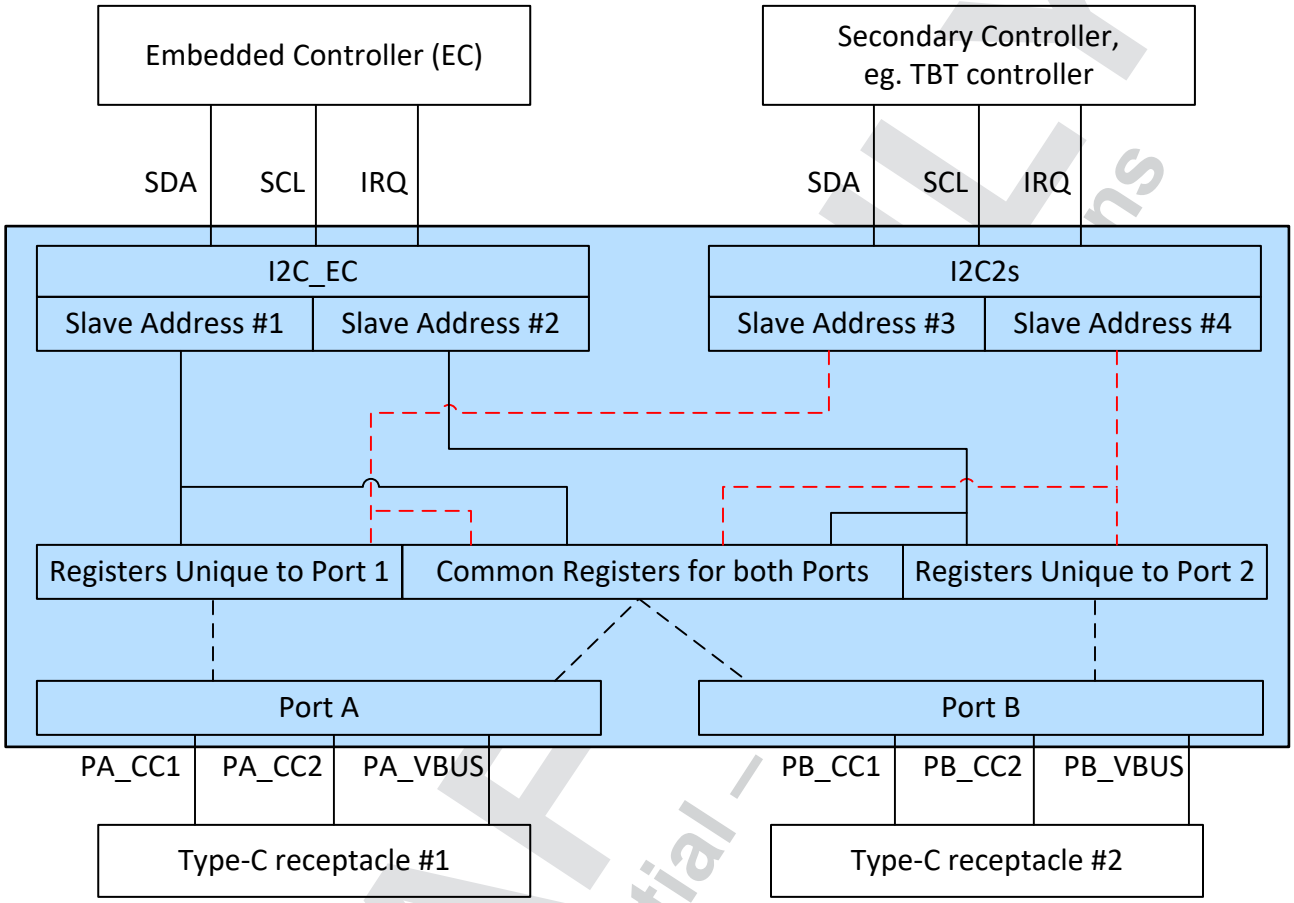

Figure 1-1. Logical connections to registers and Type-C ports in a dual-port PD controller.

The Host Interface defines how the registers are accessed from all I2C slave ports and all slave addresses. Slave Address #1 and Slave Address #2 for I2C_EC are selected by the customer using the ADCIN1 and ADCIN2 pins on the PD controller. Slave Address #3 and Slave Address #4 for I2C2s can be selected through the GLOBAL_SYSTEM_CONFIG register (0x27). See also Table 5-1 for more details about the slave addresses.

The Host Interface provides general status information to the master of these I2C interfaces about the PD Controller, ability to control the PD Controller, status of USB Type-C® Port and communications to/from a connected device (Port Partner) and/or cable plug through USB PD messages. All Host Interface communication that uses the Unique I2C address is referred to as Unique Address Interface.

The PD Controller supports a register-based Unique Address Interface. TPS65994BF Registers lists the Unique Address Interface registers and provides detailed Unique Address Interface register descriptions. For dual-port PD controllers, some registers are not unique per port; so the PD controller only has one instantiation. Other registers are unique per port, and can be accessed from either I2C slave using the slave address associated with that port.

The key to the protocol diagrams is in the SMBus Specification, version 2.0 and is repeated here in part in Figure 1-2.

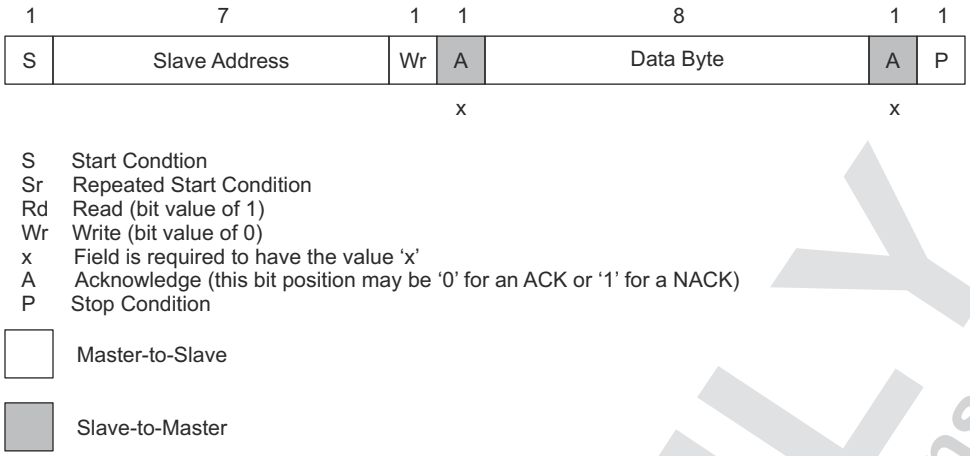

Figure 1-2. I2C Read/Write Protocol Key

1.2.2 Register and field notation

In this document the register names use an ALL CAPS notation, and the field names use a CamelBack notation. For example *TX_SOURCE_CAPS* refers to register 0x32, and *TX_SOURCE_CAPS.numValidPDOs* refers to a specific field in Byte 1 of that register.

Some registers have the same definition, but there are multiple instantiations at different register addresses. The following lists these registers.

- *INT_EVENTx ~ INT_EVENT1* (0x14) or *INT_EVENT2* (0x15)
- *INT_MASKx ~ INT_MASK1* (0x16) or *INT_MASK2* (0x17)
- *INT_CLEARx ~ INT_CLEAR1* (0x18) or *INT_CLEAR2* (0x19)
- *CMDx ~ CMD1* (0x08) or *CMD2* (0x10)
- *DATAx ~ DATA1* (0x09) or *DATA2* (0x11)

In this document, the "x" indicates that it is referring to both instantiations of that register.

1.3 Unique Address Interface

1.3.1 Unique Address Interface Protocol

The Unique Address Interface allows for complex interactions between an I2C master and a single PD Controller. The I2C Slave unique address is used to receive or respond to Host Interface protocol commands. Figure 1-3 and Figure 1-4 show the write and read protocols, respectively. The Byte Count used during a register write can be longer than the number of bytes actually written, in other words the master can issue the stop bit without writing N bytes. Similarly, during a register read, the master can issue the stop bit before reading all N bytes.

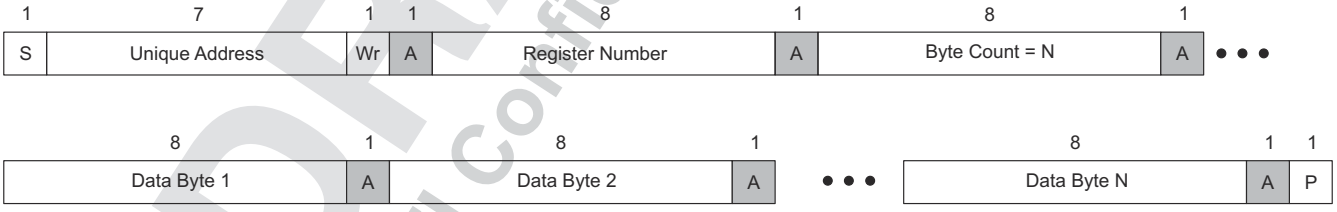

Figure 1-3. I2C Unique Address write register protocol

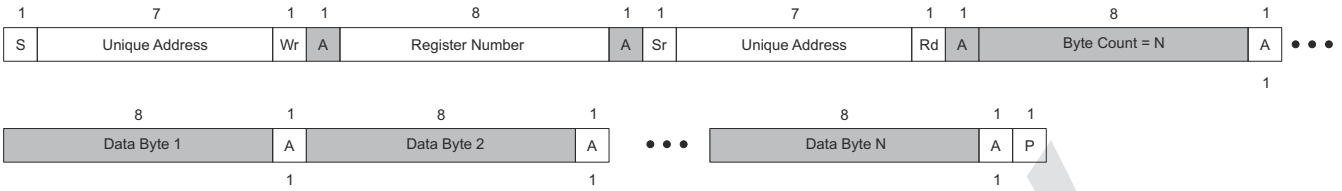

Figure 1-4. I2C Unique Address read register protocol

Chapter 2

PD Controller Policy Modes

2.1 Overview

The PD Controller implements modes for "SRC Policy" (handing out Source contracts), modes for "SNK Policy" (issuing Requests for Sink contracts), and modes for "AM Policy" (Alternate Mode negotiation).

2.2 Source Policy Mode

The PD Controller uses the *TX_SOURCE_CAPS* register (0x32) to know what PDO(s) to advertise. The PD Controller will automatically respond to Request messages as appropriate, and each port acts independently. The host can dynamically change the *TX_SOURCE_CAPS* register, then issue the 'SSrC' 4CC Task and the PD controller will advertise the new PDO(s).

2.3 Sink Policy Mode

The PD Controller will always prepare its own Request message based on the settings in the *AUTO_NEGOTIATE_SINK* register (0x37) and the *TX_SINK_CAPS* register (0x33). The PD Controller will send its prepared Request message as soon as it is ready. The host can change the *AUTO_NEGOTIATE_SINK* register and/or the *TX_SINK_CAPS* register, then issue the 'GSrC' or 'ANeg' 4CC Task and the PD controller will re-negotiate the PD contract based on the updated values.

2.4 Alternate Modes and Alternate Mode Policy

Power Delivery enables alternative modes of operation by providing the mechanisms to discover, enter, and exit Alternate Modes. The PD Specification defines mechanisms to discover, enter and exit Modes defined either by a standard or by a particular vendor. These Modes can be supported either by the Port Partner or by a cable connecting the two Port Partners.

The PD controller will automatically send the Discover Identity message to both the Cable Plug and the Port Partner in compliance wtih USB PD rules. The responses are available in the *RX Identity SOP* register (0x48) and the *RX_IDENTITY_SOPp* register (0x49). The PD controller will also automatically send a Discover SVIDs message and store the response in the *DISCOVERED_SVIDS* register (0x21). The host must wait until *INT_EVENTx.DiscoverModesComplete* is asserted to read the information that was gathered. The host can configure other automatic behavior (even automatic mode entry) using the *USER_VID_CONFIG* register (0x4A), *DP_SID_CONFIG* register (0x51), and *INTEL_VID_CONFIG* register (0x52).

When allowed by the USB PD specification, the PD controller will respond to SVDM commands as appropriate. The *TX_IDENTITY* register (0x47) is used to formulate the response when a Discover Identity SVDM is received. When an SVDM is received it is stored in the *RX_ATTENTION_VDM* register (0x4E) or *RX_OTHER_VDM* register (0x4F), and either *INT_EVENTx.AttentionReceived* or *INT_EVENTx.VDMReceived* will get assserted.

The host can use the 4CC Tasks listed in Section 4.5 to implement other VDM behaviors.

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Chapter 3
TPS6599xBG Registers

Table 3-1 lists the memory-mapped registers for the TPS6599xBG registers. All register offset addresses not listed in Table 3-1 should be considered as reserved locations and the register contents should not be modified.

Table 3-1. TPS6599XBG Registers

Offset	Acronym	Register Name	Section
0h	Vendor ID	Vendor ID	Section 3.1
1h	Device ID	Device ID	Section 3.2
2h	Protocol Version	Protocol Version	Section 3.3
3h	Mode	Mode	Section 3.4
4h	Type	Type	Section 3.5
5h	UID	UID	Section 3.6
6h	Customer Use	Customer Use	Section 3.7
8h	Command Register for I2C1	Command Register for I2C1	Section 3.8
9h	Data Register for CMD1	Data Register for CMD1	Section 3.9
Dh	Device Capabilities	Device Capabilities	Section 3.10
Fh	Version	Version	Section 3.11
10h	Command Register for I2C2	Command Register for I2C2	Section 3.12
11h	Data Register for CMD2	Data Register for CMD2	Section 3.13
14h	Interrupt Event for I2C1	Interrupt Event for I2C1	Section 3.14
15h	Interrupt Event for I2C2	Interrupt Event for I2C2	Section 3.15
16h	Interrupt Mask for I2C1	Interrupt Mask for I2C1	Section 3.16
17h	Interrupt Mask for I2C2	Interrupt Mask for I2C2	Section 3.17
18h	Interrupt Clear for I2C1	Interrupt Clear for I2C1	Section 3.18
19h	Interrupt Clear for I2C2	Interrupt Clear for I2C2	Section 3.19
1Ah	Status	Status	Section 3.20
1Fh	SX Config	SX Config	Section 3.21
20h	Set Sx App Config	Set Sx App Config	Section 3.22
21h	Discovered SVIDs	Discovered SVIDs	Section 3.23
22h	Connection Manager Status	Connection Manager Status	Section 3.24
23h	USB Config	USB Config	Section 3.25
24h	USB Status	USB Status	Section 3.26
25h	Connection Manager Control	Connection Manager Control	Section 3.27
26h	Power Path Status	Power Path Status	Section 3.28
27h	Global System Configuration	Global System Configuration	Section 3.29
28h	Port Configuration	Port Configuration	Section 3.30
29h	Port Control	Port Control	Section 3.31
2Dh	Boot Flags	Boot Flags	Section 3.32
2Eh	Build Description	Build Description	Section 3.33
2Fh	Device Information	Device Information	Section 3.34

Table 3-1. TPS6599XBG Registers (continued)

Offset	Acronym	Register Name	Section
30h	Received Source Capabilities	Received Source Capabilities	Section 3.35
31h	Received Sink Capabilities	Received Sink Capabilities	Section 3.36
32h	Transmit Source Capabilities	Transmit Source Capabilities	Section 3.37
33h	Transmit Sink Capabilities	Transmit Sink Capabilities	Section 3.38
34h	Active PDO Contract	Active PDO Contract	Section 3.39
35h	Active RDO Contract	Active RDO Contract	Section 3.40
37h	Autonegotiate Sink	Autonegotiate Sink	Section 3.41
3Ch	SPM Client Control	SPM Client Control	Section 3.42
3Dh	SPM Client Status	SPM Client Status	Section 3.43
3Fh	Power Status	Power Status	Section 3.44
40h	PD Status	PD Status	Section 3.45
41h	PD3 Status	PD3 Status	Section 3.46
42h	PD3 Configuration	PD3 Configuration	Section 3.47
47h	Tx Identity	Tx Identity	Section 3.48
48h	Received SOP Identity Data Object	Received SOP Identity Data Object	Section 3.49
49h	Received SOP Prime Identity Data Object	Received SOP Prime Identity Data Object	Section 3.50
4Ah	User Alternate Mode Configuration	User Alternate Mode Configuration	Section 3.51
4Eh	Received Attention VDM	Received Attention VDM	Section 3.52
4Fh	Received Other VDM	Received Other VDM	Section 3.53
50h	Data Control	Data Control	Section 3.54
51h	Display Port Configuration	Display Port Configuration	Section 3.55
52h	Thunderbolt Configuration	Thunderbolt Configuration	Section 3.56
55h	Special Configuration	Special Configuration	Section 3.57
57h	User VID Status	User VID Status	Section 3.58
58h	Display Port Status	Display Port Status	Section 3.59
59h	Intel VID Status	Intel VID Status	Section 3.60
5Ch	IO Config	IO Config	Section 3.61
5Fh	Data Status	Data Status	Section 3.62
60h	Received User SVID Attention VDM	Received User SVID Attention VDM	Section 3.63
61h	Received User SVID Other VDM	Received User SVID Other VDM	Section 3.64
62h	APP Config Binary Data Indices	APP Config Binary Data Indices	Section 3.65
64h	I2C Controller Config	I2C Controller Config	Section 3.66
69h	Type C State	Type C State	Section 3.67
6Ah	ADC Results	ADC Results	Section 3.68
6Ch	App Config Register	App Config Register	Section 3.69
70h	Sleep Control Register	Sleep Control Register	Section 3.70
72h	GPIO Status	GPIO Status	Section 3.71
73h	TX Manufactrer Info SOP	TX Manufactrer Info SOP	Section 3.72
74h	Received Alert Data Object	Received Alert Data Object	Section 3.73
75h	TX Alert Data Object	TX Alert Data Object	Section 3.74
77h	Tx Source Capabilities Extended Data Block	Tx Source Capabilities Extended Data Block	Section 3.75
79h	Transmitted Status Data Block (SDB) Register	Transmitted Status Data Block (SDB) Register	Section 3.76
7Ah	Trasmitted PPS Status Data Block	Trasmitted PPS Status Data Block	Section 3.77

Table 3-1. TPS6599XBG Registers (continued)

Offset	Acronym	Register Name	Section
7Bh	Transmitted Battery Status Data Objects (BSDO) Register	Transmitted Battery Status Data Objects (BSDO) Register	Section 3.78
7Dh	Tx Battery Capabilities	Tx Battery Capabilities	Section 3.79
7Eh	Transmit Sink Capabilities Extended Data Block	Transmit Sink Capabilities Extended Data Block	Section 3.80
80h	UUID Handle	UUID Handle	Section 3.81
94h	External DCDC Status	External DCDC Status	Section 3.82
95h	External DCDC Parameters	External DCDC Parameters	Section 3.83
97h	EPR Config	EPR Config	Section 3.84

Complex bit access types are encoded to fit into small table cells. Table 3-2 shows the codes that are used for access types in this section.

Table 3-2. TPS6599xBG Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

3.1 Vendor ID Register (Offset = 0h) [Reset = 00000000h]

Vendor ID is shown in Table 3-3.

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Intel-assigned Thunderbolt Vendor ID, with the most significant 8 bits of the field padded with 0's. OTP boot loader will use TI's Vendor ID by default. This register may be changed during application customization.

Table 3-3. Vendor ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Intel-assigned Thunderbolt Vendor ID	R	0h	Intel-assigned Thunderbolt Vendor ID, with the most significant 8 bits of the field padded with 0's. OTP boot loader will use TI's Vendor ID by default. This register may be changed during application customization.

3.2 Device ID Register (Offset = 1h) [Reset = 00000000h]

Device ID is shown in Table 3-4.

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Vendor-specific Device ID. Boot loader will use Device ID specific to part (expected to be different per TI part number). This register may be changed during application customization.

Table 3-4. Device ID Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Device ID	R	0h	Vendor-specific Device ID. Boot loader will use Device ID specific to part (expected to be different per TI part number). This register may be changed during application customization.

3.3 Protocol Version Register (Offset = 2h) [Reset = 00000000h]

Protocol Version is shown in Table 3-5.

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Thunderbolt Protocol Version. Required to return 1 per current specification.

Table 3-5. Protocol Version Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Protocol Version	R	0h	Thunderbolt Protocol Version. Required to return 1 per current specification.

3.4 Mode Register (Offset = 3h) [Reset = 00000000h]

Mode is shown in Table 3-6.

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Indicates the operational state of the port. The PD controller has limited functionality in some modes.

Table 3-6. Mode Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Mode	R	0h	The mode described in 4 ASCII characters.

3.5 Type Register (Offset = 4h) [Reset = 00000000h]

Type is shown in Table 3-7.

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Default response is 'I2C ' (note space as 4th character).

Table 3-7. Type Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	RESERVED	R	0h	Reserved

3.6 UID Register (Offset = 5h) [Reset = 00000000000000000000000000000000h]

UID is shown in Table 3-8.

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128-bit unique ID (unique for each PD Controller Port)

Table 3-8. UID Register Field Descriptions

Bit	Field	Type	Reset	Description
127-0	User ID	R	0h	128-bit unique ID (unique for each PD Controller Port)

3.7 Customer Use Register (Offset = 6h) [Reset = 0000000000000000h]

Customer Use is shown in Table 3-9.

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These 8 bytes are allocated for customer use as needed. The PD controller does not use this register. This register may be changed during application customization.

Table 3-9. Customer Use Register Field Descriptions

Bit	Field	Type	Reset	Description
63-0	Customer Use	R/W	0h	These 8 bytes are allocated for customer use as needed. The PD controller does not use this register. This register may be changed during application customization.

3.8 Command Register for I2C1 (Offset = 8h) [Reset = 00000000h]

Command Register for I2C1 is shown in Table 3-10.

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Command register for the primary command interface. Cleared to 0x0000_0000 by the PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register, it is replaced by a 4CC value of "!CMD".

Table 3-10. Command Register for I2C1 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Command	R/W	0h	Command register for the primary command interface. Cleared to 0x0000_0000 by the PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register, it is replaced by a 4CC value of "!CMD".

3.9 Data Register for CMD1 (Offset = 9h) [Reset = 0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000h]

Data Register for CMD1 is shown in Table 3-11.

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Data register for the primary command interface (CMD1).

Table 3-11. Data Register for CMD1 Field Descriptions

Bit	Field	Type	Reset	Description
511-0	Data	R/W	0h	Data register for the primary command interface (CMD1).

3.10 Device Capabilities Register (Offset = Dh) [Reset = 00000000h]

Device Capabilities is shown in Table 3-12.

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Description of supported features.

Table 3-12. Device Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
31-8	RESERVED	R	0h	Reserved
7	I2C3m Level	R	0h	Pull-up voltage required for I2C3m port. 0h = 1.8V or 3.3V 1h = 3.3V
6-5	BC1p2 Supported	R	0h	BC 1.2 support capability. 0h = Not supported 1h = Only source supported 2h = Reserved 3h = Source and sink
4	Single Port	R	0h	Number of USB ports supported. 0h = The device is dual-port capable 1h = The device only has one port
3	TBT Present	R	0h	Thunderboth support capability. 0h = Not supported 1h = Supported
2	USB PD Capability	R	0h	USB Power Delivery capability. 0h = Supported 1h = Not supported
1-0	Power Role	R	0h	Power Role capability. 0h = Both source and sink roles supported (DRP) 1h = Source-only 2h = Sink-only 3h = Source-only

3.11 Version Register (Offset = Fh) [Reset = 00000000h]

Version is shown in Table 3-13.

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Boot Firmware Version

Table 3-13. Version Register Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Version	R	0h	Boot Firmware Version Binary Coded Decimal version number, bootloader/application code version. Represented as VVVV.MM.RR with leading 0's removed.e.g. 65794d (decimal) to 0x00010102 to 0001.01.02 to 1.1.2 (version). The version information is returned in little Endian format i.e. byte 1 = RR, byte 2 = MM, etc. The 16-bit field RR is used as the FW version in the Source Capabilities Extended and Sink Capabilities Extended messages.

3.12 Command Register for I2C2 (Offset = 10h) [Reset = 00000000h]

Command Register for I2C2 is shown in Table 3-14.

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Command register for the secondary command interface. Shall be cleared to 0x00000000 by PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register it shall be replaced by a 4CC value of "!CMD".

Table 3-14. Command Register for I2C2 Field Descriptions

Bit	Field	Type	Reset	Description
31-0	Command	R/W	0h	Command register for the secondary command interface. Shall be cleared to 0x00000000 by PD Controller during initialization and after successful processing of every command. If an unrecognized command is written to this register it shall be replaced by a 4CC value of "!CMD".

3.13 Data Register for CMD2 (Offset = 11h) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000 000000000000000000000000000000000000000h]

Data Register for CMD2 is shown in Table 3-15.

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Data register used for the secondary command interface (CMD2).

Table 3-15. Data Register for CMD2 Field Descriptions

Bit	Field	Type	Reset	Description
511-0	Data	R/W	0h	Data register used for the secondary command interface (CMD2).

3.14 Interrupt Event for I2C1 Register (Offset = 14h) [Reset = 00000000000000002000008h]

Interrupt Event for I2C1 is shown in Table 3-16.

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Interrupt event bit field for I2C_EC_IRQ. If any bit in this register is 1, then the I2C_EC_IRQ pin is pulled low.Bytes 1 to 10 of this register are port-specific, but Byte 11(Bits 80-87) is common to all ports in the PD controller.

Table 3-16. Interrupt Event for I2C1 Register Field Descriptions

Bit	Field	Type	Reset	Description
87-83	RESERVED	R	0h	Reserved
82	I2C Controller NACked	R	0h	A transaction on the I2C Controller was NACKed.
81	Ready for Patch	R	0h	Device ready for a patch bundle from the host.
80	Patch Loaded	R	0h	Patch was loaded to the device.
79	Alert Message Received	R	0h	Alert Message received, see RX_ADO register.
78	Chunk Request Received	R	0h	Chunk Request message received.
77	Chunk Response Received	R	0h	Chunk Response message received.
76	FRS Signal Received	R	0h	FRS swap signaling received.
75	External DCDC Status Change	R	0h	
74	I2C Communication error with external PP	R	0h	
73	Mailbox Updated	R	0h	
72	RESERVED	R	0h	Reserved
71	Notsupported Received	R	0h	A NOT_SUPPORTED USB PD message was received. The EC should clear this bit before using a 4CC task that could result in receiving a Not_Supported message.
70	Event SOC ACK Timeout	R	0h	The SoC has waited too long to process an alert.
69-67	RESERVED	R	0h	Reserved
66	MBRD Buffer Ready	R	0h	Receive memory buffer full and ready to be read using the 'MBRd' command.
65	TX Memory Buffer Empty	R	0h	Transmit memory buffer empty.
64	PD3 Status Updated	R	0h	Asserted when the contents of PD3_STATUS register (0x41) change.
63	Intel VID Status Updated	R	0h	Asserted when the contents of INTEL_VID_STATUS register (0x59) change.
62	DP SID Status Updated	R	0h	Asserted when the contents of DP_SID_STATUS register (0x58) change.
61	External DCDC Event Received	R	0h	External DCDC Event received
60	RESERVED	R	0h	Reserved
59	USVID Other VDM Received	R	0h	A User VID SVDM non-Attention or unstructured VDM has been received.
58	USVID Attention VDM Received	R	0h	A User VID SVDM Attention has been received.
57	USVID Mode Exited	R	0h	A User VID alternate mode has been exited.
56	USVID Mode Entered	R	0h	A User VID alternate mode has been entered.
55	Connection Manager Update	R	0h	Connection Manager Update has changed
54	USB Status Update	R	0h	USB Status Update has occurred
53	Data Reset Start	R	0h	Set when the Data Reset process has started. The system is expected to handle the data-line terminations properly.

Table 3-16. Interrupt Event for I2C1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
52	Exit Mode Completed	R	0h	Set when the Exit Mode process is complete.
51	Discover Mode Completed	R	0h	Set when the Discover Modes process has completed.
50	RESERVED	R	0h	Reserved
49	AM Entered	R	0h	Set when any alternate mode is entered.
48	AM Entry Fail	R	0h	Set when any alternate mode attempted and failed.
47	RESERVED	R	0h	Reserved
46	Unable to Source Error	R	0h	The Source was unable to increase the voltage to the negotiated voltage of the contract.
45-44	RESERVED	R	0h	Reserved
43	Plug Early Notification	R	0h	A connection has been detected but not debounced.
42	Sink Transition Completed	R	0h	This event only occurs when in source mode (PD_STATUS.PresentPDRole = 1b). It occurs tSrcTransition (ms) after sending an Accept message to a Request message, just before sending the PS_RDY message.
41-40	RESERVED	R	0h	Reserved
39	Message Data Error	R	0h	An erroneous message was received.
38	Protocol Error	R	0h	An unexpected message was received from the partner device.
37	RESERVED	R	0h	Reserved
36	Missing Get Capabalities Message Error	R	0h	The partner device did not respond to the Get_Sink_Cap or Get_Source_Cap message that was sent.
35	Power Event Occurred Error	R	0h	An OVP, or ILIM event occurred on VBUS. Or a TSD event occurred.
34	Can Provide Voltage or Current Later Error	R	0h	The USB PD Source can provide acceptable voltage and current, but not at the present time. A "wait" message was sent or received.
33	Cannot Provide Voltage or Current Error	R	0h	The USB PD Source cannot provide an acceptable voltage and/or current. A Reject message was sent to the Sink or a Capability Mismatch was received from the Sink.
32	Device Incompatible Error	R	0h	When set to 1, a USB PD device with an incompatible specification version was connected. Or the partner device is not USB PD capable.
31	CMD2 Complete	R	0h	Set whenever a non-zero value in CMD2 register is set to zero or ! CMD.
30	CMD1 Complete	R	0h	Set whenever a non-zero value in CMD1 register is set to zero or ! CMD.
29-28	RESERVED	R	0h	Reserved
27	PD Status Updated	R	0h	Set whenever contents of PD_STATUS register (0x40) change.
26	Status Updated	R	0h	Set whenever contents of STATUS register (0x1A) change.
25	Data Status Updated	R	1h	Set whenever contents of DATA_STATUS register (0x5F) change.
24	Power Status Updated	R	0h	Set whenever contents of POWER_STATUS register (0x3F) change.
23	Power Path Switch Changed	R	0h	Set whenever contents of POWER_PATH_STATUS register (0x26) changes.
22	RESERVED	R	0h	Reserved
21	USB Host No Longer Present	R	0h	Set when STATUS.UsbHostPresent transitions to anything other than 11b.
20	USB Host Present	R	0h	Set when STATUS.UsbHostPresent transitions to 11b.
19	RESERVED	R	0h	Reserved
18	Data Swap Requested	R	0h	A DR swap was requested by the Port Partner.
17	Power Swap Requested	R	0h	A PR swap was requested by the Port Partner.
16	RESERVED	R	0h	Reserved

Table 3-16. Interrupt Event for I2C1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
15	Sink Cap Message Received	R	0h	
14	Source Capabalities Message Received	R	0h	This is asserted when a Source Capabilities message is received from the Port Partner.
13	New Contract as Provider	R	0h	An RDO from the far-end device has been accepted and the PD Controller is a Source. This is asserted after the PS_RDY message has been sent. See ACTIVE_CONTRACT_PDO register (0x34) and ACTIVE_CONTRACT_RDO register (0x35) for details.
12	New Contract as Consumer	R	0h	Far-end source has accepted an RDO sent by the PD Controller as a Sink. See ACTIVE_CONTRACT_PDO register (0x34) and ACTIVE_CONTRACT_RDO register (0x35) for details.
11	VDM Received	R	0h	A Vendor Defined Message has been received. See RX_OTHER_VDM register (0x4F) for details.
10	Attention Received	R	0h	An Attention Message has been received. See RX_ATTENTION_VDM register (0x4E) for details.
9	Overcurrent	R	0h	Set whenever an Overcurrent field (VBUS or VCONN) in the POWER_PATH_STATUS register (0x26) changes.
8	RESERVED	R	0h	Reserved
7	Source Cap Updated	R	0h	The Source Capabiliities has been updated based on some automatic behavior configured by or requested by the host. The next Source Capabilities PD message transmitted will contain the updated values. This could get asserted when GLOBAL_SYSTEM_CONFIG.EnableSPM is asserted or when the 4CC Task 'UCSI' is used to implement SET_POWER_LEVEL.
6	FR Swap Complete	R	0h	A Fast Role swap has completed.
5	Data Swap Complete	R	0h	A Data Role swap has completed. See STATUS register (0x1A) and PD_STATUS register (0x40) for port state.
4	Power Swap Complete	R	0h	A Power role swap has completed. See STATUS register (0x1A) and PD_STATUS register (0x40) for port state.
3	Plug Insert or Removal	R	1h	USB Plug Status has Changed. See Status register for more plug details.
2	RESERVED	R	0h	Reserved
1	PD Hardreset	R	0h	A PD Hard Reset has been performed. See PD_STATUS.HardResetDetails for more information.
0	RESERVED	R	0h	Reserved

3.15 Interrupt Event for I2C2 Register (Offset = 15h) [Reset = 00000000000000000000h]

Interrupt Event for I2C2 is shown in Table 3-17.

Return to the Summary Table.

Interrupt event bit field for I2C2s_IRQ. If any bit in this register is 1, then the I2C2s_IRQ pin is pulled low. Bytes 1 to 10 of this register are port-specific, but Byte 11(Bits 80-87) is common to all ports in the PD controller.

Table 3-17. Interrupt Event for I2C2 Register Field Descriptions

Bit	Field	Type	Reset	Description
87-83	RESERVED	R	0h	Reserved
82	I2C Controller NACKed	R	0h	
81	Ready for Patch	R	0h	
80	Patch Loaded	R	0h	
79	Alert Message Received	R	0h	
78	Chunk Request Received	R	0h	
77	Chunk Response Received	R	0h	
76	FRS Signal Received	R	0h	
75	External DCDC Status Change	R	0h	
74	I2C Communication error with external PP	R	0h	
73	Mailbox Updated	R	0h	
72	RESERVED	R	0h	Reserved
71	Notsupported Received	R	0h	
70	Event SOC ACK Timeout	R	0h	
69	CustomerD VDM Sent	R	0h	
68	VDM Entered Mode	R	0h	
67	CustomerD VDM Arrived	R	0h	
66	MBRD Buffer Ready	R	0h	
65	TX Memory Buffer Empty	R	0h	
64	PD3 Status Updated	R	0h	
63	Intel VID Status Updated	R	0h	
62	DP SID Status Updated	R	0h	
61	External DCDC Event Received	R	0h	External DCDC Event received
60	RESERVED	R	0h	Reserved
59	USVID Other VDM Received	R	0h	
58	USVID Attention VDM Received	R	0h	
57	USVID Mode Exited	R	0h	
56	USVID Mode Entered	R	0h	
55	Connection Manager Update	R	0h	Connection Manager Update has changed
54	USB Status Update	R	0h	USB Status Update has occurred
53	Data Reset Start	R	0h	
52	Exit mode Completed	R	0h	
51	Discover mode Completed	R	0h	
50	VDM Message Sent	R	0h	

Table 3-17. Interrupt Event for I2C2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
49	AM Entered	R	0h	
48	AM Entry Fail	R	0h	
47	RESERVED	R	0h	Reserved
46	Unable to Source Error	R	0h	
45-44	RESERVED	R	0h	Reserved
43	Plug Early Notification	R	0h	
42	Sink Transition Completed	R	0h	
41	Discharge Failed Error	R	0h	
40	RESERVED	R	0h	Reserved
39	Message Data Error	R	0h	
38	Protocol Error	R	0h	
37	RESERVED	R	0h	Reserved
36	Missing Get Capabalities Message Error	R	0h	
35	Power Event Occurred Error	R	0h	
34	Can Provide Voltage or Current Later Error	R	0h	
33	Cannot Provide Voltage or Current Error	R	0h	
32	Device Incompatible Error	R	0h	
31	CMD2 Complete	R	0h	
30	CMD1 Complete	R	0h	
29-28	RESERVED	R	0h	Reserved
27	PD Status Updated	R	0h	
26	Status Updated	R	0h	
25	Data Status Updated	R	0h	
24	Power Status Updated	R	0h	
23	Power Path Switch Changed	R	0h	
22	RESERVED	R	0h	Reserved
21	USB Host No Longer Present	R	0h	
20	USB Host Present	R	0h	
19	RESERVED	R	0h	Reserved
18	Data Swap Requested	R	0h	
17	Power Swap Requested	R	0h	
16	RESERVED	R	0h	Reserved
15	Sink Cap Message Received	R	0h	
14	Source Cap Message Received	R	0h	
13	New Contract as Provider	R	0h	
12	New Contract as Consumer	R	0h	
11	VDM Received	R	0h	
10	Attention Received	R	0h	
9	Overcurrent	R	0h	

Table 3-17. Interrupt Event for I2C2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-7	RESERVED	R	0h	Reserved
6	FR Swap Complete	R	0h	
5	Data Swap Complete	R	0h	
4	Power Swap Complete	R	0h	
3	Plug Insert or Removal	R	0h	
2	RESERVED	R	0h	Reserved
1	PD Hardreset	R	0h	
0	RESERVED	R	0h	Reserved

3.16 Interrupt Mask for I2C1 Register (Offset = 16h) [Reset = 0000000F000000CD33380Ah]

Interrupt Mask for I2C1 is shown in Table 3-18.

Return to the Summary Table.

Interrupt mask bit field for INT_EVENT1. A bit in INT_EVENT1 cannot be set if it is cleared in this register. Bytes 1 to 10 of this register are port-specific, but Byte 11(Bits 80-87) is common to all ports in the PD controller.

Table 3-18. Interrupt Mask for I2C1 Register Field Descriptions

Bit	Field	Type	Reset	Description
87-83	RESERVED	R/W	0h	Reserved
82	I2C Controller NACKed	R/W	0h	
81	Ready for Patch	R/W	0h	
80	Patch Loaded	R/W	0h	
79	Alert Message Received	R/W	0h	
78	Chunk Request Received	R/W	0h	
77	Chunk Response Received	R/W	0h	
76	FRS Signal Received	R/W	0h	
75	External DCDC Status Change	R/W	0h	
74	I2C Communication error with external PP	R/W	0h	
73	Mailbox Updated	R/W	0h	
72	RESERVED	R/W	0h	Reserved
71	Notsupported Received	R/W	0h	
70	Event SOC ACK Timeout	R/W	0h	
69	CustomerD VDM Sent	R/W	0h	
68	VDM Entered Mode	R/W	0h	
67	CustomerD VDM Arrived	R/W	0h	
66	MBRD Buffer Ready	R/W	0h	
65	TX Memory Buffer Empty	R/W	0h	
64	PD3 Status Updated	R/W	0h	
63	Intel VID Status Updated	R/W	0h	
62	DP SID Status Updated	R/W	0h	
61	External DCDC Event Received	R/W	0h	External DCDC Event received
60	RESERVED	R/W	0h	Reserved
59	USVID Other VDM Received	R/W	1h	
58	USVID Attention VDM Received	R/W	1h	
57	USVID Mode Exited	R/W	1h	
56	USVID Mode Entered	R/W	1h	
55	Connection Manager Update	R/W	0h	
54	USB Status Update	R/W	0h	
53	Data Reset Start	R/W	0h	
52	Exit mode Completed	R/W	0h	
51	Discover mode Completed	R/W	0h	
50	VDM Message Sent	R/W	0h	

Table 3-18. Interrupt Mask for I2C1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
49	AM Entered	R/W	0h	
48	AM Entry Fail	R/W	0h	
47	RESERVED	R/W	0h	Reserved
46	Unable to Source Error	R/W	0h	
45-44	RESERVED	R/W	0h	Reserved
43	Plug Early Notification	R/W	0h	
42	Sink Transition Completed	R/W	0h	
41	Discharge Failed Error	R/W	0h	
40	RESERVED	R/W	0h	Reserved
39	Message Data Error	R/W	0h	
38	Protocol Error	R/W	0h	
37	RESERVED	R/W	0h	Reserved
36	Missing Get Capabalities Message Error	R/W	0h	
35	Power Event Occurred Error	R/W	0h	
34	Can Provide Voltage or Current Later Error	R/W	0h	
33	Cannot Provide Voltage or Current Error	R/W	0h	
32	Device Incompatible Error	R/W	0h	
31	CMD2 Complete	R/W	1h	
30	CMD1 Complete	R/W	1h	
29-28	RESERVED	R/W	0h	Reserved
27	PD Status Updated	R/W	1h	
26	Status Updated	R/W	1h	
25	Data Status Updated	R/W	0h	
24	Power Status Updated	R/W	1h	
23	Power Path Switch Changed	R/W	0h	
22	RESERVED	R/W	0h	Reserved
21	USB Host No Longer Present	R/W	1h	
20	USB Host Present	R/W	1h	
19	RESERVED	R/W	0h	Reserved
18	Data Swap Requested	R/W	0h	
17	Power Swap Requested	R/W	1h	
16-15	RESERVED	R/W	0h	Reserved
14	Source Cap Message Received	R/W	0h	
13	New Contract as Provider	R/W	1h	
12	New Contract as Consumer	R/W	1h	
11	VDM Received	R/W	1h	
10	Attention Received	R/W	0h	
9	Overcurrent	R/W	0h	
8-7	RESERVED	R/W	0h	Reserved
6	FR Swap Complete	R/W	0h	

Table 3-18. Interrupt Mask for I2C1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	Data Swap Complete	R/W	0h	
4	Power Swap Complete	R/W	0h	
3	Plug Insert or Removal	R/W	1h	
2	RESERVED	R/W	0h	Reserved
1	PD Hardreset	R/W	1h	
0	RESERVED	R/W	0h	Reserved

3.17 Interrupt Mask for I2C2 Register (Offset = 17h) [Reset = 00000000000000002000408h]

Interrupt Mask for I2C2 is shown in Table 3-19.

Return to the Summary Table.

Interrupt mask bit field for INT_EVENT2. A bit in INT_EVENT2 cannot be set if it is cleared in this register. Bytes 1 to 10 of this register are port-specific, but Byte 11(Bits 80-87) is common to all ports in the PD controller.

Table 3-19. Interrupt Mask for I2C2 Register Field Descriptions

Bit	Field	Type	Reset	Description
87-83	RESERVED	R/W	0h	Reserved
82	I2C Controller NACKed	R/W	0h	
81	Ready for Patch	R/W	0h	
80	Patch Loaded	R/W	0h	
79	Alert Message Received	R/W	0h	
78	Chunk Request Received	R/W	0h	
77	Chunk Response Received	R/W	0h	
76	FRS Signal Received	R/W	0h	
75	External DCDC Status Change	R/W	0h	
74	I2C Communication error with external PP	R/W	0h	
73	Mailbox Updated	R/W	0h	
72	RESERVED	R/W	0h	Reserved
71	Notsupported Received	R/W	0h	
70	Event SOC ACK Timeout	R/W	0h	
69	CustomerD VDM Sent	R/W	0h	
68	VDM Entered Mode	R/W	0h	
67	CustomerD VDM Arrived	R/W	0h	
66	MBRD Buffer Ready	R/W	0h	Reserved.
65	TX Memory Buffer Empty	R/W	0h	
64	PD3 Status Updated	R/W	0h	
63	Intel VID Status Updated	R/W	0h	
62	DP SID Status Updated	R/W	0h	
61	External DCDC Event Received	R/W	0h	External DCDC Event received
60	RESERVED	R/W	0h	Reserved
59	USVID Other VDM Received	R/W	0h	
58	USVID Attention VDM Received	R/W	0h	
57	USVID Mode Exited	R/W	0h	
56	USVID Mode Entered	R/W	0h	
55	Connection Manager Update	R/W	0h	
54	USB Status Update	R/W	0h	
53	Data Reset Start	R/W	0h	
52	Exit mode Completed	R/W	0h	
51	Discover mode Completed	R/W	0h	
50	VDM Message Sent	R/W	0h	

Table 3-19. Interrupt Mask for I2C2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
49	AM Entered	R/W	0h	
48	AM Entry Fail	R/W	0h	
47	RESERVED	R/W	0h	Reserved
46	Unable to Source Error	R/W	0h	
45-44	RESERVED	R/W	0h	Reserved
43	Plug Early Notification	R/W	0h	
42	Sink Transition Completed	R/W	0h	
41	Discharge Failed Error	R/W	0h	
40	RESERVED	R/W	0h	Reserved
39	Message Data Error	R/W	0h	
38	Protocol Error	R/W	0h	
37	RESERVED	R/W	0h	Reserved
36	Missing Get Capabalities Message Error	R/W	0h	
35	Power Event Occurred Error	R/W	0h	
34	Can Provide Voltage or Current Later Error	R/W	0h	
33	Cannot Provide Voltage or Current Error	R/W	0h	
32	Device Incompatible Error	R/W	0h	
31	CMD2 Complete	R/W	0h	
30	CMD1 Complete	R/W	0h	
29-28	RESERVED	R/W	0h	Reserved
27	PD Status Updated	R/W	0h	
26	Status Updated	R/W	0h	
25	Data Status Updated	R/W	1h	
24	Power Status Updated	R/W	0h	
23	Power Path Switch Changed	R/W	0h	
22	RESERVED	R/W	0h	Reserved
21	USB Host No Longer Present	R/W	0h	
20	USB Host Present	R/W	0h	
19	RESERVED	R/W	0h	Reserved
18	Data Swap Requested	R/W	0h	
17	Power Swap Requested	R/W	0h	
16-15	RESERVED	R/W	0h	Reserved
14	Source Cap Message Received	R/W	0h	
13	New Contract as Provider	R/W	0h	
12	New Contract as Consumer	R/W	0h	
11	VDM received	R/W	0h	
10	Attention Received	R/W	1h	
9	Overcurrent	R/W	0h	
8-7	RESERVED	R/W	0h	Reserved
6	FR Swap Complete	R/W	0h	

Table 3-19. Interrupt Mask for I2C2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
5	Data Swap Complete	R/W	0h	
4	Power Swap Complete	R/W	0h	
3	Plug Insert or Removal	R/W	1h	
2	RESERVED	R/W	0h	Reserved
1	PD Hardreset	R/W	0h	
0	RESERVED	R/W	0h	Reserved

3.18 Interrupt Clear for I2C1 Register (Offset = 18h) [Reset = 00000000000000000000h]

Interrupt Clear for I2C1 is shown in Table 3-20.

Return to the Summary Table.

Interrupt clear bit field for INT_EVENT1. Bits set in this register are cleared from INT_EVENT1. Bytes 1 to 10 of this register are port-specific, but Byte 11(Bits 80-87) is common to all ports in the PD controller.

Table 3-20. Interrupt Clear for I2C1 Register Field Descriptions

Bit	Field	Type	Reset	Description
87-83	RESERVED	R/W	0h	Reserved
82	I2C Controller NACKed	R/W	0h	
81	Ready for Patch	R/W	0h	
80	Patch Loaded	R/W	0h	
79	Alert Message Received	R/W	0h	
78	Chunk Request Received	R/W	0h	
77	Chunk Response Received	R/W	0h	
76	FRS Signal Received	R/W	0h	
75	External DCDC Status Change	R/W	0h	
74	I2C Communication error with external PP	R/W	0h	
73	Mailbox Updated	R/W	0h	
72	RESERVED	R/W	0h	Reserved
71	Notsupported Received	R/W	0h	
70	Event SOC ACK Timeout	R/W	0h	
69	CustomerD VDM Sent	R/W	0h	
68	VDM Entered Mode	R/W	0h	
67	CustomerD VDM Arrived	R/W	0h	
66	MBRD Buffer Ready	R/W	0h	
65	TX Memory Buffer Empty	R/W	0h	
64	PD3 Status Updated	R/W	0h	
63	Intel VID Status Updated	R/W	0h	
62	DP SID Status Updated	R/W	0h	
61	External DCDC Event Received	R/W	0h	External DCDC Event received
60	RESERVED	R/W	0h	Reserved
59	USVID Other VDM Received	R/W	0h	
58	USVID Attention VDM Received	R/W	0h	
57	USVID Mode Exited	R/W	0h	
56	USVID Mode Entered	R/W	0h	
56-55	Connection Manager Update	R/W	0h	
57-55	RESERVED	R/W	0h	Reserved
56-54	RESERVED	R/W	0h	Reserved
55-54	USB Status Update	R/W	0h	Reserved.
53	Data Reset Start	R/W	0h	
52	Exit mode Completed	R/W	0h	

Table 3-20. Interrupt Clear for I2C1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
51	Discover mode Completed	R/W	0h	
50	VDM Message Sent	R/W	0h	
49	AM Entered	R/W	0h	
48	AM Entry Fail	R/W	0h	
47	RESERVED	R/W	0h	Reserved
46	Unable to Source Error	R/W	0h	
45-44	RESERVED	R/W	0h	Reserved
43	Plug Early Notification	R/W	0h	
42	Sink Transition Completed	R/W	0h	
41	Discharge Failed Error	R/W	0h	
40	RESERVED	R/W	0h	Reserved
39	Message Data Error	R/W	0h	
38	Protocol Error	R/W	0h	
37	RESERVED	R/W	0h	Reserved
36	Missing Get Capabalities Message Error	R/W	0h	
35	Power Event Occurred Error	R/W	0h	
34	Can Provide Voltage or Current Later Error	R/W	0h	
33	Cannot Provide Voltage or Current Error	R/W	0h	
32	Device Incompatible Error	R/W	0h	
31	CMD2 Complete	R/W	0h	
30	CMD1 Complete	R/W	0h	
29-28	RESERVED	R/W	0h	Reserved
27	PD Status Updated	R/W	0h	
26	Status Updated	R/W	0h	
25	Data Status Updated	R/W	0h	
24	Power Status Updated	R/W	0h	
23	Power Path Switch Changed	R/W	0h	
22	RESERVED	R/W	0h	Reserved
21	USB Host No Longer Present	R/W	0h	
20	USB Host Present	R/W	0h	
19	RESERVED	R/W	0h	Reserved
18	Data Swap Requested	R/W	0h	
17	Power Swap Requested	R/W	0h	
16-15	RESERVED	R/W	0h	Reserved
14	Source Cap Message Received	R/W	0h	
13	New Contract as Provider	R/W	0h	
12	New Contract as Consumer	R/W	0h	
11	VDM received	R/W	0h	
10	Attention Received	R/W	0h	
9	Overcurrent	R/W	0h	

Table 3-20. Interrupt Clear for I2C1 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-7	RESERVED	R/W	0h	Reserved
6	FR Swap Complete	R/W	0h	
5	Data Swap Complete	R/W	0h	
4	Power Swap Complete	R/W	0h	
3	Plug Insert or Removal	R/W	0h	
2	RESERVED	R/W	0h	Reserved
1	PD Hardreset	R/W	0h	
0	RESERVED	R/W	0h	Reserved

3.19 Interrupt Clear for I2C2 Register (Offset = 19h) [Reset = 00000000000000000000h]

Interrupt Clear for I2C2 is shown in Table 3-21.

Return to the Summary Table.

Interrupt clear bit field for INT_EVENT2. Bits set in this register are cleared from INT_EVENT2. Bytes 1 to 10 of this register are port-specific, but Byte 11(Bits 80-87) is common to all ports in the PD controller.

Table 3-21. Interrupt Clear for I2C2 Register Field Descriptions

Bit	Field	Type	Reset	Description
87-83	RESERVED	R/W	0h	Reserved
82	I2C Controller NACKed	R/W	0h	
81	Ready for Patch	R/W	0h	
80	Patch Loaded	R/W	0h	
79	Alert Message Received	R/W	0h	
78	Chunk Request Received	R/W	0h	
77	Chunk Response Received	R/W	0h	
76	FRS Signal Received	R/W	0h	
75	External DCDC Status Change	R/W	0h	
74	I2C Communication error with external PP	R/W	0h	
73	Mailbox Updated	R/W	0h	
72	RESERVED	R/W	0h	Reserved
71	Notsupported Received	R/W	0h	
70	Event SOC ACK Timeout	R/W	0h	
69	CustomerD VDM Sent	R/W	0h	
68	VDM Entered Mode	R/W	0h	
67	CustomerD VDM Arrived	R/W	0h	
66	MBRD Buffer Ready	R/W	0h	
65	TX Memory Buffer Empty	R/W	0h	
64	PD3 Status Updated	R/W	0h	
63	Intel VID Status Updated	R/W	0h	
62	DP SID Status Updated	R/W	0h	
61	External DCDC Event Received	R/W	0h	External DCDC Event received
60	RESERVED	R/W	0h	Reserved
59	USVID Other VDM Received	R/W	0h	
58	USVID Attention VDM Received	R/W	0h	
57	USVID Mode Exited	R/W	0h	
56	USVID Mode Entered	R/W	0h	
56-55	Connection Manager Update	R/W	0h	
57-55	RESERVED	R/W	0h	Reserved
56-54	RESERVED	R/W	0h	Reserved
55-54	USB Status Update	R/W	0h	
53	Data Reset Start	R/W	0h	
52	Exit mode Completed	R/W	0h	

Table 3-21. Interrupt Clear for I2C2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
51	Discover mode Completed	R/W	0h	
50	VDM Message Sent	R/W	0h	
49	AM Entered	R/W	0h	
48	AM Entry Fail	R/W	0h	
47	RESERVED	R/W	0h	Reserved
46	Unable to Source Error	R/W	0h	
45-44	RESERVED	R/W	0h	Reserved
43	Plug Early Notification	R/W	0h	
42	Sink Transition Completed	R/W	0h	
41	Discharge Failed Error	R/W	0h	
40	RESERVED	R/W	0h	Reserved
39	Message Data Error	R/W	0h	
38	Protocol Error	R/W	0h	
37	RESERVED	R/W	0h	Reserved
36	Missing Get Capabalities Message Error	R/W	0h	
35	Power Event Occurred Error	R/W	0h	
34	Can Provide Voltage or Current Later Error	R/W	0h	
33	Cannot Provide Voltage or Current Error	R/W	0h	
32	Device Incompatible Error	R/W	0h	
31	CMD2 Complete	R/W	0h	
30	CMD1 Complete	R/W	0h	
29-28	RESERVED	R/W	0h	Reserved
27	PD Status Updated	R/W	0h	
26	Status Updated	R/W	0h	
25	Data Status Updated	R/W	0h	
24	Power Status Updated	R/W	0h	
23	Power Path Switch Changed	R/W	0h	
22	RESERVED	R/W	0h	Reserved
21	USB Host No Longer Present	R/W	0h	
20	USB Host Present	R/W	0h	
19	RESERVED	R/W	0h	Reserved
18	Data Swap Requested	R/W	0h	
17	Power Swap Requested	R/W	0h	
16-15	RESERVED	R/W	0h	Reserved
14	Source Cap Message Received	R/W	0h	
13	New Contract as Provider	R/W	0h	
12	New Contract as Consumer	R/W	0h	
11	VDM received	R/W	0h	
10	Attention Received	R/W	0h	
9	Overcurrent	R/W	0h	

Table 3-21. Interrupt Clear for I2C2 Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
8-7	RESERVED	R/W	0h	Reserved
6	FR Swap Complete	R/W	0h	
5	Data Swap Complete	R/W	0h	
4	Power Swap Complete	R/W	0h	
3	Plug Insert or Removal	R/W	0h	
2	RESERVED	R/W	0h	Reserved
1	PD Hardreset	R/W	0h	
0	RESERVED	R/W	0h	Reserved

3.20 Status Register (Offset = 1Ah) [Reset = 0000000000h]

Status is shown in Table 3-22.

Return to the Summary Table.

Status bit field for non-interrupt events.

Table 3-22. Status Register Field Descriptions

Bit	Field	Type	Reset	Description
39-34	RESERVED	R	0h	Reserved
33-32	AM Status	R	0h	Status of alternate mode negotiations. 0h = No Alternate Modes attempted 1h = At least one Alternate Mode entry successful 2h = At least one Alternate Mode entry unsuccessful 3h = Some Alt Mode entries successful and some failed
31	RESERVED	R	0h	Reserved
30	SOC Ack Timeout	R	0h	Indicates whether the attached SoC has responded timely. 0h = SoC has responded timely 1h = SoC has not responded timely
29-28	RESERVED	R	0h	Reserved
27	BIST	R	0h	Indicates if a BIST procedure is in progress. 0h = No BIST in progress 1h = BIST in progress
26	RESERVED	R	0h	Reserved
25-24	Acting as Legacy	R	0h	Indicates when PD Controller has gone into a mode where it is acting like a legacy (non PD) device. It can take approximately 10 seconds for the PD controller to determine that it is attached to a legacy source or sink. 0h = PD Controller is not in a legacy (non PD) mode 1h = PD Controller is acting like a legacy sink 2h = PD Controller is acting like a legacy source 3h = Acting as legacy sink due to dead-battery.
23-22	USB Host Present	R	0h	USB host attachment status. 0h = No host present 1h = Attached source is not data capable 2h = Attached source is not USB PD capable 3h = Host present
21-20	VBUS Status	R	0h	Indicates the present state of VBUS. 0h = At vSafe0V (less than 0.8V) 1h = At vSafe5V (4.75V to 5.5V) 2h = Within expected limits 3h = Not within any of the other specified ranges
19-8	RESERVED	R	0h	Reserved
7	EPR Mode Is Active	R	0h	
6	Data Role	R	0h	PD controller data role. This is only valid once there is a connection. 0h = Upward-facing port (UFP) 1h = Downward-facing port (DFP)
5	Port Role	R	0h	Current state of PD Controller CCx terminations. This also indicates the PD Controller Power Role, once connected. This bit does not toggle during Unattached.* state transitions. 0h = PD Controller is in the Sink role 1h = PD Controller is Source (CCx pull-up active)
4	Plug Orientation	R	0h	Plug orientation indicator. Indicates port orientation when known (requires connection). 0h = Upside-up orientation (plug CC on CC1) 1h = Upside-down orientation (plug CC on CC2)

Table 3-22. Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-1	Connection State	R	0h	Details of a connected plug. 0h = No connection 1h = Port is disabled 2h = Audio connection (Ra/Ra) 3h = Debug connection (Rd/Rd) 4h = No connection Ra detected (Ra but no Rd) 5h = Reserved (may be used for Rp/Rp Debug connection) 6h = Connection present no Ra detected 7h = Connection present Ra detected
0	Plug Present	R	0h	Status of the plug 0h = No plug is connected 1h = A plug is connected

3.21 SX Config Register (Offset = 1Fh) [Reset = 00000000000000000000000000000000000000000000000000h]

SX Config is shown in Table 3-23.

Return to the Summary Table.

Power state configuration. The Host may write the current system power state, and a change in power state triggers a new Application Configuration to be applied. Virtual App Config GPIO are also triggered in this register.

Table 3-23. SX Config Register Field Descriptions

Bit	Field	Type	Reset	Description
191-148	RESERVED	R	0h	Reserved
147-145	S5 Config Address Port 1	R	0h	Port1 virtual address of S5 config. This config will be loaded in S5.
144	S5 Config Enable	R	0h	Enables App Config loading upon entry to S5.
143-100	RESERVED	R	0h	Reserved
99-97	S4 Config Address Port 1	R	0h	Port1 virtual address of S4 config. This config will be loaded in S4.
96	S4 Config Enable	R	0h	Enables App Config loading upon entry to S4.
95-52	RESERVED	R	0h	Reserved
51-49	S3 Config Address Port 1	R	0h	Port1 virtual address of S3 config. This config will be loaded in S3.
48	S3 Config Enable	R	0h	Enables App Config loading upon entry to S3.
47-4	RESERVED	R	0h	Reserved
3-1	S0 Config Address Port 1	R	0h	Port1 virtual address of S0 config. This config will be loaded in S0.
0	S0 Config Enable	R	0h	Enables App Config loading upon entry to S0.

3.22 Set Sx App Config Register (Offset = 20h) [Reset = 0000h]

Set Sx App Config is shown in Table 3-24.

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Configuration based on system state. The Host may write the current system power state, and a change in power state triggers a new Application Configuration to be applied. Virtual App Config GPIO are also triggered in this register.

Table 3-24. Set Sx App Config Register Field Descriptions

Bit	Field	Type	Reset	Description
15-3	RESERVED	R/W	0h	Reserved
2-0	Sleep State	R/W	0h	Current sleep state. When a change in sleep state occurs, a new app config will be applied per the settings in 0x1F 0h = S0 1h = S3 2h = S4 3h = S5 4h = S0ix 5h = Reserved

3.23 Discovered SVIDs Register (Offset = 21h) [Reset = 0000000000000000000000000000000000000000000000000000000000000000h]

Discovered SVIDs is shown in Table 3-25.

Return to the Summary Table.

Received Discover SVID ACK message(s). This register contains the SVID information returned from Discover SVIDs REQ messages.

Table 3-25. Discovered SVIDs Register Field Descriptions

Bit	Field	Type	Reset	Description
263-248	SVID SOPPrime 7	R	0h	Eighth SVID supported by SOP' cable plug
247-232	SVID SOPPrime 6	R	0h	Seventh SVID supported by SOP' cable plug
231-216	SVID SOPPrime 5	R	0h	Sixth SVID supported by SOP' cable plug
215-200	SVID SOPPrime 4	R	0h	Fifth SVID supported by SOP' cable plug
199-184	SVID SOPPrime 3	R	0h	Fourth SVID supported by SOP' cable plug
183-168	SVID SOPPrime 2	R	0h	Third SVID supported by SOP' cable plug
167-152	SVID SOPPrime 1	R	0h	Second SVID supported by SOP' cable plug
151-136	SVID SOPPrime 0	R	0h	First SVID supported by SOP' cable plug
135-120	SVID SOP 7	R	0h	Eighth SVID supported by SOP port partner
119-104	SVID SOP 6	R	0h	Seventh SVID supported by SOP port partner
103-88	SVID SOP 5	R	0h	Sixth SVID supported by SOP port partner
87-72	SVID SOP 4	R	0h	Fifth SVID supported by SOP port partner
71-56	SVID SOP 3	R	0h	Fourth SVID supported by SOP port partner
55-40	SVID SOP 2	R	0h	Third SVID supported by SOP port partner
39-24	SVID SOP 1	R	0h	Second SVID supported by SOP port partner
23-8	SVID SOP 0	R	0h	First SVID supported by SOP port partner
7-4	Number SOPPrime SVIDS	R	0h	Number of SVIDs discovered on SOP'
3-0	Number SOP SVIDS	R	0h	Number of SVIDs discovered on SOP.

3.24 Connection Manager Status Register (Offset = 22h) [Reset = 00h]

Connection Manager Status is shown in Table 3-26.

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Connection Manager Status shows the capabilities of the host connected

Table 3-26. Connection Manager Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	PCIe Host Connected	R	0h	PCIe Host Connected 0h = No PCIe Host Connected 1h = PCIe Host Connected
5	USB4 Host Connected	R	0h	USB4 Host Connected 0h = No USB4 Host Connected 1h = USB4 Host Connected
4	TBT Host Connected	R	0h	TBT Host Connected 0h = No TBT Host Connected 1h = TBT Host Connected
3	DP Host Connected	R	0h	DP Host Connected 0h = No DP Host Connected 1h = DP Host Connected
2	USB3 Host Connected	R	0h	USB3 Host Connected 0h = No USB3 Host Connected 1h = USB3 Host Connected
1	USB2 Host Connected	R	0h	USB2 Host Connected 0h = No USB2 Host Connected 1h = USB2 Host Connected
0	RESERVED	R	0h	Reserved

3.25 USB Config Register (Offset = 23h) [Reset = 0001E000h]

USB Config is shown in Table 3-27.

Return to the Summary Table.

USB configuration. This register is used to formulate Enter_USB message when applicable. If the host requires changes to this register to take effect for an existing connection it must issue the 'DRST' 4CC task after writing the USB_CONFIG register. The recommended sequence is as follows: Write the changes to the USB_CONFIG register and issue the 'DRST' 4CC Task.The PD controller will then follow the USB data reset process.Once the data reset is complete, the PD controller will use the latest values in the USB_CONFIG register to formulate any Enter_USB message it sends.

Table 3-27. USB Config Register Field Descriptions

Bit	Field	Type	Reset	Description
31-27	RESERVED	R/W	0h	Reserved
26	USB4 DRD	R/W	0h	Dual-role data capability for USB4. Assert if capable of operating as a USB4 device. Note that the USB PD spec requirements dictate that if this bit is asserted, the system also has to be device capable for USB 2.0.
25	USB3 DRD	R/W	0h	Dual-role data capability for USB3. Assert if capable of operating as a USB3 device.
24-17	RESERVED	R/W	0h	Reserved
16	PCIe Supported	R/W	1h	PCIe control. This is used to set the "PCIe Support" bit when transmitting the Enter_USB message.
15	DP Supported	R/W	1h	DP support control. This is used to set the "DP Support" bit when transmitting the Enter_USB message.
14	TBT3 Supported	R/W	1h	TBT3 support control. This is used to set the "TBT Support" bit when transmitting the Enter_USB message.
13	Host Present	R/W	1h	Host present control. This is used to set the "Host Present" bit when transmitting the Enter_USB message.
12-0	RESERVED	R/W	0h	Reserved

3.26 USB Status Register (Offset = 24h) [Reset = 0000000000000000h]

USB Status is shown in Table 3-28.

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USB status. This register provides status of transmitted or received Enter_USB message when applicable.

Table 3-28. USB Status Register Field Descriptions

Bit	Field	Type	Reset	Description
71-40	TBT Enter Mode VDO Data Rx Tx	R	0h	vPro mode VDO. This is the VDO received by the UFP or transmitted by the DFP when vPro mode was entered.
39-8	USB4 Enter USB Rx Tx	R	0h	Enter_USB Data Object (EUDO). This follows the USB PD definition for EUDO, it is sent by the DFP and received by the UFP.
7	RESERVED	R	0h	Reserved
6	USB Rentry Needed	R	0h	Asserted when USB Re-entry is needed.
5	Vpro Entry Failed	R	0h	vPro mode error. This bit is asserted if an error occurred while trying to enter the vPro mode.
4	USB Mode Active on Plug	R	0h	USB4 mode status with Cable Plug. This bit is asserted when the mode required for USB4 has been entered on Cable Plug.
3-2	USB4 Required Plug Mode	R	0h	USB4 mode requirement for Cable Plug. This field indicates which mode must be entered on the Cable Plug to enable USB4 mode. 0h = None 1h = Reserved 2h = USB4 3h = TBT3
1-0	EUDO Sop Sent/Received	R	0h	USB4 status indicator with Port Partner. This bit is asserted while the USB4 mode is active with Port Partner. 0h = No Enter_USB. Enter_USB has not been sent as DFP 1h = Enter_USB timeout. The UFP should have received an 2h = Enter_USB failure. In DFP mode the transmitted En 3h = Successful Enter_USB. An Enter_USB was transmitted

3.27 Connection Manager Control Register (Offset = 25h) [Reset = 00h]

Connection Manager Control is shown in Table 3-29.

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Connection Manager Control used to exchange the capabilities from Connection Manager Status

Table 3-29. Connection Manager Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	PCIe Host Connected	R/W	0h	PCIe Host Connected 0h = No PCIe Host Connected 1h = PCIe Host Connected
5	USB4 Host Connected	R/W	0h	USB4 Host Connected 0h = No USB4 Host Connected 1h = USB4 Host Connected
4	TBT Host Connected	R/W	0h	TBT Host Connected 0h = No TBT Host Connected 1h = TBT Host Connected
3	DP Host Connected	R/W	0h	DP Host Connected 0h = No DP Host Connected 1h = DP Host Connected
2	USB3 Host Connected	R/W	0h	USB3 Host Connected 0h = No USB3 Host Connected 1h = USB3 Host Connected
1	USB2 Host Connected	R/W	0h	USB2 Host Connected 0h = No USB2 Host Connected 1h = USB2 Host Connected
0	RESERVED	R/W	0h	Reserved

3.28 Power Path Status Register (Offset = 26h) [Reset = 0000000000h]

Power Path Status is shown in Table 3-30.

Return to the Summary Table.

Power Path Status.

Table 3-30. Power Path Status Register Field Descriptions

Bit	Field	Type	Reset	Description
39-38	Power Source	R	0h	Indicates current PD Controller power source. NOTE: Since the Dead Battery flag forces PD Controller to be powered from VBUS, only 10b is valid when this flag is set. Any other setting indicates that the Dead Battery flag is not set. 0h = Reserved 1h = PD Controller is powered from VIN_3V3 2h = PD Controller is powered from VBUS 3h = Reserved
37-36	RESERVED	R	0h	Reserved
35	PPCable2 Overcurrent	R	0h	PP_CABLE2 overcurrent indicator. Asserted if an overcurrent condition exists on PP_CABLE2 (VCONN).
34	PPCable1 Overcurrent	R	0h	PP_CABLE1 overcurrent indicator. Asserted if an overcurrent condition exists on PP_CABLE1 (VCONN).
33-30	RESERVED	R	0h	Reserved
29	PP2 Overcurrent	R	0h	PP_5V2 overcurrent indicator. Asserted if an overcurrent conditions exists on PP2 switch (PP_5V2).
28	PP1 Overcurrent	R	0h	PP_5V1 overcurrent indicator. Asserted if an overcurrent conditions exists on PP1 switch (PP_5V1).
27-24	RESERVED	R	0h	Reserved
23-21	PP6 Switch	R	0h	Indicates current state of PP6 (Virtual). 0h = PP6 switch disabled 1h = The PP5 switch is currently disabled due to fault (system output) 2h = PP6 switch enabled (system output) 3h = PP6 switch enabled (system input)
20-18	PP5 Switch	R	0h	Indicates current state of PP5 (Virtual). 0h = PP5 switch disabled 1h = The PP5 switch is currently disabled due to fault (system output) 2h = PP5 switch enabled (system output) 3h = PP5 switch enabled (system input)
17-15	PP4 Switch	R	0h	Indicates current state of PP4 (PP_EXT2). 0h = PP4 switch disabled 1h = The PP4 switch is currently disabled 2h = PP4 switch enabled (system output) 3h = PP4 switch enabled (system input)
14-12	PP3 Switch	R	0h	Indicates current state of PP3 (PP_EXT1). 0h = PP3 switch disabled 1h = PP3 switch currently disabled due to fault 2h = PP3 switch enabled (system output) 3h = PP3 switch enabled (system input)
11-9	PP2 Switch	R	0h	Indicates current state of PP2 switch (PP_5V2). 0h = PP2 switch disabled 1h = PP2 switch currently disabled due to fault 2h = PP2 switch enabled (system output)
8-6	PP1 Switch	R	0h	Indicates current state of PP1 switch (PP_5V1). 0h = PP1 switch disabled 1h = PP1 switch currently disabled due to fault 2h = PP1 switch enabled (system output)
5-4	RESERVED	R	0h	Reserved

Table 3-30. Power Path Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	PPCable2 Switch	R	0h	Indicates current state of PP_CABLE2 switch. 0h = PP_CABLE2 switch disabled 1h = PP_CABLE2 switch currently disabled 2h = PP_CABLE2 switch CC1 enabled (system output) 3h = PP_CABLE2 switch CC2 enabled (system output)
1-0	PPCable1 Switch	R	0h	Indicates current state of PP_CABLE1 switch. 0h = PP_CABLE1 switch disabled 1h = PP_CABLE1 switch currently disabled 2h = PP_CABLE1 switch CC1 enabled (system output) 3h = PP_CABLE1 switch CC2 enabled (system output)

3.29 Global System Configuration Register (Offset = 27h) [Reset = 0000000000000001A07198C12AD25h]

Global System Configuration is shown in Table 3-31.

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Global system configuration (all ports). This register contains configuration bits that define hardware that is common to all ports and in most cases will not change in normal operation or will not require immediate action if changed. Any modifications to this register will cause a port disconnect and reconnect with the new settings. Initialized by Application Customization.

Table 3-31. Global System Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
115-83	RESERVED	R/W	0h	Reserved
82	Wait for Minimum Power	R/W	0h	Stalls the PD in PTCH mode until a power connection is made that meets the needed conditions then continues initialization
81	Wait for VIN_3V3	R/W	0h	Stalls the PD in PTCH mode until Vsys is present. Meant for Desktop designs only
80	Vsys Prevents High Power	R/W	0h	Halts setting up External DCDC configuration until 5V power is present from the system. Will not configure any DCDC devices in Dead-Battery Mode
79-72	Port2 I2C2 Target Address	R/W	0h	Target address for Port 2 on I2C2s.
71-64	Port1 I2C2 Target Address	R/W	0h	Target address for Port 1 on I2C2s.
63-56	External DCDC Status Polling Interval	R/W	0h	
55-54	RESERVED	R/W	0h	Reserved
53-49	RESERVED	R/W	0h	Reserved
48	RESERVED	R/W	0h	Reserved
47	Enable AM entry/exit on low-power mode exit/entry	R/W	0h	
46	EPR Supported As Sink	R/W	0h	
45	EPR Supported As Source	R/W	0h	
44-43	USB Default Current	R/W	0h	This field selects the value for USB default current. It is used in conjunction with the MinimumCurrentAdvertisement field. 1h = 900mA 2h = 150 mA 3h = Reserved
42	I2C 3M Voltage Threshold	R/W	1h	Pull-up voltage for I2C3m. This is set to 3.3V by default. 0h = 1.8 V 1h = 3.3 V
41	I2C 2S Voltage Threshold	R/W	1h	Pull-up voltage for I2C2s. This is set to 1.8V by default. 0h = 1.8 V 1h = 3.3 V
40	I2C EC Voltage Threshold	R/W	1h	Pull-up voltage for I2C_EC. This is set to 1.8V by default. 0h = 1.8 V 1h = 3.3 V
39	Minimum Current Advertisement	R/W	0h	Configuration for SPM. If the PD controller is configured to automatically reduce the current advertisement, it reduces to this value. 0h = USB default 1h = 1.5 A
38	Emulate Single Port	R/W	0h	Assert this bit to disable one port. If this bit is asserted the PD controller will only support one Type-C port (Port A).
37	Disable EEPROM Updates	R/W	0h	EEPROM updates not allowed if this bit asserted.

Table 3-31. Global System Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
36-34	I2C Timeout	R/W	6h	I2C bus timeout. The PD controller will reset its I2C target hardware if for some reason it holds the SCL line low for more than the time selected in this register. This prevents locking up the I2C bus. This applies to both I2C1s_SCL and I2C2s_SCL. 0h = 25 ms 1h = 50 ms 2h = 75 ms 3h = 100 ms 4h = 125 ms 5h = 150 ms 6h = 175 ms 7h = 1000 ms
33	Enable I2CMultiController Mode	R/W	0h	Enables I2C Multi Controller mode
32-31	MultiPort Sink Non Overlap Time	R/W	3h	Delay configuration for MultiPortSinkPolicy. Controls the amount of time a new Sink input path closes after the old Sink input path opens. This forms a break-before-make condition when controlling Sink paths from both ports. This is only applicable when MultiPortSinkPolicy = 01b and applies to externally controlled switch paths (PP3 or PP4). This feature may be deprecated in the future. 0h = 1 ms 1h = 5 ms 2h = 10 ms 3h = 15 ms
30-29	RESERVED	R/W	0h	Reserved
28-26	TBT Controller Type	R/W	3h	Type of TBT controller. Controls specific behavior for different TBT controllers. See documentation for each TBT controller for details. 0h = Default 4h = GR Platform 5h = BR Platform
25	RESERVED	R/W	0h	Reserved
24	MultiPort Sink Policy	R/W	0h	Automatic sink-path coordination. This configures the how the PD controller controls input switches of each port when both ports are operating as a Sink. 0h = No Sink Management 1h = Highest Power
23-22	RCP Threshold	R/W	0h	Threshold used for RCP on PP_EXT. 0h = 6 mV (nominal) 1h = 8 mV (nominal) 2h = 10 mV (nominal) 3h = 12 mV (nominal)
21-19	PP4 Config	R/W	2h	PP4 configuration. This register configures PP4 switch controls. 0h = PP4 not used and disabled 1h = PP4 is a Source (output) 2h = PP4 is a Sink (input) 3h = PP4 is sink but waits for 'SRDY' 4h = PP3 is bi-directional 5h = PP4 is bi-directional but waits for 'SRDY'
18-16	PP3 Config	R/W	2h	PP3 configuration. This register configures PP3 switch controls. 0h = PP3 not used and disabled 1h = PP3 is a Source (output) 2h = PP3 is a Sink (input) 3h = PP3 is sink but waits for 'SRDY' 4h = PP3 is bi-directional 5h = PP3 is bi-directional but waits for 'SRDY'
15-14	ILIM Over Shoot	R/W	2h	PP_5V ILIM configuration. Controls the amount of overshoot used by the FW to select the current limit for the PP5V to Px_VBUS. 0h = No additional overshoot margin 1h = Overshoot margin of at least 100 mA 2h = Overshoot margin of at least 200 mA 3h = Reserved

Table 3-31. Global System Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-11	PP2 Config	R/W	5h	PP2 configuration (PP_5V2). 0h = Not used (disabled) 1h = PP2 configured as source
10-8	PP1 Config	R/W	5h	PP1 configuration (PP_5V1). 0h = Not used (disabled) 1h = PP1 configured as source
7-6	PP6 Config	R/W	0h	PP6 configuration (Virtual). 0h = Not used (disabled) 1h = PP6 configured as source
5-4	PP5 Config	R/W	2h	PP5 configuration (Virtual). 0h = Not used (disabled) 1h = PP5 configured as source
3	RESERVED	R/W	0h	Reserved
2	PP Cable2 Switch Config	R/W	1h	Enable PP_CABLE2. If this bit is asserted the PD controller will enable VCONN on PP_CABLE2 when required for USB specification compliance.
1	RESERVED	R/W	0h	Reserved
0	PP Cable1 Switch Config	R/W	1h	Enable PP_CABLE1. If this bit is asserted the PD controller will enable VCONN on PP_CABLE1 when required for USB specification compliance.

3.30 Port Configuration Register (Offset = 28h) [Reset = 00000000000000000000000000002F4802h]

Port Configuration is shown in Table 3-32.

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Configuration for port-specific hardware. This register configures hardware that is specific for each port and in most cases will not change in normal operation or will not require immediate action if changed. Any modifications to this register will cause a port disconnect and reconnect with the new settings. Initialized by Application Customization.

Table 3-32. Port Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
135-130	RESERVED	R/W	0h	Reserved
129-128	Fixed PDO ILIM	R/W	0h	Added current offset for Fixed PDO Contract 0h = No Offset 1h = 150mA 2h = 300mA 3h = 450mA
127-96	RESERVED	R/W	0h	Reserved
95-80	Greater Than Threshold Voltage	R/W	0h	Threshold voltage to trigger the GREATER_THAN_THRESHOLD_VOLTAGE GPIO Event (50mV per LSB).
79-73	RESERVED	R/W	0h	Reserved
72	Sink Mode I2C IRQ Config	R/W	0h	Enables support for GPIO10 to I2C IRQ
71-64	External DCDC Type	R/W	0h	External DCDC Type 0h = Marina Bay 1h = Reserved
63-48	VBUS For Valid PPS Status	R/W	0h	
47-32	APDO VBUS Uvp TripPoint Offset	R/W	0h	
31	RESERVED	R/W	0h	Reserved
30-29	APDO ILIM Over Shoot	R/W	0h	
28-27	APDO VBUS UVP Threshold	R/W	0h	
26-24	VBUS Sink UVP Trip HV	R/W	0h	VBUS disconnect when power role is sink. The disconnect threshold is set to (1-VBUS_SinkUvpTripHV)*(min expected VBUS). The 000b setting follows the USB-C specification requirements. Use a non-zero value for additional margin. 0h = 5% 1h = 10% 2h = 15% 3h = 20% 4h = 25% 5h = 30% 6h = 40%
23-22	RESERVED	R/W	0h	Reserved
21-20	OVP for PP5V	R/W	2h	VBUS OVP settings while sourcing from PP5V. This applies while sourcing through PP1 or PP2. See data-sheet for voltage range. 0h = Use setting 0: 5.25 V (typical) 1h = Use setting 1: 5.5 V (typical) 2h = Use setting 2: 5.8 V (typical) 3h = Use setting 3: 6.1 V (typical)
19-18	Soft Start	R/W	3h	Soft start configuration settings. Controls the soft start for the sinking power path switch. 0h = 0.41 V/ms (typical) 1h = 0.79 V/ms (typical) 2h = 1.57 V/ms (typical) 3h = 3.39 V/ms (typical)

Table 3-32. Port Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
17-16	VBUS OVP Usage	R/W	3h	OVP configuration settings. These two bits are used to select the OVP trip-point. The PD controller automatically computes the lowest threshold that does not overlap with the expected maximum voltage (including maximum tolerance allowed by USB PD specification). The OVP trip-point will be set at the selected percentage of the computed threshold. 0h = 100% 1h = 105% 2h = 111% 3h = 114%
15	RESERVED	R/W	0h	Reserved
14-13	USB3 Rate	R/W	2h	USB3 configuration. 0h = USB3 not supported 1h = USB3 Gen1 signaling rate supported 2h = USB3 Gen2 signaling rate supported 3h = Reserved
12	DebugAccessory Support	R/W	0h	
11	USB Communication Capable	R/W	1h	USB communications capable. Assert this bit in systems that are USB communications capable.
10	Disable PD	R/W	0h	Assert this bit to disable USB PD.
9-8	TypeC Support Options	R/W	0h	Configuration for optional features. This register controls whether optional Type-C state machine states are supported. NOTE: These states are mutually-exclusive and these options only exist when specific Type-C state machines are used. 0h = No Type-C optional states are supported 1h = Try.SRC state is supported 3h = Reserved
7-2	RESERVED	R/W	0h	Reserved
1-0	TypeC State machine	R/W	2h	Port Configuration. 0h = Sink state machine only 1h = Source state machine only 2h = DRP state machine 3h = Disabled

3.31 Port Control Register (Offset = 29h) [Reset = 00C1C051h]

Port Control is shown in Table 3-33.

Return to the Summary Table.

Configuration bits affecting system policy. These bits may change during normal operation and are used for controlling the respective port. The PD Controller will not take immediate action upon writing. Changes made to this register will take effect the next time the appropriate policy is invoked. Initialized by Application Customization.

Table 3-33. Port Control Register Field Descriptions

Bit	Field	Type	Reset	Description
31-30	Charger Detect Enable	R/W	0h	Configure the types of legacy chargers to detect. 0h = Do not detect any legacy chargers 1h = Detect BC 1.2 chargers 2h = Reserved do not use 3h = Detect BC 1.2 and proprietary legacy chargers
29	USB Disable	R/W	0h	Overrides USB connections in DATA_STATUS. If this bit is asserted, it forces USB2Connection and USB3Connection in the DATA_STATUS (0x5F) register to be zero.
28-26	Charger Advertise Enable	R/W	0h	Configure the types of legacy chargers to emulate. 0h = Do not emulate any legacy charger 1h = BC 1.2 CDP only 2h = BC 1.2 DCP only 3h = Reserved 4h = Reserved 5h = DCP Auto 1 (2.7V and DCP) 6h = DCP Auto 2 (1.2V 2.7V and DCP) 7h = Reserved
25-24	RESERVED	R/W	0h	Reserved
23	VCONN Current Limit	R/W	1h	Current limit configuration for PP_CABLEx. 0h = 410 mA (typical) 1h = 590 mA (typical)
22	FR Swap Enabled	R/W	1h	Enable Fast-Role Swap as initial sink. Assert this bit to enable Fast-Role Swap detection. If the amount of current the Port Partner requires during Fast-Role Swap process is less than or equal to the current in TX_SOURCE_CAPS.TXSourcePDO1 when an FRS signal is detected, then the device will perform a fast-role swap.
21	Sink Control Bit	R/W	0h	Configure reaction to UnconstrainedPower bit. This configures whether the state of the UnconstrainedPower bit affects PP3 or PP4. 0h = No affect on sink switches 1h = Disable sink switches automatically
20	Enable Current Monitor	R/W	0h	Assert this bit to enable the current monitor (peak and average) that are read from the ADC_RESULTS register. While asserted the PD controller will remain in the active power mode.
19	Unconstrained Power	R/W	0h	External power configuration. This also sets the Unconstrained Power bit defined by USB PD. When this bit is changed from 1 to 0 the PD controller will not attempt a power role swap with the Port Partner. If a power role swap is desired the host should issue a 'SWSr' 4CC command. 0h = No external power 1h = External power present
18	Force USB3 Gen1	R/W	0h	Forced Gen1 operation 0h = DATA_STATUS 1h = DATA_STATUS
17	AM Intrusive Mode	R/W	0h	Assert to allow host to manage Alt mode process. It is recommended that this bit be set to 0b so that the PD controller can automatically handle Alternate Mode entry and exit. 0h = Do not operate in Alternate Mode Intrusive mode 1h = Disable automatic mode entry

Table 3-33. Port Control Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
16	Automatic ID Request	R/W	1h	Configure identity discovery for SOP. If this bit is asserted, the PD Controller will automatically issue Discover Identity VDM for all SOP types when appropriate.
15	Initiate Swap to DFP	R/W	1h	Configure DR_Swap to DFP initiation. If this bit is asserted, the PD Controller automatically initiates and sends DR_Swap requests to the Port Partner when appropriate if presently operating as UFP.
14	Process Swap to DFP	R/W	1h	Configure response to DR_Swap to DFP. If this bit is asserted, the PD Controller will automatically accept a DR_Swap request to become a DFP. Otherwise, the PD Controller will reject such a request.
13	Initiate Swap to UFP	R/W	0h	Configure DR_Swap to UFP initiation. If this bit is asserted, the PD Controller automatically initiates and sends DR_Swap requests to the Port Partner when appropriate if presently operating as DFP.
12	Process Swap to UFP	R/W	0h	Configure response to DR_Swap to UFP. If this bit is asserted, the PD Controller will automatically accept a DR_Swap request to become a UFP. Otherwise, the PD Controller will reject such a request.
11	RESERVED	R/W	0h	Reserved
10	Auto PPS Status Enable	R/W	0h	When this bit is enabled, the PD controller calculates the message field then automatically returns PPS_Status message when a Get_PPS_Status message is received. When this bit is cleared, register value in TX_PPS_SDB(0x7A) prior to clearing the bit is retained until the TX_PPS_SDB is overridden by an external controller.
9	RESERVED	R/W	0h	Reserved
8	Automatic Cap Request	R/W	0h	When enabled the PD controller will issue a Get Sink Cap request automatically during the negotiation process. The bit is required to see the applicability of Fast Role Swap from the port partner.
7	Initiate Swap to Source	R/W	0h	Configure PR_Swap to source initiation. If this bit is asserted, the PD Controller automatically initiates and sends PR_Swap requests to the Port Partner when appropriate if presently operating as Sink (C/P).
6	Process Swap to Source	R/W	1h	Configure response to PR_Swap to source. If this bit is asserted, the PD Controller will automatically accept a PR_Swap request to become a Source. Otherwise, the PD Controller will reject such a request.
5	Initiate Swap to Sink	R/W	0h	Configure PR_Swap to sink initiation. If this bit is asserted, the PD Controller automatically initiates and sends PR_Swap requests to the Port Partner when appropriate if presently operating as Source (P/C).
4	Process Swap to Sink	R/W	1h	Configure response to PR_Swap to sink. If this bit is asserted, the PD Controller will automatically accept a PR_Swap request to become a Sink. Otherwise, the PD Controller will reject such a request.
3-2	RESERVED	R/W	0h	Reserved
1-0	TypeC Current	R/W	1h	Type-C Current advertisement. This setting is ignored if a Source role is not enabled and active. This setting is also ignored during an explicit USB PD contract, where the Rp value is used for collision avoidance as required by the USB PD specification. Note that when PP5V is low, the FW will only use the default Type-C current regardless of the value in this field. 0h = USB Default Current 1h = 1.5 A 2h = 3.0 A 3h = Reserved

3.32 Boot Flags Register (Offset = 2Dh) [Reset = 0000000000h]

Boot Flags is shown in Table 3-34.

Return to the Summary Table.

Detailed status of boot process. This register provides details on PD Controller boot flags, Customer OTP configuration, and silicon revision

Table 3-34. Boot Flags Register Field Descriptions

Bit	Field	Type	Reset	Description
39-32	Revision ID	R	0h	Revision ID for the PD controller.
31-29	Patch Config Source	R	0h	Source of patch configuration. This field indicates the source of the configuration patch that has been successfully loaded. 0h = No configuration has been loaded 1h = Source-only default configuration 00b 2h = Source-only default configuration 01b 3h = Source-only default configuration 10b 4h = Reserved 5h = A configuration has been loaded from EEPROM 6h = A configuration has been loaded from I2C 7h = Reserved
28-27	RESERVED	R	0h	Reserved
26-25	RESERVED	R	0h	
24	RESERVED	R	0h	Reserved
23-20	RESERVED	R	0h	Reserved
19	System TSD	R	0h	System thermal shut-down indicator. This bit is asserted if the PD controller is rebooting after the system thermal sensor caused a reset.
18	PP4 Switch	R	0h	PP4 switch status. This bit is asserted when the PP4 sink path was enabled during dead-battery mode
17	PP3 Switch	R	0h	PP3 switch status. This bit is asserted when the PP3 sink path was enabled during dead-battery mode
16-14	RESERVED	R	0h	Reserved
13	Region 1 CRC Fail	R	0h	Region 1 CRC status indicator. This bit is asserted when the CRC of data read from Region 1 of EEPROM memory failed.
12	Region 0 CRC Fail	R	0h	Region 0 CRC status indicator. This bit is asserted when the CRC of data read from Region 0 of EEPROM memory failed.
11	RESERVED	R	0h	Reserved
10	Patch Download Error	R	0h	Asserted when a patch download error occurs.
9	Region 1 EEPROM Error	R	0h	Region 1 status indicator. This bit is asserted when an error occurred attempting to read Region 1 of EEPROM memory. A retry may have been successful.
8	Region 0 EEPROM Error	R	0h	Region 0 status indicator. This bit is asserted when an error occurred attempting to read Region 0 of EEPROM memory. A retry may have been successful.
7	Region 1 Invalid	R	0h	Region 1 header status indicator. This bit is asserted when Region 1 header of the EEPROM memory was invalid.
6	Region 0 Invalid	R	0h	Region 0 header status indicator. This bit is asserted when Region 0 header of the EEPROM memory was invalid.
5	Region 1	R	0h	Region 1 attempted indicator. This bit is asserted when Region 1 of the EEPROM memory was attempted.
4	Region 0	R	0h	Region 0 attempted indicator. This bit is asserted when Region 0 of the EEPROM memory was attempted.
3	I2C EEPROM Present	R	0h	EEPROM presence indicator. This bit is asserted when an EEPROM device was discovered on I2C3m during boot.
2	Dead Battery Flag	R	0h	Dead Battery flag indicator. This bit is asserted when the PD Controller booted in dead-battery mode.

Table 3-34. Boot Flags Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1	RESERVED	R	0h	Reserved
0	Patch Header Error	R	0h	Asserted when a patch bundle header errors.

3.33 Build Description Register (Offset = 2Eh) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000h]

Build Description is shown in Table 3-35.

Return to the Summary Table.

Build description. This is an ASCII string that uniquely identifies custom build information.

Table 3-35. Build Description Register Field Descriptions

Bit	Field	Type	Reset	Description
391-0	Build Description	R	0h	Build description. This is an ASCII string that uniquely identifies custom build information.

3.34 Device Information Register (Offset = 2Fh) [Reset = 0000000000000000000000000000000000000000000000000000000000000000h]

Device Information is shown in Table 3-36.

Return to the Summary Table.

Device information. This is an ASCII string with hardware and firmware version information of the PD Controller.

Table 3-36. Device Information Register Field Descriptions

Bit	Field	Type	Reset	Description
319-0	Device Info	R	0h	Device information. This is an ASCII string with hardware and firmware version information of the PD Controller.

3.35 Received Source Capabilities Register (Offset = 30h) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000h]

Received Source Capabilities is shown in Table 3-37.

Return to the Summary Table.

Received Source Capabilties. This register stores latest Source Capabilities message received over BMC.

Table 3-37. Received Source Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
423-392	Source PDO 13	R	0h	EPR Sixth Source Capabilities PDO received
391-360	Source PDO 12	R	0h	EPR Fifth Source Capabilities PDO received
359-328	Source PDO 11	R	0h	EPR Fourth Source Capabilities PDO received
327-296	Source PDO 10	R	0h	EPR Third Source Capabilities PDO received
295-264	Source PDO 9	R	0h	EPR Second Source Capabilities PDO received
263-232	Source PDO 8	R	0h	EPR First Source Capabilities PDO received
231-200	Source PDO 7	R	0h	Seventh Source Capabilities PDO received
199-168	Source PDO 6	R	0h	Sixth Source Capabilities PDO received
167-136	Source PDO 5	R	0h	Fifth Source Capabilities PDO received
135-104	Source PDO 4	R	0h	Fourth Source Capabilities PDO received
103-72	Source PDO 3	R	0h	Third Source Capabilities PDO received
71-40	Source PDO 2	R	0h	Second Source Capabilities PDO received
39-8	Source PDO 1	R	0h	First Source Capabilities PDO received
7	RESERVED	R	0h	Reserved
6	Last Src Cap Received is EPR	R	0h	
5-3	Number of Valid EPR PDOs	R	0h	
2-0	Number Valid PDOs	R	0h	Number of valid PDOs in this register. Each PDO is 4 bytes. (max of 7)

3.36 Received Sink Capabilities Register (Offset = 31h) [Reset = 000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000 0000000000000000h]

Received Sink Capabilities is shown in Table 3-38.

Return to the Summary Table.

Received Sink Capabilities. This register stores latest Sink Capabilities message received over BMC.

Table 3-38. Received Sink Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
423-392	Sink PDO 13	R	0h	EPR Sixth Sink Capabilities PDO received
391-360	Sink PDO 12	R	0h	EPR Fifth Sink Capabilities PDO received
359-328	Sink PDO 11	R	0h	EPR Fourth Sink Capabilities PDO received
327-296	Sink PDO 10	R	0h	EPR Third Sink Capabilities PDO received
295-264	Sink PDO 9	R	0h	EPR Second Sink Capabilities PDO received
263-232	Sink PDO 8	R	0h	EPR First Sink Capabilities PDO received
231-200	Sink PDO 7	R	0h	Seventh Sink Capabilities PDO received
199-168	Sink PDO 6	R	0h	Sixth Sink Capabilities PDO received
167-136	Sink PDO 5	R	0h	Fifth Sink Capabilities PDO received
135-104	Sink PDO 4	R	0h	Fourth Sink Capabilities PDO received
103-72	Sink PDO 3	R	0h	Third Sink Capabilities PDO received
71-40	Sink PDO 2	R	0h	Second Sink Capabilities PDO received
39-8	Sink PDO 1	R	0h	First Sink Capabilities PDO received
7	RESERVED	R	0h	Reserved
6	Last Sink Cap Received Is EPR	R	0h	Flag showing if the last received Sink Capability is an EPR capability.
5-3	RX Sink Num Valid EPR PDOs	R	0h	Number of valid EPR PDOs in this register. Each EPR PDO is 4 bytes. (max of 6)
2-0	Number Valid PDOs	R	0h	Number of valid PDOs in this register. Each PDO is 4 bytes. (max of 7)

3.37 Transmit Source Capabilities Register (Offset = 32h) [Reset = 000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000h]

Transmit Source Capabilities is shown in Table 3-39.

Return to the Summary Table.

Source Capabilities for sending. This register stores PDOs and settings for outgoing Source Capabilities PD messages. Initialized by Application Customization.

Table 3-39. Transmit Source Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
503-485	RESERVED	R/W	0h	Reserved
484	Virtual Switch Enable for PDO13	R/W	0h	Enable external power path control via GPIO event for PDO13
483	Virtual Switch Enable for PDO12	R/W	0h	Enable external power path control via GPIO event for PDO12
482	Virtual Switch Enable for PDO11	R/W	0h	Enable external power path control via GPIO event for PDO11
481	Virtual Switch Enable for PDO10	R/W	0h	Enable external power path control via GPIO event for PDO10
480	Virtual Switch Enable for PDO9	R/W	0h	Enable external power path control via GPIO event for PDO9
479	Virtual Switch Enable for PDO8	R/W	0h	Enable external power path control via GPIO event for PDO8
478	Virtual Switch Enable for PDO7	R/W	0h	Enable external power path control via GPIO event for PDO7
477	Virtual Switch Enable for PDO6	R/W	0h	Enable external power path control via GPIO event for PDO6
476	Virtual Switch Enable for PDO5	R/W	0h	Enable external power path control via GPIO event for PDO5
475	Virtual Switch Enable for PDO4	R/W	0h	Enable external power path control via GPIO event for PDO4
474	Virtual Switch Enable for PDO3	R/W	0h	Enable external power path control via GPIO event for PDO3
473	Virtual Switch Enable for PDO2	R/W	0h	Enable external power path control via GPIO event for PDO2
472	Virtual Switch Enable for PDO1	R/W	0h	Enable external power path control via GPIO event for PDO1
471-452	RESERVED	R/W	0h	Reserved
451-450	Power Path for PDO 13	R/W	0h	Configures which PP to use for PDO13. 0h = Reserved 1h = Reserved 2h = PP_EXT1 is used for this PDO 3h = PP_EXT2 is used for this PDO
449-448	Power Path for PDO 12	R/W	0h	Configures which PP to use for PDO12. 0h = Reserved 1h = Reserved 2h = PP_EXT1 is used for this PDO 3h = PP_EXT2 is used for this PDO
447-446	Power Path for PDO 11	R/W	0h	Configures which PP to use for PDO11. 0h = Reserved 1h = Reserved 2h = PP_EXT1 is used for this PDO 3h = PP_EXT2 is used for this PDO

Table 3-39. Transmit Source Capabilities Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
445-444	Power Path for PDO 10	R/W	0h	Configures which PP to use for PDO10. 0h = Reserved 1h = Reserved 2h = PP_EXT1 is used for this PDO 3h = PP_EXT2 is used for this PDO
443-442	Power Path for PDO 9	R/W	0h	Configures which PP to use for PDO9. 0h = Reserved 1h = Reserved 2h = PP_EXT1 is used for this PDO 3h = PP_EXT2 is used for this PDO
441-440	Power Path for PDO 8	R/W	0h	Configures which PP to use for PDO8. 0h = Reserved 1h = Reserved 2h = PP_EXT1 is used for this PDO 3h = PP_EXT2 is used for this PDO
439-408	TX Source PDO 13	R/W	0h	EPR Sixth Sink Capabilities PDO received
407-376	TX Source PDO 12	R/W	0h	EPR Fifth Sink Capabilities PDO received
375-344	TX Source PDO 11	R/W	0h	EPR Fourth Sink Capabilities PDO received
343-312	TX Source PDO 10	R/W	0h	EPR Third Sink Capabilities PDO received
311-280	TX Source PDO 9	R/W	0h	EPR Second Sink Capabilities PDO received
279-248	TX Source PDO 8	R/W	0h	EPR First Sink Capabilities PDO received
247-216	TX Source PDO 7	R/W	0h	Seventh Source Capabilities PDO contents.
215-184	TX Source PDO 6	R/W	0h	Sixth Source Capabilities PDO contents.
183-152	TX Source PDO 5	R/W	0h	Fifth Source Capabilities PDO contents.
151-120	TX Source PDO 4	R/W	0h	Fourth Source Capabilities PDO contents.
119-88	TX Source PDO 3	R/W	0h	Third Source Capabilities PDO contents.
87-56	TX Source PDO 2	R/W	0h	Second Source Capabilities PDO contents.
55-24	TX Source PDO 1	R/W	0h	First Source Capabilities PDO contents.
23-22	RESERVED	R/W	0h	Reserved
21-20	Power Path for PDO 7	R/W	0h	Configures which PP to use for PDO7. Same format as PowerPathForPDO2.
19-18	Power Path for PDO 6	R/W	0h	Configures which PP to use for PDO6. Same format as PowerPathForPDO2.
17-16	Power Path for PDO 5	R/W	0h	Configures which PP to use for PDO5. Same format as PowerPathForPDO2.
15-14	Power Path for PDO 4	R/W	0h	Configures which PP to use for PDO4. Same format as PowerPathForPDO2.
13-12	Power Path for PDO 3	R/W	0h	Configures which PP to use for PDO3. Same format as PowerPathForPDO2.
11-10	Power Path for PDO 2	R/W	0h	Configures which PP to use for PDO2. 0h = Reserved 1h = Reserved 2h = PP_EXT1 is used for this PDO 3h = PP_EXT2 is used for this PDO
9-8	Power Path for PDO 1	R/W	0h	Configures which PP to use for PDO1. 0h = PP_5V1 is used for this PDO 1h = PP_5V2 is used for this PDO 2h = PP_EXT1 is used for this PDO 3h = PP_EXT2 is used for this PDO
7-6	RESERVED	R/W	0h	Reserved
5-3	TX Source Num Valid EPR PDOs	R/W	0h	

Table 3-39. Transmit Source Capabilities Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	Number Valid PDOs	R/W	0h	Number of valid PDOs in this register. Each PDO is 4 bytes. (max of 7)

3.38 Transmit Sink Capabilities Register (Offset = 33h) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000AF271360B939D02h]

Transmit Sink Capabilities is shown in Table 3-40.

Return to the Summary Table.

Sink Capabilities for sending. This register stores PDOs for outgoing Sink Capabilities USB PD messages. Initialized by Application Customization. The PD controller transmits the contents of this register as a Sink_Capabilities message after receiving a Get_Sink_Cap message unless its configuration or USB PD rules require a different response in the context. Writes to this register have no immediate effect. The PD controller updates and uses this register each time it needs to send a Sink Capabilities message.Each PDO in this TX_SINK_CAPS register follows the definition from the USB PD specification. For more details on the meaning of each field refer to the USB PD specification.

Table 3-40. Transmit Sink Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
423-392	TX Sink PDO 13	R/W	0h	EPR Sixth Sink Capabilities PDO received
391-360	TX Sink PDO 12	R/W	0h	EPR Fifth Sink Capabilities PDO received
359-328	TX Sink PDO 11	R/W	0h	EPR Fourth Sink Capabilities PDO received
327-296	TX Sink PDO 10	R/W	0h	EPR Third Sink Capabilities PDO received
295-264	TX Sink PDO 9	R/W	0h	EPR Second Sink Capabilities PDO received
263-232	TX Sink PDO 8	R/W	0h	EPR First Sink Capabilities PDO received
231-200	TX Sink PDO 7	R/W	0h	Seventh Sink Capabilities PDO contents.
199-168	TX Sink PDO 6	R/W	0h	Sixth Sink Capabilities PDO contents.
167-136	TX Sink PDO 5	R/W	0h	Fifth Sink Capabilities PDO contents.
135-104	TX Sink PDO 4	R/W	0h	Fourth Sink Capabilities PDO contents.
103-72	TX Sink PDO 3	R/W	0h	Third Sink Capabilities PDO contents.
71-40	TX Sink PDO 2	R/W	000AF271h	Second Sink Capabilities PDO contents.
39-8	TX Sink PDO 1	R/W	360B939Dh	First Sink Capabilities PDO contents.
7-6	RESERVED	R/W	0h	Reserved
5-3	TX Sink Num Valid EPR PDOs	R/W	0h	
2-0	Number Valid PDOs	R/W	2h	

3.39 Active PDO Contract Register (Offset = 34h) [Reset = 000000000000h]

Active PDO Contract is shown in Table 3-41.

Return to the Summary Table.

Power data object for active contract. This register stores PDO data for the current explicit USB PD contract, or all zeroes if no contract.

Table 3-41. Active PDO Contract Register Field Descriptions

Bit	Field	Type	Reset	Description
47-42	RESERVED	R	0h	Reserved
41-32	First PDO Control Bits	R	0h	Contains bits 29:20 of the first PDO. It does not matter which PDO was selected, this field is always drawn from the first PDO.
31-0	Active PDO	R	0h	Power data object. This field contains the contents of the PDO Requested by PD Controller as Sink and Accepted by Source, once it is Accepted by Source.

3.40 Active RDO Contract Register (Offset = 35h) [Reset = 000000000000000000000000h]

Active RDO Contract is shown in Table 3-42.

Return to the Summary Table.

Power data object for the active contract. This register stores the RDO of the current explicit USB PD contract, or all zeroes if no contract.

Table 3-42. Active RDO Contract Register Field Descriptions

Bit	Field	Type	Reset	Description
95-64	Sink EPR Mode DO	R	0h	
63-32	Source EPR Mode DO	R	0h	
31-28	Object Position	R	0h	As defined by USB PD.
27	Give Back Flag	R	0h	As defined by USB PD.
26	Capability Missmatch	R	0h	As defined by USB PD.
25	USB Communication Capable	R	0h	As defined by USB PD.
24	No USB Suspend	R	0h	As defined by USB PD.
23	Unchunked Supported	R	0h	As defined by USB PD.
22	EPR Mode Capable	R	0h	As defined by USB PD.
21-20	RESERVED	R	0h	Reserved
19-10	Operating Current	R	0h	As defined by USB PD.
9-0	Max Min Operation Current	R	0h	As defined by USB PD.

3.41 Autonegotiate Sink Register (Offset = 37h) [Reset = 0000000000000000000000000000000000000191904114503Eh]

Autonegotiate Sink is shown in Table 3-43.

Return to the Summary Table.

Configuration for sink power negotiations. This register defines the voltage range between which the system can function properly, allowing the PD Controller to negotiate its own contracts. Initialized by Application Customization.

Table 3-43. Autonegotiate Sink Register Field Descriptions

Bit	Field	Type	Reset	Description
191-181	RESERVED	R/W	0h	Reserved
180-169	EPR AVS Output Voltage	R/W	0h	This is the desired output voltage in 25mV units. This is inserted as-is into the Request USB PD message. Note that some PD controllers are unable to turn on the gate-drivers if VBUS less than 3.8V, check the VBUS UVLO value in the data-sheet.
168-167	RESERVED	R/W	0h	Reserved
166-160	EPR AVS Operating Current	R/W	0h	Operation current in Sink PPS mode. This is the desired operating current in 50 mA units. This is inserted as-is into the Request USB PD message.
159-129	RESERVED	R/W	0h	Reserved
128	EPR AVS Enable Sink Mode	R/W	0h	Enable Sink EPR AVS mode. If this bit is asserted, then the PD controller will attempt to negotiate a EPR AVS sink contract.
127-116	RESERVED	R/W	0h	Reserved
115-105	PPS Output Voltage	R/W	0h	This is the desired output voltage in 20mV units. This is inserted as-is into the Request USB PD message. Note that some PD controllers are unable to turn on the gate-drivers if VBUS less than 3.8V, check the VBUS UVLO value in the data-sheet.
104-103	RESERVED	R/W	0h	Reserved
102-96	PPS Operating Current	R/W	0h	Operation current in Sink PPS mode. This is the desired operating current in 50 mA units. This is inserted as-is into the Request USB PD message.
95-70	RESERVED	R/W	0h	Reserved
69	PPS Disable Sink Upon Non APDO Contract	R/W	0h	Sink path handling during supply type transition. If this bit is asserted and the selected supply type is NOT a PPS APDO, then the sink path is disabled before sending the Request message. The host should only assert this bit after a PPS contract has been negotiated. This bit has no effect unless PPSEnableSinkMode is asserted.
68	PPS Required Full Voltage Range	R/W	0h	Select only a source with full voltage range. If this bit is asserted, a PPS supply type is not selected unless the APDO.MinVoltage ≤ TX_SINK_CAPS.MinPpsVoltage, APDO.MaxVoltage ≥ TX_SINK_CAPS.MaxPpsVoltage, and APDO.MaxCurrent ≥ TX_SINK_CAPS.MaxPpsCurrent. This bit has no effect unless PPSEnableSinkMode is asserted.
67	PPS Source Operating Mode	R/W	0h	Selection for CV or CC mode. If this bit is set to 1, then the PD controller assumes the system is in constant voltage mode and sets the VBUS disconnect threshold accordingly. If this bit is set to 0, then the PD controller will assume the system is in current limit mode and it will lower the VBUS disconnect threshold accordingly.
66-65	PPS Request Interval	R/W	0h	Sink PPS request interval. This field sets the frequency at which the PD controller will send a new request to the source even if the host has not made any change in the request. 0h = 8 seconds 1h = 4 seconds 2h = 2 seconds 3h = 1 second

Table 3-43. Autonegotiate Sink Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
64	PPS Enable Sink Mode	R/W	0h	Enable Sink PPS mode. If this bit is asserted, then the PD controller will attempt to negotiate a PPS sink contract. PPS contracts are prioritized over any other supply type.
63-62	RESERVED	R/W	0h	Reserved
61-52	Auto Neg Capabilities Mismatch Power	R/W	0h	Capabilities Mismatch Power Threshold. If the selected PDO offers less power than what is specified in this register, then the PD controller will assert the Capability Mismatch bit in its Request message unless NoCapabilityMismatch is set to 1. (250mW per LSB)
51-42	Auto Neg Min Voltage	R/W	64h	MInimum voltage to request. During PD power contract negotiation, the PD controller will only select voltages that are greater than or equal to the value specified in this field. Not used unless AutoComputeSinkMinVoltage=0. (50mV per LSB)
41-32	Auto Neg Max Voltage	R/W	190h	Maximum voltage to request. During PD power contract negotiation, the PD controller will only select voltages that are less than or equal to the value specified in this field. Not used unless AutoComputeSinkMinVoltage=0. (50mV per LSB)
31-22	Auto Neg Sink Min Required Power	R/W	104h	Minimum operating power required by the Sink. The PD Controller will always attempt to receive this power level from the Source. (250mW per LSB) See description in AutoComputeSinkMinPower field
21-12	Auto Neg Max Current	R/W	145h	Maximum current to request. The PD controller will not request more current than indicated by this field. The host should ensure that the max current for all PDO's in the TX_SINK_CAPS register do not exceed this value. (10mA per LSB).
11-8	RESERVED	R/W	0h	Reserved
7	Auto Disable Input for Sink Standby	R/W	0h	Disable the sinking path during contract negotiation, and enable it back after receiving PS-RDY from SRC
6	Auto Disable Sink Upon Capability Mismatch	R/W	0h	Sink path and capability mismatch settings. If this bit is asserted, then any time the implicit or explicit power contract would cause the Capability Mismatch bit to be set the PD controller will disable the sinking path. The 'SRDY' 4CC task can override and enable the sink path. However, if the contract changes after the the 'SRDY' has completed, the PD controller will disable the sink path if the contract causes a capability mismatch. This bit should only be asserted if the NoCapabilityMismatch bit is set to 0.
5	Auto Compute Sink Max Voltage	R/W	1h	Configuration for maximum voltage. The PD controller can automatically compute ANMaxVoltage, or allow the host to specify it. 0h = Provided by host 1h = Computed by PD controller
4	Auto Compute Sink Min Voltage	R/W	1h	Configuration for minimum voltage. The PD controller can automatically compute ANMinVoltage, or allow the host to specify it. 0h = Provided by host 1h = Computed by PD controller
3	No Capability Mismatch	R/W	1h	Configuration for capability mismatch in RDO. There are two conditions that will trigger a capability mismatch: • If the attached source does not offer a PDO whose power is greater or equal to the ANSinkCapMismatchPower field in this register. • PPS is enabled in this register and the attached source did not offer a PPS PDO that matches the requirements in TX_SINK_CAPS. If either condition is true, then the PD controller will assert the capability mismatch bit in its request unless this bit is asserted. 0h = Capabiltiy mismatch enabled 1h = Capability mismatch disabled. The capability misma

Table 3-43. Autonegotiate Sink Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2	Auto Compute Sink Min Power	R/W	1h	Minimum power sink requires. The minimum sink power is the largest power reported in any valid PDO in the TX_SINK_CAPS (0x33). The power for a particular PDO from the TX_SINK_CAPS follows for each supply type: • Battery Supply: OperatingPower • Variable Supply: MaxVoltage*OperatingCurrent • Fixed Supply: Voltage*OperatingCurrent. However, if the TX_SINK_CAPS register includes Battery supply type PDO(s), then ANSinkMinRequiredPower = maximum OperatingPower in a Battery supply type PDO. 0h = Provided by host 1h = Computed by PD controller
1	No USB Suspend	R/W	1h	Value used for the NoUSBSusp Flag in the RDO. This is as defined by USB PD.
0	Auto Neg RDO Priority	R/W	0h	Configuration for tie-breaker in PDO selection. The PD controller will find the set of PDO's that fulfill the voltage requirements. From that set of PDO's it will pick the one with higher power. If two acceptable PDO's have the same power, Fixed Supply Type is preferred, and then Variable Supply has second preference. If two PDO's have the same power and the same type, then this bit determines which PDO is selected. 0h = Higher voltage 1h = Lower voltage

3.42 SPM Client Control Register (Offset = 3Ch) [Reset = 0036010001000Ah]

SPM Client Control is shown in Table 3-44.

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Source Policy Manager Client Control register used to allocate power to the port. All PDO voltages are exposed, current for each PDO is adjusted to stay within the allocated power.

Table 3-44. SPM Client Control Register Field Descriptions

Bit	Field	Type	Reset	Description
55-40	SPM Forced Safe State Power	R/W	36h	SPM Force Safe State Power is used to force the port a abolute minimum power. This is triggered by the GPIO DMC_FORCE_SAFE_STATE_EVENT (25 mW per LSB)
39-33	RESERVED	R/W	0h	Reserved
32	Port Disabled By SPM	R/W	1h	SPM Port Disable. Must be cleared to re-enable the port.
31-16	SPM Guaranteed Power	R/W	1h	Guaranteed Power for the port and is recommended to leave this constant and modify only the SPM Allocated Extra Power field. (25 mW per LSB)
15-0	SPM Allocated Extra Power	R/W	Ah	The total power allocated to the port is the SPM Allocated Extra Power + SPM Guaranteed Power. The SPM Allocated Extra Power is modified according to the power capabilities in the system. (25 mW per LSB)

3.43 SPM Client Status Register (Offset = 3Dh) [Reset = 00010001000Ah]

SPM Client Status is shown in Table 3-45.

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Source Policy Manager Client Status register used to indicate power at the port.

Table 3-45. SPM Client Status Register Field Descriptions

Bit	Field	Type	Reset	Description
47-33	RESERVED	R/W	0h	Reserved
32	SPM Cap Mismatch	R/W	1h	Capabilities Mismatch bit is set on the PDO request message. Cleared when no Capabilities Mismatch or disconnected.
31-16	SPM Requested Total VBUS Power	R/W	1h	Only valid with SPM Cap Mismatch is set. Indicates how much power the sink needs and is cleared upon a disconnect (25 mW per LSB)
15-0	SPM Totat Vbus Power Used	R/W	Ah	The total power used at the port and is based on the negotiated PD Contract. (25 mW per LSB)

3.44 Power Status Register (Offset = 3Fh) [Reset = 0000h]

Power Status is shown in Table 3-46.

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Details about the power of the connection. This register reports status regarding the power of the connection.

Table 3-46. Power Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15-4	RESERVED	R	0h	Reserved
3-2	TypeC Current	R	0h	This field is redundant with PD_STATUS.CCPullUp in register 0x40 when SourceSink is 1b. This field is redundant with PORT_CONTROL.TypeCCurrent in register 0x29 when SourceSink is 0b. In the future, this redundant field may be removed. This field is intended for Type-C Sink operation. If the port is connected as source, the field is updated upon initial connection only. 0h = USB Default Current 1h = 1.5 A 2h = 3.0 A 3h = Explicit PD contract sets current
1	SourceSink	R	0h	Source / Sink indicator. This bit is equivalent to PresentPDRole in register 0x40. It is replicated in this register for convenience. In the future, this redundant bit may be removed. 0h = Connection requests power 1h = Connection provides power (PD Controller as sink)
0	Power Connection	R	0h	Asserted if there is a connection. This bit is asserted when PlugPresent is TRUE and ConnState is greater than 5h. So it is redundant with information from register 0x1A. It is replicated in this register for convenience. In the future this redundant bit may be removed. 0h = No connection 1h = Connection present

3.45 PD Status Register (Offset = 40h) [Reset = 00000000h]

PD Status is shown in Table 3-47.

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Status of PD and Type-C state-machine. This register contains details regarding the status of PD messages and the Type-C state machine.

Table 3-47. PD Status Register Field Descriptions

Bit	Field	Type	Reset	Description
31	RESERVED	R	0h	Reserved
30-28	Data Reset Details	R	0h	Reason for Data Reset. 0h = Reset value: no data reset 0x1=Data Reset message received from port partner 2h = Requested by host: 'DRST'. 3h = Requested by host: DATA_CONTROL 0x4=Exit USB4 following DR_Swap 0x5=Reserved1 0x6=Reserved2 0x7=Reserved3
27-22	Error Recovery Details	R	0h	Reason for Error Recovery 0h = reset value: no error recovery 1h = System: over-temperature shut-down 2h = System: PP5V went low unexpectedly 3h = System: fault input GPIO was asserted 4h = System: Over-voltage detected on the Px_VBUS pin 0x5=Reserved 6h = System: ILIM on PP_5V 7h = System: ILIM on PP_CABLE 8h = System: OVP on CC detected 0x9=Back to Normal System Power State 10h = Protocol error: invalid DR_Swap 0x11=no Good_CRC during a PR_Swap sequence. 0x12=no Good_CRC during a FR_Swap sequence. 0x15=NoResponse timer timed out 0x16=PSSourceOffTimer timed out during PR_Swap 0x17=PSSourceOnTimer timed out during PR_Swap 0x18=PSSourceOnTimer timed out during FR_Swap 0x19=The Type-C source failed to change during FR_Swap 0x1a=SenderResponseTimer timed out during FR_Swap 0x1b=PSSourceOffTimer timed out during FR_Swap 1Ch = Policy Engine: Error reaching the Attached 20h = HI: PortConfig 21h = HI: Error with DATA_CONTROL 22h = HI: Swapping error during dead-battery 0x23=Host updated the GLOBAL_SYSTEM_CONFIG 24h = HI: Host issued the 4CC 'GAID' command 25h = HI: Host issued the 4CC 'Gaid' command 26h = HI: Host issued the 4CC 'DISC' command 0x27=Host issued a reset using the 'UCSI' 30h = Type-C: an error occurred in the Attached 31h = Type-C: VCONN failed to discharge 0x32=System Power State 0x33=Host Data Control USB disable 0x34=SPM Client Port disable changed 0x35=GPIO event TypeC disable 0x36=CC OVP 0x37=SBU_OVP 0x38=SBU_RX_OVP

Table 3-47. PD Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
21-16	Hard Reset Details	R	0h	Reason for Hard Reset 0h = Reset value no hard reset 1h = Received from Port Partner 2h = Requested by host 3h = Invalid DR_Swap request during Active Mode 4h = DischargeFailed. 5h = NoResponseTimeOut. 6h = SendSoftReset. 7h = Sink_SelectCapability. 8h = Sink_TransitionSink. 9h = Sink_WaitForCapabilities. Ah = SoftReset. Bh = SourceOnTimeout. Ch = Source_CapabilityResponse. Dh = Source_SendCapabilities. Eh = SourcingFault. Fh = UnableToSource. 10h = FRS failure 11h = Unexpected message 12h = Failure to to complete the VCONN recovery sequence within 200ms after PP5V rising edge
15-13	RESERVED	R	0h	Reserved
12-8	Soft Reset Details	R	0h	Reason for Soft Reset 0h = Reset value no soft reset 1h = Soft reset received from Port Partner 2h = Reserved 3h = Reserved 4h = Received source capabilities message was invalid 5h = Message retries were exhausted 6h = Received an accept message unexpectedly 7h = Received a control message unexpectedly 8h = Received a GetSinkCap message unexpectedly 9h = Received a GetSourceCap message unexpectedly Ah = Received a GotoMin message unexpectedly Bh = Received a PS_RDY message unexpectedly Ch = Received a Ping message unexpectedly Dh = Received a Reject message unexpectedly Eh = Received a Request message unexpectedly Fh = Received a Sink Capabilities message unexpectedly 10h = Received Source Capabilities message unexpected 11h = Received a Swap message unexpectedly 12h = Received a Wait Capabilities message unexpectedly 13h = Received an unknown control message 14h = Received an unknown data message 15h = To initialize SOP' controller in plug 16h = To initialize SOP'' controller in plug 17h = Received an Extended message unexpectedly 18h = Received an unknown Extended message 19h = Received a data message unexpectedly 1Ah = Received a Not Supported message unexpectedly 1Bh = Received a Get_Status message unexpectedly
7	RESERVED	R	0h	Reserved
6	Present PD Role	R	0h	Present PD power role. The PD Controller is acting under this PD power role. 0h = Sink 1h = Source
5-4	Port Type	R	0h	Present Type-C power role. The PD Controller is acting under this Type-C power role. 0h = Sink/Source 1h = Sink 2h = Source 3h = Source/Sink

Table 3-47. PD Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
3-2	CC Pullup	R	0h	CC Pull-up value. The pull-up value detected by PD Controller when in CC Pull-down mode. 0h = Not in CC pull-down mode / no CC pull-up detected 1h = USB Default current 2h = 1.5 A (SinkTxNG) 3h = 3.0 A (SinkTxOK)
1-0	RESERVED	R	0h	Reserved

3.46 PD3 Status Register (Offset = 41h) [Reset = 0000000000000000h]

PD3 Status is shown in Table 3-48.

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Status bit field for PD3.0 messages and state machine.

Table 3-48. PD3 Status Register Field Descriptions

Bit	Field	Type	Reset	Description
63-60	Revision Major	R	0h	Revision Major
59-56	Revision Minor	R	0h	Revision Minor
55-52	Version Major	R	0h	Version Major
51-48	Version Minor	R	0h	Version Minor
47-32	RESERVED	R	0h	
31	Use Unchunked Messages	R	0h	Unchunking support (SOP). Indicates if Port Partner supports unchunked messages.
30-29	Plug Negotiated Spec Revision	R	0h	USB PD specification revision (SOP'). As negotiated with Cable Plug. 0h = Revision 1 1h = Revision 2 2h = Revision 3 3h = Reserved
28-27	Port Negotiated Spec Revision	R	0h	USB PD specification revision (SOP). As negotiated with Port Partner. 0h = Revision 1 1h = Revision 2 2h = Revision 3 3h = Reserved
26-25	Plug Negotiated VDM Version	R	0h	SVDM specification version (SOP'). As negotiated with Cable Plug. 0h = Version 1 1h = Version 2 2h = Version 3 3h = Reserved
24-23	Port Negotiated VDM Version	R	0h	SVDM specification version (SOP). As negotiated with Port Partner. 0h = Version 1 1h = Version 2 2h = Version 3 3h = Reserved
22-21	Plug Negotiated VDM Version Minor	R	0h	SVDM specification minor version (SOP'). As negotiated with Cable Plug. 0h = Version 2.0 1h = Version 2.1 2h = Reserved1 3h = Reserved2
20-19	Port Negotiated VDM Version Minor	R	0h	SVDM specification minor version (SOP). As negotiated with Port Partner. 0h = Version 2.0 1h = Version 2.1 2h = Reserved1 3h = Reserved2
18-14	RESERVED	R	0h	Reserved
13	Firmware Update Request Message dropped	R	0h	Firmware Update Request Message dropped
12	RESERVED	R	0h	Reserved
11	Firmware Update Response Message dropped	R	0h	
10	RESERVED	R	0h	Reserved
9-8	RESERVED	R	0h	Reserved

Table 3-48. PD3 Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
7	EPR Mode On	R	0h	
6	RESERVED	R	0h	Reserved
5	Firmware Update Request Message received	R	0h	Firmware Update Request Message received
4	RESERVED	R	0h	Reserved
3	RESERVED	R	0h	Reserved
2	RESERVED	R	0h	Reserved
1	RESERVED	R	0h	Reserved
0	Firmware Update Response Message Received	R	0h	Firmware Update Response Message received

3.47 PD3 Configuration Register (Offset = 42h) [Reset = 001F1F1Ah]

PD3 Configuration is shown in Table 3-49.

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PD3.0 configuration settings.

Table 3-49. PD3 Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
31-25	RESERVED	R/W	0h	Reserved
24	Override SVDM Version 2.1	R/W	0h	PD Controller defaults to SVDM v2.1 unless this bit is set or PD v2 is used
23-22	RESERVED	R/W	0h	Reserved
21	Support Vendor Defined Extended	R/W	0h	
20	Support PPS Status	R/W	1h	
19	Support Get Revision	R/W	1h	Supports Get Revision
18	Support Get Source Info	R/W	1h	Supports Get Source Info
17	Support Sink Cap Extended	R/W	1h	Support Sink Capabilities Extended message. If this bit is asserted the PD controller will respond to a Get_Sink_Capabilities_Extended message USB PD message with the contents of the TX_SKEDB register (0x7E).
16	Support Country Code Info	R/W	1h	Support Country Code and information messages. If this bit is asserted the PD controller will use the data stored during application configuration to respond to a Get_Country_Code and Get_Country_Info message. See also BINARYDATA_INDICES register (0x62).
15	RESERVED	R/W	0h	Reserved
14	Supported Firmware Upgrade Message	R/W	0h	Enable firmware upgrade message
13	RESERVED	R/W	0h	Reserved
12	Support Manufacture Info Message	R/W	1h	Support Manufacturing Info message. If this bit is asserted the PD controller will respond to a Get_Manufacturer_Info USB PD message with the contents of the TX_MIDB_SOP register (0x73).
11	Support Battery Status Message	R/W	1h	Support Battery Status message. If this bit is asserted the PD controller will respond to a Get_Battery_Status USB PD message with the contents of the TX_BSDO register (0x7B).
10	Support Battery Capabilities Message	R/W	1h	Support Battery Capability message. If this bit is asserted the PD controller will respond to a Get_Battery_Capabilities USB PD message with the contents of the TX_BCDB register (0x7D).
9	Support Status Message	R/W	1h	Enable Status message. If this bit is asserted the PD controller will respond to a Get_Status USB PD message with the contents of the TX_SDB register (0x79).
8	Support Source Extended Message	R/W	1h	Enable Source Capabilities Extended. If this bit is asserted the PD controller will respond to a Get_Source_Capabilities_Extended USB PD message with the contents of the TX_SCEDB register (0x77).
7-5	RESERVED	R/W	0h	Reserved
4	Unchunked Supported	R/W	1h	Enable unchunked support. If this bit is asserted the PD controller will support unchunked messaging (up to 260 bytes). The host is responsible to consume the unchunked message before the PD controller will be able to receive another long unchunked message.
3-2	Plug Max Spec Revision	R/W	2h	Cable Plug's highest USB PD spec revision. 0h = Reserved 1h = Revision 2 (USB PD 2.0) 2h = Revision 3 (USB PD 3.0) 3h = Reserved

Table 3-49. PD3 Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
1-0	Port Max Spec Revision	R/W	2h	Port Partner's highest USB PD spec revision. 0h = Reserved 1h = Revision 2 (USB PD 2.0) 2h = Revision 3 (USB PD 3.0) 3h = Reserved

3.48 Tx Identity Register (Offset = 47h) [Reset = 0000000000000000000000000000000000000000000000000000000000000000000000000000000000000046CD5400D5506h]

Tx Identity is shown in Table 3-50.

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Data to use for Discover Identity ACK. This data is sent in the response to Discover Identity REQ message. Initialized by Application Customization. The PD controller is not designed to transmit Product Type VDO as part of this ACK message, that is only required for Alternate Mode Adaptors (AMA), VCONN Powered Devices (VPD), and cables. Writes to this register have no immediate effect. PD Controller will update and use the contents of this register each time a Discover Identity SVDM is received before generating the Discover Identity SVDM ACK message. Depending upon the product type the three VDO's in this register starting at byte 14 (ProductTypeVdo0SOP, ProductTypeVdo1SOP, ProductTypeVdo2SOP) have different meanings as defined by the USB PD specification. See the USB PD specification for definition of DFP VDO, UFP VDO1, and UFP VDO2

Table 3-50. Tx Identity Register Field Descriptions

Bit	Field	Type	Reset	Description
391-200	RESERVED	R/W	0h	Reserved
199-168	DFP1 VDO	R/W	0h	
167-136	RESERVED	R/W	0h	Reserved
135-104	UFP1 VDO	R/W	0h	
103-88	USB Product ID	R/W	0h	Product ID. The value written for PID here is used to populate the PID in other registers as well: TX_MIDB_SOP, TX_SCEDB, and TX_SKEDB.
87-72	BCD Device	R/W	0h	This field is read-only and contains the FW version for the PD controller.
71-40	Certification Test ID	R/W	46Ch	This contains the 32-bit XID assigned by USB-IF. The value written for XID here is used to populate the XID in other registers as well: TX_SCEDB, and TX_SKEDB.
39	USB Communication Capable as Host	R/W	1h	Assert if USB communications capable as a host.
38	USB Communication Capable as Device	R/W	1h	Assert if USB communications capable as a device.
37-35	Product Type UFP	R/W	2h	This is as defined in the USB PD specification. bits 15:0 are the VID. The value written for VID here is used to populate the VID in other registers as well: TX_MIDB_SOP, TX_SCEDB, and TX_SKEDB.
34	Modal Operation Supported	R/W	1h	Assert this bit if Alternate Modes are supported.
33-31	Product Type DFP	R/W	2h	This is as defined in the USB PD specification.
30-29	RESERVED	R/W	0h	Reserved
28-24	RESERVED	R/W	0h	Reserved
23-8	Vendor ID	R/W	D55h	This is as defined in the USB PD specification. The value written for VID here is used to populate the VID in other registers as well: TX_MIDB_SOP, TX_SCEDB, and TX_SKEDB.
7-3	RESERVED	R/W	0h	Reserved

Table 3-50. Tx Identity Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
2-0	Number Valid VDOs	R/W	6h	Number of valid VDO's in this register. This field causes special behavior: • When 0, the PD Controller will NAK USB PD Discover Identity message. • When 1, the PD Controller will respond with BUSY message. • When 2, the PD Controller will respond with Not_Supported (PD3) or no response (PD2). • When 3, 4, 5, or 6 the PD Controller will respond with an ACK message. • The value 7 is reserved. (Max of 6)

3.49 Received SOP Identity Data Object Register (Offset = 48h) [Reset = 00000000000000000000000000000000000000000000000000000000h]

Received SOP Identity Data Object is shown in Table 3-51.

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Received Discover Identity ACK (SOP). Latest Discover Identity response received over USB PD using SOP.

Table 3-51. Received SOP Identity Data Object Register Field Descriptions

Bit	Field	Type	Reset	Description
199-168	RX ID SOP VDO 6	R	0h	6th VDO. The sixth Data Object for Discover Identity response is context-specific.
167-136	RX ID SOP VDO 5	R	0h	5th VDO. The fifth Data Object for Discover Identity response is context-specific.
135-104	RX ID SOP VDO 4	R	0h	4th VDO. The fourth Data Object for Discover Identity response is context-specific as defined in USB PD.
103-72	RX ID SOP VDO 3	R	0h	Product VDO. The third Data Object for Discover Identity response.
71-40	RX ID SOP VDO 2	R	0h	Cert Stat VDO. The second Data Object for Discover Identity response.
39-8	RX ID SOP VDO 1	R	0h	ID Header VDO. The first Data Object in Discover Identity response.
7-6	Response Type	R	0h	Type of response received. 0h = SOP Discover Identity REQ not sent or pending 1h = Responder ACK received 2h = Responder NAK received or response timeout 3h = Responder BUSY received
5-3	RESERVED	R	0h	Reserved
2-0	Number Valid VDOs	R	0h	Number of valid VDO's in this register. (Max of 6)

3.50 Received SOP Prime Identity Data Object Register (Offset = 49h) [Reset = 00000000000000000000000000000000000000000000000000000000h]

Received SOP Prime Identity Data Object is shown in Table 3-52.

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Received Discover Identity ACK (SOP' or SOP''). Latest Discover Identity response received over USB PD using SOP'.

Table 3-52. Received SOP Prime Identity Data Object Register Field Descriptions

Bit	Field	Type	Reset	Description
199-168	RX ID SOPPrime VDO 6	R	0h	6th VDO. The sixth Data Object for Discover Identity response is context-specific.
167-136	RX ID SOPPrime VDO 5	R	0h	5th VDO. The fifth Data Object for Discover Identity response is context-specific.
135-104	RX ID SOPPrime VDO 4	R	0h	4th VDO. The fourth Data Object for Discover Identity response is context-specific as defined in USB PD.
103-72	RX ID SOPPrime VDO 3	R	0h	Product VDO. The third Data Object for Discover Identity response.
71-40	RX ID SOPPrime VDO 2	R	0h	Cert Stat VDO. The second Data Object for Discover Identity response.
39-8	RX ID SOPPrime VDO 1	R	0h	ID Header VDO. The first Data Object in Discover Identity response.
7-6	Response Type	R	0h	Type of response received. 0h = SOP' Discover Identity REQ not sent or pending 1h = Responder ACK received 2h = Responder NAK received or response timeout 3h = Responder BUSY received
5-3	RESERVED	R	0h	Reserved
2-0	Number Valid VDOs	R	0h	Number of valid VDO's in this register. (Max of 6)

3.51 User Alternate Mode Configuration Register (Offset = 4Ah) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000100000000h]

User Alternate Mode Configuration is shown in Table 3-53.

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User VID Configuration. Initialized by Application Customization. This register is sampled each time the PD controller needs the information. For example, each time the PD controller implements the discovery process it checks the contents of this register and carries out the discovery process accordingly.

Table 3-53. User Alternate Mode Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
503-496	User Mode Auto Send VDO Count	R/W	0h	Number of VDOs in UVDM. If auto send unstructured VDM enabled, number of VDOs to send. (Max of 6)
495-494	RESERVED	R/W	0h	Reserved
493-480	User Mode Auto Send Vendor Use Data	R/W	0h	Additional data for UVDM. If auto send unstructured VDM enabled, up to an additional 14 bits may be sent as part of the Unstructured VDM header.
479-288	User Mode Auto Send VDO Data	R/W	0h	Data for UVDM. If auto send unstructured VDM enabled, up to 24 bytes may be sent.
287-256	User ALT Mode 4 Value	R/W	0h	User VID mode 4 name.
255-224	User ALT Mode 3 Value	R/W	0h	User VID mode 3 name.
223-192	User ALT Mode 2 Value	R/W	0h	User VID mode 2 name.
191-160	User ALT Mode 1 Value	R/W	0h	User VID mode 1 name.
159-153	RESERVED	R/W	0h	Reserved
152	User Mode 4 Load Config Data	R/W	0h	Load App Config upon entry to User VID mode 4. Assert this bit to load application data upon entry to User VID mode 4.
151-145	RESERVED	R/W	0h	Reserved
144	User Mode 3 Load Config Data	R/W	0h	Load App Config upon entry to User VID mode 3. Assert this bit to load application data upon entry to User VID mode 3.
143-137	RESERVED	R/W	0h	Reserved
136	User Mode 2 Load Config Data	R/W	0h	Load App Config upon entry to User VID mode 2. Assert this bit to load application data upon entry to User VID mode 2.
135-129	RESERVED	R/W	0h	Reserved
128	User Mode 1 Load Config Data	R/W	0h	Load App Config upon entry to User VID mode 1. Assert this bit to load application data upon entry to User VID mode 1.
127-121	RESERVED	R/W	0h	Reserved
120	User Mode 4 Auto Send Unstruct VDM	R/W	0h	Enable auto-sending of UVDM for User VID mode 4.
119-113	RESERVED	R/W	0h	Reserved
112	User Mode 3 Auto Send Unstruct VDM	R/W	0h	Enable auto-sending of UVDM for User VID mode 3.
111-105	RESERVED	R/W	0h	Reserved
104	User Mode 2 Auto Send Unstruct VDM	R/W	0h	Enable auto-sending of UVDM for User VID mode 2.
103-97	RESERVED	R/W	0h	Reserved
96	User Mode 1 Auto Send Unstruct VDM	R/W	0h	Enable auto-sending of UVDM for User VID mode 1.
95-89	RESERVED	R/W	0h	Reserved
88	User Mode 4 Auto Entry Allowed	R/W	0h	Enable auto-entry for User VID mode 4.
87-81	RESERVED	R/W	0h	Reserved

Table 3-53. User Alternate Mode Configuration Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
80	User Mode 3 Auto Entry Allowed	R/W	0h	Enable auto-entry for User VID mode 3.
79-73	RESERVED	R/W	0h	Reserved
72	User Mode 2 Auto Entry Allowed	R/W	0h	Enable auto-entry for User VID mode 2.
71-65	RESERVED	R/W	0h	Reserved
64	User Mode 1 Auto Entry Allowed	R/W	0h	Enable auto-entry for User VID mode 1.
63-57	RESERVED	R/W	0h	Reserved
56	User Mode 4 Enabled	R/W	0h	Assert this bit to enable User VID mode 4.
55-49	RESERVED	R/W	0h	Reserved
48	User Mode 3 Enabled	R/W	0h	Assert this bit to enable User VID mode 3.
47-41	RESERVED	R/W	0h	Reserved
40	User Mode 2 Enabled	R/W	0h	Assert this bit to enable User VID mode 2.
39-33	RESERVED	R/W	0h	Reserved
32	User Mode 1 Enabled	R/W	1h	Assert this bit to enable User VID mode 1.
31-16	User ALT Mode SVID Value	R/W	0h	User VID
15-2	RESERVED	R/W	0h	Reserved
1	RESERVED	R/W	0h	Reserved
0	USVID Enabled	R/W	0h	Assert this bit to enable User VID.

3.52 Received Attention VDM Register (Offset = 4Eh) [Reset = 0000000000000000h]

Received Attention VDM is shown in Table 3-54.

Return to the Summary Table.

Received Attention message. Latest Structured VDM Attention Initiator message received over USB PD. The PD controller does not queue received Attention messages. This register contains the most recently received message. NOTE: Only Structured VDM "Attention" messages get stored in this buffer. See RX_OTHER_VDM register 0x4F for all other inbound VDMs.

Table 3-54. Received Attention VDM Register Field Descriptions

Bit	Field	Type	Reset	Description
71-40	RX VDMs 2	R	0h	Second data object. The vendor defined object (VDO) received with the Attention message (if any).
39-8	RX VDMs 1	R	0h	Structured VDM header. This contains the first Data Object of most recently received Attention SVDM.
7-5	Sequence Number	R	0h	Sequence number. This field increments by one every time this register is updated, rolls over upon reflow
4-3	RESERVED	R	0h	Reserved
2-0	Number Valid VDOs	R	0h	Number of valid data objects in this register.

3.53 Received Other VDM Register (Offset = 4Fh) [Reset = 00000000000000000000000000000000000000000000000000000000h]

Received Other VDM is shown in Table 3-55.

Return to the Summary Table.

Received VDM (not Attention). This register contains the latest VDM message received over USB PD except for Structured VDM Attention Initiator messages and SOP*_Debug messages. The PD controller does not queue received SVDM messages. This register contains the most recently received message. Structured VDM "Attention" Initiator messages are only stored in register 0x4E, not this register.

Table 3-55. Received Other VDM Register Field Descriptions

Bit	Field	Type	Reset	Description
231-200	RX VDMs 7	R	0h	Seventh Data Object of most recently received VDM.
199-168	RX VDMs 6	R	0h	Sixth Data Object of most recently received VDM.
167-136	RX VDMs 5	R	0h	Fifth Data Object of most recently received VDM.
135-104	RX VDMs 4	R	0h	Fourth Data Object of most recently received VDM.
103-72	RX VDMs 3	R	0h	Third Data Object of most recently received VDM.
71-40	RX VDMs 2	R	0h	Second Data Object of most recently received VDM.
39-8	RX VDMs 1	R	0h	First Data Object of most recently received VDM.
7-5	Sequence Number	R	0h	
4-3	SOP Type	R	0h	
2-0	Number Valid VDOs	R	0h	

3.54 Data Control Register (Offset = 50h) [Reset = 000000000000h]

Data Control is shown in Table 3-56.

Return to the Summary Table.

Data provided by the Thunderbolt Controller. This register provides shortcuts that set other bits in other registers, for convenience of the Thunderbolt Controller or other host. It also holds data that the TBT controller wants to write to the Debug Mode Register of the Retimer through the PD controller. The TBT Controller initiates the PD controller's write to the Debug Mode Register of the Retimer using the DATA_CONTROL Register as well. In systems with an EC a second host (eg. TBT controller or SoC) that requires access to this register, the EC should not write to this register since it may cause a conflict with the other host.

Table 3-56. Data Control Register Field Descriptions

Bit	Field	Type	Reset	Description
47	Trace Mode	R/W	0h	
46	Enable	R/W	0h	
45-44	Debug Mode Type	R/W	0h	
43	RESERVED	R/W	0h	Reserved
42-40	Additional Skew	R/W	0h	
39-38	Lane Count	R/W	0h	
37-36	Freq	R/W	0h	
35-34	EMPHASISDB	R/W	0h	
33-32	AMPDB	R/W	0h	
31	Debug RX Locked	R/W	0h	
30-24	RESERVED	R/W	0h	Reserved
23-22	TPS Type	R/W	0h	
21-20	Requested Window Size	R/W	0h	
19-18	EMPHASISICL	R/W	0h	
17-16	AMPICL	R/W	0h	
15-14	RESERVED	R/W	0h	Reserved
13	IRQ ACK	R/W	0h	Writing this bit as 1 will clear DATA_STATUS.HpdIrqSticky after a delay.
12	Write to Retimer	R/W	0h	If asserted the PD controller will write bytes 3-6 to to Retimer on I2C3m.
11-8	RESERVED	R/W	0h	Reserved
7	Power Reset	R/W	0h	If asserted the PD controller will initiate Error Recovery on the connector.
6	Data Reset	R/W	0h	If asserted the PD controller will initiate Data Reset process.
5-3	RESERVED	R/W	0h	Reserved
2	Interrupt ACK	R/W	0h	When set, causes INT_MASK2 value to be written to INT_CLEAR2 (clearing all interrupt events).
1	Soft Reset	R/W	0h	When set, causes a soft-reset of PD Controller. Equivalent to Gaid 4CC.
0	Thunderbolt Host Connected	R/W	0h	Assert this bit when a TBT host is connected. The TBT controller may also assert this bit to 1 then 0 to force a port disconnect/ reconnect.

3.55 Display Port Configuration Register (Offset = 51h) [Reset = 0100001C0603h]

Display Port Configuration is shown in Table 3-57.

Return to the Summary Table.

DisplayPort Alternate Mode configuration. Initialized by Application Customization. This register is sampled each time the PD controller needs the information. For example, each time the PD controller implements the discovery process it checks the contents of this register and carries out the discovery process accordingly.

Table 3-57. Display Port Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
47-41	RESERVED	R/W	0h	Reserved
40	DP Mode Auto Entry Allowed	R/W	1h	Assert this bit to enable auto-entry.
39	RESERVED	R/W	0h	Reserved
38-37	DP VDO Version	R/W	0h	0h = DP v2.0 1h = DP v2.1
36-35	DFPD_UFPD Connected	R/W	0h	This field indicates the status of the connection. 0h = Neither UFP_D nor DFP_D is connected 1h = DFP_D is connected 2h = UFP_D is connected 3h = Both UFP_D and DFP_D is connected
34-33	RESERVED	R/W	0h	Reserved
32	Multi Function Preferred	R/W	0h	Assert this bit if multi-function is preferred.
31-24	UFPD Pin Assignment	R/W	0h	UFP_D Pin Assignments Supported. Each bit corresponds to an allowed pin assignment. Multiple pin assignments may be allowed. 40,RESERVEDh = 0x80]
23-16	DFPD Pin Assignment	R/W	1Ch	DFP_D Pin Assignments Supported. Each bit corresponds to an allowed pin assignment. Multiple pin assignments may be allowed. 40,RESERVEDh = 0x80]
15	USB2 Signalling Not Used	R/W	0h	USB r2.0 signaling requirement on A6 - A7 or B6 - B7 (D+/D-) while in DP configuration 0h = May be required 1h = Not required
14	RESERVED	R/W	0h	Reserved
13-10	DP Transport Signalling	R/W	1h	Signaling for transport of DisplayPort protocol. 0h = USB signaling 1h = DP signaling
9-8	DP Port Capability	R/W	2h	Display port capabilities 0h = Reserved 1h = UFP_D-capable (including Branch device) 2h = DFP_D-capable (including Branch device) 3h = Reserved
7-2	RESERVED	R/W	0h	Reserved
1	DP Mode	R/W	1h	Assert this bit to enable DisplayPort Alternate mode.
0	Enable DP SID	R/W	1h	Assert this bit to enable DisplayPort SVID.

3.56 Thunderbolt Configuration Register (Offset = 52h) [Reset = 000200000000E003h]

Thunderbolt Configuration is shown in Table 3-58.

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Thunderbolt Configuration. This register also contains TBT Alternate mode configurations. Initialized by Application Customization. This register is sampled each time the PD controller needs the information. For example, each time the PD controller implements the discovery process it checks the contents of this register and carries out the discovery process accordingly.

Table 3-58. Thunderbolt Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	Source VCONN Delay	R/W	0h	Configurable delay for BR. (10ms per LSB)
55-50	RESERVED	R/W	0h	Reserved
49	Thunderbolt Auto Entry Allowed	R/W	1h	Assert this bit to enable TBT auto-entry.
48-27	RESERVED	R/W	0h	Reserved
26	VPRO Support	R/W	0h	
25-17	RESERVED	R/W	0h	Reserved
16	Legacy TBT Adapter	R/W	0h	
15	Retimer Compliance Support	R/W	1h	If this bit is set to 1b, then asserting the Retimer_SOC_OVR_Force_Power GPIO causes the PD controller to place an attached Intel Retimer into compliance mode. De-asserting the Retimer_SOC_OVR_Force_Power GPIO places the retimer into normal operation.
14	Data Status HPD Events	R/W	1h	This bit controls how HPD events are configured. 0h = HPD over GPIO 1h = Virtual HPD
13	TBT Retimer Present	R/W	1h	Enable first retimer on each port. Assert this bit when there is a TBT retimer on this port.
12	Dual TBT retimer Present	R/W	0h	Enable second retimer on each port. Assert this bit when there is a second TBT retimer on this port.
11	RESERVED	R/W	0h	Reserved
10	AN Min Power Required	R/W	0h	Power required for TBT mode entry. 0h = Power does not matter 1h = TBT not fully connected unless power is available
9	TBT Emarker Override	R/W	0h	Configuration for non-responsive Cable Plug. 0h = Assume non-TBT cable 1h = Assume TBT cable
8	RESERVED	R/W	0h	Reserved
7	PL4 Handling Enabled	R/W	0h	
6-3	I2C3 Configurable Delay	R/W	0h	Delay for the Controller I2C commands at power on. Min value is 0 sec and Max Value is 5 sec. (0.5s per LSB)
2	Advertise 900mA Implicit Contract	R/W	0h	
1	Thunderbolt Mode Enabled	R/W	1h	Assert this bit to enable TBT mode. When this bit is asserted The PD Controller as UFP will advertise Thunderbolt Mode. The PD Controller as DFP will negotiate Thunderbolt Mode.
0	Thunderbolt VID Enabled	R/W	1h	Assert this bit to enable Thunderbolt VID.

3.57 Special Configuration Register (Offset = 55h) [Reset = 00000000h]

Special Configuration is shown in Table 3-59.

Return to the Summary Table.

Table 3-59. Special Configuration Register Field Descriptions

Bit	Field	Type	Reset	Description
31-16	RESERVED	R/W	0h	Reserved
15-14	OVP OCP Error Recovery Tries	R/W	0h	Number of re-tries (error recovery) before Vbus is disabled
13-0	RESERVED	R/W	0h	Reserved

3.58 User VID Status Register (Offset = 57h) [Reset = 0000h]

User VID Status is shown in Table 3-60.

Return to the Summary Table.

User VID Status.

Table 3-60. User VID Status Register Field Descriptions

Bit	Field	Type	Reset	Description
15-13	RESERVED	R	0h	Reserved
12	Mode 4 Status	R	0h	Asserted when Mode4 has been entered.
11	Mode 3 Status	R	0h	Asserted when Mode3 has been entered.
10	Mode 2 Status	R	0h	Asserted when Mode2 has been entered.
9	Mode 1 Status	R	0h	Asserted when Mode1 has been entered.
8-5	RESERVED	R	0h	Reserved
4-2	USVID Error Code	R	0h	Error code
1	USVID Active	R	0h	Asserted when a User VID is active.
0	USVID Detected	R	0h	Asserted when a User VID has been detected.

3.59 Display Port Status Register (Offset = 58h) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000h]

Display Port Status is shown in Table 3-61.

Return to the Summary Table.

DisplayPort Alternate Mode Status.

Table 3-61. Display Port Status Register Field Descriptions

Bit	Field	Type	Reset	Description
326-304	RESERVED	R	0h	Reserved
303	DP UFP VDO Version	R	0h	DP UFP VDP Version 0h = VDO Original Version 1h = VDO Version 1
302-301	Cable Active Component	R	0h	Cable Active Component 0h = Passive 1h = Active Retimer 2h = Active Redriver 3h = Optical
300	Cable UHBR13.5 Support	R	0h	Cable UHBR13.5 Support 0h = UHBR13.5 Not Supported 1h = UHBR13.5 Supported
299-296	DP Signalling Rate	R	0h	Signaling for Cable Information Transport of DisplayPort Protocol 2,UHBR20 UHBR10 HBR3h = 0x4]
295-264	DP mode data SOPPrime	R	0h	Discover Mode ACK (SOP'). This field contains the contents of DP Discover Mode response from Cable Plug
263-232	DP Config from Plug	R	0h	Received DP config message (SOP'). This field contains the contents of DP Configure message received from Cable Plug
231-200	DP Config to Plug	R	0h	DP Config message (SOP'). This field contains the contents of DP Configure message sent to Cable Plug
199-168	DP Status ACK from Plug	R	0h	DP Status acknowledgement (SOP'). This field contains the most recently received DP Status Acknowledgment from Cable Plug
167-136	DP Status to Plug	R	0h	DP Status (SOP'). This field contains the current Outgoing DP Status message contents to Cable Plug
135-104	DP Mode Data	R	0h	DP Discover Mode response. This field contains the contents of the DP Discover Mode response when received (DFP_U).
103-72	DP Configure Message	R	0h	Contents of DP Config message when sent (DFP_U).
71-40	DP Status RX	R	0h	Most recently received DP Status message contents.
39-8	DP Status TX	R	0h	Current Outgoing DP Status message contents
7-2	RESERVED	R	0h	Reserved
1	DP Mode Active	R	0h	DP mode entered. DFP_U: This bit is asserted when PD Controller has entered DisplayPort Mode with attached UFP_U. UFP_U: Attached DFP_U has entered DisplayPort Mode. DP mode entered. This bit is asserted when PD Controller has entered DisplayPort Mode with attached UFP_U.
2-0	RESERVED	R	0h	Reserved
0	DP SID Detected	R	0h	Port Partner is Display Port capable. This bit is asserted when UFP_U returns DP SID in Discover SVIDs response or responded with ACK to DP SID SVDM Commands.

3.60 Intel VID Status Register (Offset = 59h) [Reset = 00000000000000000000h]

Intel VID Status is shown in Table 3-62.

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Intel VID Thunderbolt Alternate Mode Status.

Table 3-62. Intel VID Status Register Field Descriptions

Bit	Field	Type	Reset	Description
87-72	TBT Mode Data RX on SOPPrime	R	0h	Data for Discover Modes (SOP'). This field contains the upper 16 bits of SOP' Discover Modes Cable response for TBT Mode. Lower 16 bits of the response are always 0x0001
71-56	TBT Mode Data RX on SOP	R	0h	Data for Discover Modes response. This field contains the upper 16 bits of SOP Discover Modes response for TBT Mode when received (DFP) or sent (UFP). Lower 16 bits of the response are always 0x0001. NOTE: In the UFP role, this register simply copies the contents of the Intel VID Configuration register bits 23:8 at the time the Discover Modes response is generated.
55-40	TBT Enter Mode Data	R	0h	Data for TBT Enter mode message. This field contains the upper 16 bits of second VDO to Thunderbolt Enter Mode command when sent (DFP) or received (UFP).
39-8	TBT Attention Data	R	0h	Attention message contents. This field contains the contents of the Attention VDO in Thunderbolt Mode when sent (UFP) or received (DFP).
7-3	RESERVED	R	0h	Reserved
2	Forced TBT Mode	R	0h	Retimer in TBT state and ready for FW update. A value of 1 indicates that the PD controller has placed the retimer in the TBT state and it is ready for FW update.
1	TBT Mode Active	R	0h	
0	Intel VID Detected	R	0h	

3.61 IO Config Register (Offset = 5Ch) [Reset = 00000000000000000000000000000000000000000000000000000000000000000000000000000000000015044B4F00003191h]

IO Config is shown in Table 3-63.

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Application-specific GPIO Configurations.

Table 3-63. IO Config Register Field Descriptions

Bit	Field	Type	Reset	Description
391-384	GPIO 12 Mapped Event	R	0h	Event table mapping for GPIO12. See GPIO Event table.
383-376	GPIO 11 Mapped Event	R	0h	Event table mapping for GPIO11. See GPIO Event table.
375-368	GPIO 10 Mapped Event	R	0h	Event table mapping for GPIO10. See GPIO Event table.
367-360	GPIO 9 Mapped Event	R	0h	Event table mapping for GPIO9. See GPIO Event table.
359-352	GPIO 8 Mapped Event	R	0h	Event table mapping for GPIO8. See GPIO Event table.
351-344	GPIO 7 Mapped Event	R	0h	Event table mapping for GPIO7. See GPIO Event table.
343-336	GPIO 6 Mapped Event	R	0h	Event table mapping for GPIO6. See GPIO Event table.
335-328	GPIO 5 Mapped Event	R	0h	Event table mapping for GPIO5. See GPIO Event table.
327-320	GPIO 4 Mapped Event	R	0h	Event table mapping for GPIO4. See GPIO Event table.
319-312	GPIO 3 Mapped Event	R	0h	Event table mapping for GPIO3. See GPIO Event table.
311-304	GPIO 2 Mapped Event	R	0h	Event table mapping for GPIO2. See GPIO Event table.
303-296	GPIO 1 Mapped Event	R	0h	Event table mapping for GPIO1. See GPIO Event table.
295-288	GPIO 0 Mapped Event	R	0h	Event table mapping for GPIO0. See GPIO Event table.
287-269	RESERVED	R	0h	Reserved
268-256	GPIO Event Polarity	R	0h	Controls polarity of a selected output event for each GPIO. Assert the bit for a given GPIO to invert the polarity of the event mapped to it. This field has no impact for input GPIO Events.
255-230	RESERVED	R	0h	Reserved
229	GPIO 5 Analog Input Control	R	0h	Assert when GPIO5 is used as an analog input. This must also be asserted when PORT_CONTROL.ChargerDetectEnable or ChargerAdvertiseEnable is non-zero.
228	GPIO 4 Analog Input Control	R	0h	Assert when GPIO4 is used as an analog input. This must also be asserted when PORT_CONTROL.ChargerDetectEnable or ChargerAdvertiseEnable is non-zero.
227-205	RESERVED	R	0h	Reserved
204-192	Internal Pull Up Enable	R	0h	Controls weak pull-up setting for each configurable GPIO (1=Enabled, 0=Disabled).
191-173	RESERVED	R	0h	Reserved
172-160	Internal Pull Down Enable	R	0h	Controls weak pull-down setting for each configurable GPIO (1=Enabled, 0=Disabled).
159-140	RESERVED	R	0h	Reserved
139-128	Multiplexing for GPIO Pin	R	0h	Selects between GPIO (0) and Secondary Function (1) for each GPIO. See the subsection below for more details.
127-109	RESERVED	R	0h	Reserved
108-96	Open Drain Output Enable	R	0h	Controls push-pull (0) vs. open-drain (1) setting for each configurable GPIO.
95-77	RESERVED	R	0h	Reserved
76-64	Initial Value	R	0h	Controls default output level for each GPIO enabled as output (0=Drive Low, 1=Drive High)
63-45	RESERVED	R	0h	Reserved

Table 3-63. IO Config Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
44-32	GPIO Interrupt Enable	R	B4Fh	Controls interrupt enable for each GPIO (1=Interrupt Enabled, 0=Interrupt Disabled). Note that all GPIO pins may not be configured as inputs (see the data-sheet).
31-13	RESERVED	R	0h	Reserved
12-0	GPIO Output Enable	R	1191h	Controls output enable for each GPIO (1=Output Enabled, 0=Hi-Z). Note that all GPIO may not be configurable as an output (see data-sheet).

3.62 Data Status Register (Offset = 5Fh) [Reset = 0000000000h]

Data Status is shown in Table 3-64.

Return to the Summary Table.

Table 3-64. Data Status Register Field Descriptions

Bit	Field	Type	Reset	Description
39-32	Debug Alternate Mode ID	R	0h	NIDnT Overlay Number
31-30	RESERVED	R	0h	Reserved
29-28	TBT Cable Generation	R	0h	Thunderbolt cable generation. 0h = 3rd generation TBT (10.3125 and 20.625 Gb/s) 1h = 4th generation TBT (10.0 10.3125 20.0 and 20.625 Gb/s)
27-25	TBT Cable Support	R	0h	0h = Reserved 1h = USB3.1 gen1 cable (10Gb/s Thunderbolt support) 2h = 10Gb/s only 3h = 10Gb/s and 20Gb/s only 4h = 10Gb/s 20Gb/s and 40Gb/s only
24	RESERVED	R	0h	Reserved
23	USB4 Connection	R	0h	Asserted when USB4 mode is entered with the "Host Present" bit asserted.
22	Active Cable	R	0h	Indicates if cable is passive (0) or active (1).
21	Debug Alternate Mode	R	0h	Asserted when a debug alternate mode is entered.
20	Active Link Training	R	0h	Asserted when the cable is active with uni-directional LSRX communication.
19	VPRO Dock Detected	R	0h	Asserted when vPro dock detected.
18	Cable Type	R	0h	Indicates the type of cable: Non-Optical (0) or Optical (1)
17	TBT Type	R	0h	Indicates the type of Thunderbolt connection: Type-C to Type-C cable (0) or Legacy Adaptor (1)
16	TBT Connection	R	0h	Status of Thunderbolt connection. 0h = No Thunderbolt connection 1h = Thunderbolt connection present
15	HPD Level	R	0h	Status of HPD Level. This is the HPD level received from DisplayPort Sink to TBT controller through the PD controller. This bit is applicable only when the port is acting as a DisplayPort host in virtual HPD signalling mode.
14	HPD IRQ Sticky	R	0h	Status of HPD IRQ event received. This event is from DP Sink to TBT controller through the PD controller. This bit is applicable only when the port is acting as a DisplayPort host in virtual HPD signalling mode.
13	RESERVED	R	0h	Reserved
12	Debug Accessory Mode	R	0h	Asserted when debug accessory is present.
11-10	DP Pin Assignment	R	0h	DisplayPort Pin Assignments 0h = Legacy' DP USB-C to DP cable 1h = Legacy' DP USB-C to USB-C cable 2h = New' DP USB-C to USB-C cable 3h = Reserved
9	DP Source Sink	R	0h	The PD controller does not support DP sink. So this bit always reads back as 0b.
8	DP Connection	R	0h	Asserted when there is a DisplayPort connection.
7	Data Role	R	0h	USB data role: DFP (0) or UFP (1).
6	USB3 Speed	R	0h	USB3 data speed 0h = Limited to Gen 1 speed (5Gbps) 1h = Allowed to Gen 2 speed (10Gbps)
5	USB3 Connection	R	0h	Status of USB3 connection 0h = No USB3 connection 1h = USB3 connection

Table 3-64. Data Status Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
4	USB2 Connection	R	0h	Status of USB2 connection 0h = No USB2 connection to USB_RP 1h = USB2 connection to USB_RP on 'Mission' D+/D- pair
3	Over Current or Temperature	R	0h	Over-current or over-temperature has occurred.
2	Retimer or Redriver	R	0h	Indicates type of active element in the cable. 0h = Re-driver 1h = Re-timer
1	Connection Orientation	R	0h	Plug orientation 0h = Plug is oriented on CC1 (upside-up) 1h = Plug is oriented on CC2 (upside-down)
0	Data Connection	R	0h	Status of data connection. 0h = No data connection 1h = Data connection present

3.63 Received User SVID Attention VDM Register (Offset = 60h) [Reset = 0000000000000000h]

Received User SVID Attention VDM is shown in Table 3-65.

Return to the Summary Table.

Received Attention message for User VID. This register contains the latest Structured VDM Attention Initiator message received for User VID. Only Structured VDM messages for User SVID with Command Type = Initiator (00b) and Command = Attention (6) get stored in this buffer. See register 0x61 for all other inbound VDMs

Table 3-65. Received User SVID Attention VDM Register Field Descriptions

Bit	Field	Type	Reset	Description
71-40	RX VDM Data Object 2	R	0h	Second Data Object of most recently received Attention SVDM. This is the VDO (if present).
39-8	RX VDM Data Object 1	R	0h	VDM header. This field contains the first Data Object of most recently received Attention SVDM.
7-5	Sequence Number	R	0h	Increments by one every time this register is updated, rolls over upon reflow.
4-3	RESERVED	R	0h	Reserved
2-0	Number Valid VDOs	R	0h	Number of valid VDOs received. Each VDO is 4 bytes. The USB PD spec does not allow more than two VDO's.

3.64 Received User SVID Other VDM Register (Offset = 61h) [Reset = 00000000000000000000000000000000000000000000000000000000h]

Received User SVID Other VDM is shown in Table 3-66.

Return to the Summary Table.

Latest Unstructured VDM or a non-Attention Structured VDM received for User VID.

Table 3-66. Received User SVID Other VDM Register Field Descriptions

Bit	Field	Type	Reset	Description
231-200	RX VDM Data Object 7	R	0h	
199-168	RX VDM Data Object 6	R	0h	Sixth Data Object of most recently received VDM.
167-136	RX VDM Data Object 5	R	0h	Fifth Data Object of most recently received VDM.
135-104	RX VDM Data Object 4	R	0h	Fourth Data Object of most recently received VDM.
103-72	RX VDM Data Object 3	R	0h	Third Data Object of most recently received VDM.
71-40	RX VDM Data Object 2	R	0h	Second Data Object of most recently received VDM.
39-8	RX VDM Data Object 1	R	0h	First Data Object of most recently received VDM.
7-5	Sequence Number	R	0h	Increments by one every time this register is updated, rolls over upon reflow.
4-3	SOP Type	R	0h	Frame type of the message in this register. 0h = VDM came from SOP 1h = VDM came from SOP' 2h = VDM came from SOP" 3h = VDM came from SOP*_Debug
2-0	Number Valid VDOs	R	0h	Number of DO's received.

3.65 APP Config Binary Data Indices Register (Offset = 62h) [Reset = 0000000000000000h]

APP Config Binary Data Indices is shown in Table 3-67.

Return to the Summary Table.

This register can only be changed as part of Application Customization. It allows the PD controller to be configured to write specific commands to the I2C3m port when certain events occur. This register also allows for country code information to be customized. The Application Customization tool creates this register automatically.

Table 3-67. APP Config Binary Data Indices Register Field Descriptions

Bit	Field	Type	Reset	Description
63-56	Number of I2C Port 2 Events	R	0h	Number of I2C Events port 2. (Max of 99)
55-48	I2C Event Start Index Port 2	R	0h	Start index of I2C Events for Port 2. This is an offset into the Application customization binary buffer. (Max of 99)
47-40	Number of I2C Port 1 Events	R	0h	Number of I2C Events port 1. (Max of 99)
39-32	I2C Event Start Index Port 1	R	0h	Start index of I2C Events for Port 1. This is an offset into the Application customization binary buffer. (Max of 99)
31-24	Number of I2C Common Events	R	0h	Number of I2C Events for both ports. (Max of 99)
23-16	I2C Event Start Index Common	R	0h	Start index of I2C Events for both ports. This is an offset into the Application customization binary buffer.
15-8	Number of Country Codes	R	0h	Number of Country Codes supported. (Max of 12)
7-0	Country Code Start Index	R	0h	Start index of the Country Codes. This is an offset into the Application customization binary buffer.

3.66 I2C Controller Config Register (Offset = 64h) [Reset = 00000000000000000000040h]

I2C Controller Config is shown in Table 3-68.

Return to the Summary Table.

This register allows the PD controller to be configured to write specific commands to specific target addresses on the I2C3m port. These can be associated with certain events. This register is created automatically by the Application Customization tool.

Table 3-68. I2C Controller Config Register Field Descriptions

Bit	Field	Type	Reset	Description
95	RESERVED	R	0h	Reserved
94-88	External DCDC Target Address	R	0h	Configure external DCDC target address here
87-79	RESERVED	R	0h	Reserved
78-72	Target Address TBT 2	R	0h	Thunderbolt retimer target address for the second Retimer on this port. This is only used if INTEL_VID_CONFIG.DualTBTRetimerPresent is set to 1.
71	RESERVED	R	0h	Reserved
70-64	Target Address TBT 1	R	0h	Thunderbolt retimer target address for the first Retimer on this port. This is only used if INTEL_VID_CONFIG.TBTRetimerPresent is set to 1.
63	RESERVED	R	0h	Reserved
62-56	Target Address 8	R	0h	Sets I2C address associated with events for index 8.
55	RESERVED	R	0h	Reserved
54-48	Target Address 7	R	0h	Sets I2C address associated with events for index 7.
47	RESERVED	R	0h	Reserved
46-40	Target Address 6	R	0h	Sets I2C address associated with events for index 6.
39	RESERVED	R	0h	Reserved
38-32	Target Address 5	R	0h	Sets I2C address associated with events for index 5.
31	RESERVED	R	0h	Reserved
30-24	Target Address 4	R	0h	Sets I2C address associated with events for index 4.
23	RESERVED	R	0h	Reserved
22-16	Target Address 3	R	0h	Sets I2C address associated with events for index 3.
15	RESERVED	R	0h	Reserved
14-8	Target Address 2	R	0h	Sets I2C address associated with events for index 2.
7	RESERVED	R	0h	Reserved
6-0	Target Address 1	R	40h	Sets I2C address associated with events for index 1.

3.67 Type C State Register (Offset = 69h) [Reset = 00000000h]

Type C State is shown in Table 3-69.

Return to the Summary Table.

Contains current status of both CCn pins.

Table 3-69. Type C State Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	TypeC Port State	R	0h	Present state of Type-C state-machine. 0h = Disabled 5h = ErrorRecovery 24h = Unattached.Accessory 2Bh = AttachWait.Accessory 45h = Try.SRC 4Eh = TryWait.SNK 4Fh = Try.SNK 50h = TryWait.SRC 60h = Attached.SRC 61h = Attached.SNK 62h = AudioAccessory 63h = DebugAccessory 64h = AttachWait.SRC 65h = AttachWait.SNK 66h = Unattached.SNK 67h = Unattached.SRC
23-16	CC2 Pin State	R	0h	State of CC2 pin 0h = Not connected 1h = Ra detected (Source only) 2h = Rd detected (Source only) 3h = USB Default Advertisement detected (SInk only) 4h = 1.5A Advertisement detected (Sink Only) 5h = 3.0A Advertisement detected (Sink Only)
15-8	CC1 Pin State	R	0h	State of CC1 pin 0h = Not connected 1h = Ra detected (Source only) 2h = Rd detected (Source only) 3h = USB Default Advertisement detected (SInk only) 4h = 1.5A Advertisement detected (Sink Only) 5h = 3.0A Advertisement detected (Sink Only)
7-0	CC Pin for PD	R	0h	CC pin used for PD communication. 0h = Not connected 1h = CC1 is used for USB PD communication 2h = CC2 is used for USB PD communication

3.68 ADC Results Register (Offset = 6Ah) [Reset = 00000000000000000000000000000000h]

ADC Results is shown in Table 3-70.

Return to the Summary Table.

Provides access to measurements from the internal ADC. The PD controller periodically measures the pins mentioned in this register and updates the register accordingly. The frequency of the update depends upon the mode of the PD controller. For example, in Unconnected Sleep the PD controller will not update these registers.

Table 3-70. ADC Results Register Field Descriptions

Bit	Field	Type	Reset	Description
119-112	IVBUS2_Peak	R	0h	Most recent current peak estimate through PP_5V2. If PORT_CONTROL.EnableCurrentMonitor = 1, this field is an estimate of the recent peak current. It is cleared upon attach for a new connection.(16.5mA per LSB)
111-104	IVBUS1_Mean	R	0h	Most recent current peak estimate through PP_5V2. If PORT_CONTROL.EnableCurrentMonitor = 1, this field is an estimate of the recent average current. It is cleared upon attach for a new connection.(16.5mA per LSB)
103-96	IVBUS2_Peak	R	0h	Most recent current peak estimate through PP_5V1. If PORT_CONTROL.EnableCurrentMonitor = 1, this field is an estimate of the recent peak current. It is cleared upon attach for a new connection.(16.5mA per LSB)
95-88	IVBUS1_Mean	R	0h	Most recent current peak estimate through PP_5V1. If PORT_CONTROL.EnableCurrentMonitor = 1, this field is an estimate of the recent mean current. It is cleared upon attach for a new connection.(16.5mA per LSB)
87-72	RESERVED	R	0h	Reserved
71-64	GPIO5	R	0h	Most recent voltage on the GPIO5 pin. (14mV per LSB)
63-56	GPIO4	R	0h	Most recent voltage on the GPIO4 pin. (14mV per LSB)
55-48	IVBUS2	R	0h	Most recent current measurement through PP_5V2. (16.5mA per LSB)
47-40	IVBUS1	R	0h	Most recent current measurement through PP_5V1. (16.5mA per LSB)
39-32	VBUS2	R	0h	Most recent voltage on the PB_VBUS pin. (98mV per LSB)
31-24	VBUS1	R	0h	Most recent voltage on the PA_VBUS pin. (98mV per LSB)
23-16	LDO3V3	R	0h	Most recent voltage on the LDO_3V3 pin. (14mV per LSB)
15-8	ADCIN2	R	0h	Most recent voltage on the ADCIN2 pin. (14mV per LSB)
7-0	ADCIN1	R	0h	Most recent voltage on the ADCIN1 pin. (14mV per LSB)

3.69 App Config Register (Offset = 6Ch) [Reset = 0000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000000h]

App Config Register is shown in Table 3-71.

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Configures special actions to take when a User SVID mode is entered or exited. This register can only be changed as part of Application Customization. It allows the PD controller to be configured to take specific actions when certain events occur. The Application Customization tool creates this register automatically.

Table 3-71. App Config Register Field Descriptions

Bit	Field	Type	Reset	Description
479-448	Command 2 Exit Group Mode 3	R	0h	Second 4CC command to use upon GPIO asserted low or Alternate Mode exit events. This command may be a Task Command.
447-416	Command 1 Exit Group Mode 3	R	0h	First 4CC command to use upon GPIO asserted low or Alternate Mode exit events. This command cannot be a Task Command.
415-384	Command 2 Enter Group Mode 3	R	0h	Second 4CC command to use upon GPIO asserted high or Alternate Mode entered events. This may be a Task Command.
383-352	Command 1 Enter Group Mode 3	R	0h	First 4CC command to use upon GPIO asserted high or Alternate Mode entered events. This command cannot be a Task Command.
351-345	RESERVED	R	0h	Reserved
344	Command 2 Interface Mode 3	R	0h	Indicates that this command is applied to CMD1 (0) or CMD2 (1).
343-337	RESERVED	R	0h	Reserved
336	Command 1 Interface Mode 3	R	0h	Indicates that this command is applied to CMD1 (0) or CMD2 (1).
335-328	APP Config Index Exit Mode 3	R	0h	Index pointing to application configuration to use upon GPIO asserted low or Alternate Mode exit events.
327-320	APP Config Index Entry Mode 3	R	0h	Index pointing to application configuration to use upon GPIO asserted high or Alternate Mode entered events.
319-288	Command 2 Exit Group Mode 2	R	0h	Second 4CC command to use upon GPIO asserted low or Alternate Mode exit events. This command may be a Task Command.
287-256	Command 1 Exit Group Mode 2	R	0h	First 4CC command to use upon GPIO asserted low or Alternate Mode exit events. This command cannot be a Task Command.
255-224	Command 2 Enter Group Mode 2	R	0h	Second 4CC command to use upon GPIO asserted high or Alternate Mode entered events. This may be a Task Command.
223-192	Command 1 Enter Group Mode 2	R	0h	First 4CC command to use upon GPIO asserted high or Alternate Mode entered events. This command cannot be a Task Command.
191-185	RESERVED	R	0h	Reserved
184	Command 2 Interface Mode 2	R	0h	Indicates that this command is applied to CMD1 (0) or CMD2 (1).
183-177	RESERVED	R	0h	Reserved
176	Command 1 Interface Mode 2	R	0h	Indicates that this command is applied to CMD1 (0) or CMD2 (1).
175-168	APP Config Index Exit Mode 2	R	0h	Index pointing to application configuration to use upon GPIO asserted low or Alternate Mode exit events.
167-160	APP Config Index Entry Mode 2	R	0h	Index pointing to application configuration to use upon GPIO asserted high or Alternate Mode entered events.
159-128	Command 2 Exit Group Mode 1	R	0h	Second 4CC command to use upon GPIO asserted low or Alternate Mode exit events. This command may be a Task Command.
127-96	Command 1 Exit Group Mode 1	R	0h	First 4CC command to use upon GPIO asserted low or Alternate Mode exit events. This command cannot be a Task Command.
95-64	Command 2 Enter Group Mode 1	R	0h	Second 4CC command to use upon GPIO asserted high or Alternate Mode entered events. This may be a Task Command.

Table 3-71. App Config Register Field Descriptions (continued)

Bit	Field	Type	Reset	Description
63-32	Command 1 Enter Group Mode 1	R	0h	First 4CC command to use upon GPIO asserted high or Alternate Mode entered events. This command cannot be a Task Command.
31-25	RESERVED	R	0h	Reserved
24	Command 2 Interface Mode 1	R	0h	Indicates that this command is applied to CMD1 (0) or CMD2 (1).
23-17	RESERVED	R	0h	Reserved
16	Command 1 Interface Mode 1	R	0h	Indicates that this command is applied to CMD1 (0) or CMD2 (1).
15-8	APP Config Index Exit Mode 1	R	0h	Index pointing to application configuration to use upon GPIO asserted low or Alternate Mode exit events.
7-0	APP Config Index Entry Mode 1	R	0h	Index pointing to application configuration to use upon GPIO asserted high or Alternate Mode entered events.

3.70 Sleep Control Register (Offset = 70h) [Reset = 00h]

Sleep Control Register is shown in Table 3-72.

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Sleep configurations.

Table 3-72. Sleep Control Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R/W	0h	Reserved
2-1	Sleep Time	R/W	0h	Minimum time the PD controller waits before entering sleep mode. 0h = Reserved 1h = 100 ms 2h = 1200 ms 3h = Reserved
0	Sleep Mode Allowed	R/W	0h	If this bit is asserted the PD controller will enter sleep modes after device is idle for Sleep Time.

3.71 GPIO Status Register (Offset = 72h) [Reset = 0000000000000000h]

GPIO Status is shown in Table 3-73.

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Captures status and settings of all GPIO pins. Check the device-specific datasheet for the available GPIO because it may vary by device type.

Table 3-73. GPIO Status Register Field Descriptions

Bit	Field	Type	Reset	Description
63-41	RESERVED	R	0h	Reserved
40	GPIO 8 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
39	GPIO 7 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
38	GPIO 6 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
37	GPIO 5 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
36	GPIO 4 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
35	GPIO 3 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
34	GPIO 2 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
33	GPIO 1 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
32	GPIO 0 Direction	R	0h	This bit is asserted when this GPIO is configured as an output.
31-13	RESERVED	R	0h	Reserved
12	GPIO 12 Data	R	0h	Asserted if a logic high is detected on the GPIO.
11-9	RESERVED	R	0h	Reserved
8	GPIO 8 Data	R	0h	Asserted if a logic high is detected on the GPIO.
7	GPIO 7 Data	R	0h	Asserted if a logic high is detected on the GPIO.
6	GPIO 6 Data	R	0h	Asserted if a logic high is detected on the GPIO.
5	GPIO 5 Data	R	0h	Asserted if a logic high is detected on the GPIO.
4	GPIO 4 Data	R	0h	Asserted if a logic high is detected on the GPIO.
3	GPIO 3 Data	R	0h	Asserted if a logic high is detected on the GPIO.
2	GPIO 2 Data	R	0h	Asserted if a logic high is detected on the GPIO.
1	GPIO 1 Data	R	0h	Asserted if a logic high is detected on the GPIO.
0	GPIO 0 Data	R	0h	Asserted if a logic high is detected on the GPIO.

3.72 TX Manufactrer Info SOP Register (Offset = 73h) [Reset = 00000000000000000000000000000000000000000000000h]

TX Manufactrer Info SOP is shown in Table 3-74.

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Transmit Manufacturer Info Data Block SOP (MIDB). The host must enable this feature using the SupportManufacturerInfoMsg bit in the PD3 Configuration register (0x42). If the SupportManufacturerInfoMsg bit is set to 0, then when a Get_Manufacturer_Info message is received the PD controller responds with a Not_Supported message. If the SupportManufacturerInfoMsg bit is set to 1, then the PD controller responds to a Get_Manufacturer_Info message with a target specified as "Port" by pulling the VID and PID from the TX_IDENTITY register (0x47) and appending the contents of this register. If received Get_Manufacturer_Info message has a target specified as "Battery", then the PD controller responds by pulling the VID and PID from the TX_IDENTITY register (0x47) and appending the ASCII string "Not Supported" followed by a zero byte.

Table 3-74. TX Manufactrer Info SOP Register Field Descriptions

Bit	Field	Type	Reset	Description
175-0	Manufacturer String	R/W	0h	Manufacturer String as defined in USB PD. This must be a null terminated string. The PD controller always sends all 22 bytes.

3.73 Received Alert Data Object Register (Offset = 74h) [Reset = 00000000h]

Received Alert Data Object is shown in Table 3-75.

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Received Alert Message as defined by USB PD.

Table 3-75. Received Alert Data Object Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Type of Alert	R	0h	Type of alert as defined by USB PD. 40,EXTENDED ALERTh = 0x80]
23-20	Fixed Batteries	R	0h	Status of fixed batteries when selected by AlertType. 4,BATTERY 3h = 0x8]
19-16	Hot Swappable Batteries	R	0h	Status of hot swappable batteries when selected by AlertType 4,BATTERY 7h = 0x8]
15-4	RESERVED	R	0h	Reserved
3-0	Extended Alert Event Type	R	0h	When the Extended Alert Event bit in the Type of Alert field equals '1', then the Extended Alert Event Type field indicates the event which has occurred 0h = Reserved 1h = Power state change (DFP only) 2h = Power button press (UFP only) 3h = Power button release (UFP only) 4h = Controller initiated wake (UFP only)

3.74 TX Alert Data Object Register (Offset = 75h) [Reset = 00000000h]

TX Alert Data Object is shown in Table 3-76.

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Alert message to transmit as defined by USB PD. The PD controller transmits this data as-is from this register when 'ALRT' is issued.When the host issues the 4CC command 'ALRT' the contents of this register are used to send the Alert message. Note that this register is not duplicated for each port. The host should use the following sequence to send the same Alert message on both ports: Write Transmit Alert Data Object (0x75), issue the 4CC 'ALRT' command to Port 1 and issue the 4CC 'ALRT' command to Port 2. The host should use the following sequence to send two different Alert messages on each port (only relevant for dual-port PD controllers): Write Transmit Alert Data Object (0x75), issue the 4CC 'ALRT' command to Port 1, wait for the command to complete, write Transmit Alert Data Object (0x75) and issue the 4CC 'ALRT' command to Port 2.

Table 3-76. TX Alert Data Object Register Field Descriptions

Bit	Field	Type	Reset	Description
31-24	Type of Alert	R/W	0h	Type of alert as defined by USB PD. 40,EXTENDED ALERTh = 0x80]
23-20	Fixed Batteries	R/W	0h	Status of fixed batteries when selected by AlertType. 4,BATTERY 3h = 0x8]
19-16	Hot Swappable Batteries	R/W	0h	Status of hot swappable batteries when selected by AlertType 4,BATTERY 7h = 0x8]
15-4	RESERVED	R/W	0h	Reserved
3-0	Extended Alert Event Type	R/W	0h	When the Extended Alert Event bit in the Type of Alert field equals '1', then the Extended Alert Event Type field indicates the event which has occurred 0h = Reserved 1h = Power state change (DFP only) 2h = Power button press (UFP only) 3h = Power button release (UFP only) 4h = Controller initiated wake (UFP only)

3.75 Tx Source Capabilities Extended Data Block Register (Offset = 77h) [Reset = 0000000000000000F0F0000000000h]

Tx Source Capabilities Extended Data Block is shown in Table 3-77.

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Transmit Source Capabilities Extended Data Block (SCEDB). If the PD3 configuration register (0x42) bit SourceCapExtMsg is set to zero, the PD controller responds to a Get_Source_Cap_Extended USB PD message with a Not_Supported message. If the SourceCapExtMsg bit is set to 1 then the response is generated from the contents of this register based on USB PD requirements. The VID, PID, and XID fields are taken from the TX_IDENTITY Register (0x47), the FW version is taken from the RR word in the Version register (0x0F), the HW version is taken from the REV_ID word in the Boot Flags register (0x2D), then the contents of this register are appended.

Table 3-77. Tx Source Capabilities Extended Data Block Register Field Descriptions

Bit	Field	Type	Reset	Description
119-112	Source EPR PDP	R/W	0h	Source's EPR PDP rating as defined by the USB PD specification.
111	RESERVED	R/W	0h	Reserved
110-104	Source PDP	R/W	0h	Source's PDP rating as defined by the USB PD specification.
103-100	Number Hot Swappable Batteries	R/W	0h	Number of hot swappable batteries / battery slots as defined by the USB PD specification. (Max of 1)
99-96	Number Fixed Batteries	R/W	0h	Number of fixed batteries / battery slots as defined by the USB PD specification. (Max of 3)
95-88	Source Inputs	R/W	0h	Source inputs as defined by the USB PD specification. The Barrel_Jack_Event GPIO Event can modify bit 0 of this field automatically upon rising and falling edges. The host may choose to set bit 1 of this field to 1 when it enables the Barrel_Jack_Event GPIO Event.
87-80	Touch Temperature	R/W	0h	Touch temperature as defined by the USB PD specification.
79-64	Peak Current 3	R/W	0h	Peak Current 3 as defined by the USB PD specification.
63-48	Peak Current 2	R/W	Fh	Peak Current 2 as defined by the USB PD specification.
47-32	Peak Current 1	R/W	F00h	Peak Current 1 as defined by the USB PD specification.
31-24	Touch Current	R/W	0h	Touch current as defined by the USB PD specification.
23-16	Compliance	R/W	0h	Compliance as defined by the USB PD specification.
15-8	Hold Up Time	R/W	0h	Hold up time as defined by the USB PD specification.
7-0	Voltage Regulation	R/W	0h	Voltage regulation as defined by the USB PD specification.

3.76 Transmitted Status Data Block (SDB) Register (Offset = 79h) [Reset = 00000000000000h]

Transmitted Status Data Block (SDB) Register is shown in Table 3-78.

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Transmit Status Data Block (SDB).

Table 3-78. Transmitted Status Data Block (SDB) Register Field Descriptions

Bit	Field	Type	Reset	Description
55-54	RESERVED	R/W	0h	Reserved
53-51	New Power State Indicator	R/W	0h	Power state change as defined by the USB PD specification 0h = Off LED 1h = On LED 2h = Blinking LED 3h = Breathing LED
50-48	New Power State	R/W	0h	Power state change as defined by the USB PD specification 0h = Status not supported 1h = S0 2h = Modern Standby 3h = S3 4h = S4 5h = S5 6h = G3 7h = Reserved
47-40	Power Status	R/W	0h	Power status as defined by the USB PD specification. 10,TEMPERATUREh = 0x20]
39-35	RESERVED	R/W	0h	Reserved
34-33	Temperature Status	R/W	0h	Temperature status as defined by the USB PD specification. 0h = Not Supported 1h = Normal 2h = Warning 3h = Over temperture
32	RESERVED	R/W	0h	Reserved
31-24	Event Flags	R/W	0h	Event flags as defined by the USB PD specification. 4,OVPh = 0x8]
23-16	Present Battery Input	R/W	0h	Present battery input as defined by the USB PD specification. 40,BATTERY 7h = 0x80]
15-8	Present Input	R/W	0h	Present input as defined by the USB PD specification. 8,INTERNAL POWER FROM NON-BATTERYh = 0x10]
7-0	Internal Temperature	R/W	0h	Internal temperature as defined by the USB PD specification. (1C per LSB)

3.77 Trasmitted PPS Status Data Block Register (Offset = 7Ah) [Reset = 00000000h]

Trasmitted PPS Status Data Block is shown in Table 3-79.

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Table 3-79. Trasmitted PPS Status Data Block Register Field Descriptions

Bit	Field	Type	Reset	Description
31-28	RESERVED	R/W	0h	Reserved
27	OMF	R/W	0h	Real Time Flag as defined by the USB PD spec.
26-25	PTF	R/W	0h	Real Time Flag as defined by the USB PD spec.
24	RESERVED	R/W	0h	Reserved
23-16	Output Current	R/W	0h	Output current as defined by the USB PD spec. (50mA per LSB). 0xFF = this field not supported
15-0	Output Voltage	R/W	0h	Output voltage as defined by the USB PD spec.(20mV per LSB, 0xFFFF = this field not supported)

3.78 Transmitted Battery Status Data Objects (BSDO) Register (Offset = 7Bh) [Reset = 00000000000000000000000FFFF0200h]

Transmitted Battery Status Data Objects (BSDO) Register is shown in Table 3-80.

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Transmit Battery Status Data Objects (BSDO). The host should also program the Tx Source Capabilities Extended register (0x77) in order to specify the number of each type of battery such that it is consistent with the contents of this register. This feature must be enabled in the PD3_CONFIG register (0x42) SupportBatteryStatusMsg bit. The PD controller does not take any automatic action if this register is written. The host is responsible for issuing 4CC 'ALRT' command to inform the Port Partner that the Battery Status is changed. If the SupportBatteryStatusMsg bit is set to 0 and a Get_Battery_Status message is received, then this register is ignored and the PD controller sends a Not_Supported message. If the SupportBatteryStatusMsg bit is set to 1, and a Get_Battery_Status message is received then the contents of this register are sent in response.

Table 3-80. Transmitted Battery Status Data Objects (BSDO) Register Field Descriptions

Bit	Field	Type	Reset	Description
127-112	Hot Swappable Battery 0 Present Info	R/W	0h	Battery status data object returned for fixed battery index 0.
111-104	Hot Swappable Battery 0 Battery Info	R/W	0h	Battery status data object returned for hot-swappable battery index 0.
103-96	RESERVED	R/W	0h	Reserved
95-80	Fixed Battery 2 Present Capacity	R/W	0h	Battery status data object returned for fixed battery index 0.
79-72	Fixed Battery 2 Battery Info	R/W	0h	Battery status data object returned for fixed battery index 2.
71-64	RESERVED	R/W	0h	Reserved
63-48	Fixed Battery 1 Present Capacity	R/W	0h	Battery status data object returned for fixed battery index 0.
47-40	Fixed Battery 1 Battery Info	R/W	0h	Battery status data object returned for fixed battery index 1.
39-32	RESERVED	R/W	0h	Reserved
31-16	Fixed Battery 0 Present Capacity	R/W	FFFFh	Battery status data object returned for fixed battery index 0.
15-8	Fixed Battery 0 Battery Info	R/W	2h	Battery status data object returned for fixed battery index 0.
7-0	RESERVED	R/W	0h	Reserved

3.79 Tx Battery Capabilities Register (Offset = 7Dh) [Reset = 0000000000000000000000000000000000000000000000000000000000000000h]

Tx Battery Capabilities is shown in Table 3-81.

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Transmit Battery Capability Data Block (BCDB). The host should also program the Tx Source Capabilities Extended register (0x77) in order to specify the number of each type of battery such that it is consistent with the contents of this register. This feature must be enabled in the PD3_CONFIG register (0x42) bit SupportBatteryCapMsg. The PD controller does not take any automatic action if this register is written. If the SupportBatteryCapMsg is 0 and a Get_Battery_Capabilities message is received, then the contents of this register are ignored and the PD controller sends a Not_Supported message. If the SupportBatteryCapMsg is 1 and a Get_Battery_Capabilities message is received, then the contents of this register are sent in response.

Table 3-81. Tx Battery Capabilities Register Field Descriptions

Bit	Field	Type	Reset	Description
287-280	Battery Type	R/W	0h	Battery type for hot-swappable battery index 0.
279-264	Battery Last Full Charge Capacity	R/W	0h	Battery last full charge capacity for hot-swappable battery index 0.
263-248	Battery Design Capacity	R/W	0h	Battery design capacity for hot-swappable battery index 0.
247-232	PID 3	R/W	0h	PID for hot-swappable battery index 0.
231-216	VID 3	R/W	0h	VID for hot-swappable battery index 0.
215-208	Battery Type	R/W	0h	Battery type for fixed battery index 2.
207-192	Battery Last Full Charge Capacity	R/W	0h	Battery last full charge capacity for fixed battery index 2.
191-176	Battery Design Capacity	R/W	0h	Battery design capacity for fixed battery index 2.
175-160	PID 2	R/W	0h	PID for fixed battery index 2.
159-144	VID 2	R/W	0h	VID for fixed battery index 2.
143-136	Battery Type	R/W	0h	Battery type for fixed battery index 1.
135-120	Battery Last Full Charge Capacity	R/W	0h	Battery last full charge capacity for fixed battery index 1.
119-104	Battery Design Capacity	R/W	0h	Battery design capacity for fixed battery index 1.
103-88	PID 1	R/W	0h	PID for fixed battery index 1.
87-72	VID 1	R/W	0h	VID for fixed battery index 1.
71-64	Battery Type	R/W	0h	Battery type for fixed battery index 0.
63-48	Battery Last Full Charge Capacity	R/W	0h	Battery last full charge capacity for fixed battery index 0.
47-32	Battery Design Capacity	R/W	0h	Battery design capacity for fixed battery index 0.
31-16	PID 0	R/W	0h	PID for fixed battery index 0.
15-0	VID 0	R/W	0h	VID for fixed battery index 0.

3.80 Transmit Sink Capabilities Extended Data Block Register (Offset = 7Eh) [Reset = 0000000000000A01424241412D08h]

Transmit Sink Capabilities Extended Data Block is shown in Table 3-82.

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Transmit Sink Capabilities Data Block (SKEDB). This feature must be enabled in the PD3_CONFIG register (0x42) bit SupportSinkCapExtended. The PD controller does not take any automatic action if this register is written. If the SupportSinkCapExtended bit is 0 and a Get_Sink_Cap_Extended message is received, then the contents of this register are ignored and the PD controller sends a Not_Supported message. If the SupportSinkCapExtended bit is 1 and a Get_Sink_Cap_Extended message is received, then the contents of this register are used to formulate the response. The PD controller also pulls the VID, PID, XID from the TX_IDENTITY register (0x47), the FW version is taken from the RR word in the Version register (0x0F), the HW version is taken from the REV_ID word in the Boot Flags register (0x2D). Finally, the PD controller appends the contents of this register. Refer to the latest USB PD specification for detailed description of each field. The values in this register are not used by the PD controller to affect behavior, it just simply uses these contents to respond.

Table 3-82. Transmit Sink Capabilities Extended Data Block Register Field Descriptions

Bit	Field	Type	Reset	Description
111-104	EPR Sink Maximum PDP	R/W	0h	
103-96	EPR Sink Operational PDP	R/W	0h	
95-88	EPR Sink Minimum PDP	R/W	0h	
87-80	Sink Maximum PDP	R/W	0h	Sink maximum PDP as defined in the USB PD specification.
79-72	Sink Operational PDP	R/W	0h	Sink operational PDP as defined in the USB PD specification.
71-64	Sink Minimum PDP	R/W	0h	Sink minimum PDP as defined in the USB PD specification.
63-56	Sink Modes	R/W	Ah	Sink modes as defined in the USB PD specification.
55-48	Battery Info	R/W	1h	Battery information as defined in the USB PD specification.
47-40	Touch Temprature	R/W	42h	Touch temperature as defined by the USB PD specification.
39-32	Compliance	R/W	42h	Compliance as defined by the USB PD specification.
31-16	Sink Load Char	R/W	4141h	Sink load characteristics as defined in the USB PD specification.
15-8	Load Step	R/W	2Dh	Load step as defined in the USB PD specification.
7-0	SKEDB Version	R/W	8h	SKEDB Version as defined in the USB PD specification.

3.81 UUID Handle Register (Offset = 80h) [Reset = 00000000000000000000000000000000h]

UUID Handle is shown in Table 3-83.

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BR/GR UUID

Table 3-83. UUID Handle Register Field Descriptions

Bit	Field	Type	Reset	Description
127-0	UUID Handle	R/W	0h	BR/GR UUID

3.82 External DCDC Status Register (Offset = 94h) [Reset = 00h]

External DCDC Status is shown in Table 3-84.

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Table 3-84. External DCDC Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SCP	R	0h	Short Circuit Protection 0h = No short ciruit 1h = Short circuit. Reset back to 0 once read
6	OCP	R	0h	Over Current Protection 0h = No OCP 1h = Output current reached ILIM sensed at ISP and ISN
5	OVP	R	0h	Over Voltage Protection 0h = No OVP 1h = Output voltage exceeds the OVP threshold. Reset b
4	TSD	R	0h	Thermal ShutDown 0h = No TSD 1h = TSD occurred. Reset back to 0 once read
3-2	RESERVED	R	0h	Reserved
1-0	Status	R	0h	Operating Status 0h = Boost 1h = Buck 2h = Buck-Boost 3h = Reserved

3.83 External DCDC Parameters Register (Offset = 95h) [Reset = 00000000000000000000000000000000000000000000h]

External DCDC Parameters is shown in Table 3-85.

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Generic External DCDC Parameters

Table 3-85. External DCDC Parameters Register Field Descriptions

Bit	Field	Type	Reset	Description
167-162	RESERVED	R/W	0h	Reserved
161	Enable Calibration	R/W	0h	Shall be enabled only for LM5176 based EPR-SRC systems. Else, shall be disabled. FW doesn't explicitly check for all these conditions when enabling the calibration for LM51756.
160	Big Endian	R/W	0h	Set this bit to indicate FW to inject the calculated code for V and I in in the respective container in MSB First endianness. When not set, code is injected in LSB first endianness.
159-152	Current Code Length	R/W	0h	What is the length of the ILIM field in I2C_CONTROLLER_EVENT__EXTDCDC_SET_ILIM_CONTAINER data buffer in bits?
151-144	Current Code Offset	R/W	0h	At what bit offset should the FW inject the calcuated ILIM code in I2C_CONTROLLER_EVENT__EXTDCDC_SET_ILIM_CONTAINER data buffer?
143-136	Voltage Code Length	R/W	0h	What is the length of the VOUT field in I2C_CONTROLLER_EVENT__EXTDCDC_SET_VOUT_CONTAINER data buffer in bits?
135-128	Voltage Code Offset	R/W	0h	At what bit offset should the FW inject the calcuated VOUT code in I2C_CONTROLLER_EVENT__EXTDCDC_SET_VOUT_CONTAINER data buffer?
127-96	Code 0 Current	R/W	0h	ILIM of DCDC in uA when writing 0 code to ILIM field (Y intersection (c) for the line) (+/-1 uA per LSB as uA)
95-64	LSB Current	R/W	0h	LSB of DCDC in uA/code for setting desired ILIM (Slope (m) for the line) (+/-1 uA/code per LSB as uA/code)
63-32	Code 0 Voltage	R/W	0h	VOUT of DCDC in uV when writing 0 code to Voltage field (Y intersection (c) for the line) (+/-1 uV per LSB as uV)
31-0	LSB Voltage	R/W	0h	LSB of DCDC in uV/code for generating desired VOUT (Slope (m) for the line) (+/-1 uV/code per LSB as uV/code)

3.84 EPR Config Register (Offset = 97h) [Reset = 360001010Ah]

EPR Config is shown in Table 3-86.

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EPR configuration for external hardware

Table 3-86. EPR Config Register Field Descriptions

Bit	Field	Type	Reset	Description
39-32	Divider Ratio	R/W	36h	VBUS divider ratio (0.78125 % per LSB)
31-24	Vbus Threshold Margin	R/W	0h	VBUS Threshold Margin
23-16	Voltage Divider Turn On Small	R/W	1h	Voltage Divider Turn On Small In ms (1 ms per LSB as ms)
15-8	Voltage Divider Turn Off	R/W	1h	Voltage Divider Turn Off In ms (1 ms per LSB as ms)
7-0	Voltage Divider Turn On	R/W	Ah	Voltage Divider Turn On In ms (1 ms per LSB as ms)

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Chapter 4
4CC Task Detailed Descriptions

4.1 Overview

This section describes the 4CC Tasks defined by the PD Controller Host Interface. The Tasks are categorized into various sub-groups in this section. All Tasks that return data using the DATAx registers will always ensure the proper output data is loaded into those registers before setting the CMDx register to 0 to indicate Task completion. DATAx is never modified by PD Controller after CMDx has been changed to 0, to ensure the Host can retrieve data from the previously-executed Task, and to ensure the Host can load these registers for a future Task without risk of overwriting. Note that other registers can continue to be updated after a Task completes, as Tasks can have additional side effects.

Many of the Tasks return a status code in the first byte of the DATAx register. The standard Task response byte is defined in Table 4-1. The remaining DATAx bytes can be used at each Task's discretion.

Table 4-1. Standard Task Response

Description	**Tasks are a special form of Tasks that return a status code in the first byte of the DATAX register.**			
Output DATAX	**Bit**	**Name**	**Description**	
	Byte 1: Task Return Code			
	7:4	Reserved	Reserved for standard Tasks. May be used by certain Tasks for Task-specific return codes. Successful return codes can use this byte provided TaskResult is 0x0.	
	3:0	TaskResult	Standard Task return codes.	
			0x0	Task completed successfully.
			0x1	Task timed-out or aborted by 'ABRT' Request.
			0x2	Reserved.
			0x3	Task rejected.
			0x4	Task rejected because the Rx Buffer was locked. This is for Tasks that can require the PD controller to use the Rx Buffer.
			0x5-0xF	Reserved for standard Tasks. May be used by certain Tasks for Task-specific error codes. Treated as an error when encountered.

4.2 CPU Control Tasks

4.2.1 'Gaid' - Return to normal operation

Table 4-2. 'Gaid' - Return to normal operation.

Description	The 'Gaid' Task causes a warm restart of the PD Controller processor.
INPUT DATAX	None
OUTPUT DATAX	None
Task Completion	Technically this Task never completes because the processor restarts. However, because all HI registers return to their default state upon reboot, all CMDx/DATAx registers will return to 0, which will mark this Task as complete.
Side Effects	The 'Gaid' Task causes a warm restart of the PD Controller processor. PD Controller can momentarily NAK I2C transactions while rebooting.
Additional Information	The PD controller is in the 'APP ' mode, then it immediately goes to the Error Recovery state then after delaying 1 second (typical) it does a warm restart.

4.2.2 'GAID' - Cold reset request

Table 4-3. 'GAID' - Cold reset request

Description	The 'GAID Task causes a cold restart of the PD Controller processor.
INPUT DATAX	None
OUTPUT DATAX	None
Task Completion	Technically this Task never completes because the processor restarts. However, because all HI registers return to their default state upon reboot, all CMDx/DATAx registers will return to 0, which will mark this Task as complete. This Task forces the PD Controller to reboot its OTP bootloader.
Side Effects	The 'Gaid' Task causes a warm restart of the PD Controller processor. PD Controller can momentarily NAK I2C transactions while rebooting.
Additional Information	The PD controller immediately goes to the Error Recovery state, then after delaying 1 second (typical) it does a cold restart.

4.3 Modal Tasks

The following Tasks are considered "Modal" for the PD Controller. Only one Modal Task can be active at a time, if the MODE register (0x03) reports any value other than 'APP ' when a Modal Task is issued the Task will be Rejected unless this Modal Task is considered a higher-priority, in which case it can cancel other Modal Tasks. Modal Tasks change the value of the Mode register as described below, and this value remains unless the Task defines its own mechanism for disabling the mode, or if a 'Gaid'/'GAID' Task is issued to reboot PD Controller and clear the Mode.

4.3.1 'DISC' - Simulate port disconnect

Table 4-4. 'DISC' - Simulate port disconnect

Description	**The 'DISC' Modal Task causes the PD Controller to act as if the USB-C port is disconnected, with an optional Host-specified delay to restoring normal port operation. If currently there is no USB-C connection on the port, then this task will be rejected. The port that will be disconnected when writing the 'DISC' Task will correspond to the I2C slave address used when writing the 'DISC' Task.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	7:0	DISCdelay	8-bit value in seconds for disconnect time. If 0, there is no automatic reconnect.
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.		
Task Completion	This Task always completes successfully, it has no reason to be rejected or timed-out. If another Modal Task was already active the 'DISC' Modal Task will cancel that Modal Task and take its place. The 'DISC' Modal Task completes immediately, it does not wait for the re-connect delay		
Side Effects	Effectively the action of this Modal Task is to force the Type-C state machine into the Disabled state, which disables the CC pull-up/downs. Any power switch that was enabled as input or output will be disabled either as a direct result of this Modal Task or an indirect result due to the disconnect event. This causes any existing connection to be lost, and the HI registers will be updated as appropriate for a disconnect event. No new connections will be detected because the port is in the Disabled state. The Type-C state machine does not return to normal operation unless DISCdelay is non-zero and the specified delay passes or a 'Gaid'/'GAID' Task is issued to reboot PD Controller .The MODE register (0x03) is changed to 'DIS#' (where # is the port number that is being disconnected) while this Modal Task is active to indicate that PD Controller is not in its normal operating state. If DISCdelay is non-zero when the specified delay expires the Mode register will return to 'APP '.If another Modal Task is enabled that cancels this one then the port shall be re-enabled at that time, regardless of DISCdelay and even if the timer had not yet expired. NOTE: If a hot-VBUS Source is attached VBUS can still be present at the input to PD Controller even though it is in the Disabled state. Some VBUS-related registers can report this voltage presence as usual, however PD Controller will keep its power switches disabled until normal operation is restored.		
Additional Information	None		

4.4 PD Message Tasks

4.4.1 'SWSk' - PD PR_Swap to Sink

Table 4-5. 'SWSk' - PD PR_Swap to Sink

Description	The 'SWSk' Task instructs PD Controller to attempt to become a Sink through PR_Swap at the first opportunity while maintaining policy engine compliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'SWSk' Task completes either when the PR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the Source. The 'SWSk' Task shall be considered rejected if: • The Source indicated through Source Capabilities that it does not support Dual-Role Power. • The PR_Swap is Rejected. The 'SWSk' Task shall be considered timed-out if: • The PR_Swap is Accepted but failed to complete per the PD spec. The 'SWSk' Task shall be considered successful if: • PD Controller is already in the Sink power role. • The PR_Swap is Accepted and completes normally.
Side Effects	When the 'SWSk' Task completes successfully PD Controller will have transitioned to the Sink power role, which impacts other registers. If the PR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

4.4.2 'SWSr' - PD PR_Swap to Source

Table 4-6. 'SWSr' - PD PR_Swap to Source

Description	The 'SWSr' Task instructs PD Controller to attempt to become a Source through PR_Swap at the first opportunity while maintaining policy engine compliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'SWSr' Task completes either when the PR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the Sink. The 'SWSr' Task shall be considered rejected if: • The Sink previously indicated through Sink or Source Capabilities that it does not support Dual-Role Power. • The PR_Swap is Rejected. The 'SWSr' Task shall be considered timed-out if: • The PR_Swap is Accepted but failed to complete per the PD spec. The 'SWSr' Task shall be considered successful if: • PD Controller is already in the Source power role. • The PR_Swap is Accepted and completes normally.
Side Effects	When the 'SWSr' Task completes successfully PD Controller will have transitioned to the Source power role, which impacts other registers. If the PR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

4.4.3 'SWDF' - PD DR_Swap to DFP

Table 4-7. 'SWDF' - PD DR_Swap to DFP

Description	**The 'SWDF' Task instructs PD Controller to attempt to become a DFPthrough DR_Swap at the first opportunity while maintaining policy enginecompliance. If there are any active Alternate Modes as a UFP PD Controller willattempt to exit those Modes first before sending the DR_Swap.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'SWDF' Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the DFP. The 'SWDF' Task shall be considered rejected if: • The UFP indicated through Source or Sink Capabilities that it does not support Data Role Swap. • The DR_Swap is Rejected. The 'SWDF' Task shall be considered successful if: • PD Controller is already in the DFP data role. • The DR_Swap is Accepted and completes normally.
Side Effects	When the 'SWDF' Task completes successfully PD Controller will have transitioned to the DFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

4.4.4 'SWUF' - PD DR_Swap to UFP

Table 4-8. 'SWUF' - PD DR_Swap to UFP

Description	**The 'SWUF' Task instructs PD Controller to attempt to become a UFPthrough DR_Swap at the first opportunity while maintaining policy enginecompliance. If there are any active Alternate Modes as a DFP PD Controller willexit those Modes first before attempting the DR_Swap.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'SWUF' Task completes either when the DR_Swap is finished or it is otherwise determined to not be possible or fails. The Task can continue to run because of Wait messages being sent by the UFP. The 'SWUF' Task shall be considered rejected if: • The DFP indicated through Source or Sink Capabilities that it does not support Data Role Swap. • The DR_Swap is Rejected. The 'SWUF' Task shall be considered successful if: • PD Controller is already in the UFP data role. • The DR_Swap is Accepted and completes normally.
Side Effects	When the 'SWDF' Task completes successfully PD Controller will have transitioned to the UFP data role, which impacts other registers. If the DR_Swap fails after the Accept is sent then Soft and/or Hard Resets are likely to occur per PD spec requirements.
Additional Information	None

4.4.5 'GSkC' - PD Get Sink Capabilities

Table 4-9. 'GSkC' - PD Get Sink Capabilities

Description	The 'GSkC' Task instructs PD Controller to issue a Get_Sink_Capmessage to the Port Partner at the first opportunity while maintaining policyengine compliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'GSkC' Task completes either when the Sink Capabilities message is received or the Task otherwise fails. • The Port Partner is a Source and indicated it was not Dual-Role Power. • The Port Partner responds to the Get_Sink_Cap message with a Reject or Not_Supported message. The 'GSkC' Task shall be considered timed-out if: • The Port Partner fails to respond within the time required by the PD spec. The 'GSkC' Task shall be considered successful if: • The Get_Sink_Cap message is sent, GoodCRC'ed and a Sink Capabilities response is received and processed.
Side Effects	When the 'GSkC' Task completes successfully the *RX_SINK_CAPS* register (0x31) will have been updated.
Additional Information	None

4.4.6 'GSrC' - PD Get Source Capabilities

Table 4-10. 'GSrC' - PD Get Source Capabilities

Description	The 'GSrC' Task instructs PD Controller to issue a Get_Source_Capmessage to the Port Partner device at the first opportunity while maintainingpolicy engine compliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'GSrC' Task completes either when the Source Capabilities message is received or the Task otherwise fails. The 'GSrC' Task shall be considered rejected if: • The Port Partner is a Sink and indicated (through previous Source or Sink Capabilities) it was not Dual-Role Power. • The Port Partner responds to the Get_Source_Cap message with a Reject or Not_Supported message. The 'GSrC' Task shall be considered timed-out if: • The Port Partner fails to respond within the time required by the PD spec. The 'GSrC' Task shall be considered successful if: • The Get_Source_Cap message is sent, GoodCRC'ed and a Source Capabilities response is received and processed.
Side Effects	When the 'GSrC' Task completes successfully the *RX_SOURCE_CAPS* register (0x30) will have been updated.
Additional Information	None

4.4.7 'GPPI' - PD Get Port Partner Information

The 'GPPI' Task can be used to cause the PD controller to issue these types of USB PD Get messages:

- Get_Source_Cap_Extended (control message)
- Get_Sink_Cap_Extended (control message)
- Get_Status (Control message)
- Get_Country_Codes (Control message)
- Get_Country_Info (Data message)
- Get_Battery_Status (Extended message)
- Get_Battery_Cap (Extended message)
- Get_Manufacturer_Info (Extended message)

The PD controller does not have dedicated registers to store the response to these messages. The host must get that response from the DATAX register associated with this Task.

The host must NOT use 'GPPI' to send Get_Sink_Capabilities or Get_Source_Capabilities messages, because the USB PD spec requires specific actions be taken by the PD controller any time those messages are received. While executing the 'GPPI' Task, the PD controller does not parse the returned message to carry out those checks. Instead, the host must use 'GSkC' to send Get_Sink_Capabilities and 'GSrC' to send Get_Source_Capabilities messages.

This Task is defined to enable supporting any new Get message that can be defined by USB PD in the future.

Table 4-11. 'GPPI' - Send a USB PD Get* Message

Description	**The 'GPPI' Task instructs PD Controller to issue a specific USB PDmessage to the Port Partner at the first opportunity while maintaining policyengine compliance.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	15	Reserved		
	14:13	FrameType	00b	SOP
			01b	SOP'
			10b	SOP''
			11b	Reserved
	12:8	NumBytes		
	7	Reserved		
	6:5	MessageCategory	00b	Control message (no payload)
			01b	Data message (requires payload)
			10b	Extended message (requires payload)
			11b	Reserved
	4:0	MessageType	This field must be the MessageType as defined in the USB PD specification. It specifies the Type of message the PD controller will send.	
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.			

Table 4-11. 'GPPI' - Send a USB PD Get* Message (continued)

Description	The 'GPPI' Task instructs PD Controller to issue a specific USB PDmessage to the Port Partner at the first opportunity while maintaining policyengine compliance.
Task Completion	The 'GPPI' Task completes either when the appropriate message is received or the Task otherwise fails. The 'GPPI' Task shall be considered rejected if: • Sending the requested message can violate the USB PD spec. For example, the Port Partner is a Sink and indicated (through previous Source or Sink Capabilities) it was not Dual-Role Power. • The PortPartner replies with a Reject or Not_Supported message. • The USB PD spec revision (PlugPartnerNegSpecRev or PortPartnerNegSpecRev in PD3_STATUS register (0x41) does not allow sending the requested message. The 'GPPI' Task shall be considered timed-out if: • The requested message is sent, GoodCRC'ed and the recipient (Port Partner or Cable Plug) fails to respond within the time required by the PD spec. • A PD Hard Reset or a disconnection happens before the Task completes. The 'GPPI' Task shall be considered successful if: • The requested message is sent, GoodCRC'ed and an appropriate response is received and processed. The 'GPPI' Task shall be aborted when the Rx Buffer is locked. The Rx Buffer is locked after data from a receive message is placed in the DATAX register. The Rx Buffer is unlocked after disconnect and by the 'MBRd' Task.
Side Effects	If necessary, the PD controller can issue a VCONN_Swap in order to send the requested message to a Cable Plug. If the PD controller is in the sink power role and it reads Rp = SinkTxNG, it will wait until Rp = SinkTxOK before initiating the atomic message sequence requested by this 'GPPI' Task. This can cause an non-deterministic delay in completing the Task.
Additional Information	The PD controller will continue trying to execute this Task until it times out or aborts as described above. The host can want to issue the 'ABRT' Task if the process takes too long. Some scenarios where this can happen are: • The PD controller is required to be the VCONN_Source in order to send any message on SOP or SOP'. The PD controller will continue trying to become the VCONN provider until it is successful. • The PD controller with a sink power role (that is PresentRole = Sink) is required to wait for Rp = SinkTxOK before initiating an Atomic Message Sequence. The PD controller will continue waiting for Rp = SinkTxOK until it is able to send the appropriate message required for this 'GPPI' Task. The host must wait until CMDx reads as 0 or INT_EVENT1.CmdComplete is asserted before issuing the 'MBRd' 4CC Task to read the Rx Buffer after issuing this 'GPPI' Task. While executing the 'GPPI' Task, the PD controller uses the same shared buffer that is used to store other extended messages. Therefore, the host must not use the 'GPPI' Task when any other atomic message sequence is ongoing. To read the PD response received as a result of issuing the 'GPPI' Task after it is completed, the host must use the 'MBRd' 4CC command. The 'MBRd' Task must also be used to unlock the Rx Buffer for other incoming message.

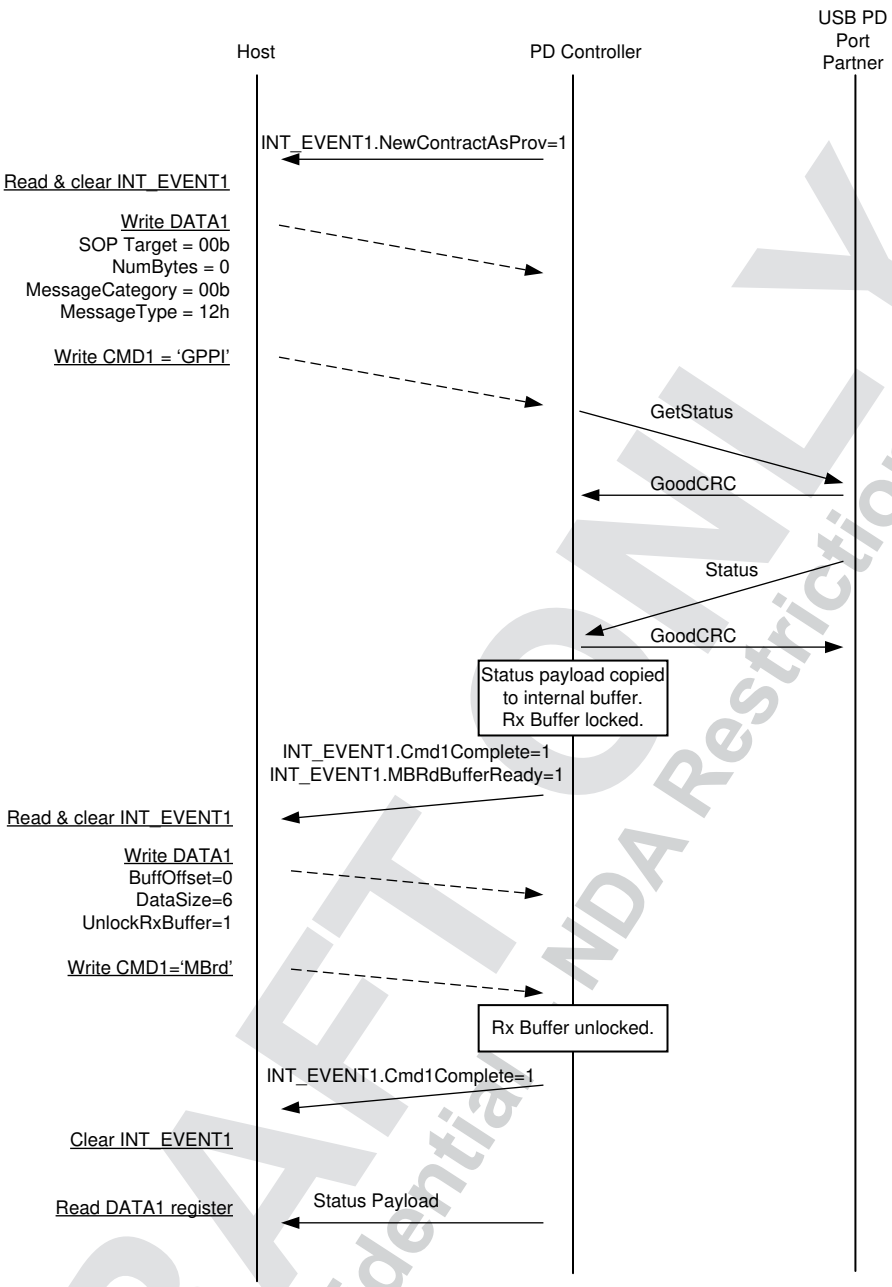


Figure 4-1. Example Sequence for 'GPPI' Task When Host Uses INT_EVENT1

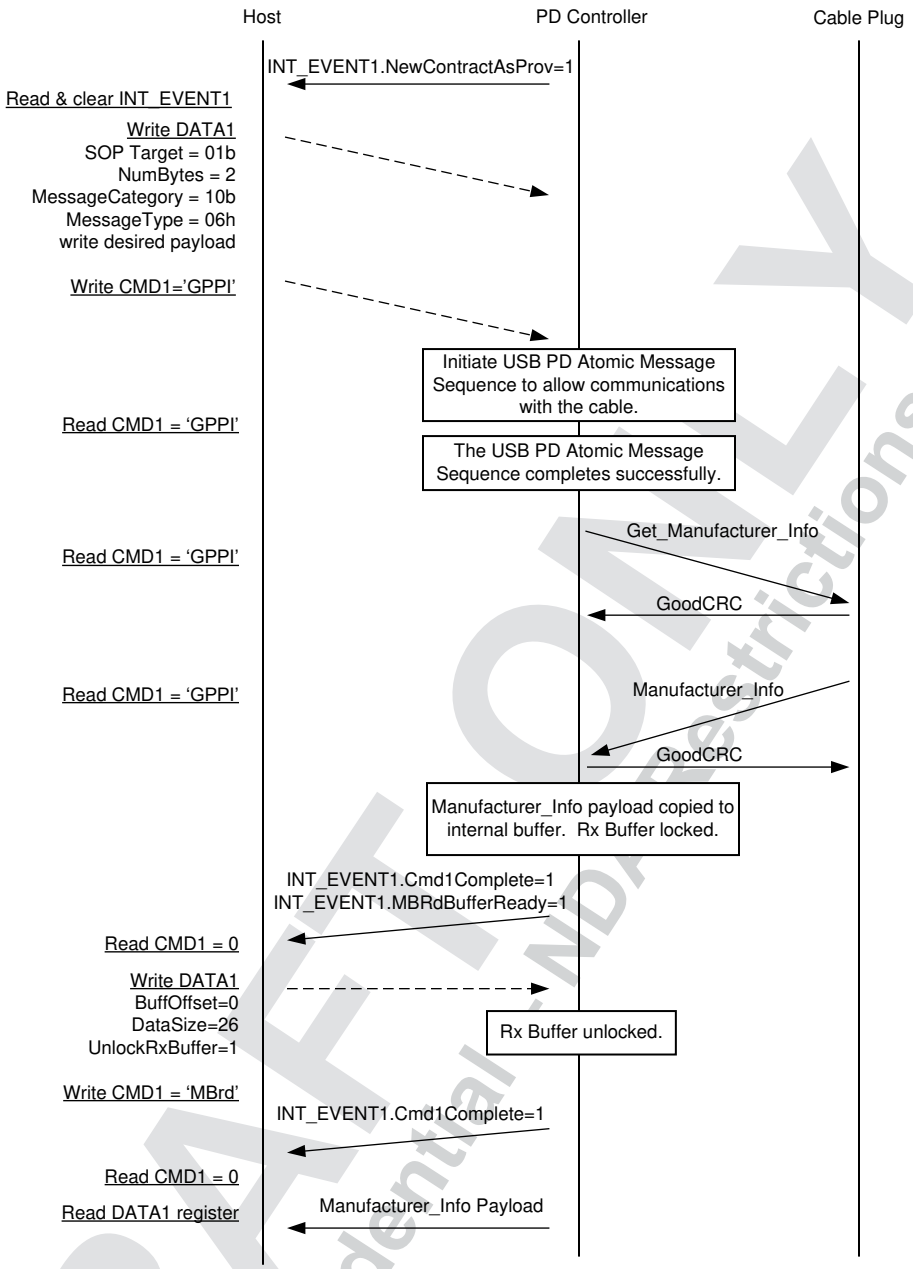


Figure 4-2. Example Sequence for 'GPPI' Task When Host Uses CMD1 Polling

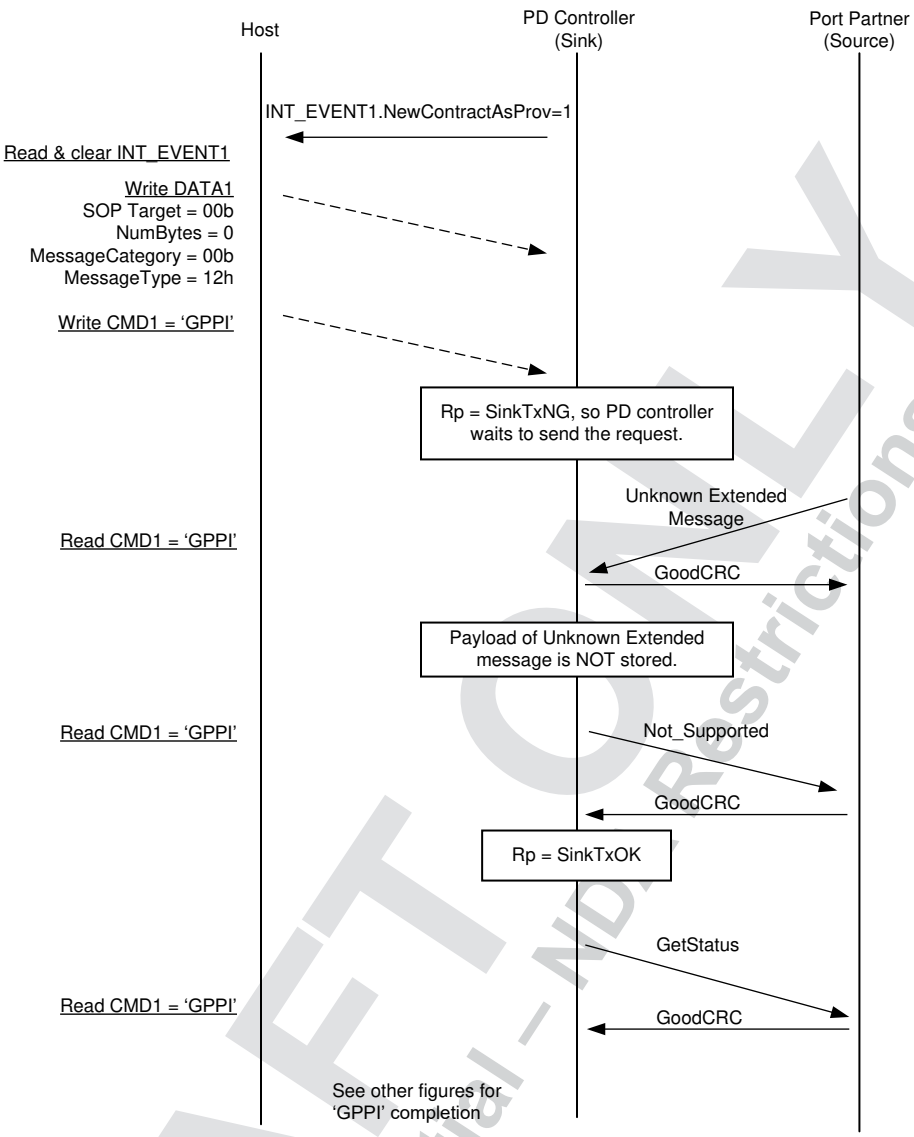


Figure 4-3. 'GPPI' Interrupted by an Unknown Message

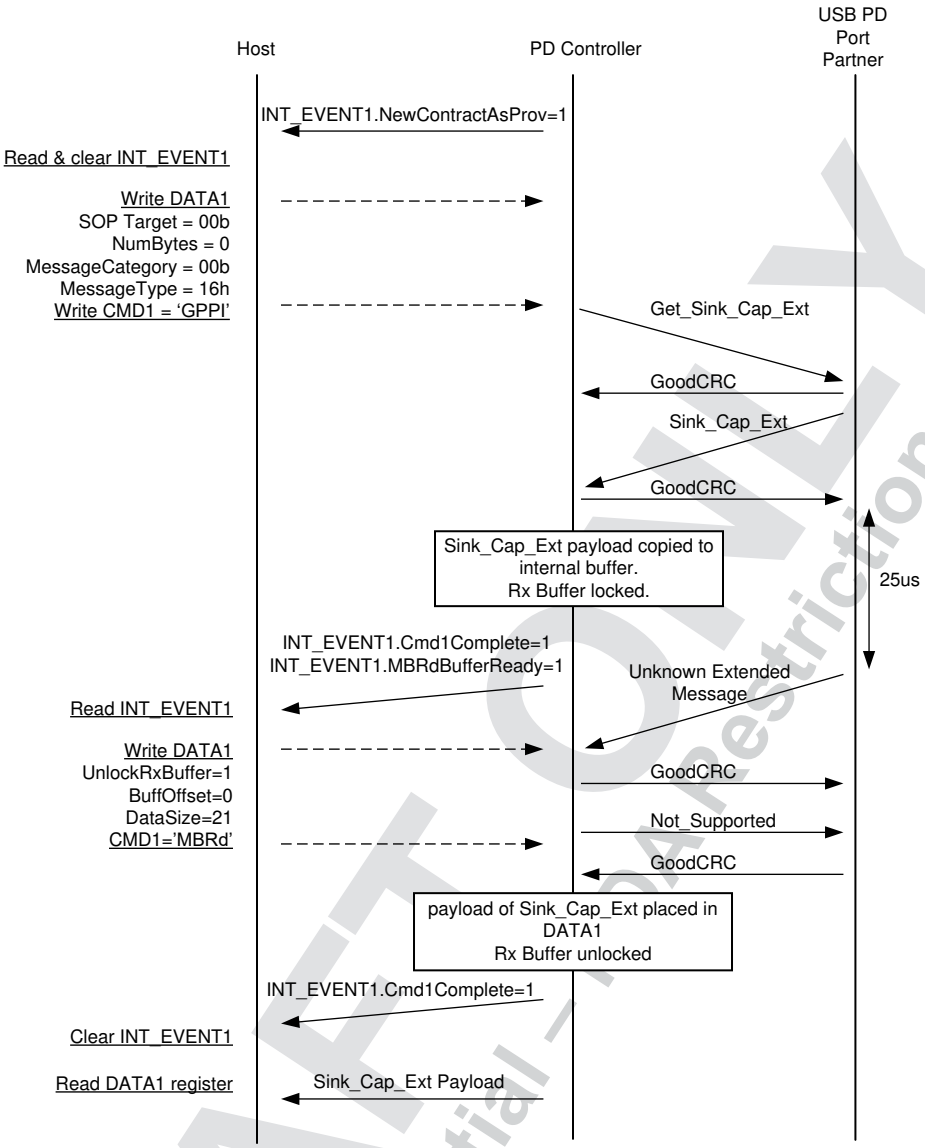


Figure 4-4. 'GPPI' Interrupted by an Unknown Extended Message

4.4.8 'SSrC' - PD Send Source Capabilities

Table 4-12. 'SSrC' - PD Send Source Capabilities

Description	The 'SSrC' Task instructs the PD Controller to send a SourceCapabilities message at the first opportunity while maintaining policy enginecompliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'SSrC' Task completes either when the Sink Capabilities message GoodCRC is received or the Task otherwise fails. The 'SSrC' Task shall be considered rejected if: • PD Controller is not in a Source role. The 'SSrC' Task shall be considered timed-out if: • The Source Capabilities message was sent but no GoodCRC was received. The 'SSrC' Task shall be considered successful if: • The Source Capabilities message was sent and a GoodCRC is received.
Side Effects	Other registers can change as a result of the contract negotiation that begins with the new Source Capabilities message.
Additional Information	None

4.4.9 'DRST' - PD Data Reset

Table 4-13. 'DRST' - Execute a Data Reset per USB specifications

Description	The 'DRST' Task instructs PD Controller to issue Data Reset PD message at the first opportunity while maintaining policy engine compliance.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	This Task shall be rejected if: • The negotiated specification revision is less than 3.0 (PD3_STATUS.portNegotiatedSpecRev < 10b). This Task shall time-out if: • If the expected response from the Port Partner is not received within the time allowed by the USB PD spec. This Task shall complete successfully if: • The PD controller receives an Accept message in response to the transmitted Data Reset message.
Side Effects	Unless this Task is rejected, it will cause the PD controller to transmit a Data Reset USB PD message and begin the Data Reset process per the USB PD requirements.
Additional Information	The Data Reset process can lead to Error Recovery and reset of the connection if the Port Partner does not respond as expected.

4.4.10 'MBRd' - Message Buffer Read

Table 4-14. 'MBRd' - Read from PD message buffer.

Description	**The MBRd Task instructs the PD Controller to read data from the extended message buffer previously received from the Port Partner.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	23	Reserved	Reserved (Write as 0).	
	22	UnlockRxBuffer	This input controls whether or not the PD controller unlocks its internal buffer after this Task is completed. It is recommended to unlock the internal buffer as soon as possible to make room for other incoming messages. It is important that the host only set this bit to 1 after it has received an alert that the Rx Buffer is locked (that is INT_EVENTx.MBRdBufferReady asserted).	
			0b	Do not clear the internal buffer, another 'MBRd' Task can be used later.
			1b	Clear the internal buffer after this Task completes and the requested data is in the DATAx register.
	21:16	DataSize	Number of data bytes to be read in from the message buffer. Up to 62 bytes can be read at after.	
	15:0	BuffOffset	Buffer Offset. Values 0 to 259 are possible.	
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	511:16	DataByte1	First Byte of data read at BuffOffset.	
	15:0	MessageSize	Size of message in bytes.	
Task Completion	The MBRd Task completes after buffer data of DataSize at BuffOffset has been read from the message buffer.			
Side Effects	None			
Additional Information	This Task is required for the host to obtain the information from the response due to the usage of the 'GPPI' Task . The PD controller has a single buffer per port that is shared for these messages.			

4.4.11 'ALRT' - Send Alert Message

Table 4-15. 'ALRT' - Send a USB PD Alert message.

Description	**The ALRT Task instructs the PD Controller to issue a Alert message to the Port Partner at the first opportunity while maintaining policy engine compliance. Contents of the Alert message sent come from *TX_ADO* register (0x75).**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The Task will complete when the Alert message is sent and GoodCRC'ed or the Task is otherwise rejected. The 'ALRT' Task shall be considered rejected if: • A Not_Supported message is received in response to the Alert message. The 'ALRT' Task shall be considered timed-out if: • The Port Partner fails to respond within the time required by the PD specification. The 'ALRT' Task shall be considered successful if: • The Alert message is sent and GoodCRC'ed.
Side Effects	None
Additional Information	None

4.5 Alternate Mode Tasks

4.5.1 'AMEn' - PD send Enter Mode

Table 4-16. 'AMEn' - PD send Enter Mode

Description	**The PD controller will automatically send the Enter Mode Command for appropriate Alternate Modes discovered based in its configuration settings. For the normal PD state machine process of entering Alternate Modes, the Host does not need to interact. However, if the Host ever must manually exit an Alternate Mode, and then at a later time wants to re-enter an Alternate Mode, then this 4CC Task must be used. If the Alternate Mode trying to be re-entered requires any cable negotiation (SOP', SOP'') in addition to negotiation with the other USB-C port (SOP), then the 'AMEn' Task will automatically negotiate the Alternate Mode with all the required SOP* targets.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	Bytes 2-3: AMEn SVID		
	15:0	SVIDTarget	SVID to use for Enter Mode SVDM Task.
	Byte 1: AMEn Task Header		
	7:5	ObjPos	Object Position of Mode to enter. A value of 111b will result in the Task being rejected. Any other value will cause the PD Controller to send an Enter Mode SVDM command to the requested SOPTarget. The host must not use the value of 000b.
	4:0	Reserved	Reserved (write 0).
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.		
Task Completion	The 'AMEn' Task completes when the Enter Mode SVDM command is delivered and a GoodCRC is received and an ACK Response is received, or the Task is otherwise rejected or times-out. If PD policy does not currently allow an SVDM to be sent (for example no Explicit Contract has been achieved) this Task will wait until PD policy allows the SVDM to be sent. The PD spec currently does not allow a BUSY response to an Enter Mode SVDM command, however if PD Controller receives a BUSY Response the 'AMEn' Task will remain active and continue to retry the Enter Mode SVDM command.		
Side Effects	Assuming the 'AMEn' Task succeeds in sending the Enter Mode SVDM command and receives a SVDM Response, PD Controller will update the *STATUS* register (0x1A) to indicate that a Mode is active. For SVIDs and Modes that PD Controller supports it will also update the appropriate VID/SID Status and *Data Status* registers (for example the DPModeActive field in *DP SID Status* when a SVDM ACK is received to the DP SID Enter Mode Command for the DisplayPort Object Position). As each SVDM Response is received it will be stored in the *RX_OTHER_VDM* register (0x4F) as usual, allowing the Host to perform any additional processing of the SVDM Response. Note that if ObjPos is set to 000b Enter Mode SVDM commands can be sent to multiple SOP* Ordered Sets, meaning multiple Enter Mode SVDM Responses can be received, only the final response (most likely SOP because cable mode entry is generally done first) will remain in the *RX VDM* register.The 'AMEn' Task can be sent to a SVID and Mode that PD Controller does not recognize. In this case PD Controller will update the ModeEntered field in the *Status* register (assuming the Enter Mode was ACKed) and store the SVDM Response in the *RX VDM* register, but no other register updates will be made because PD Controller does not have any register fields that pertain to the requested SVID / Mode.		
Additional Information	None		

4.5.2 'AMEx' - PD send Exit Mode

Table 4-17. 'AMEx' - PD send Exit Mode

Description	**The PD Controller will automatically discover and enter into Alternate Modes according to its configuration settings. It will also exit Alternate Modes on its own whenever needed to maintain PD compliance. However, the Host can command the PD controller to exit the Alternate Mode using this Task. After an Alternate Mode has been exited using 'AMEx', then the PD controller will only enter the Alternate Mode if commanded to through 'AMEn'. When using the 'AMEx" Task to exit an Alternate Mode, all SOP* targets that require an Exit Mode SVDM command to properly exit the Alternate Mode will be sent an Exit Mode SVDM command.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	Bytes 2-3: AMEx SVID		
	15:0	SVIDTarget	SVID to use for Exit Mode SVDM command.
	Byte 1: AMEx Task Header		
	7:5	ObjPos	Object Position of Mode to exit. If 111b PD Controller will use 111b in its Exit Mode SVDM command to exit all Modes associated with the SVID. SOPTarget must be 11b when this option is used. 000b is Reserved and the 'AMEx' Task will be rejected if used.
	4:0	Reserved	Reserved (write 0).
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.		
Task Completion	The 'AMEx' Task completes when the Exit Mode SVDM command(s) are delivered and a GoodCRC is received and an ACK Response is received, or the Task is otherwise rejected or times-out. There must be no reason for PD policy to prevent the SVDM to be sent or else a Mode must not have been able to be entered in the first place. The PD spec currently does not allow a BUSY response to an Exit Mode SVDM command, however if PD Controller receives a BUSY Response the 'AMEx' Task will remain active and continue to retry the Exit Mode SVDM command.		
Side Effects	Assuming the 'AMEx' Task succeeds in sending the Exit Mode SVDM command(s) and receives a SVDM Response PD Controller will take the appropriate action for exiting the Mode. The PD Controller will also update the appropriate VID/SID Status and *Data Status* registers (for example the DPModeActive field in *DP SID Status* when a SVDM ACK is received to the DP SID Exit Mode Command for the DisplayPort Object Position). As each SVDM Response is received it will be stored in the *RX_OTHER_VDM* register (0x4F) as usual, allowing the Host to perform any additional processing of the SVDM Response. Note that because the PD controller will send Exit Modes messages on all SOP targets as appropriate, the SOP' and SOP" Exit Mode SVDM Responses can be overwritten by additional Exit Mode SVDM Responses, because the last Exit Mode is sent to SOP, its SVDM Response will be the final value in the *RX VDM* register.		
Additional Information	None		

4.5.3 'AMDs' - PD Start Alternate Mode Discovery

Table 4-18. 'AMDs' - Start discovery process

Description	The 'AMDs' Task instructs PD Controller to start the Alternate ModeDiscovery process.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	This task will complete after the PD controller has sent the Discover Identity, Discover SVIDs, and Discover Modes messages that take place during that Alternate Mode Discovery process, or when the task is otherwise rejected. The 'AMDs' Task shall be considered rejected if: • Not a DFP for PD2.0 operation. • The Discover Identity message was sent and GoodCRC'ed and a NAK response was received. • The Discover SVIDs message was sent and GoodCRC'ed and a NAK response was received. The 'AMDs' Task shall be considered successful if: • Both the Discover Identity and the Discover SVIDs messages were sent and GoodCRC'ed, and ACK Responses were returned for both of them.
Side Effects	As a part of the Alternate Mode Discovery process, the DISCOVERED_SVIDS register (0x21), RX_IDENTITY_SOP register (0x48), RX_IDENTITY_SOPp register (0x49), USER_VID_STATUS register (0x57), DP_SID_STATUS register (0x58), CUSTOMD_STATUS (0x5A) and INTEL_VID_STATUS register (0x59) can be updated. Which registers get updated will depend on how many of the Alternate Mode Discovery process PD message successfully get responses, which also influences whether or not the Task returns it completed successfully or not in the Output DATAx register
Additional Information	None

4.5.4 'GCdm' - Get Custom Discovered Modes

Table 4-19. 'GCdm' - Get custom discovered modes

Description	After a successful 'GCdm' Task, PD Controller returns a list of VDOs along with their respective object position.		
INPUT DATAX	**Bit**	**Name**	**Description**
	7:0	Reserved	Reserved
	23:8	SVID	SVID
OUTPUT DATAX	**Bit**	**Name**	**Description**
	31:0	VDOMode1	VDO for Mode 1
	39:32	VDOMode1Pos	Object Position for Mode 1
	71:40	VDOMode2	VDO for Mode 2
	79:72	VDOMode2Pos	Object Position for Mode 2
	111:80	VDOMode3	VDO for Mode 3
	119:112	VDOMode3Pos	Object Position for Mode 3
	151:120	VDOMode4	VDO for Mode 4
	159:152	VDOMode4Pos	Object Position for Mode 4
	191:160	VDOMode5	VDO for Mode 5
	199:192	VDOMode5Pos	Object Position for Mode 5
	231:200	VDOMode6	VDO for Mode 6
	239:232	VDOMode6Pos	Object Position for Mode 6
	271:240	VDOMode7	VDO for Mode 7
	279:272	VDOMode7Pos	Object Position for Mode 7
Task Completion	The 'GCdm' Task completes when Output is updated with VDO modes and positions.		
Side Effects	None		
Additional Information	This 'GCdm' Task does not initiate sending of any USB PD messages. Instead, it just returns information gathered during the discovery phase automatically done by the PD controller. Therefore, it must not be issued until INT_EVENTx.DiscoverModeComplete has been asserted. The PD controller does not generally discover modes for a SVID that is disabled, so this 'GCdm' task must only be issued with a SVID that has been enabled such as USER_VID_CONFIG.User_AltMode_SVID_Value when USER_VID_CONFIG.UserVidEnabled is asserted.		

4.5.5 'VDMs' - PD send VDM

Table 4-20. 'VDMs' - PD send VDM

Description	The 'VDMs' Task instructs PD Controller to send a Vendor DefinedMessage (VDM) at the first opportunity while maintaining policy enginecompliance.			
INPUT DATAX	**Bit**	**Name**	**Description**	
	Byte 31: Initiator Wait State Timer Configuration			
	7:0	InitiatorWaitTimer	Configurable Initiator Wait State Timer. Please note, this timer is only used if the InitiatorResponder bit in byte 30 is set to 1b. The PD controller will wait for this amount of time for a response. (1ms per LSB)	
	Byte 30: VDMs Configuration			
	7:1	Reserved		
	0	InitiatorResponder	The VDMs can be sending a response or initiating a sequence.	
			0b	This is a response so the PD controller will transmit the message regardless of the collision avoidance Rp value. Example, an ACK message is responding.
			1b	This is initiating a VDM sequence, so the PD controller will follow USB PD collision avoidance requirements. Example, a REQ message is initiating a new VDM sequence.
	Bytes 26-29: VDO #7 (treated as 32-bit little endian value)			
	31:0	VDO7	Contents of seventh VDO, if applicable.	
	Bytes 22-25: VDO #6 (treated as 32-bit little endian value)			
	31:0	VDO6	Contents of sixth VDO, if applicable.	
	Bytes 18-21: VDO #5 (treated as 32-bit little endian value)			
	31:0	VDO5	Contents of fifth VDO, if applicable.	
	Bytes 14-17: VDO #4 (treated as 32-bit little endian value)			
	31:0	VDO4	Contents of fourth VDO, if applicable.	
	Bytes 10-13: VDO #3 (treated as 32-bit little endian value)			
	31:0	VDO3	Contents of third VDO, if applicable.	
	Bytes 6-9: VDO #2 (treated as 32-bit little endian value)			
	31:0	VDO2	Contents of second VDO, if applicable.	
	Bytes 2-5: VDO #1 (treated as 32-bit little endian value)			
	31:0	VDO1	Contents of first VDO (VDM Header if SVDM).	
	Byte 1: VDMs Task Header			
	7	AMIntrusiveModeResponse	When set this message satisfies a pending AMIntrusiveMode interaction, PD Controller will stop sending BUSY Responses to the last received SVDM command.	
	6	Reserved	write as 0b	
	5:4	SOPTarget	Ordered Set to send VDM to.	
			00b	SOP.
			01b	SOP'.
			10b	SOP".
			11b	SOP*_Debug (SOP'_Debug for Source, SOP"_Debug for Sink).
	3	Version	To maintain backwards compatibility, this field is used to indicate whether bytes 30-31 are ignored or used.	
			0b	VDMs version 1 (ignores bytes 30-31). The PD controller always waits 30ms for a response.
			1b	VDMs version 2 (implements bytes 30-31)
	2:0	NumDOs	Number of VDOs to transmit (1-7), includes VDM Header for SVDMs.	
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.			

Table 4-20. 'VDMs' - PD send VDM (continued)

Description	The 'VDMs' Task instructs PD Controller to send a Vendor DefinedMessage (VDM) at the first opportunity while maintaining policy enginecompliance.
Task Completion	The 'VDMs' Task completes when the VDMs is delivered and a GoodCRC is received or the appropriate number of retries have been attempted without a GoodCRC, or the Task is rejected. This Task does not wait for a VDM response because there is no guarantee of a response especially for Unstructured VDMs. The 'VDMs' Task shall be considered rejected if: • NumDOs is set to 0. • PD policy does not allow a VDM to be sent at this time. • DFP/UFP is instructed to send to SOP' when not appropriate (for example DFP during Implicit Contract following a PR_Swap) or a UFP is instructed to send to SOP". The 'VDMs' Task shall be considered timed-out if: • The VDM was sent but no GoodCRC was received. The 'VDMs' Task shall be considered successful if: • The VDM was sent and a GoodCRC was received.
Side Effects	If the 'VDMs' Task succeeds in sending the requested VDM, PD Controller is not aware of the VDM it sent, so it will not be expecting a response. All incoming VDMs that are not Initiator Attention messages will be stored in the *RX_OTHER_VDM* register (0x4F) regardless of PD Controller 's current state so the response can be processed by the Host, but it will not otherwise be processed by PD Controller . For example, if VDMs is used to send a Discover Identity SVDM Command to SOP', the *RX Identity SOP'* register does not get updated because PD Controller 's PD state machine was not in the proper state to receive this response. There can be some delay before the VDM is transmitted. See the table below for details.
Additional Information	The host must not send back-to-back 'VDMs' command to quickly. In particular, if the SOPTarget was not SOP, then the host shall wait for at least 35 ms while the PD controller awaits a response from the cable. It is recommended that the host wait 35 ms in between consecutive 'VDMs' messages for SOPTarget=SOP as well.

The table below summarizes the situations for which the PD controller will delay transmission of the VDM.

Table 4-21. Description of delay before sending the VDM for 'VDMs'.

PD_STATUS	PD3_STATUS	VDO1[15]	VDO1[7]	VDO1[6]	Description of Delay
PresentPDRole	**portNegotiatedSpecRev**				
X	01b (PD2)	X	X	X	No Delay
0b (Sink)	10b (PD3)	X	X	X	Delayed until PD_STATUS.CCPullUp=11b (SinkTxOK).
1b (Source)		0b(1)	X	X	The PD controller will act as the Atomic Message Sequence Initiator. USB PD collision avoidance requirements can cause a delay of tSinkTx before the VDM is sent.
		1b(2)	0b	0b	
			0b	1b	No delay
			1b	0b	
			1b	1b	

(1) Unstructured VDM.
(2) Structured VDM (SVDM)

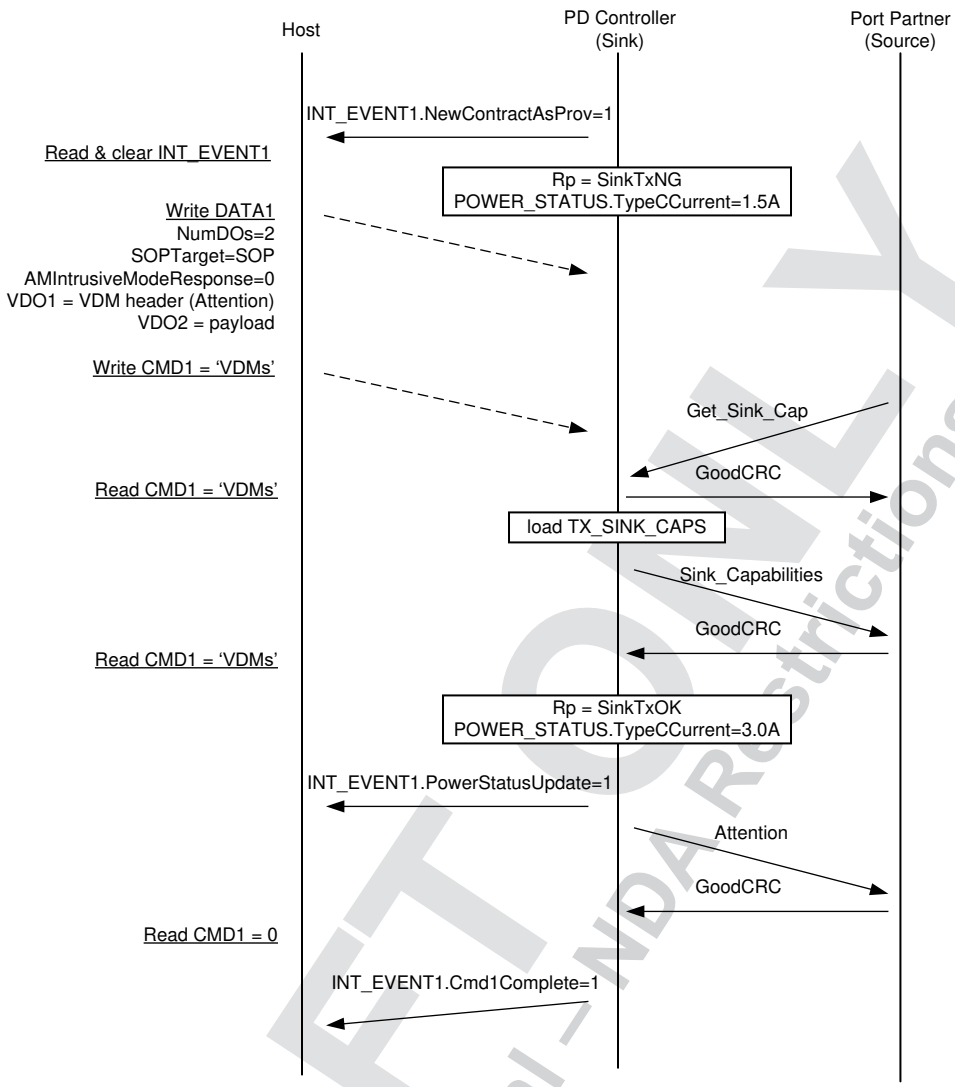


Figure 4-5. 'VDMs' example sequence.

4.6 Power Switch Tasks

4.6.1 'SRDY' - System ready to sink power

Table 4-22. 'SRDY' - System ready to sink power

Description	The 'SRDY' Task instructs PD Controller to enable a power switch forinput.			
INPUT DATAX	**Bit**	**Name**	**Description**	
	Byte 1: SRDY Task Header			
	7:3	Reserved	Reserved (write 0).	
	2:0	SwitchSelect	Specifies which switch will be enabled. Switches must be configured as inputs that wait for SYS_RDY Task (SRDY).	
			000b	PP1 (PP_5V1)
			001b	PP2 (PP_5V2)
			010b	PP3 (PP_EXT1)
			011b	PP4 (PP_EXT2)
			100b - 101b	Reserved
			110b	Automatically-selected by the PP*Config field in the GLOBAL_SYSTEM_CONFIG register (0x27) . Assumes a single switch is configured as an input. This allows a Host to issue this Task without having to know which switch that is.
			111b	Automatically-selected by PD Controller policy. Used primarily to re-enable a switch that has been turned off for some reason.
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.			
Task Completion	The 'SRDY' Task completes when the selected input switch is successfully enabled or the Task otherwise fails.			
Side Effects	When 'SRDY' completes power switches can have been re-configured, which will affect the Status register.			
Additional Information	When this 'SRDY' Task is issued, the selected switch will enable with soft-start. The turn-on time of the switch and the system load must be considered along with the Safe-Operating Area (SOA) of the switch. In most cases, the system must draw a very small load until the switch is enabled.			

4.6.2 'SRYR' - SRDY reset

Table 4-23. 'SRYR' - SRDY reset

Description	**The 'SRYR' Task instructs PD Controller to disable the currently-enabled input switch, if there is one. This command applies only to the port to which it is addressed (through I2C slave address). The sink port for the other port (for dual-port controllers) is not affected.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'PBMs' Task completes after output has a valid PatchStartStatus. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.
Side Effects	When the 'PBMs' is successful, the second slave address will be set to the input value.
Additional Information	The host can only issue a 'PBMs' Task to the I2C_EC port of the PD controller. If the host issues 'PMBs' a second time, then the PD controller ignores the DATAX input, restarts the burst-mode timer, and resets the pointer to the beginning of the patch space in RAM. If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMs' Task.

4.7 Patch Bundle Update Tasks

The following tasks are used for updating a Patch Bundle.

4.7.1 'PBMs' - Start Patch Burst Mode Download Sequence

Table 4-24. 'PBMs' - Start Patch Burst Download Sequence

Description	**The 'PBMs' Task starts the patch loading sequence. This Task initializes the firmware in preparation for a patch bundle load sequence and indicates what the patch bundle will contain.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	Byte 6: Burst Mode Timeout		
	7:6	Reserved	
	5:0	Timeout value	Timeout value for this task. A non-zero value must be used, it is recommended to always use 0x32 in this field (5 seconds) (LSB of 100ms).
	Byte 5: I2C slave for downloading patch.		
	7	Reserved	
	6:0	I2C Slave Address	The following slave addresses are not valid: • 0x00 • The I2C1s slave address of any port selected using the ADCINx pins. Refer to data-sheet.
	Bytes 0-3: Low Region Binary bundle size in of bytes: [Byte4, Byte3, Byte2, Byte1]		
	39:32	Byte4 of bundle size	
	31:24	Byte3 of bundle size	
	23:16	Byte2 of bundle size	
	15:8	Byte1 of bundle size	
OUTPUT DATAX	**Bit**	**Name**	**Description**
	7:0	PatchStartStatus	Status of the patch start.
			0x00 Patch start success
			0x04 Invalid bundle size
			0x05 Invalid slave address
			0x06 Invalid Timeout value
Task Completion	The 'PBMs' Task completes after output has a valid PatchStartStatus. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.		
Side Effects	When the 'PBMs' is successful, the second slave address will be set to the input value.		
Additional Information	The host can only issue a 'PBMs' Task to the I2C_EC port of the PD controller. If the host issues 'PMBs' a second time, then the PD controller ignores the DATAX input, restarts the burst-mode timer, and resets the pointer to the beginning of the patch space in RAM. If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMs' Task.		

4.7.2 'PBMc' - Patch Burst Mode Download Complete

Table 4-25. 'PBMc' - Patch Burst Download Complete

Description	The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.			
INPUT DATAX	None			
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	319:288	acCalculatedCRC	The CRC calculated in FW for the configuration data.	
	287:256	acTransferredCRC	The CRC transferred along with the configuration data	
	255:240	Reserved	reads as 0	
	239:224	acIndicatedDataSize	The indicated DataSize in the transferred configuration data.	
	223:216	acHeaderVersion	The indicated header version in the transferred configuration data.	
	215:208	acFailCode	An error code indicating why the app config data failed to apply, if it failed to apply	
			0x00	AC_FAIL_NONE: No failure
			0x01	AC_FAIL_WRONG_HEADER_VERSION: The header version is expected to be 1 and was not
			0x02	AC_FAIL_TOO_MUCH_DATA: The DataSize field indicates that you are trying to load more configuration data that there is allocated SRAM for
			0x03	AC_FAIL_CRC_CHECK_FAIL: The CRC comparison failed
	207:200	acState	The current internal state of the AppConfig state machine	
			0x00	AC_NODATA: No configuration data found yet, because we haven't started looking
			0x01	AC_LOADING_DEFAULT: Attempting to load configuration data from a factory default
			0x02	AC_LOADING_SRAM: Attempting to load configuration data from SRAM
			0x03	AC_LOADING_FLASH: Attempting to load configuration data from Flash
			0x04	AC_LOADING_I2C: Attempting to load configuration data from I2C
			0x05	AC_LOADING_DONE: Done loading configuration data, we found valid data
			0x06	AC_ERROR: A generic error state
			0x07	AC_DONE_SUCCESS: Completely done with the app customization process and the records were applied successfully.
			0x08	AC_DONE_FAIL: Completely done with the app customization process and the records were not applied
	199:192	configBundleGood	1 if the top-level state machine found a valid configuration bundle, otherwise 0.	
	191:160	rpRomVersionExpected	The romVersionExpected in the transferred bundle's patch header	
	159:144	rpBundleTotalSize	The bundleTotalSize in the transferred bundle's patch header	
	143:128	rpBundleFlags	The bundleFlags in the transferred bundle's patch header	
	127:96	rpPatchBodyCrc	The patchBodyCrc in the transferred bundle's patch header	
	95:64	rpPatchHeaderCrc	The patchHeaderCrc in the transferred bundle's patch header	

Table 4-25. 'PBMc' - Patch Burst Download Complete (continued)

Description	**The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.**			
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	55:48	rpBundleSignature	The bundleSignature in the transferred bundle's patch header	
	47:40	rpState	The current internal state of the RomPatch state machine.	
			0x00	RP_NOPATCH: No patch has been loaded
			0x01	RP_LOADING: In the process of loading patch data
			0x02	RP_LOADINGDONE: All patch data has been received
			0x03	RP_RUNNING: A patch has been loaded and is running. Could also indicate that a NULL patch is active.
			0x04	RP_EARLYLOAD_SKIPPED: Indicates that the early boot process does not need to wait for a patch over I2C
			0x05	RP_UARTBOOTED: Checking for a patch in RAM
			0x06	RP_ERROR: A generic error state
	39:32	patchBundleGood	0x01 if the top-level state machine found a good ROM patch, otherwise 0x00.	
	31:24	AppConfigPatchCompleteStatus	0x00	
			0x40	Warning
			0x80	Failure
	23:16	DevicePatchCompleteStatus	A return code indicating whether the RomPatch state machine executed successfully. This value is always valid, and reflective of the internal state of the RomPatch mechanism, but must only be considered if the bundle transferred did in fact include patch data.	
			0x00	Success
			0x20	Not ready
			0x40	Not a patch
			0x41	Patch header checksum mismatch
			0x42	Patch not compatible with this version of ROM
			0x43	Patch code checksum mismatch
			0x44	Null patch received
			0x45	Error patch received
	15:8	cpReturn	Always returns success, there is no way for it to fail.	
	Byte 1: Return Code			
	7:4	rpReturnIndicator	The most significant nibble of the rpReturn value.	
			0x0	Success
			0x2	Informational
			0x4	Warning
			0x8	Error
	3:0	acReturnIndicator	The most significant nibble of the acReturn value.	
			0x0	Success
			0x2	Informational
			0x4	Warning
			0x8	Error
Task Completion	The 'PBMc' Task completes as output has a valid DevicePatchCompleteStatus and AppConfigPatchCompleteStatus. This Task is rejected if the DATAX input does not contain the total patch size. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.			

Table 4-25. 'PBMc' - Patch Burst Download Complete (continued)

Description	**The 'PBMc' Task ends the patch loading sequence. Send this Task after all patch data has been transferred. This Task will initiate the CRC check on the binary patch data that has been transferred, and if the CRC is successful, the patch_init function contained within the patch will be executed.**
Side Effects	Before this Task completes it will change the I2C slave address from the patch address back to the normal value. Upon successful completion of this Task the PD controller will change the MODE register (0x03) to 'APP ' and move to the application mode.
Additional Information	When the CMDx register goes to 0 check the Output DATAX register for status. If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMc' Task.

4.7.3 'PBMe' - End Patch Burst Mode Download Sequence

Table 4-26. 'PBMe' - Patch Burst Mode Exit

Description	The 'PBMe' Task ends the patch loading sequence. This Task instructs the PD controller to complete the patch loading process.
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'PBMe' Task completes after it has ended the patch loading sequence. If MODE register (0x03) is equal to 'APP ', then this Task will be rejected.
Side Effects	When the 'PBMe' is successful, the second slave address will be restored to the value configured by the ADCINx pins. The PD controller leaves the MODE register (0x03) as 'PTCH' and will wait for the patching process to restart.
Additional Information	If the MODE register is 'APP ' indicating that the PD controller is in the APP mode, then it will reject the 'PBMe' Task.

4.7.4 'GO2P' - Go to Patch Mode

Table 4-27. 'GO2P' - Forces PD controller to return to 'PTCH' mode and wait for patch over I2C.

Description	The 'GO2P' Task causes the PD controller to re-enter the patch mode (MODE = 'PTCH').
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'GO2P' Task completes after the PD controller has re-entered the patch mode. • If the PD controller has re-entered the patch mode and the MODE register reads as 'PTCH'. The 'GO2P' Task is considered rejected if: • The PD controller did not enter the 'APP ' mode without receiving a patch over I2C. • BOOT_STATUS.PatchConfigSource does not read as 3h or 4h.
Side Effects	When the 'GO2P' Task is successful, the MODE register will read as 'PTCH' and the USB PD PHY will be disabled. The PD Controller can temporarily NAK I2C transactions. The host must wait for the IRQ signal to assert (because INT_EVENT1.ReadyForPatch is asserted), and then push the patch as soon as possible.
Additional Information	The 'GO2P' Task must only be used when the ADCINx configuration option NegotiateHighVoltage is used.

4.7.5 'FLrd' - Flash Memory Read

Table 4-28. 'FLrd' - External EEPROM Read

Description	The 'FLrd' Task reads the flash at the specified address.		
INPUT DATAX	**Bit**	**Name**	**Description**
	31:0	Flash Address	Flash Address
OUTPUT DATAX	**Bit**	**Name**	**Description**
	127:0	Memory Contents	Memory contents (little-endian).
Task Completion	The 'FLrd' Task completes after selected memory locations are loaded.		
Side Effects	The PD controller ignores the I2C3m_IRQ pin until this Task is completed.		
Additional Information	None		

4.7.6 'FLad' - Flash Memory Write Start Address

Table 4-29. 'FLad' - External EEPROM Start Address

Description	The 'FLad' Task sets start address in preparation the flash write.		
INPUT DATAX	**Bit**	**Name**	**Description**
	31:0	Flash Address	Flash address (treated as 32-bit little-endian value).
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.		
Task Completion	The 'FLad' Task completes after selected memory address is loaded.		
Side Effects	The PD controller ignores the I2C3m_IRQ pin until this Task is completed.		
Additional Information	None		

4.7.7 'FLwd' - Flash Memory Write

Table 4-30. 'FLwd' - External EEPROM Memory Write

Description	**The 'FLwd' Task writes data beginning at the flash start address defined by the 'FLad' Task. The address is auto-incremented.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	511:0	Flash Address	Up to 32 bytes of flash data.	
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	7:0	ReturnCode	Status of write.	
			0x00h	Flash memory write successful
			0xFFh	Error, flash is busy
Task Completion	The 'FLwd' Task completes after selected the flash is written.			
Side Effects	The PD controller ignores the I2C3m_IRQ pin until this Task is completed.			
Additional Information	None			

4.7.8 'FLvy' - Flash Memory Verify

Table 4-31. 'FLvy' - External EEPROM Verify

Description	**The 'FLvy' Task verifies if the patch/configuration is valid.**			
INPUT DATAX	**Bit**	**Name**	**Description**	
	31:0	Flash Address	Flash Address	
OUTPUT DATAX	**Bit**	**Name**	**Description**	
	7:0	ReturnCode	0x00h	The patch/configuration is valid.
			0x01h	The patch/configuration is not valid.
Task Completion	The 'FLvy' Task completes after header is checked and validated.			
Side Effects	The PD controller ignores the I2C3m_IRQ pin until this Task is completed.			
Additional Information	None			

4.8 System Tasks

4.8.1 'ABRT' - Abort current Task

Table 4-32. 'ABRT' - Abort current task

Description	**The 'ABRT' Request is not exactly a Task of its own, it is a value that when written to a CMDX register can affect a long-running Task that is currently running on that CMDX interface. Normally a Host is not allowed to write anything to CMDX if it reads back as anything other than 0 or '!CMD', but the 'ABRT' value can always be written to CMDX.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	As the 'ABRT' Request is not actually a task it is difficult to say when it completes. If no Task was active the top-level command processing loop will simply ignore it and clear CMDX. If a Task is running then 'ABRT' will remain in CMDX until the Task completes (either because it completed normally or because it detected the 'ABRT' and aborted).
Side Effects	Writing 'ABRT' to a CMDX register must have no side effects other than canceling the active Task. The aborted Task must perform any necessary cleanup.
Additional Information	None

4.8.2 'ANeg' - Auto Negotiate Sink Update

Table 4-33. 'ANeg' - Re-evaluate the auto-negotiate sink register

Description	**The 'ANeg' Task instructs PD Controller to re-evaluate the *Auto Negotiate Sink* register (0x37). If the re-evaluation produces a different RDO than the Active Contract RDO then a new Request message is sent.**
INPUT DATAX	None
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.
Task Completion	The 'ANeg' Task completes after the new RDO is calculated and PD Controller either decides to send a new Request message (and that message is sent and the GoodCRC received) or determines that no Request is necessary. The task is rejected of the PD controller is not in a sink power role.
Side Effects	The side effects include a new PD contract negotiation and updates to the associated registers.
Additional Information	None

4.8.3 'DBfg' - Clear Dead Battery Flag

Table 4-34. 'DBfg' - Clear Dead Battery Flag

Description	The 'DBfg' Task is used to clear the dead battery flag. This Task does not disable the PP_EXT input switch that can have been enabled during dead battery operation.
INPUT DATAX	None
OUTPUT DATAX	None
Task Completion	The 'DBfg' Task completes after the effects of clearing the Dead Battery Flag are complete.
Side Effects	The Dead Battery Flag causes the PD Controller to take specific actions, so clearing this flag will have side effects. PD Controller 's power input is forced to VBUS until the Dead Battery Flag is cleared, so executing this Task will change PD Controller 's power input.
Additional Information	None

There are several limitations placed on the PD controller while the Dead-Battery Flag is asserted (PowerPathStatus.PowerSource = 10b).

- Fast-Role swap is not supported (on either port).
- A Hard Reset will not be transmitted while in the sink role (on either port).
- VBUS is selected as the main supply for the PD controller, even if the 3.3 V input is present.
- The PD controller will reject PR_Swap requests to become source (on either port).
- The 2nd port in the PD controller that is unconnected will only offer the USB Type-C Default Rp (PortControl.TypeCCurrent is ignored) if it connects as a source.
- A port connected to a source will only act as a Type-C sink regardless of the configuration.
- If no Source Capabilities message is received after the boot process is complete (Status.ActingAsLegacy=11b), the PD controller will not send a Hard Reset until the Dead-Battery Flag is cleared even if the SinkWaitCapTimer expires.

4.8.4 'MuxR' - Error handling for I2C3m transactions

Table 4-35. 'MuxR' - Repeats transactions on I2C3m under certain conditions.

Description	'MuxR' - this task provides a way for the host to handle errors that occur on the I2C master port.		
INPUT DATAX	**Bit**	**Name**	**Description**
	15:9	Reserved	
	8	EnRetryOnSlaveAddrTbt	If this bit is asserted, the PD controller will use I2C3m to write the DATA_STATUS register with I2CMASTER_CONFIG.SlaveAddrTbt1 as the slave address. It will also repeat the write using I2CMASTER_CONFIG.SlaveAddrTbt2 as the slave address.
	7	EnRetryOnSlaveAddr8	If this bit is asserted, the PD controller will retry the last transaction on the I2C3m port that used I2CMASTER_CONFIG.SlaveAddr8 as the slave address.
	6	EnRetryOnSlaveAddr7	If this bit is asserted, the PD controller will retry the last transaction on the I2C3m port that used I2CMASTER_CONFIG.SlaveAddr7 as the slave address.
	5	EnRetryOnSlaveAddr6	If this bit is asserted, the PD controller will retry the last transaction on the I2C3m port that used I2CMASTER_CONFIG.SlaveAddr6 as the slave address.
	4	EnRetryOnSlaveAddr5	If this bit is asserted, the PD controller will retry the last transaction on the I2C3m port that used I2CMASTER_CONFIG.SlaveAddr5 as the slave address.
	3	EnRetryOnSlaveAddr4	If this bit is asserted, the PD controller will retry the last transaction on the I2C3m port that used I2CMASTER_CONFIG.SlaveAddr4 as the slave address.
	2	EnRetryOnSlaveAddr3	If this bit is asserted, the PD controller will retry the last transaction on the I2C3m port that used I2CMASTER_CONFIG.SlaveAddr3 as the slave address.
	1	EnRetryOnSlaveAddr2	If this bit is asserted, the PD controller will retry the last transaction on the I2C3m port that used I2CMASTER_CONFIG.SlaveAddr2 as the slave address.
	0	EnRetryOnSlaveAddr1	If this bit is asserted, the PD controller will retry the last transaction on the I2C3m port that used I2CMASTER_CONFIG.SlaveAddr1 as the slave address.
	OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.	
Task Completion	If the I2C master queue is full or if the I2C master is disabled, then this task is rejected. Otherwise, the task will complete successfully.		
Side Effects	One or more I2C transactions can be repeated on the I2C master port (I2C3m).		
Additional Information	If all bits in DATAX are set to zero when CMDx is written as 'MuxR', then the PD controller clears its history of the last events for slave addresses 1 to 8. If EnRetryOnSlaveAddrX is asserted and no transaction has occurred on that I2C address because the history was cleared, then the PD controller will not execute any I2C transaction on that slave address as there is no event to repeat. The contents of the last transaction on a given I2C slave address is defined through the App Config loaded as part of the patch bundle. The BINARYDATA_INDICES register (0x62) contains the various events that can occur on each slave address along with the payload for the transaction associated with each. When the 'MuxR' Task is executed, then for each EnRetryOnSlaveAddr* that is asserted it will be as if the last event for that slave address has occurred again.		

4.8.5 'Trig' - Trigger an Input GPIO Event

Table 4-36. 'Trig' - Emulate a GPIO input event

Description	The 'Trig' Task can be used to trigger an input GPIO Event (see for a list), The GPIO Event need not be assigned to any physical GPIO pin, so this allows implementing virtual input GPIO events.			
INPUT DATAX	**Bit**	**Name**	**Description**	
	15:8	GPIO Event	69d (45h)	MRESET: No assumption is made about the initial state of this virtual GPIO. No action is taken until 'Trig' is received.
			56d (38h)	I2C3_MASTER_IRQ_EVENT: No assumption is made about the initial state of this virtual GPIO. No action is taken until 'Trig' is received.
			47d (2Fh)	Prevent_High_Current_Contract_Event: This virtual GPIO is assumed to be high until 'Trig' is received. The GLOBAL_SYSTEM_CONFIG.EnableSPM bit must be asserted in order to use this virtual GPIO.
			42d (2Ah)	Retimer_SoC_OVR_Force_PWR_Event: This virtual GPIO is assumed to be low until 'Trig' is received with EdgeType set to 1b. This means that the Retimer_Force_PWR_Event_Port1 and Retimer_Force_PWR_Event_Port2 GPIO's are left in the state specified for them in GPIO_CONFIG.GPIOData until 'Trig' is received. INTEL_VID_STATUS.RetimerForcePower reflects the state of this virtual GPIO.
			34d (22h)	Fault_Input_Event_Port2: This virtual GPIO is assumed to be high until 'Trig' is received with EdgeType set to 0b.
			33d (21h)	Fault_Input_Event_Port1: This virtual GPIO is assumed to be high until 'Trig' is received with EdgeType set to 0b.
			else	The task will be rejected.
	7:1	Reserved		
	0	EdgeType	0b	Falling edge
			1b	Rising edge
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.			
Task Completion	This task completes successfully after the applicable actions for the GPIO event are executed. The task is rejected if the GPIO event is not a valid input GPIO event. This task must not be issued for a GPIO event that is assigned to a physical GPIO in the GPIO_CONFIG register.			
Side Effects	Depending upon the selected GPIO event various actions can be taken by the PD controller. Refer to the description of each GPIO event in .			
Additional Information	The PD controller executes the event handler for the rising or falling edge as given in the input of this command. Therefore, it is possible to execute consecutive rising edges or consecutive falling edges. Although, in most cases subsequent rising edges will not have any action, it is not recommended that the host issue consecutive 'Trig' tasks with the same EdgeType and GPIO Event #.			

4.8.6 'I2Cr' - I2C read transaction

Table 4-37. 'I2Cr' - Executes I2C read transaction on I2C3m.

Description	**The 'I2Cr' task can be used to cause the PD controller to read from a specified slave address and register offset using a I²C read transaction through the I2C3m_SDA and I2C3m_SCL pins.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	Byte 3: Number of bytes to read from the slave.		
	7:0	NumBytes	
	Byte 2: Register offset to use in the I2C read transaction.		
	7:0	RegisterOffset	
	Byte 1: Slave Address		
	7	Reserved	
	6:0	Slave to use for the transaction.	
OUTPUT DATAX	**Bit**	**Name**	**Description**
	Bytes 2-65: Data Bytes read from the slave (in order received)		
	511:0	Data	
	Byte 1: Standard Task Return Code. See also Table 4-1.		
Task Completion	The PD controller completes after it has succesfully read the specified number of bytes, or the I²C transaction terminated for some other reason.		
Side Effects	This task will cause the PD controller to issue a command on the I2C3m port. It can result in INT_EVENTx.I2CMasterNACKed being asserted.		
Additional Information	None		

4.8.7 'I2Cw' - I2C write transaction

Table 4-38. 'I2Cw' - Executes I2C write transaction on I2C3m.

Description	**The 'I2Cw' task can be used to cause the PD controller to write a particular I²C transaction using I2C3m_SDA and I2C3m_SCL.**		
INPUT DATAX	**Bit**	**Name**	**Description**
	Bytes 5-14: Payload for the I2C transaction		
	Byte 4: Register Offset for the I2C transaction		
	7:0	Register offset	
	Bytes 2-3: Length		
	15:8	Reserved	
	7:0	Number of bytes in the transaction payload.	
	Byte 1: Slave Address		
	7	Reserved	
	6:0	Slave to use for the transaction.	
OUTPUT DATAX	Byte 1: Standard Task Return Code. See also Table 4-1.		
Task Completion	The PD controller maintains a queue of transactions to send on the I2C3m port. If the PD controller has been configured to send transactions upon certain events, it is possible there is a transaction in the queue when the 'I2Cw' task is received. In that case the task will complete successfully after the transaction is inserted into the queue. If the PD controller fails to insert the task into the queue for any reason, the task is rejected. Therefore, when this task is completed succesfully it does not guarantee that the I2C transaction is complete. If possible, the host must use the 'I2Cr' 4CC task to confirm the write was successful.		
Side Effects	When successful, this task will cause the PD controller to issue a command on the I2C3m port. This can result in INT_EVENTx.I2CMasterNACKed being asserted.		
Additional Information	If the DATAX register is written with more than 14 bytes, all bytes beyond byte 14 are ignored. The PD controller has a limit on the maximum length of the I²C write transaction.		

5.1 PD Controller Application Customization

The PD Controller application binary can be pushed over I2C using the I2C_EC port, or the PD controller can read it from an external EEPROM at slave address 0x50 on the I2C3m port. The PD Controller application binary provides a way to customize and initialize the settings of the PD Controller. It allows for any register bit accessible through the Host Interface to be changed *before* the PD Controller application starts normal operation, to configure system-related settings that must be correct before any application decision is made. TI provides a GUI tool to create the PD Controller application binary.

5.2 Loading a Patch Bundle

The patch bundle can contain Application Customization data and a Patch binary that modifies the default application firmware in the PD controller. This section will describe how the host can load the patch bundle. The host uses the I2C_EC bus for all transactions related to loading the patch bundle. As noted in the flow diagram below, the I2C slave address varies depending upon which mode the PD controller is in. The Patch Burst Mode allows the host to push the Patch Bundle to multiple PD controllers simultaneously.

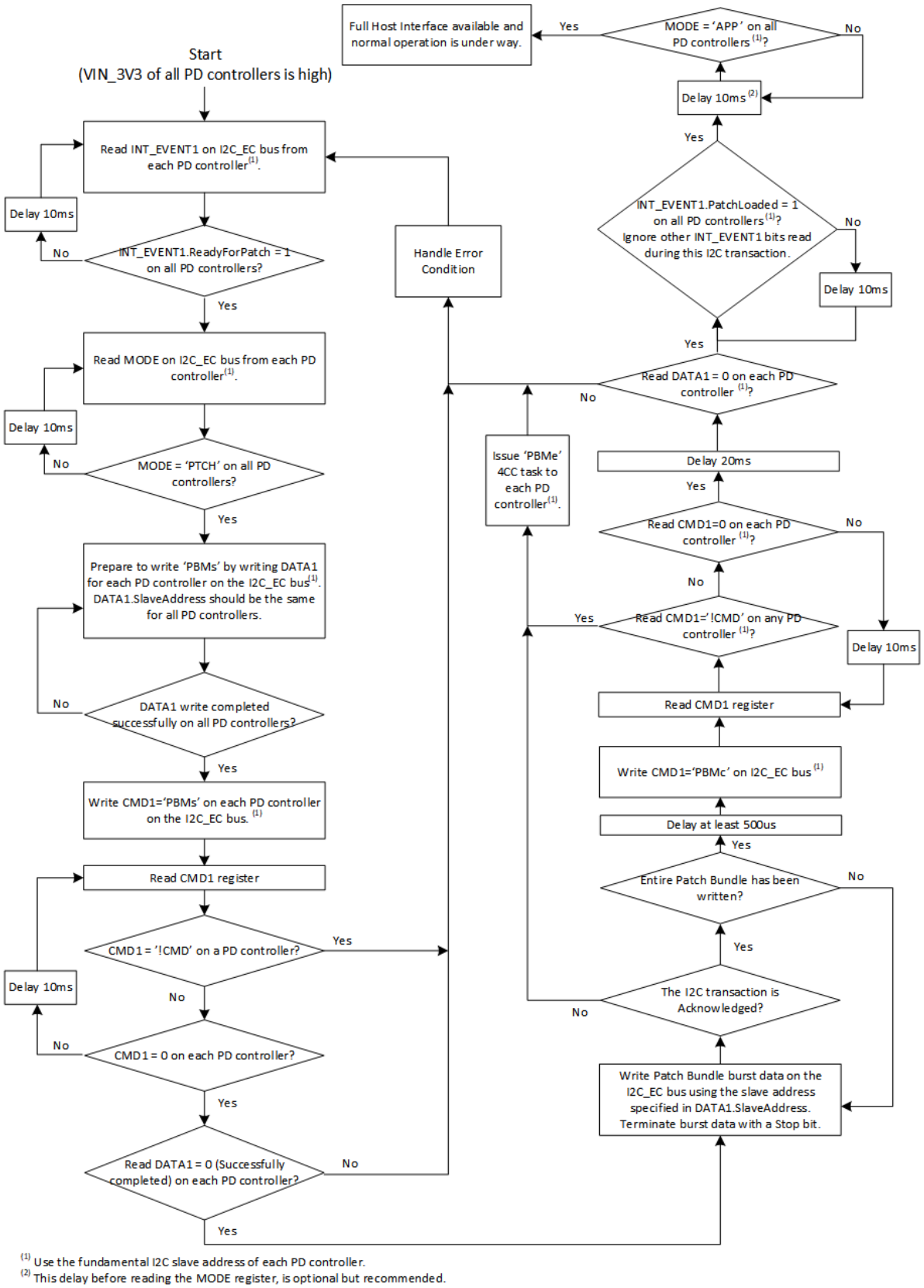
The following flow diagram illustrates the normal successful patch loading process. Other error handling steps can be necessary depending upon the nature of the errors encountered for a particular system. The EC can reset and restart the patch process by issuing a 'PBMe' 4CC Task.

The PD controller can listen for I2C transactions on two unique slave addresses on each I2C port. The following table summarizes the slave addresses in the different modes of operation. GLOBAL_SYSTEM_CONFIG for the I2C2s bus.

Table 5-1. Usage of slave addresses during different modes of operation.

MODE register read-back value	I2C_EC		I2C2s	
	Slave Address #1	Slave Address #2	Slave Address #1	Slave Address #2
'BOOT'	As configured by ADCINx pins for Port A. This is the "Fundamental" I2C slave address.	As configured by ADCINx pins for Port B.	N/A, this port must not be used.	N/A, this port must not be used.
'PTCH'(1)		As specified in the 'PBMs' DATAX input.		
'APP '(2)		As configured by ADCINx pins for Port B.	As specified in Patch Bundle Application Customization for GLOBAL_SYSTEM_CONFIG.Port1I2C2sSlaveAddress.	As specified in Patch Bundle Application Customization for GLOBAL_SYSTEM_CONFIG.Port2I2C2sSlaveAddress.

(1) A successful 'PBMs' Task puts the PD controller into the 'PTCH' mode.
(2) A successful 'PBMc' Task puts the PD controller into the 'APP ' mode.



(1) Use the fundamental I2C slave address of each PD controller.
(2) This delay before reading the MODE register, is optional but recommended.

Figure 5-1. Flow for pushing a Patch Bundle over the I2C_EC bus to multiple PD controllers at the same time.

While the host is writing the Patch Bundle burst data, the I2C protocol in the following figure must be followed. The host can send the entire Patch Bundle in a single I2C transaction, or it can break it up into multiple transactions. The PD controller increments the pointer into its patch memory space with each byte received on the Patch Slave address that was configured by DATA1.SlaveAddress as part of the 'PBMs' 4CC Task. The EC can re-issue a 'PBMs' 4CC Task or it can issue a 'PBMe' 4CC Task in order to reset the pointer.

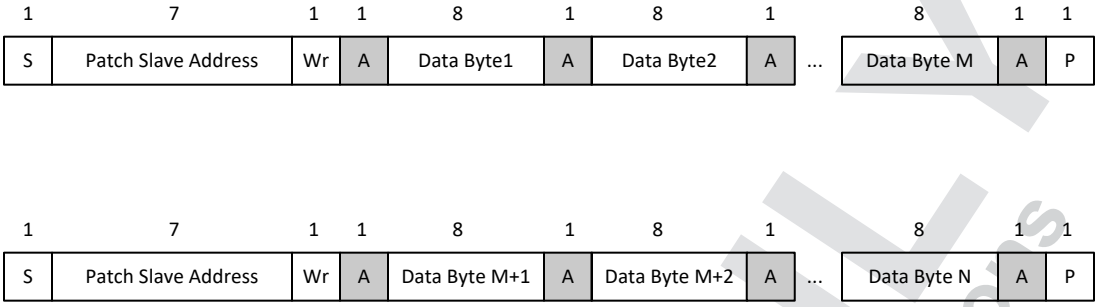


Figure 5-2. Protocol of Patch Bundle burst data assuming it is broken into two transactions.

5.3 EEPROM boot flow

During the boot process, the PD controller will load the Patch Bundle from the external EEPROM connected to the I2C3m port as described below. After the PD controller is in the APP mode, that is MODE register reads as 'APP ', the host can write to the EEPROM as described below in order to update the Patch Bundle used for booting the PD controller. During the process the previous Patch Bundle is kept intact so that the PD controller can boot from it if anything goes wrong writing the new Patch Bundle into the EEPROM.

The Patch Bundle contains a FW patch image in addition to a set of configurations that set the default value of the HI registers.

The EEPROM is divided into two regions to allow for it being updated without invalidating the previous Patch Bundle until the new Patch Bundle has been verified. The active region is the one containing the latest Patch Bundle.

5.3.1 Boot process

At boot, the PD controller will first read the Header_ID from the Low Region at the address LowRegionStart + LowAppConfigOffset. If any error occurs in reading the Low Region Header_ID, the PD controller will then read the Header_ID from the High Region at the address HighRegionStart + HighAppConfigOffset. If any error occurs in reading the High Region Header_ID, the PD controller will loop back and try the Low Region again. The PD controller will only make two attempts, after that it aborts the EEPROM loading process.

If the PD controller reads the correct Header_ID (it is expecting 0xACE0_0001) in the Low Region, then it will begin reading the Patch Bundle from the Low Region. *If there is a CRC error while reading the Patch Bundle, the PD controller does not attempt to read from the High Region*. If the PD controller reads the correct Header_ID in the High Region, then it will begin reading the Patch Bundle from the High Region. If there is a CRC error while reading the Patch Bundle, the PD controller will attempt to read from the Low Region. However, the PD controller does not make more than two attempts on any region.

Therefore, when updating one of the regions of the EEPROM it is critical to verify the new Patch Bundle in the region before pointing the Region Start to it.

If the EEPROM loading process is aborted, then the PD controller will update the BOOT_STATUS register accordingly and assert the INT_EVENTx.ReadyForPatch interrupt. It will then wait indefinitely for the host to load a patch over the I2C_EC slave port or to issue a 'GAID' to reboot the PD controller. This is also what happens when there is no EEPROM present.

Figure 5-3 shows the memory map of the EEPROM and where the pointers and offsets reside assuming that the EEPROM has initially been written with the same Patch Bundle in both regions. The PD controller looks for the Header_ID of the Low Region at address LowRegionStart + LowAppConfigOffset, and it looks for the Header_ID of the High Region at the address HighRegionStart + HighAppConfigOffset.

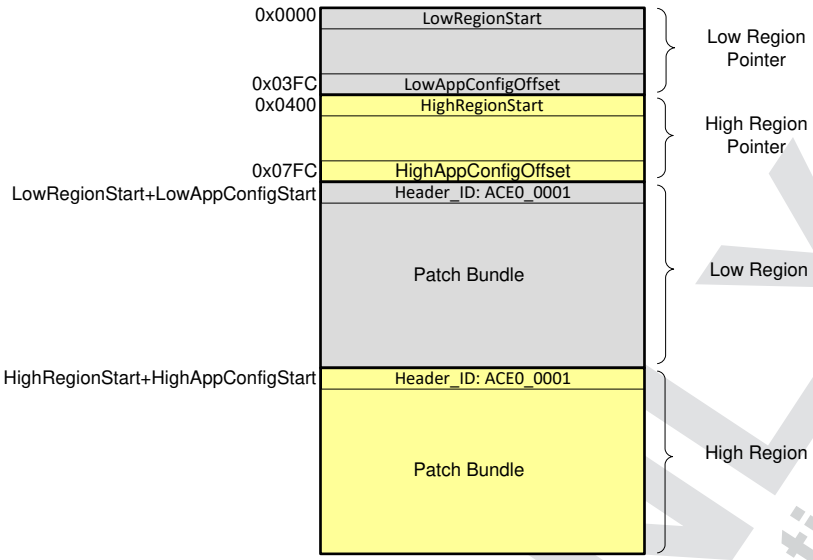


Figure 5-3. EEPROM memory map.

5.3.2 Updating the EEPROM image

When the host must update the Patch Bundle used for booting it must follow the process described in this section. The top-level flow is to update the region that the PD controller did NOT boot from as illustrated in Figure 5-4. The top-level flow executes the function UpdateRegionOfEeprom() that is illustrated in Figure 5-5.

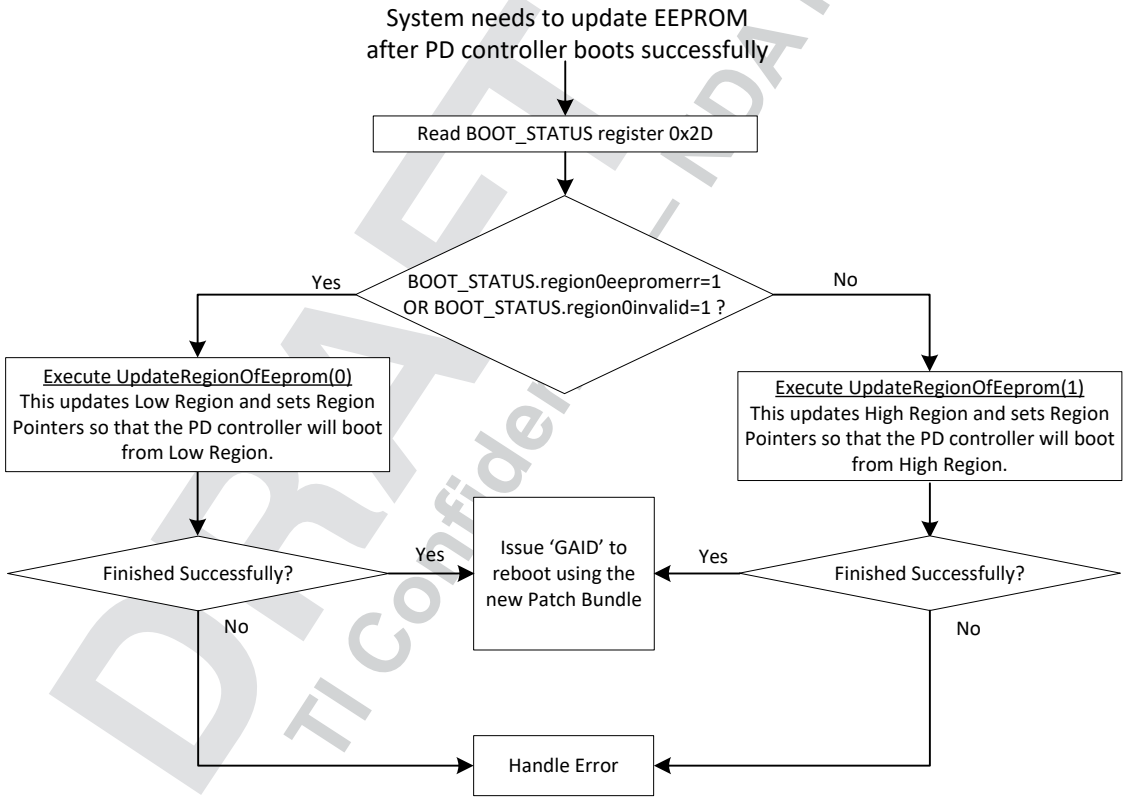


Figure 5-4. Flow for updating the EEPROM.

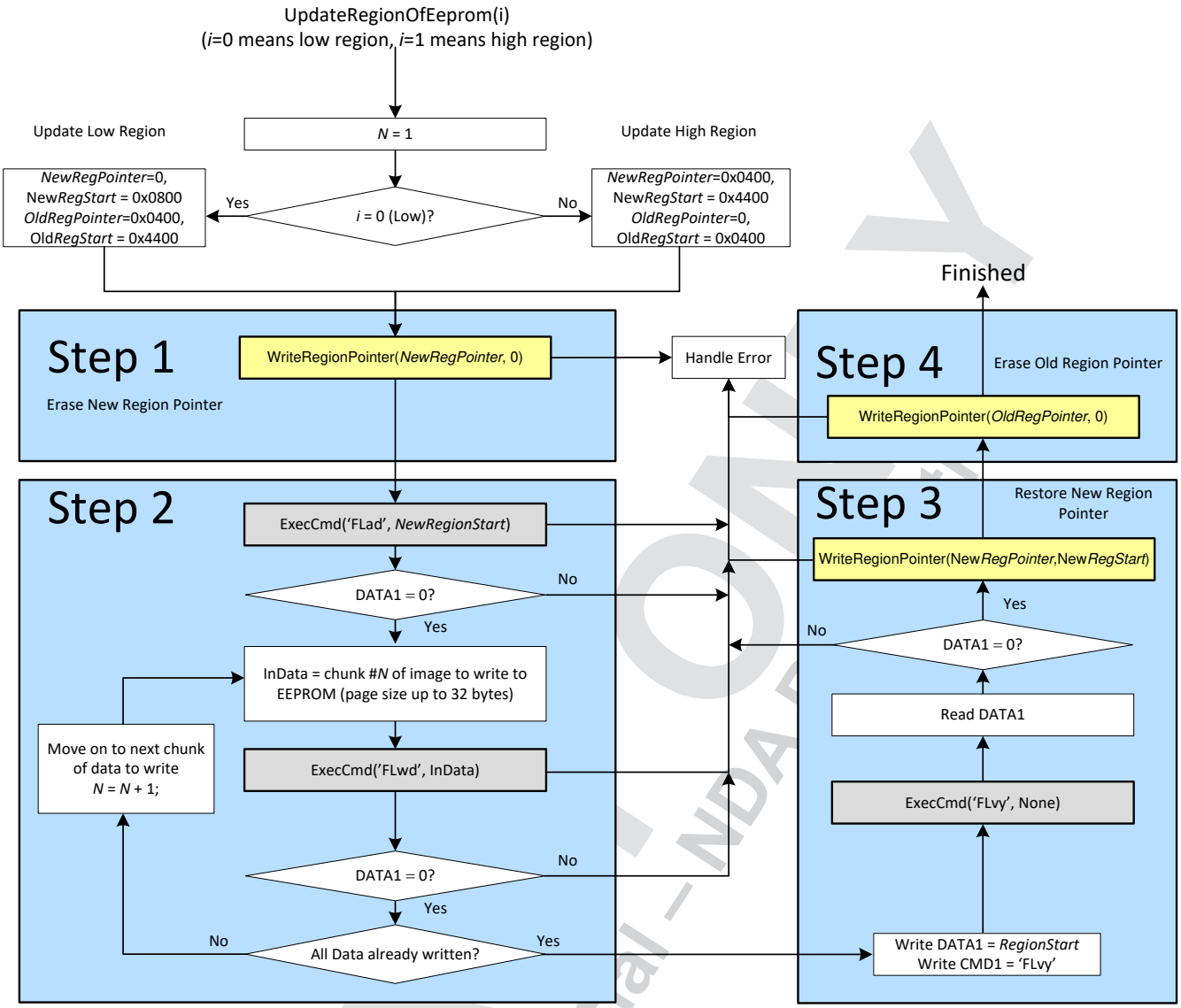


Figure 5-5. Details of the UpdateRegionOfEeprom() function used to update EEPROM.

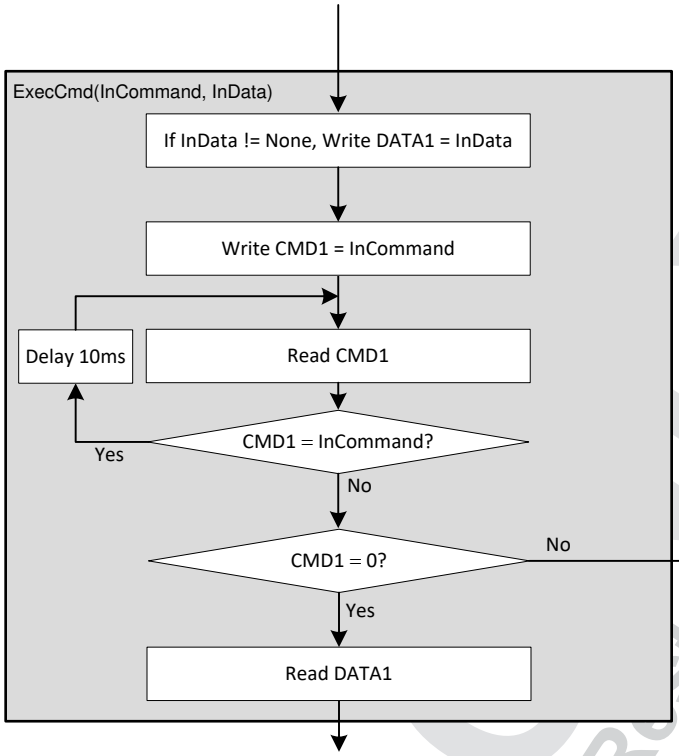


Figure 5-6. Details of the ExecCmd() block.

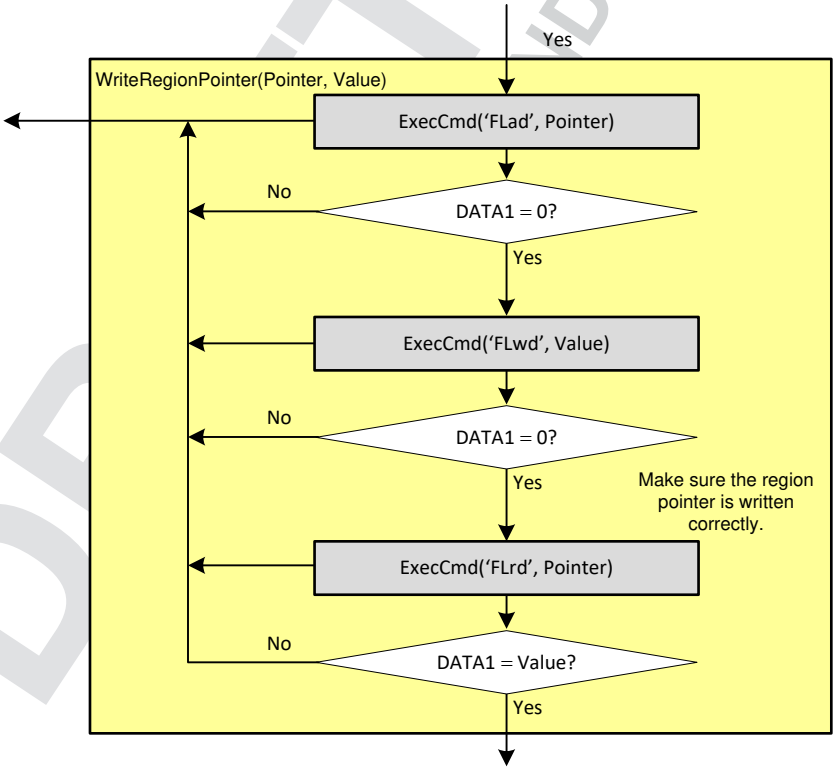


Figure 5-7. Details of the WriteRegionPointer() block.

5.3.3 EEPROM Update Example

In the example below, it is assumed that the initial state of the EEPROM is that the Low Region and the High Region both have the correct Patch Bundle. Figure 5-8 shows the EEPROM memory map for this initial condition.

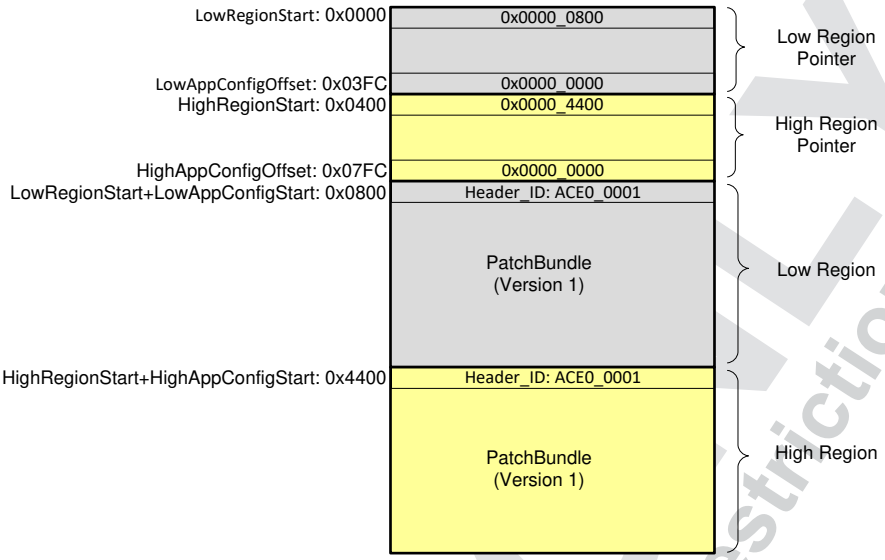


Figure 5-8. Initial state of the EEPROM. Both Low and High regions contain the same Patch Bundle. The PD controller will boot from the Low Region.

When the host must update the Patch Bundle that the PD controller uses for booting it first erases the High Region pointer so that if there is an interruption while writing the new Patch Bundle to the High Region it is guaranteed the PD controller won't try to load it. Specifically, Step 1 of the function UpdateRegionOfEeprom(1) from Figure 5-5 is executed, and Figure 5-9 shows the memory map after the High Region pointer has been erased successfully.

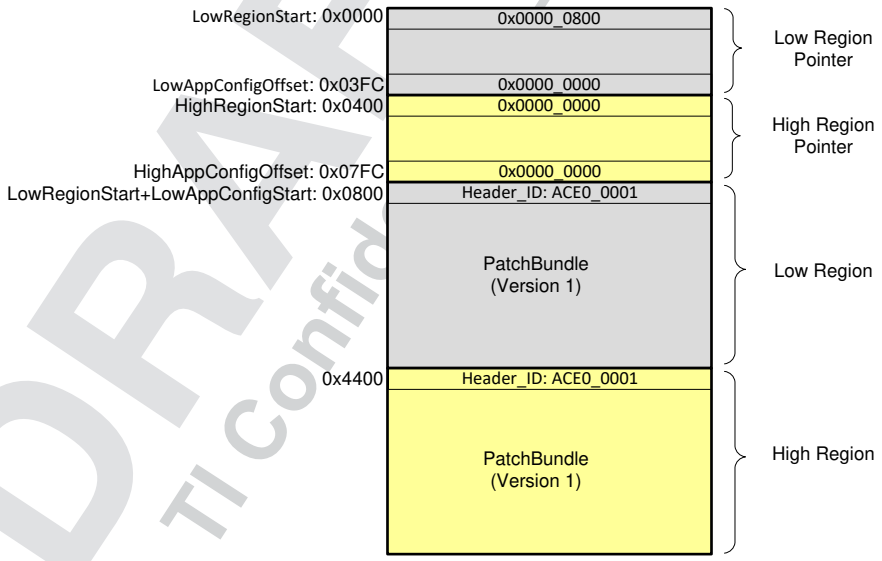


Figure 5-9. State of the EEPROM following UpdateRegionOfEeprom(1) Step 1. If booted in this state, Patch Bundle (Version 1) is loaded from Low Region.

Next, the host writes the new Patch Bundle (Version 2) to the High Region. Specifically, Step 2 of the function UpdateRegionOfEeprom(1) from Figure 5-5 is executed, and Figure 5-10 shows the memory map following this

step. Note that if the PD controller boots with the EEPROM in this state, it will still load Patch Bundle (Version 1) from the Low Region.

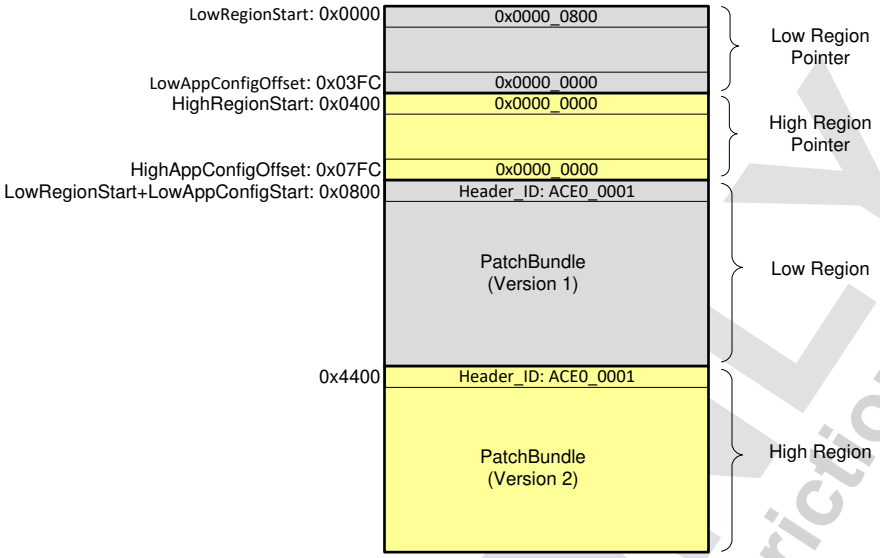


Figure 5-10. State of the EEPROM following UpdateRegionOfEeprom(1) Step 2. If booted in this state, Patch Bundle (Version 1) is loaded from Low Region.

Next, the host will verify the contents of the EEPROM High Region using the 'FLvy' command. If that succeeds, then the host will write 0x4400 into HighRegionStart at address 0x0400. This happens in Step 3 of UpdateRegionOfEeprom(1) in Figure 5-5, and Figure 5-11 shows the memory map after this is done. If the PD controller reboots with the EEPROM in this state, it will still first attempt to boot from the Low Region.

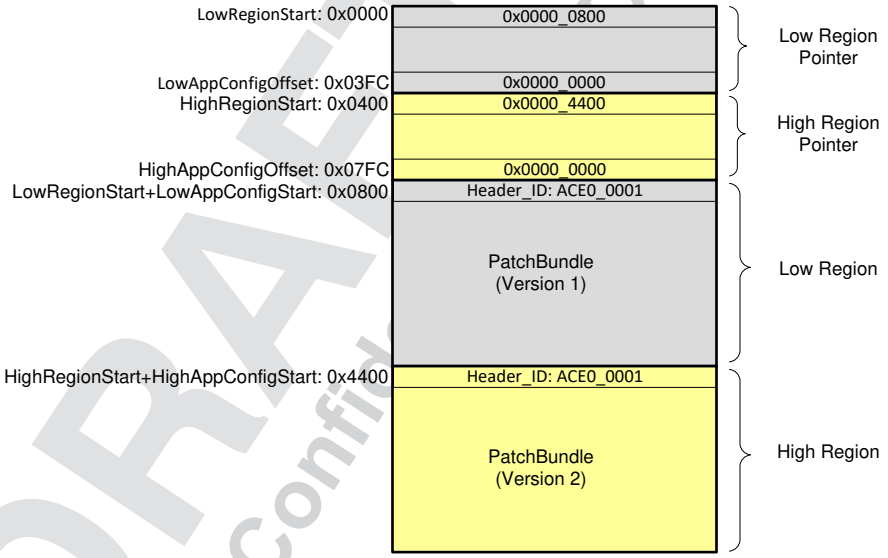


Figure 5-11. State of EEPROM following UpdateRegionOfEeprom(1) Step 3. If booted in this state, Patch Bundle (Version 1) is loaded from Low Region.

The last step is to erase the LowRegionStart value so that the PD controller will boot from the High Region. The host can use the WriteRegionPointer() functionality as shown in Step 4 of UpdateRegionOfEeprom(1) as illustrated in Figure 5-5. Figure 5-12 shows the memory map after Step 4 is complete. Because the LowRegionStart is now 0, the contents of the Low Region have no impact on how the PD controller boots.

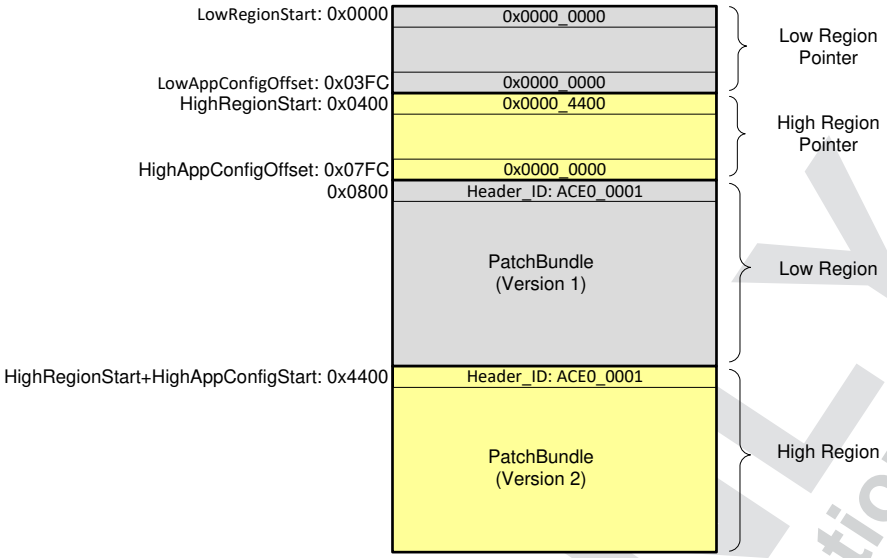


Figure 5-12. State of EEPROM following UpdateRegionOfEeprom(1) Step 4. If booted in this state, Patch Bundle (Version 2) is loaded from High Region.

The next time the host must update the EEPROM image it can execute UpdateRegionOfEeprom(0), and the process can proceed in a similar manner. The host can optionally execute UpdateRegionOfEeprom(0) immediately with the same new Patch Bundle it has just written to the High Region.

5.3.4 Source code example

This section gives example source code to implement the EEPROM flow described above.

5.3.4.1 UpdateRegionOfEeprom()

```
const uint32_t region_ptr_start[NUM_OF_REGIONS]           = {0x0  , 0x400 };
const uint32_t region_ptr_appconfig_offset[NUM_OF_REGIONS]  = {0x3FC, 0x7FC };
const uint32_t region_addr_patchbundle[NUM_OF_REGIONS]     = {0x800, 0x4400};
static int32_t UpdateRegionOfEeprom()
{
    s_AppContext *const pCtx = &gAppCtx;
    int32_t retVal = -1;
    UART_PRINT("\n\rActive Region is [%d] - Region being updated is [%d]\n\r",\
                                pCtx->active_region, pCtx->inactive_region);
    /*
     * Region-0/Region-1 is currently active, hence update Region-1/Region-0 respectively
     */
    retVal = UpdateRegionOfEeprom_Step1(pCtx->inactive_region);
    if(0 != retVal)
    {
        UART_PRINT("Region[%d] update Step 1 failed.! Next boot will happen from Region[%d]\n\r",\
                                pCtx->inactive_region, pCtx->active_region);
```

```
        goto error;
    }
    /*
     * Region-0/Region-1 is currently active, hence update Region-1/Region-0 respectively
     */
    retVal = UpdateRegionOfEeprom_Step2(pCtx->inactive_region);
    if(0 != retVal)
    {
        UART_PRINT("Region[%d] update Step 2 failed.! Next boot will happen from Region[%d]\n\r",\
                                    pCtx->inactive_region, pCtx->active_region);
        goto error;
    }
    /*
     * Write is through. Now verify if the content/copy is valid.
              * Update the corresponding region-pointer point to the new region.
     */
    retVal = UpdateRegionOfEeprom_Step3(pCtx->inactive_region);
    if(0 != retVal)
    {
        UART_PRINT("Region[%d] update Step 3 failed.! Next boot will happen from Region[%d]\n\r",\
                                    pCtx->inactive_region, pCtx->active_region);
        goto error;
    }
    /*
     * Invalidate the region-pointer of the old region.
     */
    retVal = UpdateRegionOfEeprom_Step4(pCtx->active_region);
    if(0 != retVal) {goto error;}
error:
    SignalEvent(APP_EVENT_END_UPDATE);
    return retVal;
}
```

5.3.4.2 UpdateRegionOfEeprom_Step1

```
static int32_t UpdateRegionOfEeprom_Step1(uint8_t region_number)
{
    int32_t     retVal          = -1;
    /*
```

```
    * First erases the region-pointer so that if there is an interruption while writing
    * the new Patch Bundle, it is guaranteed the PD controller won't try to load it.
    */
   retVal = WriteRegionPointer(region_number, 0);
   RETURN_ON_ERROR(retVal);
error:
   return retVal;
}
```

5.3.4.3 UpdateRegionOfEeprom_Step2()

```
static int32_t UpdateRegionOfEeprom_Step2(uint8_t region_number)
{
   uint8_t     outdata[MAX_BUF_BSIZE]  = {0};
   s_TPS_flad  fladInData      = {0};
   uint32_t    bytesUpdated    = 0;
   int32_t     retVal          = -1;
   int32_t     idx             = -1;
   /*
    * Set the start address for the next write
    */
   fladInData.flashaddr = region_addr_patchbundle[region_number];
   retVal = ExecCmd(FLad, sizeof(fladInData), (uint8_t *)&fladInData,
                    TASK_RET_CODE_LEN, &outdata[0]);
   RETURN_ON_ERROR(retVal);
   if(0 != outdata[1]) {retVal = -1; goto error;}
   for (idx = 0; idx < gSizeLowregionArray/PATCH_BUNDLE_SIZE; idx++)
   {
      /*
       * Execute FLwd with PATCH_BUNDLE_SIZE bytes of patch-data
       * in each iteration
       */
      retVal = ExecCmd(FLwd, PATCH_BUNDLE_SIZE,\
                       (uint8_t *)&tps6598x_lowregion_array[idx * PATCH_BUNDLE_SIZE],
                       TASK_RET_CODE_LEN, &outdata[0]);
      RETURN_ON_ERROR(retVal);
      if(0 != outdata[1]) {retVal = -1; goto error;}
      bytesUpdated += PATCH_BUNDLE_SIZE;
      Board_IF_Delay(75); /* in uSecs */
```

```
    }
    /* Push more bytes if any */
    if(gSizeLowregionArray > bytesUpdated)
    {
        retVal = ExecCmd(FLwd, gSizeLowregionArray - bytesUpdated,\
                    (uint8_t *)&tps6598x_lowregion_array[idx * PATCH_BUNDLE_SIZE],
                    TASK_RET_CODE_LEN, &outdata[0]);
        RETURN_ON_ERROR(retVal);
        if(0 != outdata[1]) {retVal = -1; goto error;}
    }
 error:
    return retVal;
}
```

5.3.4.4 UpdatingRegionOfEeprom_Step3()

```
static int32_t UpdateRegionOfEeprom_Step3(uint8_t new_region_number)
{
    uint8_t     outdata[MAX_BUF_BSIZE]  = {0};
    s_TPS_flvy  flvyInData      = {0};
    int32_t     retVal          = -1;
    flvyInData.flashaddr = region_addr_patchbundle[new_region_number];
    retVal = ExecCmd(FLvy, sizeof(flvyInData), (uint8_t *)&flvyInData, \
                TASK_RET_CODE_LEN, &outdata[0]);
    if(0 != outdata[1]) {retVal = -1; goto error;}
    retVal = WriteRegionPointer(new_region_number, region_addr_patchbundle[new_region_number]);
    RETURN_ON_ERROR(retVal);
error:
    return retVal;
}
```

5.3.4.5 UpdatingRegionOfEeprom_Step4()

```
static int32_t UpdateRegionOfEeprom_Step4(uint8_t old_region_number)
{
    int32_t     retVal          = -1;
    retVal = WriteRegionPointer(old_region_number, 0);
    RETURN_ON_ERROR(retVal);
error:
    return retVal;
}
```

5.3.4.6 WriteRegionPointer()

```
static int32_t WriteRegionPointer(const uint8_t region_number, const uint32_t value)
{
    uint8_t     outdata[MAX_BUF_BSIZE]  = {0};
    s_TPS_flad  fladInData  = {0};
    uint32_t    regionVal   = 0;
    int32_t     retVal      = -1;
    fladInData.flashaddr = region_ptr_start[region_number];
    retVal = ExecCmd(FLad, sizeof(fladInData), (uint8_t *)&fladInData, TASK_RET_CODE_LEN, &outdata[0]);
    RETURN_ON_ERROR(retVal);
    if(0 != outdata[1]) {retVal = -1; goto error;}
    retVal = ExecCmd(FLwd, sizeof(uint32_t), (uint8_t *)&value, TASK_RET_CODE_LEN, &outdata[0]);
    RETURN_ON_ERROR(retVal);
    if(0 != outdata[1]) {retVal = -1; goto error;}
    retVal = ExecCmd(FLrd, sizeof(uint32_t), (uint8_t *)&region_ptr_start[region_number],
sizeof(s_TPS_flrdassert), &outdata[0]);
    RETURN_ON_ERROR(retVal);
    regionVal = (outdata[4] << 24) |  (outdata[3] << 16) | (outdata[2] << 8) |  (outdata[1] << 0);
    if(value != regionVal) {retVal = -1; goto error;}
error:
    return retVal;
}
```

5.3.5 Recovering from EEPROM failure

If the EEPROM loading terminates without a valid Patch Bundle, then the INT_EVENTx.ReadyForPatch interrupt gets asserted. The host must read the BOOT_STATUS register 0x2D to discover why booting from EEPROM failed. Then the host must force the PD controller into the APP mode by pushing a patch using the 'PBMx' commands (see Section 5.2 for details). This can be the full Patch Bundle that is normally in EEPROM. After the PD controller is in the APP mode, the host can write to the EEPROM using the 'FLxx' commands and correct the problem. The figure below shows the recommended boot flow.

This boot flow requires the host to be able to correct the EEPROM. If the host requires the PD controller to enable the sink path before it can boot, then the appropriate dead-battery configuration must be selected by the ADCINx pins. In this case, the SafeMode dead-battery configuration can not be appropriate.

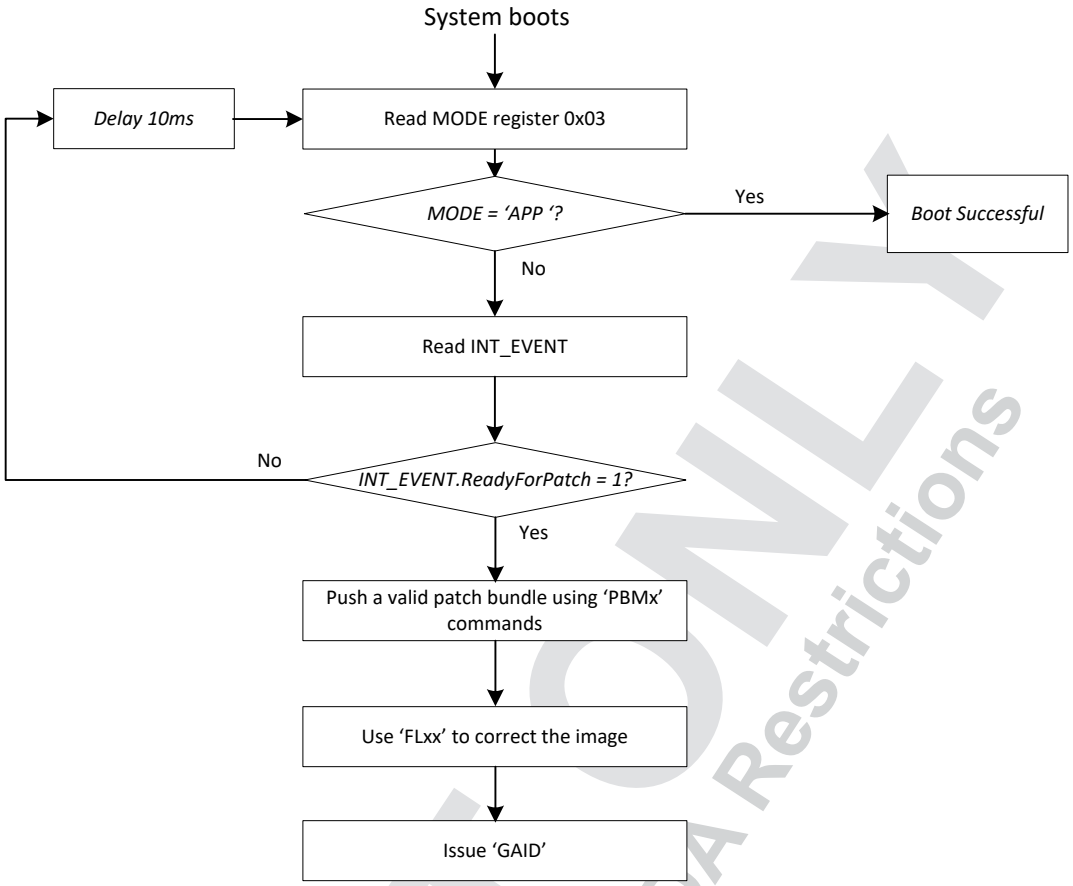


Figure 5-13. Recommended boot flow for EEPROM.

5.4 Fault Reporting

The PD controller reports various types of faults in different ways. This section summarizes the reporting.

Some registers are unique per port in a multi-port PD controller (See TPS65994BF Registers for which registers have this property). In the following table, registers that are specific to PortA or PortB are noted as PortA.REGISTER or PortB.REGISTER.

Type of Fault	Reporting
Power path PP_5V1 goes into current limit.	• POWER_PATH_STATUS.PP1_Overcurrent = 1b • POWER_PATH_STATUS.PP1switch = 001b • PortA.INT_EVENTX.ErrorPowerEventOccurred = 1b • PortA.INT_EVENTX.Overcurrent = 1b • If GPIO Fault_Condition_Active_Low_ Event_Port1 is enabled, then that GPIO gets asserted. • PortA.DATA_STATUS.OvercurrentOrTemperature = 1b
Power path PP_5V2 goes into current limit.	• POWER_PATH_STATUS.PP2_Overcurrent = 1b • POWER_PATH_STATUS.PP2switch = 001b • PortB.INT_EVENTX.ErrorPowerEventOccurred = 1b • PortB.INT_EVENTX.Overcurrent = 1b • If GPIO Fault_Condition_Active_Low_ Event_Port2 is enabled, then that GPIO gets asserted. • DATA_STATUS.OvercurrentOrTemperature = 1b
Over-Voltage on PA_VBUS while PP_EXT1 enabled	• POWER_PATH_STATUS.PP3switch = 001b • PortA.INT_EVENTX.Error_PowerEventOccurred = 1b • PortA.PD_STATUS.ErrorRecoveryDetails = 4h
Over-Voltage on PB_VBUS while PP_EXT2 enabled	• POWER_PATH_STATUS.PP4switch = 001b • PortB.INT_EVENTX.Error_PowerEventOccurred = 1b • PortB.PD_STATUS.ErrorRecoveryDetails = 4h
Over-temperature on Port A (PP_5V1 or PP_CABLE1)	• POWER_PATH_STATUS.PP1overcurrent = 1b • POWER_PATH_STATUS.PP1switch = 001b • PortA.INT_EVENTX.ErrorPowerEventOccurred = 1b • PortA.INT_EVENTX.Overcurrent = 1b • If GPIO Event Fault_Condition_Active_Low_ Event_Port1 is enabled, then that GPIO gets asserted. • PortA.DATA_STATUS.OvercurrentOrTemperature = 1b • PortA.PD_STATUS.ErrorRecoveryDetails = 1h
Over-temperature on Port B (PP_5V1 or PP_CABLE1)	• POWER_PATH_STATUS.PP2overcurrent = 1b • POWER_PATH_STATUS.PP2switch = 001b • PortB.INT_EVENTX.ErrorPowerEventOccurred = 1b • PortB.INT_EVENTX.Overcurrent = 1b • If GPIO Event Fault_Condition_Active_Low_ Event_Port2 is enabled, then that GPIO gets asserted. • PortB.DATA_STATUS.OvercurrentOrTemperature = 1b • PortB.PD_STATUS.ErrorRecoveryDetails = 1h
PP_CABLE1 goes into current limit	• PortA.POWER_PATH_STATUS.PP1_CableOvercurrent = 1b • PortA.DATA_STATUS.OvercurrentOrOvertemperature = 1b • PortA.INT_EVENTX.Overcurrent = 1b

Type of Fault	Reporting
PP_CABLE2 goes into current limit	• PortB.POWER_PATH_STATUS.PP2_CableOvercurrent = 1b • PortB.DATA_STATUS.OvercurrentOrTemperature = 1b • PortB.INT_EVENTX.Overcurrent = 1b

5.5 Alternate Mode Sequencing

The PD Controller always follows a set priority sequence for Alternate Mode entry. The sequence is listed below. If a given mode is disabled, then it is skipped. If a given mode is not possible due to incompatible Cable Plug or Port Partner, then it is skipped.

1. Enter USB for USB4 mode (if the DFP VDO in the TX_IDENTITY register has host capability set to USB4 host capable).
2. If USB4 mode was not entered, Thunderbolt 3 mode (if INTEL_VID_CONFIG.thunderBoltModeEnabled = 1 and thunderBoltAutoEntryAllowed = 1)
3. If neither USB4 mode nor TBT3 mode was entered, DisplayPort mode (if DP_SID_CONFIG.enableDPSID = 1 and DPModeAutoEntryAllowed = 1)
4. User SVID modes (if USER_VID_CONFIG.UserVidEnabled = 1 and UserModexAutoModeEntryAllowed = 1)
5. MIPI modes (if MIPI_VID_CONFIG.MipiVidEnabled = 1 and MipiDebugModeAutoEntryAllowed = 1)
6. If neither USB4 mode nor TBT3 mode nor DP mode was entered, Enter USB with USB3 mode (if the DFP VDO in the TX_IDENTITY register has host capability set to USB3.2 host capable).
7. If neither USB4 mode nor TBT3 mode nor DP mode nor USB3.2 mode was entered, Enter USB with USB2 mode (if the DFP VDO in the TX_IDENTITY register has host capability set to USB2 host capable).

Each port in a dual-port PD controller follows this sequence independently. There is not any port-to-port dependency automatically applied.

5.6 AUTO_NEGOTIATE_SINK Register

In general, writing to AUTO_NEGOTIATE_SINK register while a sink contract is in place will not cause an automatic renegotiation, changes will take effect the next time a contract is negotiated. The ANeg command forces a re-evaluation of this register and a new Request message will be issued if appropriate.

If the first four bytes of this register are written as zero, then the PD controller will always request a 5V Fixed Suppy contract at 100 mA

Below is a highlevel summary of how this register drives the PDO selection when PPS is disabled or no matching APDO is found.

- Parse the received PDO's in the register RX_SOURCE_CAPS. Discard any PDO whose voltage range is below ANMinVoltage or above ANMaxVoltage.
- Calculate the PDO power for each received PDO (RX_SOURCE_CAPS.SourcePdoX). Rank all PDO's according to the PDO power.
  - PDO Power = Voltage * MaximumCurrent (Fixed Supply)
  - PDO Power = MinimumVoltage * MaximumCurrent (Variable Supply)
  - PDO Power = MaximumPower (Battery Supply)
- The PDO with maximum PDO Power that also passes the voltage check is selected. In case there are multiple PDO's that pass the voltage check and have the same maximum PDO Power, several tie breakers are applied as described below:
  - A Fixed supply type is preferred, and Variable supply type is preferred over Battery supply type.
  - If the PDO's being compared have the same supply type, then ANRDOPriority specifies how to break the tie.

5.6.1 AUTO_NEGOTIATE_SINK usage example #1

When attached to a 36W source the PD controller has RX_SOURCE_CAPS:

- PDO1: 5V @ 3A

- PDO2: 9V @ 3A
- PDO3: 15V @ 2.4A
- PDO4: 20V @ 1.8A

The PD controller has TX_SINK_CAPS set as:

- PDO1: 5V @ 3A (fixed)
- PDO2: 20V @ 3A (fixed)

The PD controller has AUTO_NEGOTIATE_SINK set as:

- AUTO_NEGOTIATE_SINK = 0
- AUTO_NEGOTIATE_SINK.ANSinkCapMismatchPower = 240d (60W)
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinPower = 1
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinVoltage = 1
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMaxVoltage = 1
- AUTO_NEGOTIATE_SINK.NoCapabilityMismatch = x (see table below)
- AUTO_NEGOTIATE_SINK.ANRDOPriority = y (see table below)

The settings give the following results:

- ANSinkMinRequiredPower computed as 60 W
- ANMaxVoltage computed as 20V
- ANMinVoltage computed as 4.75V

Table 5-2. AUTO_NEGOTIATE_SINK usage example #1.

AUTO_NEGOTIATE_SINK		ACTIVE_CONTRACT_RDO			
NoCapabilityMismatch	ANRDOPriority	OperatingX	MinMaxOperatingX	ObjectPosition	Capability Mismatch
0	0	1.8A	3.0A	4	1
1	0	1.8A	1.8A	4	0
1	1	2.4A	2.4A	3	0

5.6.2 AUTO_NEGOTIATE_SINK usage example #2

When attached to a 36W source the PD controller has RX_SOURCE_CAPS:

- PDO1: 5V @ 3A
- PDO2: 9V @ 3A
- PDO3: 15V @ 2.4A

The PD controller has TX_SINK_CAPS set as:

- PDO1: 5V @ 0.1A (fixed)
- PDO2: 20V @ 3A (fixed)

The PD controller has AUTO_NEGOTIATE_SINK set as:

- AUTO_NEGOTIATE_SINK = 0
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinPower = 1
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinVoltage = 0
- AUTO_NEGOTIATE_SINK.ANMinVoltage = 20V
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMaxVoltage = 1
- AUTO_NEGOTIATE_SINK.NoCapabilityMismatch = x (see table below)
- AUTO_NEGOTIATE_SINK.ANRDOPriority = 0

The settings give the results in the table below. Note that ANMaxVoltage computed as 20V, but it doesn't affect the result. Because the ANMinVoltage was set to 20V, and the source is not offering 20V none of the source PDO's fulfill the sink requirements. Even though ANSinkCapMismatchPower=0 in this example, because the voltages offered are insufficient, the capability mismatch bit can still be set.

Table 5-3. AUTO_NEGOTIATE_SINK usage example #2.

AUTO_NEGOTIATE_SINK	ACTIVE_CONTRACT_RDO			
NoCapabilityMismatch	OperatingX	MinMaxOperatingX	ObjectPosition	Capability Mismatch
0	3.0A	3.0A	1	1
1	3.0A	3.0A	1	0

5.6.3 AUTO_NEGOTIATE_SINK usage example #3

When attached to a 45W source the PD controller has RX_SOURCE_CAPS:

- PDO1: 5V @ 3A
- PDO2: 9V @ 3A
- PDO3: 15V @ 3A
- PDO4: 20V @ 2.25A

The PD controller has TX_SINK_CAPS set as:

- PDO1: 5V @ 3A (fixed)
- PDO2: 20V @ 2.25A (fixed)

The PD controller has AUTO_NEGOTIATE_SINK set as:

- AUTO_NEGOTIATE_SINK = 0
- AUTO_NEGOTIATE_SINK.ANSinkCapMismatchPower = 180d (45W)
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinPower = 1
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinVoltage = 1
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMaxVoltage = 1
- AUTO_NEGOTIATE_SINK.NoCapabilityMismatch = 0
- AUTO_NEGOTIATE_SINK.ANRDOPriority = y (see table below)

The settings give the following results:

- ANSinkMinRequiredPower computed as 45 W
- ANMaxVoltage computed as 20V
- ANMinVoltage computed as 4.75V

Table 5-4. AUTO_NEGOTIATE_SINK usage example #3.

AUTO_NEGOTIATE_SINK	ACTIVE_CONTRACT_RDO			
ANRDOPriority	OperatingX	MinMaxOperatingX	ObjectPosition	Capability Mismatch
0	2.25A	2.25A	4	0
1	3.0A	3.0A	3	0

5.6.4 AUTO_NEGOTIATE_SINK usage example #4

When attached to a 100W source the PD controller has RX_SOURCE_CAPS:

- PDO1: 5V @ 3A
- PDO2: 9V @ 3A
- PDO3: 15V @ 3A
- PDO4: 20V @ 5A

The PD controller has TX_SINK_CAPS set as:

- PDO1: 5V @ 3A (fixed)
- PDO2: 20V @ 5A (fixed)

The PD controller has AUTO_NEGOTIATE_SINK set as:

- AUTO_NEGOTIATE_SINK = 0
- AUTO_NEGOTIATE_SINK.ANSinkCapMismatchPower = 240d (60W)
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinPower = 1

- AUTO_NEGOTIATE_SINK.AutoComputeSinkMinVoltage = 1
- AUTO_NEGOTIATE_SINK.AutoComputeSinkMaxVoltage = 1
- AUTO_NEGOTIATE_SINK.NoCapabilityMismatch = 0
- AUTO_NEGOTIATE_SINK.ANRDOPriority = y (see table below)

The settings give the following results:

- ANSinkMinRequiredPower computed as 100 W
- ANMaxVoltage computed as 20V
- ANMinVoltage computed as 4.75V

Table 5-5. AUTO_NEGOTIATE_SINK usage example #3.

AUTO_NEGOTIATE_SINK	ACTIVE_CONTRACT_RDO			
ANRDOPriority	**OperatingX**	**MinMaxOperatingX**	**ObjectPosition**	**Capability Mismatch**
0	5A	5A	4	0
1	5A	5A	4	0

5.7 IO_CONFIG Register

The figure below shows the interface for the GPIO hardware. The register fields GPIO_AI_EN, GPIO_PD_EN, GPIO_PU_EN, GPIO_OE, and GPIO_OD_EN listed in the table below are passed along to the GPIO hardware, independent of the GPIO Event that is configured. The PD controller will then set the signal GPIO_O to high or low to implement the selected output GPIO event. So for example, each output GPIO Event is configurable as push-pull or open-drain using the GPIO_OD_EN bit. For input GPIO events the PD controller will monitor GPIO_I from the figure.

A given GPIO Event can only be assigned to one GPIO pin.

The ProcHot_N_Event GPIO Event can be assigned to any GPIO, but for some PD controllers only a specific GPIO will have the fast reaction time feature (see device data-sheet).

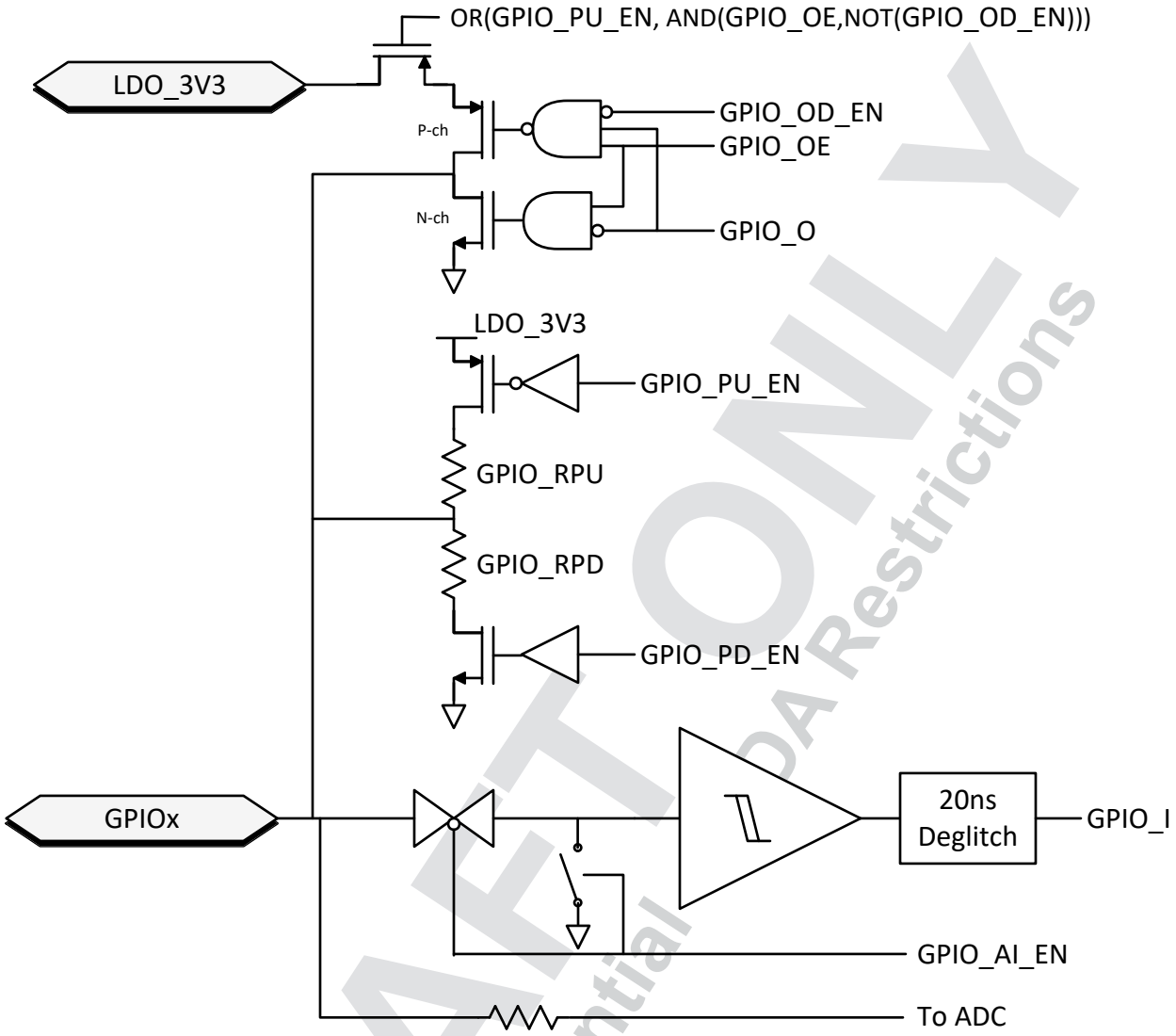


Figure 5-14. Interface to GPIO hardware

5.7.1 GPIO Multiplexor

Table 5-7 defines the GPIO Secondary Functions supported used in bytes 17-20 of the I/O Configuration Register.

Table 5-6. GPIO Secondary Functions (TPS65994BG)

Bit #	Secondary Function Name	I/O	Description
11	I2C2s_IRQ	Output	Alert signal for the I2C2s bus.
10	I2C1s_IRQ	Output	Alert signal for the I2C_EC bus.
1	HPD_TX1	Output	HPD_Tx for PortA
0	HPD_TX2	Output	HPD_Tx for PortB

Table 5-7. GPIO Secondary Functions (TPS65992xBG)

Bit #	Secondary Function Name	I/O	Description
11	I2C2s_IRQ	Output	Alert signal for the I2C2s bus.

Table 5-7. GPIO Secondary Functions (TPS65992xBG) (continued)

Bit #	Secondary Function Name	I/O	Description
10	I2C1s_IRQ	Output	Alert signal for the I2C_EC bus.
5	DM	I/O	Connect to the D- pin for BC1.2 functionality.
4	DP	I/O	Connect to the D+ pin for BC1.2 functionality.
3	HPD_RX1	Input	HPD_Rx for PortA
1	HPD_TX1	Output	HPD_Tx for PortA

5.7.2 GPIO Events

Table 5-8. GPIO Events

Event #	Event Name	I/O	Description
143	EPR_DISCHARGE_EVENT_PORT_2	Output	This GPIO is asserted during a disconnect or a negative voltage transition.
142	EPR_DISCHARGE_EVENT_PORT_1	Output	This GPIO is asserted during a disconnect or a negative voltage transition.
141	LOAD_SWITCH_DRIVE_EVENT_DELAYED_PORT_2	Output	
140	LOAD_SWITCH_DRIVE_EVENT_DELAYED_PORT_1	Output	
139	GREATER_THAN_THERSHOLD_VOLTAGE_EVENT_PORT_2	Output	This GPIO is dependent on Greater Than Threshold Voltage set in the Port Configuration 28h register. When VBUS is greater than the configured voltage the GPIO will be asserted.
138	GREATER_THAN_THERSHOLD_VOLTAGE_EVENT_PORT_1	Output	This GPIO is dependent on Greater Than Threshold Voltage set in the Port Configuration 28h register. When VBUS is greater than the configured voltage the GPIO will be asserted.
137	CapMismatchBlinking_PORT2	Output	This GPIO is a blinking indicator when a RDO is sent with a Capability Mismatch bit set. This GPIO is only applicable when acting as a power sink.
136	CapMismatchBlinking_PORT1	Output	This GPIO is a blinking indicator when a RDO is sent with a Capability Mismatch bit set. This GPIO is only applicable when acting as a power sink.
135	SBU_MUX_OE_N_EVENT_PORT2	Output	This GPIO is used to control a SBU mux and is asserted when the SBU pins need to be connected to the system. For example, when a DP, TBT3, or USB4 connection is present and the SBU pins must be connected.
134	SBU_MUX_OE_N_EVENT_PORT1	Ouput	This GPIO is used to control a SBU mux and is asserted when the SBU pins need to be connected to the system. For example, when a DP, TBT3, or USB4 connection is present and the SBU pins must be connected.
133	Reserved		
132	EXTDCDC_IRQ_EVENT_PORT_2	Output	This GPIO is asserted when an IRQ event is received from the EXT DCDC. Must be cleared using the I2Cr/I2Cw commands to removed the IRQ.
131	EXTDCDC_IRQ_EVENT_PORT_1	Output	This GPIO is asserted when an IRQ event is received from the EXT DCDC. Must be cleared using the I2Cr/I2Cw commands to removed the IRQ.
130-129	Reserved		
128	PP_VIRTUAL_SWITCH2_ENABLE	Output	GPIO is asserted for an external power path, when PP2 is configured in the Source PDO in Transmit Source Capabilities 32h
127	PP_VIRTUAL_SWITCH1_ENABLE	Output	GPIO is asserted for an external power path, when PP1 is configured in the Source PDO in Transmit Source Capabilities 32h
126	PORT_SPECIFIC_EVENT2_IRQ_PORT_2	Output	GPIO I2C2 IRQ that is specific to Port 2. This is connected to GR or a USB4 Hub to only IRQ a single port.

Table 5-8. GPIO Events (continued)

Event #	Event Name	I/O	Description
125	PORT_SPECIFIC_EVENT2_IRQ_PORT_1	Output	GPIO I2C2 IRQ that is specific to Port 1. This is connected to GR or a USB4 Hub to only IRQ a single port.
124	PORT_SPECIFIC_EVENT1_IRQ_PORT_2	Output	GPIO I2C1 IRQ that is specific to Port 2. This is connected to GR or a USB4 Hub to only IRQ a single port.
123	PORT_SPECIFIC_EVENT1_IRQ_PORT_1	Output	GPIO I2C1 IRQ that is specific to Port 1. This is connected to GR or a USB4 Hub to only IRQ a single port.
122	USB4_EVENT_PORT_1	Ouput	This GPIO is asserted when a USB4 connection is present. There is no dependecy on the cable speed or cable type, and is only based on USB4 in the EUDO TX/RX.
121	USB4_EVENT_PORT_0	Output	This GPIO is asserted when a USB4 connection is present. There is no dependecy on the cable speed or cable type, and is only based on USB4 in the EUDO TX/RX.
120	Reserved		
119	USB2_POWER_DISABLE_EVENT	Input	When this GPIO is asserted this will disable all Type-C ports. This GPIO is inteded to be controlled from a USB2 Hub, and is generally asserted by the USB2 driver.
118	GR_TYPEC_DISABLE_EVENT_PORT_2	Input	When this GPIO is asserted this will disable the Type-C port. This GPIO is inteded to be controlled from GR, and is generally asserted by the USB3/4 driver.
117	GR_TYPEC_DISABLE_EVENT_PORT_1	Input	When this GPIO is asserted this will disable the Type-C port. This GPIO is inteded to be controlled from GR, and is generally asserted by the USB3/4 driver
116	HUB_TYPEC_DISABLE_EVENT_PORT_2	Input	When this GPIO is asserted this will disable the Type-C port. This GPIO is inteded to be controlled from a USB2 Hub, and is generally asserted by the USB2 driver.
115	HUB_TYPEC_DISABLE_EVENT_PORT_1	Input	When this GPIO is asserted this will disable the Type-C port. This GPIO is inteded to be controlled from a USB2 Hub, and is generally asserted by the USB2 driver.
114	SYSTEM_POWER_STATE_S0_EVENT	Output	This GPIO is asserted when the Set Sx App Config 20h is set to S0 (System Power State). Otherwise it will be de-asserted.
113	DMC_FORCE_SAFE_STATE_EVENT	Input	When this GPIO is asserted the all of the PD ports will be reduced to 5V PD contracts. All ports will send an update 5V single source PDO.
112-104	Reserved		
103	MUX_OE_N_EVENT_PORT_2	Output	This GPIO is high when there is no connection or USB attached. It's low when there is a DP accessory attached, a TBT/USB4 device attached or a debug accessory attached.
102	MUX_OE_N_EVENT__PORT_1	Output	This GPIO is high when there is no connection or USB attached. It's low when there is a DP accessory attached, a TBT/USB4 device attached or a debug accessory attached.
101	PLUG_INSERT_OR_REMOVAL__DEVICE	Output	This GPIO output is to assert any time either port (for example device) is in an Attached state (either Attached.SRC or Attached.SNK)
100	Reserved		
99	EnableSource_HighContract_VBus_Event_Global	Output	This GPIO is asserted when there is a high-power contract as a source for either port 1 or port 2. Effectively it is an OR of the EnableSource_Port1 and EnableSource_Port2 events.
98	EnableSource_HighContract_VBus_Event_Port2	Output	It has the same behavior as EnableSource_HighContract_VBus_Event_Port1, but it applies to Port 2.

Table 5-8. GPIO Events (continued)

Event #	Event Name	I/O	Description
97	EnableSource_HighContract_VBus_Event_Port1	Output	When the PD controller sends an Accept message to start sourcing VBUS on Port1 under a high-power contract this GPIO is asserted high. It will remain high as long as the high-power contract is active. If the contract transitions from a high-power contract to a low-power contract, this GPIO will have a high-to-low transition after the PS_Rdy message is sent. A high-power contract is one for a PDO index greater than 1, or a current greater than GLOBAL_SYSTEM_CONFIG.MinimumCurrentAdvertisement.
93:88	Reserved		
87	I2C3_Master_Active	Output	Asserted when I2C Master is active
86	FAULT_OVP_GPIOEVENT_GLOBAL	Output	Asserted when OVP is detected on either Port
85	FAULT_OVP_GPIOEVENT_PORT_2	Output	Asserted when OVP is detected on Port2
84	FAULT_OVP_GPIOEVENT_PORT_1	Output	Asserted when OVP is detected on Port1
83	DP_DM_MUX_FWUP_ENABLE_EVENT_PORT	Output	Asserted high upon app config load
82	EXPLICIT_PDCONTRACT_GPIOEVENT_PORT_2	Output	Asserted high when USB Type-C contract is greater than programmed threshold value in Port Config register on Port1
81	EXPLICIT_PDCONTRACT_GPIOEVENT_PORT_1	OutputOutput	Asserted high when USB Type-C contract is greater than programmed threshold value in Port Config register on Port2
80	ENABLESOURCE_VBUS_EVENT__DEVICE	Output	Asserted when there is a high-power contract as source for either Port1 or Port2
79:77	Reserved		
76	PdNegotiationInProcess	Output	When in source mode, this GPIO is asserted after a Request message is received, before sending the Accept message. The GPIO is de-asserted after the PS_RDY message is sent. When in sink mode, this GPIO is asserted right before sending a Request message, and de-asserted after a PS_RDY message is received. In either mode, the GPIO is de-asserted when a detach occurs.
75	AttachedAsSink	Output	When the PD controller has a port that is connected to a Source, this GPIO will be asserted. The GPIO is de-asserted upon disconnect, hard reset, during power-role swap and during fast-role swap only if none of the ports in the PD controller are connected to a source.
74	EnableSource_Port2	Output	It has the same behavior as EnableSource_Port1, but it applies to Port 2.
73	EnableSource_Port1	Output	When the PD controller sends an Accept message to start sourcing VBUS on Port1 under a high-power contract this GPIO is asserted high. It will remain high as long as the high-power contract is active. If the contract transitions from a high-power contract to a low-power contract, this GPIO will have a high-to-low transition after the PS_Rdy message is sent. A high-power contract is one for a PDO index greater than 1, or a current greater than GLOBAL_SYSTEM_CONFIG.MinimumCurrentAdvertisement.
72	Reserved		
71	Reserved		
70	Reserved		

Table 5-8. GPIO Events (continued)

Event #	Event Name	I/O	Description
69	MRESET	Input	Upon a rising edge on this GPIO the PD controller will drive a rising edge on the RESETZ GPIO after a delay . Upon a falling edge on this GPIO the PD controller will drive a falling edge on the RESETZ GPIO after a delay .
68	RESETZ	Output	This works in conjunction with MRESET.
67	Fault_Condition_Active_Low_Global	Output	Asserts low on an overcurrent event on Port1 or Port2.
66	Load_Switch_Drive_Port2	Output	When the PD controller enables the PP_EXT2 sinking path, it will pull the selected GPIO low to enable a load-switch. When the PD controller disables the PP_EXT2 sinking path, it will drive the selected GPIO high.
65	Load_Switch_Drive_Port1	Output	When the PD controller enables the PP_EXT1 sinking path, it will pull the selected GPIO low to enable a load-switch. When the PD controller disables the PP_EXT1 sinking path, it will drive the selected GPIO high.
64	Reserved		
63	Reserved		
62	Dp_Dm_Mux_Enable_Event_Port2	Output	This GPIO must be used to enable/disable a USB 2.0 D+/D- mux. The GPIO is driven high upon connection, and low upon disconnect on Port2.
61	Dp_Dm_Mux_Enable_Event_Port1	Output	This GPIO must be used to enable/disable a USB 2.0 D+/D- mux. The GPIO is driven high upon connection, and low upon disconnect on Port1.
60	Reserved		
59	Reserved		
58	Reserved		
57	Reserved		
56	I2C3_MASTER_IRQ_EVENT	Input	When this GPIO is pulled low, the PD controller copies the contents of register 0x5F, clears bits 3, 4, 13, 22, 24, and 30, then writes the resulting 4 bytes to register address 0x04 using the slave address specified in the SlaveAddrTbt2 field of the I2CMASTER_CONFIG register (0x64). The PD controller always does this for both ports.
55	Prs_Ext_Vbus_Discharge_Event_Port2	Output	This GPIO is pulled low after a PR_Swap to enable an external VBUS discharge circuit during a power-role swap on Port2.
54	Prs_Ext_Vbus_Discharge_Event_Port1	Output	This GPIO is pulled low after a PR_Swap to enable an external VBUS discharge circuit during a power-role swap on Port1.
53	VCONN_On_Event_Port2	Output	This GPIO is asserted when PP_CABLE2 is enabled.
52	VCONN_On_Event_Port1	Output	This GPIO is asserted when PP_CABLE1 is enabled.
51	Debug_Accessory_Mode_Event_Port2	Output	Output: This GPIO is asserted high when an Debug Accessory is attached on Port2.
50	Debug_Accessory_Mode_Event_Port1	Output	Output: This GPIO is asserted high when a Debug Accessory is attached on Port1.
49	Audio_Mode_Event_Port2	Output	Output: This GPIO is asserted high when an Audio Accessory (Ra/Ra) is attached on Port2.
48	Audio_Mode_Event_Port1	Output	Output: This GPIO is asserted high when an Audio Accessory (Ra/Ra) is attached on Port1.

Table 5-8. GPIO Events (continued)

Event #	Event Name	I/O	Description
47	Prevent_High_Current_Contract_Event	Input	When this GPIO is high, then the PD controller will limit the amount of current it advertises to the value specified by the MinimumCurrentAdvertisement field in the Global System Configuration register (0x27) and it will only advertise one PDO. The PD controller responds to both falling and rising edges of this GPIO by increasing or decreasing its current advertisement. The adjusted current advertisement is reflected by automatically transmitting an updated Source Capabilities message for explicit contracts and by adjusting the Type-C Rp value for implicit contracts.
46	High_current_Contract_Active_Event	Output	When an explicit contract for more than the value specified by the MinimumCurrentAdvertisement field in the Global System Configuration register (0x27) is negotiated, the PD controller drives this GPIO high. When connected to a legacy device/sink this GPIO will not be driven high.
45	Prevent_DRSwap_To_UFP_Event	Input	When the GPIO is high, the PD controller will reject any DR_Swap messages from the Port Partner requesting to change the data-role from DFP to UFP.
44	UFP_Indicator_Event	Output	The GPIO is driven high when the data role of any port in the PD controller is UFP.
43	Barrel_Jack_Event	Input	When this GPIO is high, the PD controller interprets it to mean that a barrel-jack adaptor is connected and the system has Unconstrained power. A falling edge on this GPIO will automatically set PORT_CONTROL.UnconstrainedPower to 0 and TX_SCEDB.SourceInputs[0] to 0. A rising edge on this GPIO will automatically set PORT_CONTROL.UnconstrainedPower to 1 and TX_SCEDB.SourceInputs[0] to 1.
42	Retimer_SoC_OVR_Force_PWR_Event	Input	When this GPIO is low and there is not a Type-C connection on a port X, then the PD controller drives the Retimer_Force_PWR_Event_PortX GPIO and the Retimer_Reset_N GPIO low. Otherwise, the Retimer_Force_PWR_Event_PortX and Retimer_Reset_N are driven high. See DELAY_CONFIG (register 0x43) section for timing details.
41	ProcHot_N_Event	Output	This recommended to be assigned to a specific GPIO (check data-sheet). This is asserted low when certain power events occur. • When a source or sink is connected. • When the source is disconnected. • Upon entry into a new Explicit Contract as a sink that reduces voltage or current. • When a PR_swap is accepted.
40	Retimer_Reset_N_Event_Port2	Output	Reset signal for external retimer attached to Port2.
39	Retimer_Reset_N_Event_Port1	Output	Reset signal for external retimer attached to Port1.
38	Retimer_Force_PWR_Event_Port2	Output	Power control for external retimer attached to Port2.
37	Retimer_Force_PWR_Event_Port1	Output	Power control for external retimer attached to Port1.
36	Fault_Condition_Active_Low_Event_Port2	Output	Asserts low on an overcurrent event on Port2.
35	Fault_Condition_Active_Low_Event_Port1	Output	Asserts low on an overcurrent event on Port1.
34	Fault_Input_Event_Port2	Input	When set low by the system, Port2 enters the Type-C Error Recovery State. When set high, no action is taken.
33	Fault_Input_Event_Port1	Input	When set low by the system, Port1 enters the Type-C Error Recovery State. When set high, no action is taken.
32	TBT_Mode_Selection_Event_Port2	Output	Output: Asserted high when data connection on Port2 is TBT, otherwise low.

Table 5-8. GPIO Events (continued)

Event #	Event Name	I/O	Description
31	TBT_Mode_Selection_Event_Port1	Output	Output: Asserted high when data connection on Port1 is TBT, otherwise low.
30	UFP_DFP_Event_Port2	Output	Output: Asserted high when Port2 is operating as UFP. Asserted low when port is operating as DFP.
29	UFP_DFP_Event_Port1	Output	Output: Asserted high when Port1 is operating as UFP. Asserted low when port is operating as DFP.
28	DP_or_USB3_Event_Port2	Output	Output: Asserted high when data connection on Port2 is DisplayPort or USB3; Low if neither data mode is active or port is disconnected.
27	DP_or_USB3_Event_Port1	Output	Output: Asserted high when data connection on Port1 is DisplayPort or USB3; Low if neither data mode is active or port is disconnected.
26	User_SVID_Active_Event_Port2	Output	Asserted high when an Alternate Mode is entered on Port2 using the User Defined SVID.
25	User_SVID_Active_Event_Port1	Output	Asserted high when an Alternate Mode is entered on Port1 using the User Defined SVID.
24	DP_Mode_Selection_Event_Port2	Output	Output: Asserted high when data connection on Port2 is DP, otherwise low.
23	DP_Mode_Selection_Event_Port1	Output	Output: Asserted high when data connection on Port1 is DP, otherwise low.
22	USB3_Event_Port2	Output	Output: Asserted high when data connection is USB3 on Port 2, low in all other cases.
21	USB3_Event_Port1	Output	Output: Asserted high when data connection is USB3 on Port 1, low in all other cases.
20	SourcePDOContractBit2_Port2	Output	Output: Bit2 of binary encoded outputs indicating when a Source PDO1 through PDO7 on Port2 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
19	SourcePDOContractBit1_Port2	Output	Output: Bit1 of binary encoded outputs indicating when a Source PDO1 through PDO7 on Port2 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
18	SourcePDOContractBit0_Port2	Output	Output: Bit0 of binary encoded outputs indicating when a Source PDO1 through PDO7 on Port2 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
17	SourcePDO4Contract_Port2	Output	Output: Asserted high when a Source PDO4 on Port2 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired), otherwise low.
16	SourcePDO3Contract_Port2	Output	Output: Asserted high when a Source PDO3 on Port2 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired), otherwise low.
15	SourcePDO2Contract_Port2	Output	Output: Asserted high when a Source PDO2 on Port2 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired), otherwise low.
14	SourcePDO1Contract_Port2	Output	Output: Asserted high when a Source PDO1 on Port2 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired), otherwise low.
13	SourcePDOContractBit2_Port1	Output	Output: Bit2 of binary encoded outputs indicating when a Source PDO1 through PDO7 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
12	SourcePDOContractBit1_Port1	Output	Output: Bit1 of binary encoded outputs indicating when a Source PDO1 through PDO7 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).

Table 5-8. GPIO Events (continued)

Event #	Event Name	I/O	Description
11	SourcePDOContractBit0_Port1	Output	Output: Bit0 of binary encoded outputs indicating when a Source PDO1 through PDO7 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired).
10	SourcePDO4Contract_Port1	Output	Output: Asserted high when a Source PDO4 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO2 has been negotiated.
9	SourcePDO3Contract_Port1	Output	Output: Asserted high when a Source PDO3 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO2 has been negotiated.
8	SourcePDO2Contract_Port1	Output	Output: Asserted high when a Source PDO2 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO2 has been negotiated.
7	SourcePDO1Contract_Port1	Output	Output: Asserted high when a Source PDO1 on Port1 has been negotiated (the Accept message has been transmitted and the tSrcTransition timer has expired). D-asserted when a PDO other than PDO1 has been negotiated.
6	AMSEL_Event_Port2	Output	Output: Used to configure external super-speed multiplexors for the DisplayPort Alternate Mode on Port2. Set high when DisplayPort alternate mode is entered and pin assignment A/C/E. Set low when DisplayPort alternate mode is entered and pin assignment B/D/F. Set Hi-Z when DisplayPort alternate mode is not entered.
5	AMSEL_Event_Port1	Output	Output: Used to configure external super-speed multiplexors for the DisplayPort Alternate Mode on Port1. Set high when DisplayPort alternate mode is entered and pin assignment A/C/E. Set low when DisplayPort alternate mode is entered and pin assignment B/D/F. Set Hi-Z when DisplayPort alternate mode is not entered.
4	Cable_Orientation_Event_Port2	Output	Output: Indicates the plug orientation on Port2. Low when the plug is connected upside-up (CC1 connected to CC in cable) or disconnected. High when plug is connected upside-down (CC2 connected to CC in cable).
3	Cable_Orientation_Event_Port1	Output	Output: Indicates the plug orientation on Port1. Low when the plug is connected upside-up (CC1 connected to CC in cable) or disconnected. High when plug is connected upside-down (CC2 connected to CC in cable).
2	PlugEvent_Port2	Output	Output: Asserted high when plug event has occurred on Port2, otherwise low.
1	PlugEvent_Port1	Output	Output: Asserted high when plug event (attached state) has occurred on Port1, otherwise low.
0	NullEvent	NA	No event associated with this GPIO.

5.8 Transmitted Status Data Block SDB Register

This feature must be enabled in the PD3 configuration register (0x42) SupportStatusMsg bit. The PD controller does not take any automatic action if this register is written.

If the SupportStatusMsg bit set to 0 and a Get_Status message is received, then the PD controller ignores this TX_SDB register and responds with a Not_Supported message. If the SupportStatusMsg bit is set to 1 and a Get_Status message is received, then the response is determined as described below.

The Power Status byte is partially computed by the PD controller. Specifically, there are three bits the PD controller can compute:

- bit 1: The PD controller will send a Discover Identity message to the cable and if the cable reports it can handle less than the PD controller can otherwise advertise (based on Tx Source Capabilities register (0x32)) then bit1 is asserted. See Table below for cable maximum current capability determination.
- bit 2: If the host has enabled GPIO Event #80 (Prevent_High_Current_Contract_Event) then bit2 is computed as high if the associated GPIO has a low value.
- bit 3: The PD controller computes bit3 as the value of the dead-battery flag.

When a Get_Status message is received by the PD controller then it formulates the response as the first 5 bytes of this register then appending the bit-wise OR of the computed value of bits 1, 2, and 3 with the Power Status byte written by the host. Note that the Power Status byte in this register will always read back as the value written by the host.

The host must update this register when it updates the Tx Source Capabilities register (0x32).

The PD controller does not take any automatic action if this register is written. The host is responsible for issuing 4CC 'ALRT' command to inform the Port Partner that the Status is changed.

0x79 TX_SDB Register

This feature must be enabled in the PD3 configuration register (0x42) SupportStatusMsg bit. The PD controller does not take any automatic action if this register is written.

If the SupportStatusMsg bit set to 0 and a Get_Status message is received, then the PD controller ignores this TX_SDB register and responds with a Not_Supported message. If the SupportStatusMsg bit is set to 1 and a Get_Status message is received, then the response is determined as described below.

The Power Status byte is partially computed by the PD controller. Specifically, there are three bits the PD controller can compute:

- bit 1: The PD controller will send a Discover Identity message to the cable and if the cable reports it can handle less than the PD controller can otherwise advertise (based on Tx Source Capabilities register (0x32)) then bit1 is asserted. See Table below for cable maximum current capability determination.
- bit 2: If the host has enabled GPIO Event #80 (Prevent_High_Current_Contract_Event) then bit2 is computed as high if the associated GPIO has a low value.
- bit 3: The PD controller computes bit3 as the value of the dead-battery flag.

When a Get_Status message is received by the PD controller then it formulates the response as the first 5 bytes of this register then appending the bit-wise OR of the computed value of bits 1, 2, and 3 with the Power Status byte written by the host. Note that the Power Status byte in this register will always read back as the value written by the host.

The host must update this register when it updates the Tx Source Capabilities register (0x32).

The PD controller does not take any automatic action if this register is written. The host is responsible for issuing 4CC 'ALRT' command to inform the Port Partner that the Status is changed.

Table 5-9. Maximum Current Determination.

Active Cable VDO1 Information		Active Cable VDO2 information		Maximum current to advertise	Comment
VBUS Current Handling (bits 6:5)	VBUS through cable (bit 4)	SuperSpeed supported (bit 4)	SuperSpeed Lanes Supported (bit 3)		
X	0	X	X	No Limit	0
00b	1	0	X	0.5 A	Limit to USB 2.0
00b	1	1	0	0.9 A	Limit to USB 3.1
00b	1	1	1	1.5 A	Limit to USB 3.2
01b	1	X	X	3 A	
10b	1	X	X	5 A	
11b	1	X	X	No Limit	

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2022	*	Draft Release

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