TPS65992SBG USB Type-C® and USB PD Controller with Integrated Source Power Switch

1 Features

- USB Power Delivery (PD) controller
  - USB PD 3.0 certified
  - USB4 compliant
  - Fast role swap support
  - Physical layer and policy engine
  - Configurable at Boot and host-controlled
- USB Type-C ®Specification compliant
  - Cable attach and orientation detection
  - Integrated VCONN switch
  - 26-V tolerant CC pins
- Integrated VBUS sourcing port power switch
  - 5-V, 3-A, 45-mΩ Sourcing switch
  - Adjustable current limiting
  - Undervoltage and overvoltage protection
  - Fast turn-on mode to support fast-role swap
  - UL recognized component E169910
- High-voltage gate driver for sinking path
  - Reverse current protection
  - Slew rate control
  - Overvoltage protection
- Alternate mode support
  - DisplayPort source and Sink
  - Thunderbolt™
  - User configure alternate modes
- USB type-C connector system software interface (USCI) support
- Power management
  - Power supply from 3.3 V or VBUS source
  - 3.3-V LDO Output for dead battery support
- Supports extended industrial temperature range

2 Applications

- USB4 Gen3/4 Docking Stations
- DisplayPort 2.0 & 2.1 Monitors
- Extended Power Range USB PD Sources
- Thunderbolt 4 Devices

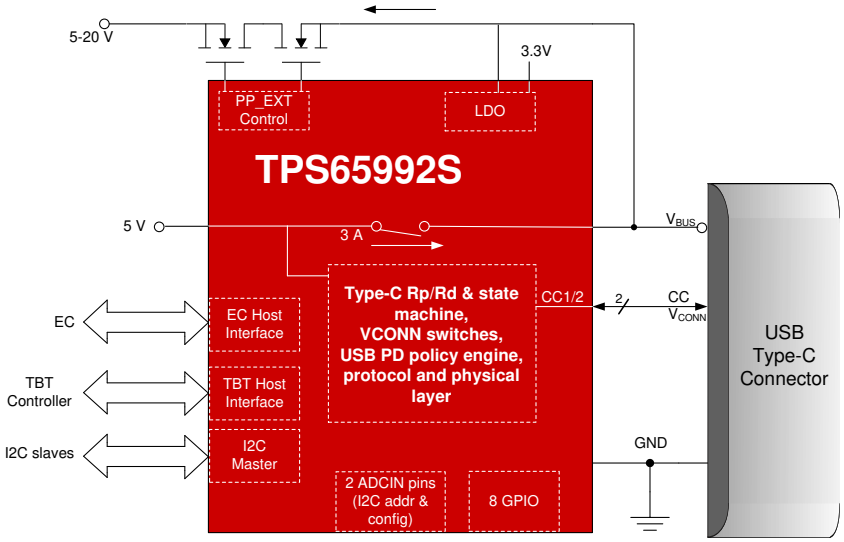
3 Description

The TPS65992SBG is a stand-alone USB Type-C controller and Power Delivery (PD) controller providing cable plug and orientation detection for one USB Type-C connector. Upon cable attachment, the TPS65992SBG performs cable detection according to the USB Type-C specification. It also communicates on the CC wire using the USB PD protocol. When cable detection and USB PD negotiation are complete, the TPS65992SBG enables the internal power path and configures alternate mode settings for external multiplexers.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
TPS65992SBG	QFN (RSM)	4.0 mm x 4.0 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
November 2022	*	Initial Release

5 Pin Configuration and Functions

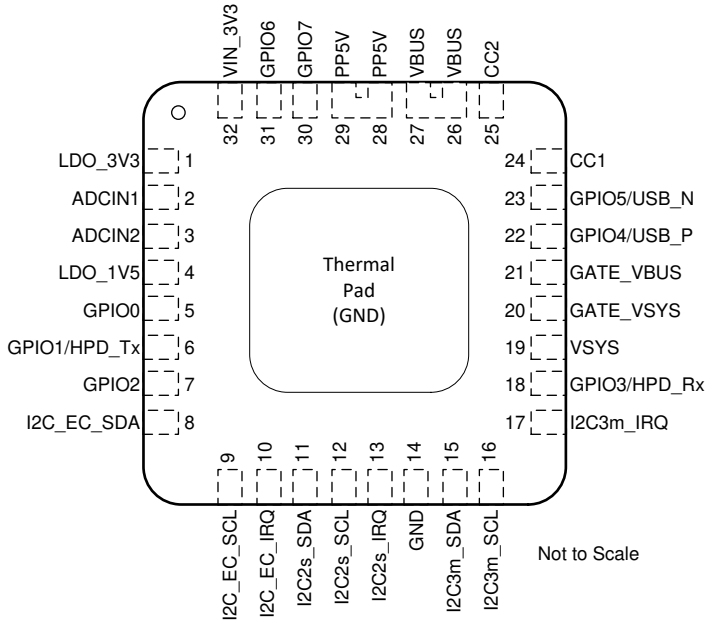


Figure 5-1. RSM Package 32-pin QFN Top View

Table 5-1. Pin Functions

PIN		TYPE[1]	RESET	DESCRIPTION
NAME	NO.			
ADCIN1	2	I	Hi-Z	Configuration input. Connect to a resistor divider to LDO_3V3.
ADCIN2	3	I	Hi-Z	Configuration input. Connect to a resistor divider to LDO_3V3.
CC1	24	I/O	Hi-Z	I/O for USB Type-C and USB PD. Filter noise with recommended capacitor to GND (C_{CCy}).
CC2	25	I/O	Hi-Z	I/O for USB Type-C and USB PD. Filter noise with recommended capacitor to GND (C_{CCy}).
GATE_VSYS	20	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to VSYS.
GATE_VBUS	21	O	Hi-Z	Connect to the N-ch MOSFET that has source tied to VBUS.
GND	14	—	—	Ground. Connect to ground plane.
GPIO0	5	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO1(HPD_Tx)	6	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused. May be used as DisplayPort HPD Tx signal.
GPIO2	7	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO3 (HPD_Rx)	18	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused. May be used as DisplayPort HPD Rx signal.
GPIO4 (USB_P)	22	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused. May be used as an ADC input. This may be connected to D+ for BC1.2 support.
GPIO5 (USB_N)	23	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused. May be used as an ADC input. This may be connected to D- for BC1.2 support.
GPIO6	31	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
GPIO7	30	I/O	Hi-Z	General purpose digital I/O. Tie to ground when unused.
I2C_EC_SCL	9	I	Hi-Z	I2C slave serial clock input. Tie to pullup voltage through a resistor. May be grounded if unused. Connect to Embedded Controller (EC).
I2C_EC_SDA	8	I/O	Hi-Z	I2C slave serial data. Open-drain input/output. Tie to pullup voltage through a resistor. May be grounded if unused. Connect to Embedded Controller (EC).
$\overline{\text{I2C_EC_IRQ}}$	10	O	Hi-Z	I2C slave interrupt. Active low. Connect to external voltage through a pull-up resistor. Connect to Embedded Controller (EC). This can be re-configured to GPIO10. Tie to ground when unused.

Table 5-1. Pin Functions (continued)

PIN		TYPE(1)	RESET	DESCRIPTION
NAME	NO.			
I2C2s_SCL	12	I	Hi-Z	I2C slave serial clock input. Tie to pull-up voltage through a resistor. May be grounded if unused.
I2C2s_SDA	11	I/O	Hi-Z	I2C slave serial data. Open-drain input/output. Tie to pullup voltage through a resistor. May be grounded if unused.
$\overline{\text{I2C2s\_IRQ}}$	13	O	Hi-Z	I2C slave interrupt. Active low. Connect to external voltage through a pull-up resistor. Tie to ground when unused. This can be re-configured to GPIO11.
I2C3m_SCL	16	O	Hi-Z	I2C master serial clock. Open-drain output. Tie to pullup voltage through a resistor when used or unused.
I2C3m_SDA	15	I/O	Hi-Z	I2C master serial data. Open-drain input/output. Tie to pullup voltage through a resistor when used or unused.
$\overline{\text{I2C3m\_IRQ}}$	17	I	Hi-Z	I2C master interrupt. Active low. Connect to external voltage through a pull-up resistor. Tie to ground when unused. This can be re-configured to GPIO12.
LDO_1V5	4	O	—	Output of the CORE LDO. Bypass with capacitance C_{LDO_1V5} to GND. This pin cannot source current to external circuits.
LDO_3V3	1	O	—	Output of supply switched from VIN_3V3 or VBUS LDO. Bypass with capacitance C_{LDO_3V3} to GND.
PP5V	28, 29	I	—	5-V System Supply to VBUS, supply for CCy pins as VCONN.
VSYS	19	I	—	High-voltage sinking node in the system. It is used to implement reverse-current-protection (RCP) for the external sinking paths controlled by GATE_VSYS.
VBUS	26, 27	I/O	—	5-V to 20-V input. Bypass with capacitance C_{VBUS} to GND.
VIN_3V3	32	I	—	Supply for core circuitry and I/O. Bypass with capacitance CVIN_3V3 to GND.

(1) I = input, O = output, I/O = input and output, GPIO = general purpose digital input and output

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Input voltage range (2)	PP5V	–0.3	6	V
	VIN_3V3	–0.3	4	
	ADCIN1, ADCIN2	–0.3	4	
	VSYS, VBUS(4)	–0.3	28	V
	CC1, CC2 (4)	–0.5	26	
	GPIOx	-0.3	6.0	
	I2C_EC_SDA, I2C_EC_SCL, $\overline{\text{I2C_EC_IRQ}}$, I2C2s_SDA, I2C2s_SCL, $\overline{\text{I2C2s_IRQ}}$, I2C3m_SDA, I2C3m_SCL , $\overline{\text{I2C3m_IRQ}}$	–0.3	4	
Output voltage range (2)	LDO_1V5(3)	–0.3	2	V
	LDO_3V3(3)	–0.3	4	
Output voltage range (2)	GATE_VBUS, GATE_VSYS(3)	–0.3	40	V
V_{GS}	V_{GATE_VBUS} - V_{VBUS}, V_{GATE_SYS} - V_{VSYS}	–0.5	12	V
Source current	Source or sink current VBUS		internally limited	A
	Positive source current on CC1, CC2		1	
	Positive sink current on CC1, CC2 while VCONN switch is enabled		1	
	positive sink current for I2C_EC_SDA, I2C_EC_SCL, I2C2s_SDA, I2C2s_SCL , I2C3m_SDA, I2C3m_SCL		internally limited	
	positive source current for LDO_3V3, LDO_1V5		internally limited	
Source current	GPIOx		0.005	A
T_J Operating junction temperature		–40	175	°C
T_{STG} Storage temperature		–55	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) All voltage values are with respect to network GND. Connect the GND pin directly to the GND plane of the board.
(3) Do not apply voltage to these pins.
(4) A TVS with a break down voltage falling between the Recommended max and the Abs max value is recommended such as TVS2200.

6.2 ESD Ratings

PARAMETER		TEST CONDITIONS	VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_I	Input voltage range (1)	VIN_3V3	3.0	3.6	V
		PP5V	4.9	5.5	
		VBUS	4	22	
		VSYS	0	22	
V_{IO}	I/O voltage range (1)	I2Cx_SDA, I2Cx_SCL, $\overline{\text{I2Cx\_IRQ}}$, ADCIN1, ADCIN2	0	3.6	V
		GPIOx	0	5.5	
		CC1, CC2	0	5.5	
I_O	Output current (from PP5V)	VBUS		3	A
		CC1, CC2		315	mA
I_O	Output current (from LDO_3V3)	GPIOx		1	mA
I_O	Output current (from VBUS LDO)	sum of current from LDO_3V3 and GPIOx		5	mA
T_A	Ambient operating temperature	$I_{PP\_5V} \le 1.5$ A, $I_{PP\_CABLE} \le 315$ mA	–40	105	°C
		$I_{PP\_5V} \le 3$ A, $I_{PP\_CABLE} \le 315$ mA	–40	85	
T_J	Operating junction temperature		–40	125	°C

(1) All voltage values are with respect to network GND. All GND pins must be connected directly to the GND plane of the board.

6.4 Recommended Capacitance

over operating free-air temperature range (unless otherwise noted)

PARAMETER(1)		VOLTAGE RATING	MIN	NOM	MAX	UNIT
C_{VIN_3V3}	Capacitance on VIN_3V3	6.3 V	5	10		µF
C_{LDO_3V3}	Capacitance on LDO_3V3	6.3 V	5	10	25	µF
C_{LDO_1V5}	Capacitance on LDO_1V5	4 V	4.5		12	µF
C_{VBUS}	Capacitance on VBUS(4)	25 V	1	4.7	10	µF
C_{PP5V}	Capacitance on PP5V	10 V	120(2)			µF
C_{VSYS}	Capacitance on VSYS Sink from VBUS	25 V		47	100	µF
C_{CCy}	Capacitance on CCy pins(3)	6.3 V	200	400	480	pF

(1) Capacitance values do not include any derating factors. For example, if 5.0 µF is required and the external capacitor value reduces by 50% at the required operating voltage, then the required external capacitor value would be 10 µF.
(2) This is a requirement from USB PD (cSrcBulkShared) for multi-port systems. Keep at least 10 µF tied directly to PP5V.
(3) This includes all external capacitance to the Type-C receptacle.
(4) The device can be configured to quickly disable the sinking power path upon certain events. When such a configuration is used, a capacitance on the higher side of this range is recommended.

6.5 Thermal Information

THERMAL METRIC(1)		TPS65992S QFN (RSM) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.5	°C/W
$R_{\theta JC}$ (top)	Junction-to-case (top) thermal resistance	24.5	°C/W
$R_{\theta JC}$	Junction-to-board (bottom) thermal resistance	2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	9.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W

THERMAL METRIC(1)		TPS65992S QFN (RSM) 32 PINS	UNIT
ψ_{JB}	Junction-to-board characterization parameter	9.7	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.6 Power Supply Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN_3V3, VBUS						
V_{VBUS_UVLO}	VBUS UVLO threshold.	rising	3.6		3.9	V
		falling	3.5		3.8	
		hysteresis		0.1		
V_{VIN3V3_UVLO}	voltage required on VIN_3V3 for power on	rising, V_{VBUS}=0	2.56	2.66	2.76	V
		falling, V_{VBUS}=0	2.44	2.54	2.64	
		hysteresis		0.12		
LDO_3V3, LDO_1V5						
V_{LDO_3V3}	voltage on LDO_3V3	V_{VIN_3V3} = 0V, 10 µA ≤ I_{LOAD} ≤ 18 mA, V_{VBUS} ≥ 3.9V	3.0	3.4	3.6	V
R_{LDO_3V3}	Rdson of VIN_3V3 to LDO_3V3	I_{LDO_3V3}=50mA			1.4	Ω
V_{LDO_1V5}	voltage on LDO_1V5	up to maximum internal loading condition.	1.49	1.5	1.65	V

6.7 Power Consumption

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V, no GPIO loading

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{VIN\_3V3,ActSrc}$	current into VIN_3V3	Active Source mode: V_{VBUS}=5.0V, V_{VIN_3V3}=3.3V		3		mA
$I_{VIN\_3V3,ActSnk}$	current into VIN_3V3	Active Sink mode: 22V ≥ V_{VBUS} ≥ 4.0V, V_{VIN_3V3}=3.3V		3	6	mA
$I_{VIN\_3V3,IdlSrc}$	current into VIN_3V3	Idle Source mode: V_{VBUS}=5.0V, V_{VIN_3V3}=3.3V		1.0		mA
$I_{VIN\_3V3,IdlSnk}$	current into VIN_3V3	Idle Sink mode: 22V ≥ V_{VBUS} ≥ 4.0V, V_{VIN_3V3}=3.3V		1.0		mA
$P_{MstbySnk}$	Power drawn into PP5V and VIN_3V3 in Modern Standby Sink Mode	CCm floating, V_{CCn}=0.4V, V_{PP5V} = 5V, V_{VIN_3V3}=3.3V, V_{VBUS}=5.0V, GATE_VBUS, GATE_VSYS disabled, and T_J=25ºC		4.1		mW
$P_{MstbySrc}$	Power drawn into PP5V and VIN_3V3 in Modern Standby Source Mode	CCm floating, CCn tied to GND through 5.1kΩ, V_{PP5V} = 5V, V_{VIN_3V3}=3.3V, I_{VBUS}=0, T_J=25ºC		4.5		mW
$I_{PP5V,Sleep}$	current into PP5V	Sleep mode: V_{VBUS}=0V, V_{VIN_3V3}=3.3V		2		µA
$I_{VIN\_3V3,Sleep}$	current into VIN_3V3	Sleep mode: V_{VBUS}=0V, V_{VIN_3V3}=3.3V		56		µA

6.8 PP_5V Power Switch Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PP_5V}	Resistance from PP5V to VBUS	I_{LOAD} = 3 A, T_J=25ºC			45	mΩ
R_{PP_5V}	Resistance from PP5V to VBUS	I_{LOAD} = 3 A, T_J=95ºC		45	60	mΩ
R_{PP_5V}	Resistance from PP5V to VBUS	I_{LOAD} = 3 A, T_J=125ºC		45	65	mΩ
I_{PP5V_REV}	VBUS to PP5V leakage current	V_{PP5V} = 0V, V_{VBUS} = 5.5V, PP_5V disabled, T_J≤85ºC, measure I_{PP5V}			5	µA

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{PP5V_FWD}	PP5V to VBUS leakage current	V_{PP5V} = 5.5V, V_{VBUS} = 0V, PP_5V disabled, T_J≤85ºC, measure I_{VBUS}			15	µA
I_{LIM5V}	Current limit setting	Configure to setting 0	1.15		1.36	A
I_{LIM5V}	Current limit setting	configure to setting 1	1.61		1.90	A
I_{LIM5V}	Current limit setting	configure to setting 2	2.3		2.70	A
I_{LIM5V}	Current limit setting	configure to setting 3	3.04		3.58	A
I_{LIM5V}	Current limit setting	configure to setting 4	3.22		3.78	A
I_{VBUS}	PP5V to VBUS current sense accuracy	3.64A ≥ I_{VBUS} ≥ 1A	3.05	3.5	3.75	A/V
$V_{PP\_5V\_RCP}$	RCP clears and PP_5V starts turning on when V_{VBUS} – V_{PP5V} < $V_{PP\_5V\_RCP}$. Measure V_{VBUS} – V_{PP5V}		10		20	mV
$t_{iOS\_PP\_5V}$	response time to VBUS short circuit	VBUS to GND through 10mΩ, C_{VBUS}=0		1.15		µs
$t_{PP\_5V\_ovp}$	response time to V_{VBUS} > $V_{OVP4RCP}$	Enable PP_5V, I_{RpDef} being drawn from PP5V, configure $V_{OVP4RCP}$ to setting 2, ramp V_{VBUS} from 4V to 20V at 100 V/ms, C_{PP5V} = 2.5 µF, measure time from OVP detection until reverse current < 100 mA		4.5		µs
$t_{PP\_5V\_uvlo}$	response time to V_{PP5V} < V_{PP5V_UVLO}, PP_VBUS is deemed off when V_{VBUS} < 0.8V	R_L = 100 Ω, no external capacitance on VBUS		4		µs
$t_{PP\_5V\_rcp}$	response time to V_{PP5V} < V_{VBUS}+$V_{PP\_5V\_RCP}$	V_{PP5V}=5.5V, I_{RpDef} being drawn from PP5V, enable PP_5V, configure $V_{OVP4RCP}$ to setting 2, ramp V_{VBUS} from 4V to 21.5V at 10 V/µs, measure V_{PP5V}. C_{PP5V} = 104 µF, C_{VBUS}=10µF, measure time from RCP detection until reverse current < 100 mA.		0.7		µs
t_{FRS_on}	Time allowed to enable the pass FET in PP_5V with 3A current limit.	Initial V_{VBUS} = 0V, 2µF ≤ C_{VBUS} ≤ 20µF, current limit configured to 3A setting 0 ≤ I_{VBUS} ≤ 0.5 A, measure time from when V_{CCx} has been below V_{FRS} for t_{FRS_DET} FET is deemed enabled when V_{VBUS} > 4.75V.			150	µs
t_{ILIM}	Current limit deglitch time			5.1		ms
t_{ON}	from enable signal to VBUS at 90% of final value	R_L = 100Ω, V_{PP5V} = 5V, C_L=0	2.3	3.3	4.3	ms
t_{OFF}	from disable signal to VBUS at 10% of final value	R_L = 100Ω, V_{PP5V} = 5V, C_L=0	0.20	0.35	0.5	ms
t_{RISE}	VBUS from 10% to 90% of final value	R_L = 100Ω, V_{PP5V} = 5V, C_L=0	1	1.4	1.8	ms
t_{FALL}	VBUS from 90% to 10% of initial value	R_L = 100Ω, V_{PP5V} = 5V, C_L=0	0.06	0.1	0.14	ms

6.9 PP_EXT Power Switch Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{GATE_ON}	Gate driver sourcing current	0 ≤ V_{GATE_VSYS}-V_{VSYS} ≤ 6 V, V_{VSYS} ≤ 22 V, V_{VBUS} > 4 V, measure I_{GATE_VSYS}	8.5		11.5	µA
		0 ≤ V_{GATE_VBUS}-V_{VBUS} ≤ 6 V, 4 V ≤ V_{VBUS} ≤ 22 V, measure I_{GATE_VBUS}	8.5		11.5	µA
V_{GATE_ON}	sourcing voltage (ON)	0 ≤ V_{VSYS} ≤ 22 V, I_{GATE_VSYS} < 4 µA, measure V_{GATE_VSYS} – V_{VSYS}, V_{VBUS} > 4 V.	6		12	V
		4 V ≤ V_{VBUS} ≤ 22 V, I_{GATE_VBUS} < 4 µA, measure V_{GATE_VBUS} – V_{VBUS}.	6		12	V
V_{RCP}	comparator mode RCP threshold, V_{VSYS} - V_{VBUS}.	setting 0, 4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	2	6	10	mV
		setting 1, 4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	4	8	12	mV
		setting 2, 4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	6	10	14	mV
		setting 3, 4 V ≤ V_{VBUS} ≤ 22 V, V_{VIN_3V3} ≤ 3.63 V	8	12	16	mV
I_{GATE_OFF}	Sinking strength	normal turnoff: V_{VSYS} = 5V, V_{GATE_VSYS}=6V, measure I_{GATE_VSYS}	13			µA
		normal turnoff: V_{VBUS} = V_{VSYS} = 5V, V_{GATE_VBUS}=6V, measure I_{GATE_VBUS}	13			µA
R_{GATE_FSD}	Sinking strength	fast turnoff: V_{VSYS} = 5V, V_{GATE_VSYS}=6V, assert PPHV1_FAST_DISABLE, measure R_{GATE_VSYS}			85	Ω
		fast turnoff: V_{VBUS} = V_{VSYS} = 5V, V_{GATE_VBUS}=6V, assert PPHV1_FAST_DISABLE, measure R_{GATE_VBUS}			85	Ω
$R_{GATE\_OFF\_UVLO}$	Sinking strength in UVLO (safety)	V_{VIN_3V3}=0V, V_{VBUS}=3.0V, V_{GATE_VSYS}=0.1V, measure resistance from GATE_VSYS to GND			1.5	MΩ
SS	soft start slew rate for GATE_VSYS, setting 0	4 V ≤ V_{VBUS} ≤ 22 V, I_{LOAD} = 100 mA, 500pF < C_{GATE_VSYS} < 16 nF, measure slope from 10% to 90% of final VSYS value,	0.35	0.41	0.47	V/ms
	soft start slew rate for GATE_VSYS, setting 1		0.67	0.81	0.95	
	soft start slew rate for GATE_VSYS, setting 2		1.33	1.7	2.0	
	soft start slew rate for GATE_VSYS, setting 3		2.8	3.3	3.80	
$t_{GATE\_VBUS\_OFF}$	Time allowed to disable the external FET via GATE_VBUS in normal shutdown mode.(1)	V_{VBUS}=20V, Q_G of external FET = 40nC or C_{GATE_VBUS} < 3nF, Gate is off when V_{GATE_VBUS} – V_{VBUS} < 1V		450	4000	µs

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{GATE\_VBUS\_OVP}$	Time allowed to disable the external FET via GATE_VBUS in fast shutdown mode ($V_{OVP4RCP}$ exceeded).(1)	OVP: $V_{OVP4RCP}$= setting 57, V_{VBUS}=20V initially, then raised to 23V in 50ns, Q_G of external FET = 40nC or C_{GATE_VBUS} < 3nF, Gate is off when V_{GATE_VBUS} – V_{VBUS} < 1V		3	5	µs
$t_{GATE\_VBUS\_RCP}$	Time allowed to disable the external FET via GATE_VBUS in fast shutdown mode (V_{RCP} exceeded), this includes the response time of the comparator. (1)	RCP: V_{RCP}= setting 0, V_{VBUS}=5V, V_{VSYS}=5V initially, then raised to 5.5V in 50ns, Q_G of external FET = 40nC or C_{GATE_VBUS} < 3nF, Gate is off when V_{GATE_VBUS} – V_{VBUS} < 1V		1	2	µs
$t_{GATE\_VSYS\_OFF}$	Time allowed to disable the external FET via GATE_VSYS in normal shutdown mode(1)	V_{VSYS}=20V, Q_G of external FET = 40nC or C_{GATE_VBUS} < 3nF, Gate is off when V_{GATE_VSYS} – V_{VSYS} < 1V		450	4000	µs
$t_{GATE\_VSYS\_FSD}$	Time allowed to disable the external FET via GATE_VSYS in fast shutdown mode (OVP or FRS)(1)	V_{VBUS}=20V initially, then raised to 23V in 50ns, Q_G of external FET = 40nC or C_{GATE_VBUS} < 3nF, Gate is off when V_{GATE_VSYS} – V_{VSYS} < 1V, r_{OVP}=1		0.25	20	µs
$t_{GATE\_VBUS\_ON}$	time to enable GATE_VBUS (1)	measure time from when V_{GS}=0V until V_{GS}>3V, where V_{GS}=V_{GATE_VBUS} – V_{VBUS}		0.25	2	ms

(1) These values depend upon the characteristics of the external N-ch MOSFET. The typical values were measured when Px_GATE_VSYS and Px_GATE_VBUS were used to drive two CSD17571Q2 in common drain back-to-back configuration.

6.10 Power Path Supervisory

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{OVP4RCP}$	VBUS over voltage protection for RCP programmable range	OVP detected when V_{VBUS} > $V_{OVP4RCP}$	5.0		24	V
$V_{OVP4RCPH}$	hysteresis		1.75	2	2.25	%
r_{OVP}	ratio of OVP4RCP input used for OVP4VSYS comparator. r_{OVP}*$V_{OVP4VSYS}$ = $V_{OVP4RCP}$	setting 0		1		V/V
		setting 1		0.95		V/V
		setting 2		0.90		V/V
		setting 3		0.875		V/V
$V_{OVP4VSYS}$	VBUS over voltage protection range for VSYS protection	OVP detected when r_{OVP}*V_{VBUS} > $V_{OVP4RCP}$	5		27.5	V
$V_{OVP4VSYS}$	hysteresis	VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP} setting 0	1.75	2	2.25	%
		VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP} setting 1	1.8	2.1	2.4	
		VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP} setting 2	1.9	2.2	2.5	
		VBUS falling, % of $V_{OVP4VSYS}$, r_{OVP} setting 3	2	2.3	2.6	
V_{PP5V_UVLO}	Voltage required on PP5V	rising	3.9	4.1	4.3	V
		falling	3.8	4.0	4.2	
		hysteresis		0.1		

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{DSCH}	VBUS discharge current	V_{VBUS} = 22V, measure I_{VBUS}	4		15	mA

6.11 CC Cable Detection Parameters

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Type-C Source (Rp pull-up)						
$V_{OC\_3.3}$	Unattached CCy open circuit voltage while Rp enabled, no load	V_{LDO_3V3} > 2.302 V, R_{CC} = 47 kΩ	1.85			V
V_{OC_5}	Attached CCy open circuit voltage while Rp enabled, no load	V_{PP5V} > 3.802 V, R_{CC} = 47 kΩ	2.95			V
I_{Rev}	Unattached reverse current on CCy	V_{CCy} = 5.5V, V_{CCx} = 0V, $V_{LDO\_3V3\_UVLO}$ < V_{LDO_3V3} < 3.6 V, V_{PP5V} = 3.8 V , measure current into CCy			10	µA
		V_{CCy} = 5.5V, V_{CCx} = 0V, $V_{LDO\_3V3\_UVLO}$ < V_{LDO_3V3} < 3.6 V, V_{PP5V} = 0, T_J≤85ºC, measure current into CCy			10	
I_{RpDef}	current source - USB Default	0 < V_{CCy} < 1.0 V, measure I_{CCy}	64	80	96	µA
$I_{Rp1.5}$	current source - 1.5A	4.75 V < V_{PP5V} < 5.5 V, 0 < V_{CCy} < 1.5 V, measure I_{CCy}	166	180	194	µA
$I_{Rp3.0}$	current source - 3.0A	4.75 V < V_{PP5V} < 5.5 V, 0 < V_{CCy} < 2.45 V, measure I_{CCy}	304	330	356	µA
Type-C Sink (Rd pull-down)						
V_{SNK1}	Open/Default detection threshold when Rd applied to CCy	rising	0.2		0.24	V
V_{SNK1}	Open/Default detection threshold when Rd applied to CCy	falling,	0.16		0.20	V
	hysteresis			0.04		V
V_{SNK2}	Default/1.5A detection threshold	falling,	0.62		0.68	V
V_{SNK2}	Default/1.5A detection threshold	rising,	0.63	0.66	0.69	V
	hysteresis			0.01		V
V_{SNK3}	1.5A/3.0A detection threshold when Rd applied to CCy	falling,	1.17		1.25	V
V_{SNK3}	1.5A/3.0A detection threshold when Rd applied to CCy	rising,	1.22		1.3	V
	hysteresis			0.05		V
R_{SNK}	Rd pulldown resistance	0.25 V ≤ V_{CCy} ≤ 2.1 V, measure resistance on CCy	4.6		5.6	kΩ
R_{VCONN_DIS}	VCONN discharge resistance	0V ≤ V_{CCy} ≤ 5.5 V, measure resistance on CCy	4.0		6.12	kΩ
V_{CLAMP}	Dead battery Rd clamp	V_{VIN_3V3}=0V, 64 µA < I_{CCy}<96 µA	0.25		1.32	V
		V_{VIN_3V3}=0V, 166 µA < I_{CCy}<194 µA	0.65		1.32	
		V_{VIN_3V3}=0V, 304 µA < I_{CCy}< 356 µA	1.20		2.18	
R_{Open}	resistance from CCy to GND when configured as open.	V_{VBUS} = 0, V_{VIN_3V3}=3.3V, V_{CCy}=5 V, measure resistance on CCy	500			kΩ
		V_{VBUS} = 5V, V_{VIN_3V3} = 0, V_{CCy}=5 V, measure resistance on CCy	500			kΩ

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FRS}	Fast Role swap request voltage detection threshold on CCy (falling)		495	515	535	mV
V_{FRS}	hysteresis			0.01		V
t_{FRS_DET}	Fast role swap signal detection time	V_{CCy} must be below V_{FRS} for at least this long before the FRS signal is detected	30		35	µs
t_{FRS_Resp}	response time of the Fast role swap comparator (rising)	V_{CCy} rises from 0.24V to 0.64V			0.6	µs

6.12 CC VCONN Parameters

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{PP_CABLE}	Rdson of the VCONN path	V_{PP5V}=5V, I_L = 250 mA, measure resistance from PP5V to CCy			1.2	Ω
I_{LIMVC}	short circuit current limit	setting 0, V_{PP5V}=5V, R_L=10mΩ , measure I_{CCy}	350	410	470	mA
I_{LIMVC}	short circuit current limit	setting 1, V_{PP5V}=5V, R_L=10mΩ , measure I_{CCy}	540	600	660	mA
$I_{CC2PP5V}$	Reverse leakage current through VCONN FET	VCONN disabled, T_J ≤ 85 ºC, V_{CCy} = 5.5 V, V_{PP5V}=0 V, V_{VBUS}=5V, LDO forced to draw from VBUS, measure I_{CCy}			10	µA
V_{VC_OVP}	Over-voltage protection threshold for PP_CABLE	V_{PP5V} rising	5.6	5.9	6.2	V
V_{VC_RCP}	Reverse current protection threshold for PP_CABLE, sourcing VCONN through CCx	V_{PP5V} ≥ 4.9 V, V_{CCy} = V_{PP5V}, V_{CCx} rising	60	200	340	mV
		V_{PP5V} ≥ 4.9 V, V_{CCy} ≤ 4 V, V_{CCx} rising	210	340	470	mV
t_{VCILIM}	Current clamp deglitch time			1.3		ms
$t_{PP\_CABLE\_FSD}$	Time to disable PP_CABLE after V_{PP5V} > V_{VC_OVP} or V_{CCx} - V_{PP5V} > V_{VC_RCP}	C_L=0		0.5		µs
$t_{PP\_CABLE\_off}$	from disable signal to CCy at 10% of final value	I_L = 250 mA, V_{PP5V} = 5V, C_L=0	100	200	300	µs
$t_{iOS\_PP\_CABLE}$	response time to short circuit	V_{PP5V}=5V, for short circuit R_L = 10mΩ.		2		µs

6.13 CC PHY Parameters

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V or V_{VBUS} ≥ 3.9 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Transmitter						
V_{TXHI}	Transmit high voltage on CCy	Standard External load	1.05	1.125	1.2	V
V_{TXLO}	Transmit low voltage on CCy	Standard External load	-75		75	mV
Z_{DRIVER}	Transmit output impedance while driving the CC line using CCy	measured at 750 kHz	33	54	75	Ω
t_{Rise}	Rise time. 10 % to 90 % amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{CCy}= 520 pF	300			ns

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V or V_{VBUS} ≥ 3.9 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{Fall}	Fall time. 90 % to 10 % amplitude points on CCy, minimum is under an unloaded condition. Maximum set by TX mask	C_{CCy}= 520 pF	300			ns
V_{PHY_OVP}	OVP detection threshold for USB PD PHY.	0 ≤ V_{VIN_3V3} ≤ 3.6 V, 0 ≤ V_{PP5V} ≤ 5.5 V, V_{VBUS}≥4 V. Initially V_{CC1} ≤ 5.5 V and V_{CC2} ≤ 5.5 V, then V_{CCx} rises.	5.5		8.5	V
Receiver						
Z_{BMCRX}	receiver input impedance on CCy	Does not include pull-up or pulldown resistance from cable detect. Transmitter is Hi-Z.	1			MΩ
C_{CC}	Receiver capacitance on CCy(1)	Capacitance looking into the CC pin when in receiver mode			120	pF
$V_{RX\_SNK\_R}$	Rising threshold on CCy for receiver comparator	sink mode (rising)	499	525	551	mV
$V_{RX\_SRC\_R}$	Rising threshold on CCy for receiver comparator	source mode (rising)	784	825	866	mV
$V_{RX\_SNK\_F}$	Falling threshold on CCy for receiver comparator	sink mode (falling)	230	250	270	mV
$V_{RX\_SRC\_F}$	Falling threshold on CCy for receiver comparator	source mode (falling)	523	550	578	mV

(1) C_{CC} includes only the internal capacitance on a CCy pin when the pin is configured to be receiving BMC data. External capacitance is needed to meet the required minimum capacitance per the USB-PD Specifications (cReceiver). Therefore, TI recommends adding C_{CCy} externally.

6.14 Thermal Shutdown Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SD_MAIN}	Temperature shutdown threshold	Temperature rising	145	160	175	°C
		hysteresis		20		°C
T_{SD_PP5V}	Temperature controlled shutdown threshold. The PP_5V and PP_CABLE power paths have local sensors that disables them when this temperature is exceeded.	Temperature rising	135	150	165	°C
		hysteresis		10		°C

6.15 ADC Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
LSB	least significant bit	3.6V max scaling, voltage divider of 3		14		mV
		25.2V max scaling, voltage divider of 21		98		mV
		4.07A max scaling		16.5		mA
GAIN_ERR	Gain error	0.05V ≤ V_{ADCINx} ≤ 3.6V, V_{ADCINx} ≤ V_{LDO_3V3}	–2.7		2.7	%
		0.05V ≤ V_{GPIOx} ≤ 3.6V, V_{GPIOx} ≤ V_{LDO_3V3}				
		2.7V ≤ V_{LDO_3V3} ≤ 3.6V	–2.4		2.4	
		0.6V ≤ V_{VBUS} ≤ 22V	–2.1		2.1	
		1A ≤ I_{VBUS} ≤ 3A	–2.1		2.1	

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VOS_ERR	Offset error(1)	0.05V ≤ V_{ADCINx} ≤ 3.6V, V_{ADCINx} ≤ V_{LDO_3V3}	–4.1		4.1	mV
		0.05V ≤ V_{GPIOx} ≤ 3.6V, V_{GPIOx} ≤ V_{LDO_3V3}				
		2.7V ≤ V_{LDO_3V3} ≤ 3.6V	-4.5		4.5	
		0.6V ≤ V_{VBUS} ≤ 22V	-4.1		4.1	
		1A ≤ I_{VBUS} ≤ 3A	-4.5		4.5	mA

(1) The offset error is specified after the voltage divider.

6.16 Input/Output (I/O) Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
GPIO0-7 (Inputs)						
GPIO_VIH	GPIOx high-Level input voltage	V_{LDO_3V3} = 3.3V	1.3			V
GPIO_VIL	GPIOx low-level input voltage	V_{LDO_3V3} = 3.3V			0.54	V
GPIO_HYS	GPIOx input hysteresis voltage	V_{LDO_3V3} = 3.3V	0.09			V
GPIO_ILKG	GPIOx leakage current	V_{GPIOx} = 3.45 V	–1		1	µA
GPIO_RPU	GPIOx internal pull-up	pull-up enabled	50	100	150	kΩ
GPIO_RPD	GPIOx internal pull-down	pull-down enabled	50	100	150	kΩ
GPIO_DG	GPIOx input deglitch			20		ns
GPIO0-7 (Outputs)						
GPIO_VOH	GPIOx output high voltage	V_{LDO_3V3} = 3.3V, I_{GPIOx}= -2mA	2.9			V
GPIO_VOL	GPIOx output low voltage	V_{LDO_3V3} = 3.3V, I_{GPIOx}=2mA			0.4	V
ADCIN1, ADCIN2						
ADCIN_ILKG	ADCINx leakage current	V_{ADCINx} = 3.45 V, V_{VIN_3V3} = 3.3	–1		1	µA
t_{BOOT}	time from LDO_3V3 going high until ADCINx is read for configuration			10		ms

6.17 BC1.2 Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
DATA CONTACT DETECT						
I_{DP_SRC}	DCD source current	V_{LDO_3V3} = 3.3 V	7	10	13	µA
R_{DM_DWN}	DCD pulldown resistance	V_{GPIO5} = 3.6V	14.25	20	24.8	kΩ
R_{DP_DWN}	DCD pulldown resistance	V_{GPIO4} = 3.6V	14.25	20	24.8	kΩ
V_{LGC_HI}	Threshold for no connection	V_{GPIO4} ≥ V_{LGC_HI}, V_{LDO_3V3} = 3.3 V, R_{GPIO4}=300kΩ	2		3.6	V
V_{LGC_LO}	Threshold for connection	V_{GPIO5} ≤ V_{LGC_LO}, V_{LDO_3V3}=3.3V, R_{GPIO4}=24.8kΩ	0		0.8	V
Advertisement and Detection						
V_{DX_SRC}	Source voltage	C_{GPIO4} ≤ 600 pF	0.55	0.6	0.65	V
V_{DX_ILIM}	VDX_SRC current limit		250		400	µA
I_{DX_SNK}	Sink Current	V_{GPIO4} ≥ 250 mV	25	75	125	µA
I_{DX_SNK}	Sink Current	V_{GPIO5} ≥ 250 mV	25	75	125	µA

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DCP_DAT}	Dedicated Charging Port Resistance	0.5 V ≤ V_{USB_P} ≤ 0.7 V, 25 µA ≤ I_{USB_N} ≤ 175 µA			200	Ω

6.18 I2C Requirements and Characteristics

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\overline{\text{I2C\_EC\_IRQ}}$, $\overline{\text{I2C2s\_IRQ}}$						
OD_VOL_IRQ	Low level output voltage	I_{OL} = 2 mA			0.4	V
OD_LKG_IRQ	Leakage Current	Output is Hi-Z, V_{I2Cx_IRQ} = 3.45 V	–1		1	µA
I2C3m_IRQ						
IRQ_VIH	High-Level input voltage	V_{LDO_3V3} = 3.3V	1.3			V
IRQ_VIH_THRESH	High-Level input voltage threshold	V_{LDO_3V3} = 3.3V	0.72		1.3	V
IRQ_VIL	low-level input voltage	V_{LDO_3V3} = 3.3V			0.54	V
IRQ_VIL_THRESH	low-level input voltage threshold	V_{LDO_3V3} = 3.3V	0.54		1.08	V
IRQ_HYS	input hysteresis voltage	V_{LDO_3V3} = 3.3V	0.09			V
IRQ_DEG	input deglitch			20		ns
IRQ_ILKG	$\overline{\text{I2C3m\_IRQ}}$ leakage current	V_{I2C3m_IRQ} = 3.45 V	–1		1	µA
SDA and SCL Common Characteristics (Master, Slave)						
V_{IL}	Input low signal	V_{LDO_3V3}=3.3V,			0.54	V
V_{IH}	Input high signal	V_{LDO_3V3}=3.3V,	1.3			V
V_{HYS}	Input hysteresis	V_{LDO_3V3}=3.3V	0.165			V
V_{OL}	Output low voltage	I_{OL}=3 mA			0.36	V
I_{LEAK}	Input leakage current	Voltage on pin = V_{LDO_3V3}	–3		3	µA
I_{OL}	Max output low current	V_{OL}=0.4 V	15			mA
I_{OL}	Max output low current	V_{OL}=0.6 V	20			mA
t_f	Fall time from 0.7*V_{DD} to 0.3*V_{DD}	V_{DD} = 1.8V, 10 pF ≤ C_b ≤ 400 pF	12		80	ns
t_f	Fall time from 0.7*V_{DD} to 0.3*V_{DD}	V_{DD} = 3.3V, 10 pF ≤ C_b ≤ 400 pF	12		150	ns
t_{SP}	I2C pulse width surpressed				50	ns
C_I	pin capacitance (internal)				10	pF
C_b	Capacitive load for each bus line (external)				400	pF
SDA and SCL Standard Mode Characteristics (Slave)						
f_{SCLS}	Clock frequency for slave	V_{DD} = 1.8V or 3.3V			100	kHz
$t_{VD;DAT}$	Valid data time	Transmitting Data, V_{DD} = 1.8V or 3.3V, SCL low to SDA output valid			3.45	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting Data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			3.45	µs
SDA and SCL Fast Mode Characteristics (Slave)						
f_{SCLS}	Clock frequency for slave	V_{DD} = 1.8V or 3.3V	100		400	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 1.8V, SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			0.9	µs
SDA and SCL Fast Mode Plus Characteristics (Slave)						

Operating under these conditions unless otherwise noted: 3.0 V ≤ V_{VIN_3V3} ≤ 3.6 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCLS}	Clock frequency for Fast Mode Plus (1)	V_{DD} = 1.8V or 3.3V	400		1000	kHz
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 1.8V or 3.3V, SCL low to SDA output valid			0.55	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 1.8V or 3.3V, ACK signal from SCL low to SDA (out) low			0.55	µs
SDA and SCL Fast Mode Charactersistics (Master)						
f_{SCLM}	Clock frequency for master	V_{DD} = 3.3V (2)		400	410	kHz
		V_{DD} = 1.8V		390	400	
$t_{HD;STA}$	Start or repeated start condition hold time	V_{DD} = 3.3V	0.6			µs
t_{LOW}	Clock low time	V_{DD} = 3.3V	1.3			µs
t_{HIGH}	Clock high time	V_{DD} = 3.3V	0.6			µs
$t_{SU;STA}$	Start or repeated start condition setup time	V_{DD} = 3.3V	0.6			µs
$t_{SU;DAT}$	Serial data setup time	Transmitting data, V_{DD} = 3.3V	100			ns
$t_{SU;STO}$	Stop condition setup time	V_{DD} = 3.3V	0.6			µs
t_{BUF}	Bus free time between stop and start	V_{DD} = 3.3V	1.3			µs
$t_{VD;DAT}$	Valid data time	Transmitting data, V_{DD} = 3.3V, SCL low to SDA output valid			0.9	µs
$t_{VD;ACK}$	Valid data time of ACK condition	Transmitting data, V_{DD} = 3.3V, ACK signal from SCL low to SDA (out) low			0.9	µs

(1) Master must control f_{SCLS} to ensure t_{LOW} > $t_{VD;ACK}$.
(2) Measured as 400kHz when Rb=1kΩ and Cb=145 pF

6.19 Typical Characteristics

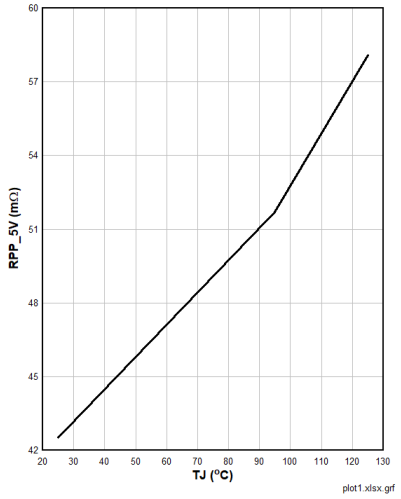


Figure 6-1. PP_5V Rdson vs. Temperature

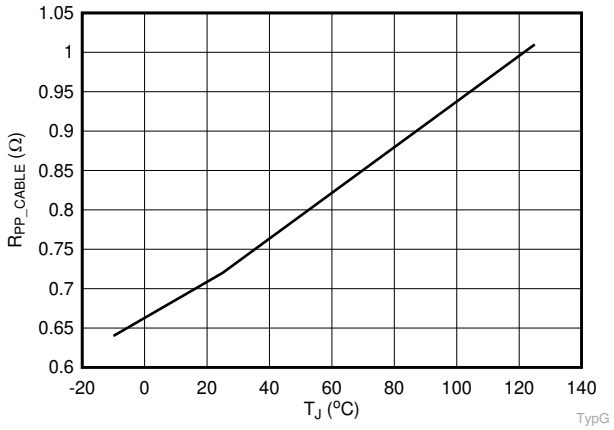


Figure 6-2. PP_CABLE Rdson vs. Temperature

6.19 Typical Characteristics (continued)

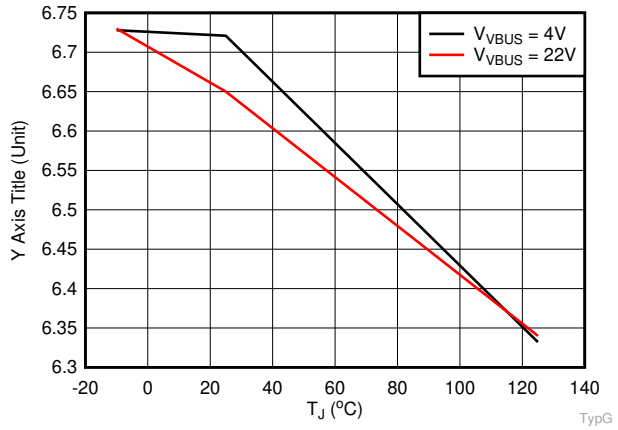


Figure 6-3. V_{RCP} vs. Temperature

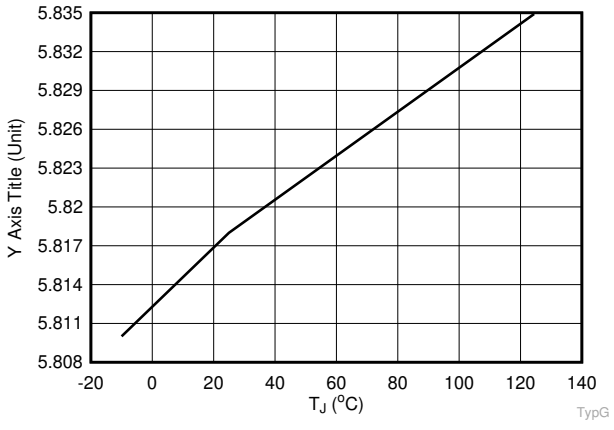


Figure 6-4. $V_{OVP4RCP}$ (Setting 2) vs. Temperature

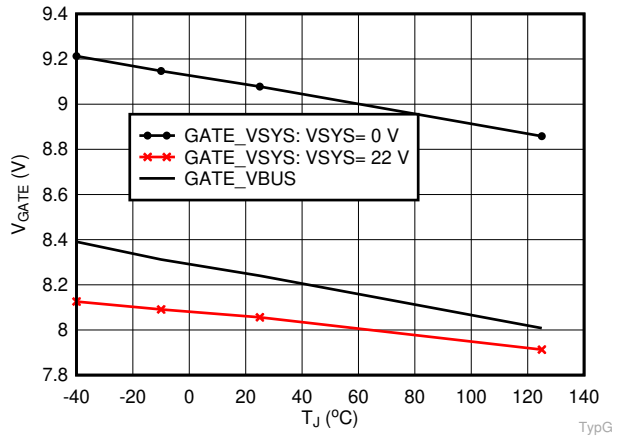


Figure 6-5. $V_{GATE\_VBUS\_ON}$ vs. Temperature

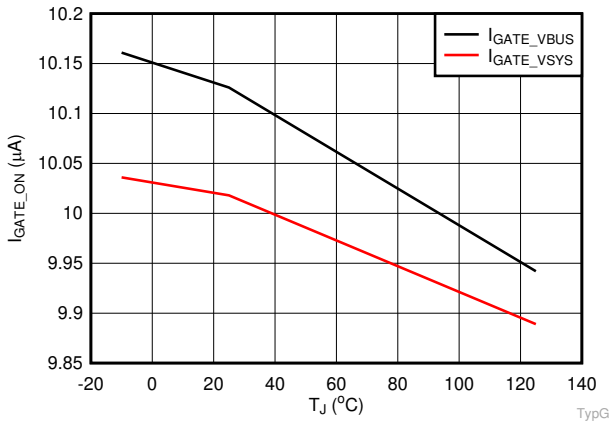


Figure 6-6. $V_{GATE\_VSYS\_ON}$ vs. Temperature

7 Parameter Measurement Information

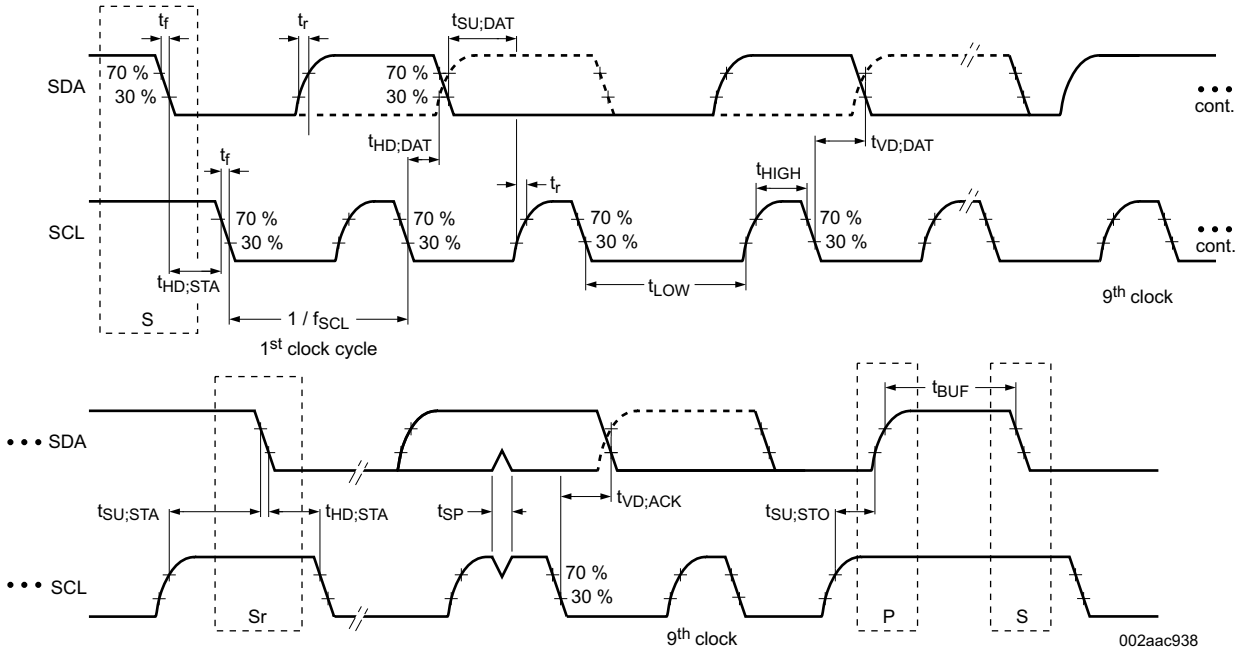


Figure 7-1. I²C Slave Interface Timing

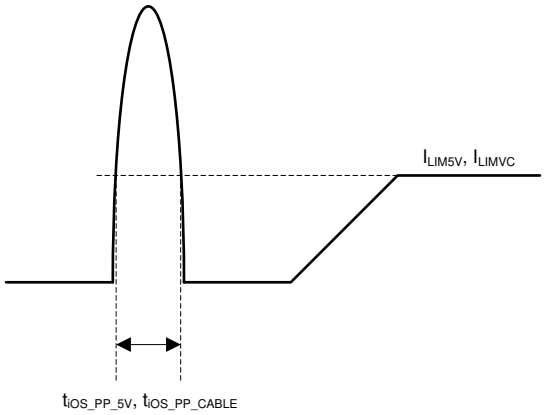


Figure 7-2. Short-Circuit Response Time for Internal Power Paths PP_5V and PP_CABLE

8 Detailed Description

8.1 Overview

The TPS65992SBG is a fully-integrated USB Power Delivery (USB-PD) management device providing cable plug and orientation detection for USB Type-C and PD receptacle. The TPS65992SBG communicates with the cable and another USB Type-C and PD device at the opposite end of the cable, enables integrated port power switch for sourcing, controls a high current port power switch for sinking and negotiates alternate modes . The TPS65992SBG may also control an attached super-speed multiplexer to simultaneously support USB data and DisplayPort video.

The TPS65992SBG is divided into several main sections: the USB-PD controller, the cable plug and orientation detection circuitry, the port power switches, the power management circuitry and the digital core.

The USB-PD controller provides the physical layer (PHY) functionality of the USB-PD protocol. The USB-PD data is output through either the CC1 pin or the CC2 pin, depending on the orientation of the reversible USB Type-C cable. For a high-level block diagram of the USB-PD physical layer, a description of its features and more detailed circuitry, see the *USB-PD Physical Layer* section.

The cable plug and orientation detection analog circuitry automatically detects a USB Type-C cable plug insertion and also automatically detects the cable orientation. For a high-level block diagram of cable plug and orientation detection, a description of its features and more detailed circuitry, see the *Cable Plug and Orientation Detection*.

The port power switches provide power to the VBUS pin and also to the CC1 or CC2 pins based on the detected plug orientation. For a high-level block diagram of the port power switches, a description of its features and more detailed circuitry, see the *Power Paths*.

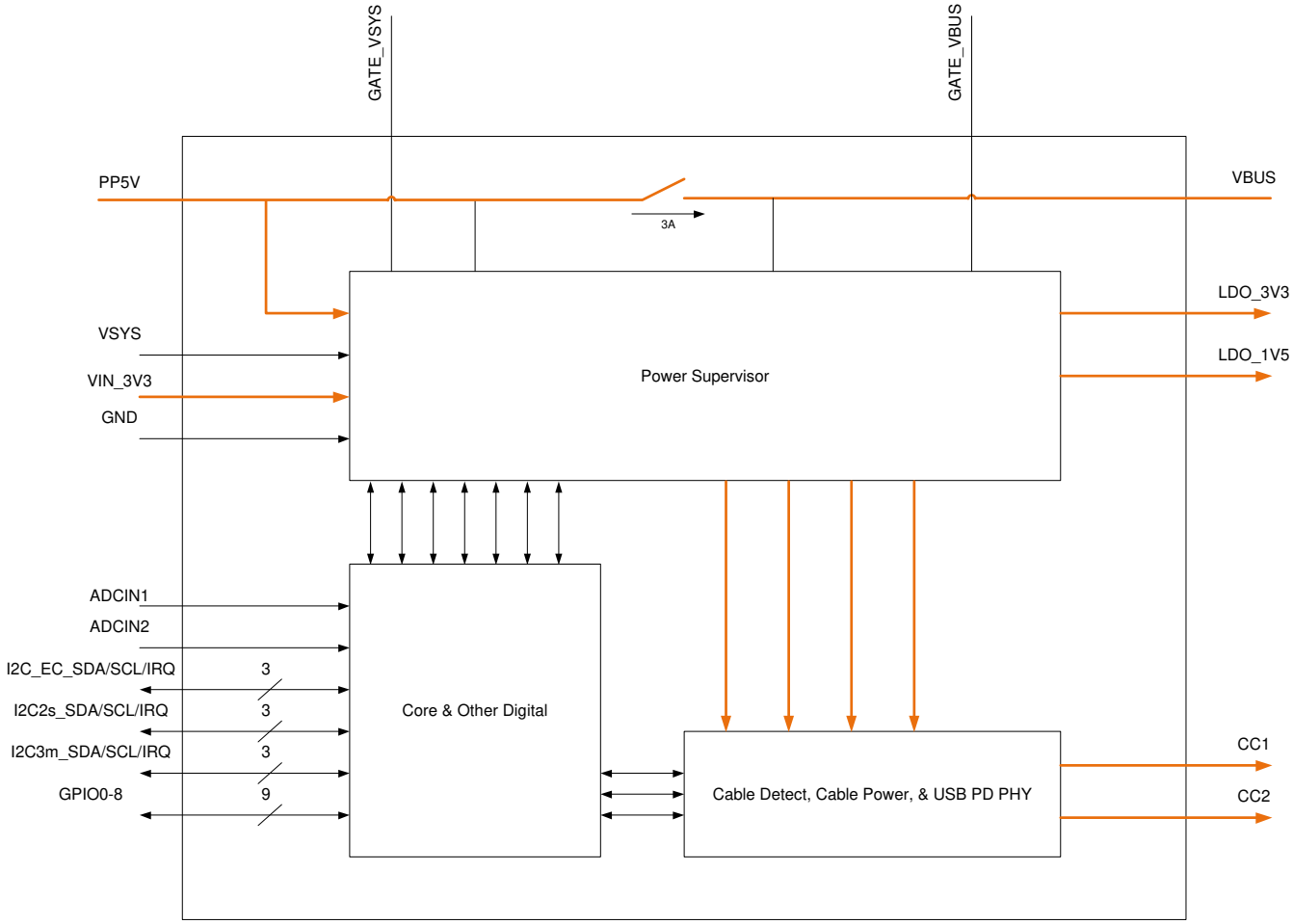
The power management circuitry receives and provides power to the TPS65992SBG internal circuitry and to the LDO_3V3 output. See the *Power Management* section for more information.

The digital core provides the engine for receiving, processing and sending all USB-PD packets as well as handling control of all other TPS65992SBG functionality. A portion of the digital core contains ROM memory which contains all the necessary firmware required to execute Type-C and PD applications. In addition, a section of the ROM, called boot code, is capable of initializing the TPS65992SBG, loading of device configuration information and loading any code patches into volatile memory in the digital core. For a high-level block diagram of the digital core, a description of its features and more detailed circuitry, see the *Digital Core* section.

The digital core of the TPS65992SBG also interprets and uses information provided by the analog-to-digital converter ADC (see the *ADC*), is configurable to read the status of general purpose inputs and trigger events accordingly, and controls general outputs which are configurable as push-pull or open-drain types with integrated pull-up or pull-down resistors. The TPS65992SBG has two I^2C slave ports to be controlled by host processors , and one I^2C master to write to and read from external slave devices such as multiplexor, retimer, or an optional external EEPROM memory (see the *I^2C Interface*).

The TPS65992SBG also integrates a thermal shutdown mechanism and runs off of accurate clocks provided by the integrated oscillator.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 USB-PD Physical Layer

Figure 8-1 shows the USB PD physical layer block surrounded by a simplified version of the analog plug and orientation detection block.

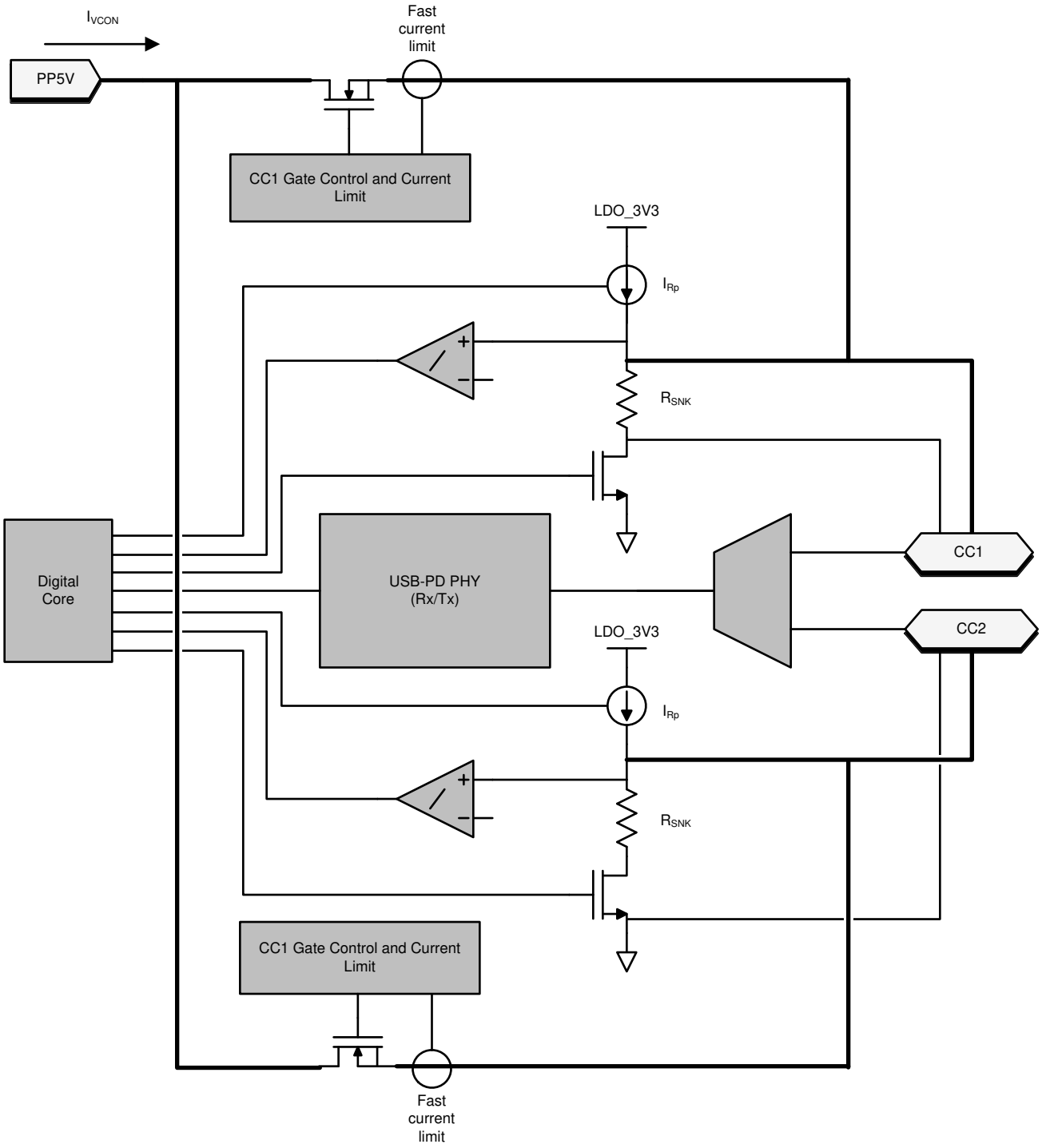


Figure 8-1. USB-PD Physical Layer and Simplified Plug and Orientation Detection Circuitry

USB-PD messages are transmitted in a USB Type-C system using a BMC signaling. The BMC signal is output on the same pin (CC1 or CC2) that is DC biased due to the Rp (or Rd) cable attach mechanism.

8.3.1.1 USB-PD Encoding and Signaling

Figure 8-2 illustrates the high-level block diagram of the baseband USB-PD transmitter. Figure 8-3 illustrates the high-level block diagram of the baseband USB-PD receiver.

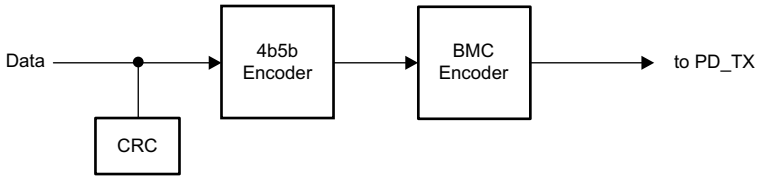


Figure 8-2. USB-PD Baseband Transmitter Block Diagram

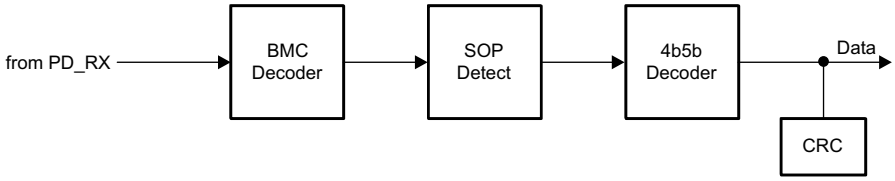


Figure 8-3. USB-PD Baseband Receiver Block Diagram

8.3.1.2 USB-PD Bi-Phase Marked Coding

The USB-PD physical layer implemented in the TPS65992SBG is compliant to the *USB-PD Specifications*. The encoding scheme used for the baseband PD signal is a version of Manchester coding called Biphase Mark Coding (BMC). In this code, there is a transition at the start of every bit time and there is a second transition in the middle of the bit cell when a 1 is transmitted. This coding scheme is nearly DC balanced with limited disparity (limited to 1/2 bit over an arbitrary packet, so a very low DC level). Figure 8-4 illustrates Biphase Mark Coding.

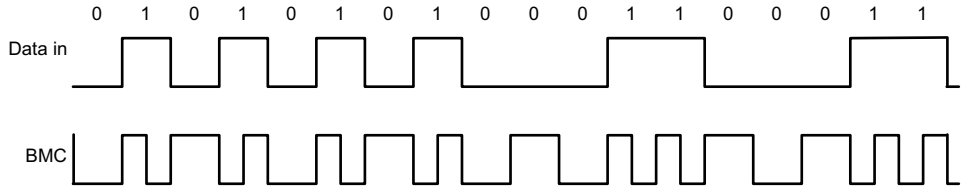


Figure 8-4. Biphase Mark Coding Example

The USB PD baseband signal is driven onto the CC1 or CC2 pin with a tri-state driver. The tri-state driver is slew rate to limit coupling to D+/D– and to other signal lines in the Type-C fully featured cables. When sending the USB-PD preamble, the transmitter starts by transmitting a low level. The receiver at the other end tolerates the loss of the first edge. The transmitter terminates the final bit by an edge to ensure the receiver clocks the final bit of EOP.

8.3.1.3 USB-PD Transmit (TX) and Receive (Rx) Masks

The USB-PD driver meets the defined USB-PD BMC TX masks. Since a BMC coded “1” contains a signal edge at the beginning and middle of the UI, and the BMC coded “0” contains only an edge at the beginning, the masks are different for each. The USB-PD receiver meets the defined USB-PD BMC Rx masks. The boundaries of the Rx outer mask are specified to accommodate a change in signal amplitude due to the ground offset through the cable. The Rx masks are therefore larger than the boundaries of the TX outer mask. Similarly, the boundaries of the Rx inner mask are smaller than the boundaries of the TX inner mask. Triangular time masks are superimposed on the TX outer masks and defined at the signal transitions to require a minimum edge rate that has minimal impact on adjacent higher speed lanes. The TX inner mask enforces the maximum limits on the rise and fall times. Refer to the *USB-PD Specifications* for more details.

8.3.1.4 USB-PD BMC Transmitter

The TPS65992SBG transmits and receives USB-PD data over one of the CCy pins for a given CC pin pair (one pair per USB Type-C port). The CCy pins are also used to determine the cable orientation and maintain the cable/device attach detection. Thus, a DC bias exists on the CCy pins. The transmitter driver overdrives the CCy DC bias while transmitting, but returns to a Hi-Z state allowing the DC voltage to return to the CCy pin when not transmitting. While either CC1 or CC2 may be used for transmitting and receiving, during a given connection only the one that mates with the CC pin of the plug is used; so there is no dynamic switching between CC1 and CC2. Figure 8-5 shows the USB-PD BMC TX and RX driver block diagram.

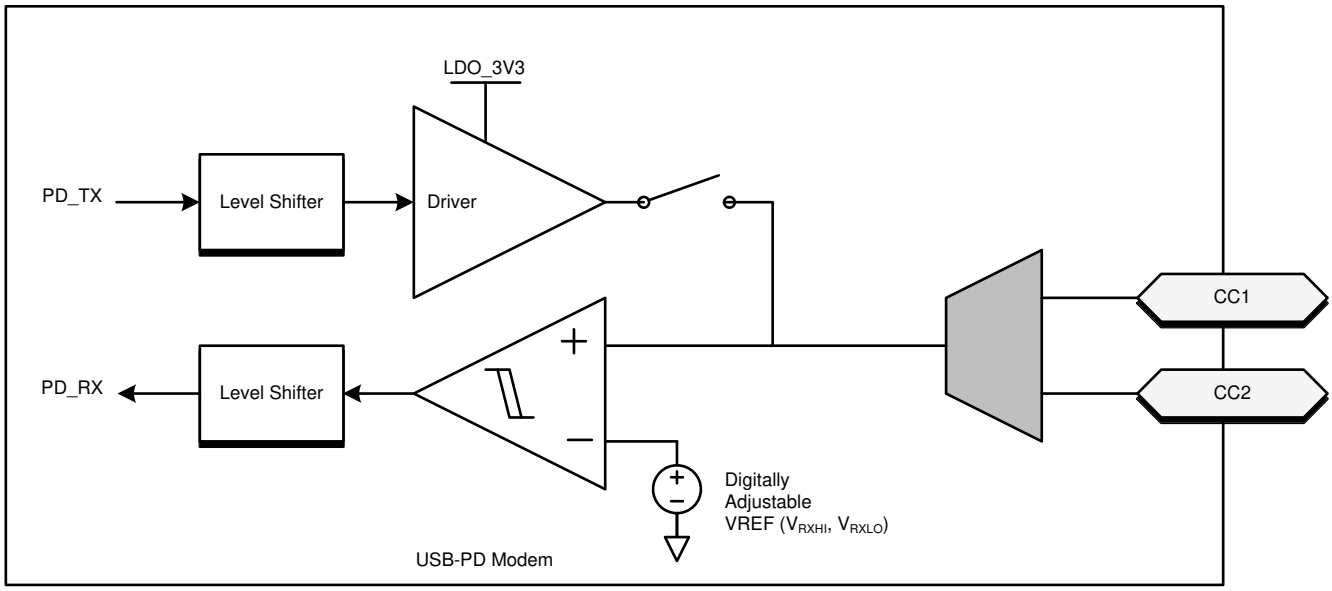


Figure 8-5. USB-PD BMC TX/Rx Block Diagram

Figure 8-6 shows the transmission of the BMC data on top of the DC bias. Note, The DC bias can be anywhere between the minimum and maximum threshold for detecting a Sink attach. This means that the DC bias can be above or below the VOH of the transmitter driver.

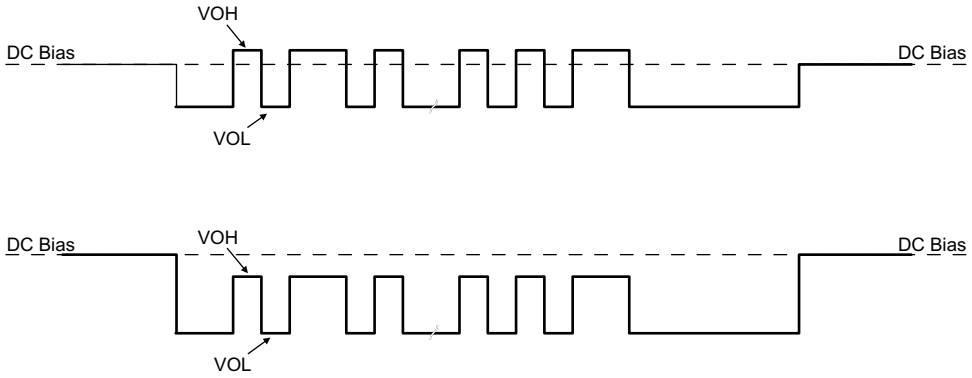


Figure 8-6. TX Driver Transmission with DC Bias

The transmitter drives a digital signal onto the CCy lines. The signal peak, V_{TXHI}, is set to meet the TX masks defined in the *USB-PD Specifications*. Note that the TX mask is measured at the far-end of the cable.

When driving the line, the transmitter driver has an output impedance of Z_{DRIVER}. Z_{DRIVER} is determined by the driver resistance and the shunt capacitance of the source and is frequency dependent. Z_{DRIVER} impacts the noise ingression in the cable.

Figure 8-7 shows the simplified circuit determining Z_{DRIVER}. It is specified such that noise at the receiver is bounded.

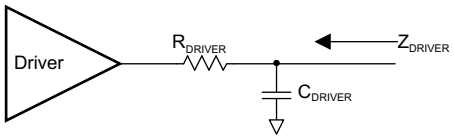


Figure 8-7. ZDRIVER Circuit

8.3.1.5 USB-PD BMC Receiver

The receiver block of the TPS65992SBG receives a signal that follows the allowed Rx masks defined in the USB PD specification. The receive thresholds and hysteresis come from this mask.

Figure 8-8 shows an example of a multi-drop USB-PD connection (only the CC wire). This connection has the typical Sink (device) to Source (host) connection, but also includes cable USB-PD Tx/Rx blocks. Only one system can be transmitting at a time. All other systems are Hi-Z (Z_{BMCRX}). The *USB-PD Specification* also specifies the capacitance that can exist on the wire as well as a typical DC bias setting circuit for attach detection.

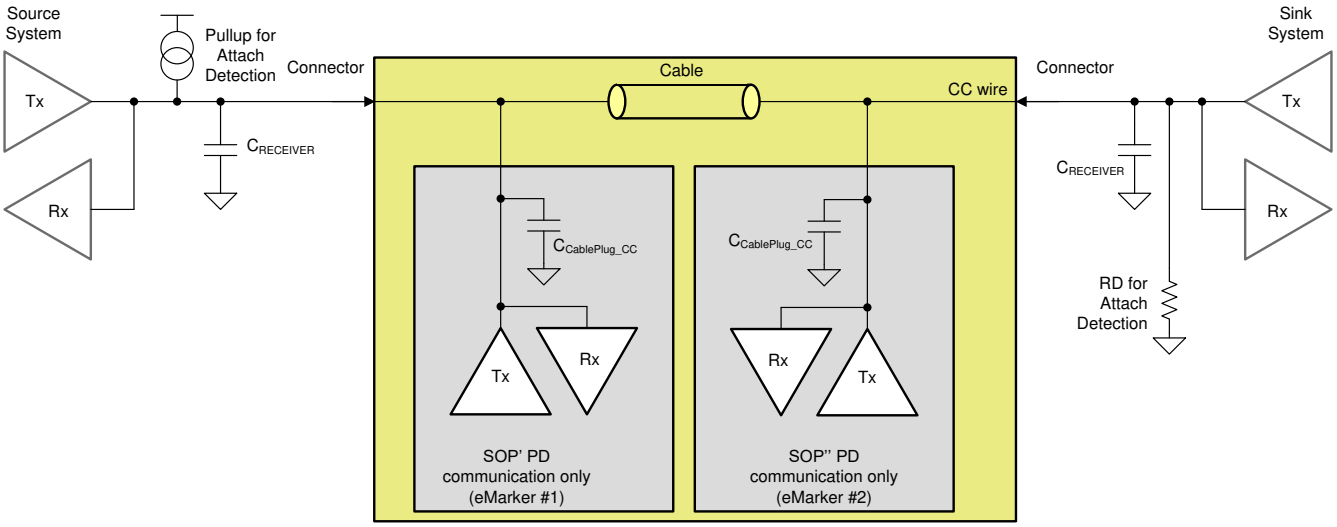


Figure 8-8. Example USB-PD Multi-Drop Configuration

8.3.1.6 Squelch Receiver

The TPS65992SBG has a squelch receiver to monitor for the bus idle condition as defined by the USB PD specification.

8.3.2 Power Management

The TPS65992SBG power management block receives power and generates voltages to provide power to the TPS65992SBG internal circuitry. These generated power rails are LDO_3V3 and LDO_1V5. LDO_3V3 may also be used as a low power output for external EEPROM memory. The power supply path is shown in Figure 8-9.

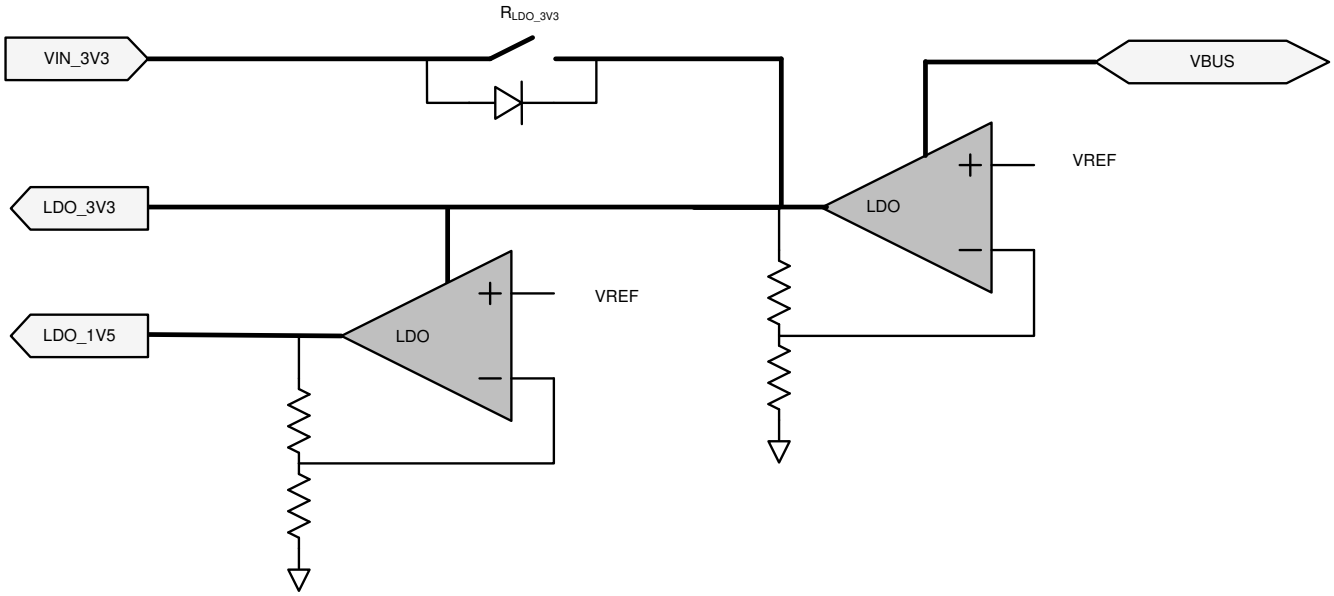


Figure 8-9. Power Supplies

The TPS65992SBG is powered from either VIN_3V3, or VBUS. The normal power supply input is VIN_3V3. When powering from VIN_3V3, current flows from VIN_3V3 to LDO_3V3 to power the core 3.3-V circuitry and I/Os. A second LDO steps the voltage down from LDO_3V3 to LDO_1V5 to power the 1.5-V core digital circuitry. When VIN_3V3 power is unavailable and power is available on VBUS it is referred to as the dead-battery startup condition. In a dead-battery startup condition, the TPS65992SBG opens the VIN_3V3 switch until the host clears the dead-battery flag via I^2C. Therefore, the TPS65992SBG is powered from the VBUS input with the higher voltage during the dead-battery startup condition and until the dead-battery flag is cleared. When powering from a VBUS input, the voltage on VBUS is stepped down through an LDO to LDO_3V3.

8.3.2.1 Power-On And Supervisory Functions

A power-on reset (POR) circuit monitors each supply. This POR allows active circuitry to turn on only when a good supply is present.

8.3.2.2 VBUS LDO

The TPS65992SBG contains an internal high-voltage LDO which is capable of converting VBUS to 3.3 V for powering internal device circuitry. The VBUS LDO is only used when VIN_3V3 is low (the dead-battery condition). The VBUS LDO is powered from VBUS.

8.3.3 Power Paths

The TPS65992SBG has internal power paths: PP_5V1 and PP_CABLE1. Each power path is described in detail in this section.

8.3.3.1 Internal Sourcing Power Paths

Figure 8-10 shows the TPS65992SBG internal sourcing power paths. The TPS65992SBG features two internal 5-V sourcing power paths. The path from PP5V to VBUS is called PP_5V. The path from PP5V to CCx is called PP_CABLE. Each path contains current clamping protection, overvoltage protection, UVLO protection and temperature sensing circuitry. PP_5V may conduct up to 3 A continuously, while PP_CABLE may conduct up to 315 mA continuously. When disabled, the blocking FET protects the PP5V rail from high-voltage that may appear on VBUS.

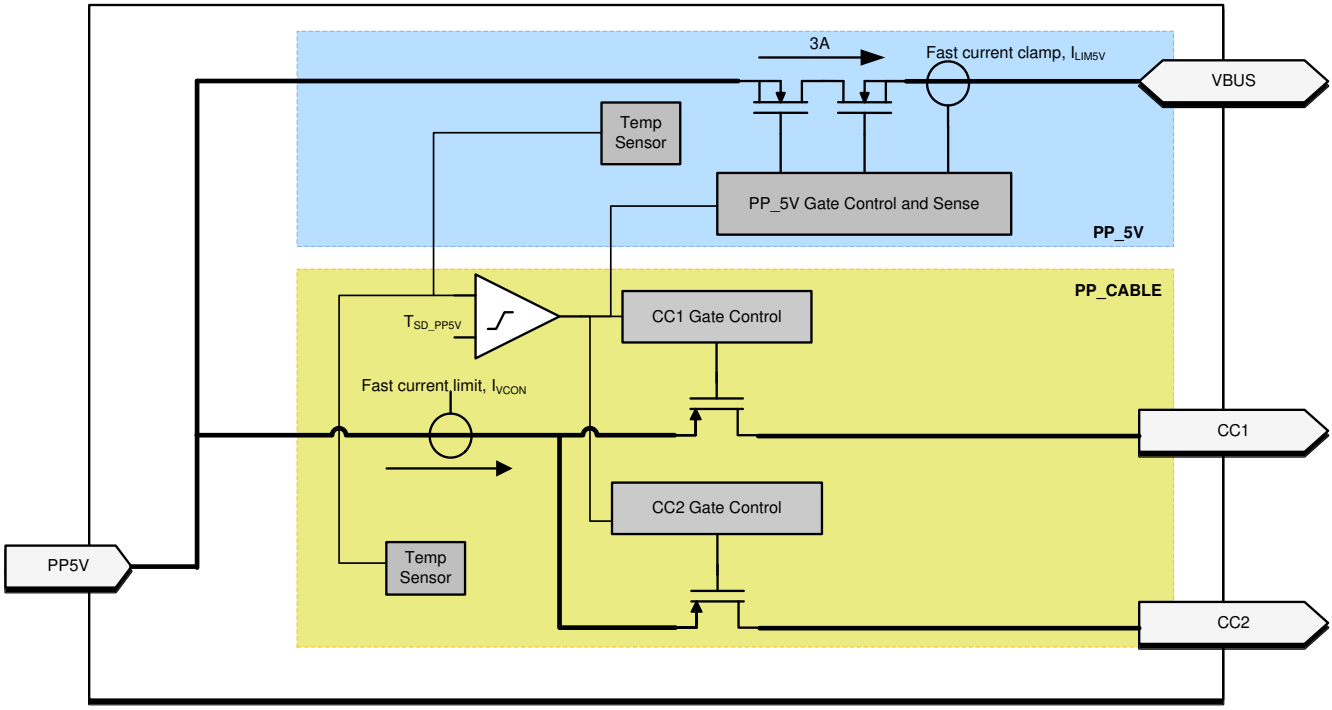


Figure 8-10. Port Power Switches

8.3.3.1.1 PP_5V Current Clamping

The current through the internal PP_5V path are current limited to I_{LIM5V}. The I_{LIM5V} value is configured by application firmware. When the current through the switch exceeds I_{LIM5V}, the current limiting circuit activates within $t_{iOS\_PP\_5V}$ and the path behaves as a constant current source. If the duration of the overcurrent event exceeds t_{ILIM}, the PP_5V switch is disabled.

8.3.3.1.2 PP_5V Local Overtemperature Shut Down (OTSD)

When PP_5V clamps the current, the temperature of the switch will begin to increase. When the local temperature sensors of PP_5V or PP_CABLE detect that $T_J > T_{SD\_PP5V}$ the PP_5V switch is disabled and the affected port enters the USB Type-C ErrorRecovery state.

8.3.3.1.3 PP_5V Current Sense

The current from PP5V to VBUS is sensed through the switch and passed to the internal ADC.

8.3.3.1.4 PP_5V OVP

The overvoltage protection level is automatically configured based on the expected maximum V_{BUS} voltage, which depends upon the USB PD contract. When the voltage on a port's VBUS pin exceeds the configured value ($V_{OVP4RCP}$) while PP_5V is enabled, then PP_5V is disabled within $t_{PP\_5V\_ovp}$ and the port enters into the Type-C ErrorRecovery state.

8.3.3.1.5 PP_5V UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold (V_{PP5V_UVLO}) while PP_5V is enabled, then PP_5V is disabled within $t_{PP\_5V\_uvlo}$ and the port that had PP_5V enabled enters into the Type-C ErrorRecovery state.

8.3.3.1.6 PP_5Vx Reverse Current Protection

If V_{VBUS} - V_{PP5V} > $V_{PP\_5V\_RCP}$, then the PP_5V path is automatically disabled within $t_{PP\_5V\_rcp}$. If the RCP condition clears, then the PP_5V path is automatically enabled within t_{ON}.

8.3.3.1.7 Fast Role Swap

The TPS65992SBG supports Fast Role Swap as defined by USB PD. The PP_5V path has a fast turn-on mode that application firmware selectively enables to support Fast Role Swap. When enabled it is engaged when

V_{VBUS} - V_{PP5V}<$V_{PP\_5V\_RCP}$, and turns on the switch within t_{FRS_on}.

8.3.3.1.8 PP_CABLE Current Clamp

When enabled and providing VCONN power the TPS65992SBG PP_CABLE power switch clamps the current to I_{VCON}. When the current through the PP_CABLE switch exceeds I_{VCON}, the current clamping circuit activates within $t_{iOS\_PP\_CABLE}$ and the switch behaves as a constant current source.

8.3.3.1.9 PP_CABLE Local Overtemperature Shut Down (OTSD)

When PP_CABLE clamps the current, the temperature of the switch will begin to increase. When the local temperature sensors of PP_5V or PP_CABLE detect that T_J>T_{SD_PP5V} the PP_CABLE switch is disabled and latched off within $t_{PP\_CABLE\_off}$. The port then enters the USB Type-C ErrorRecovery state.

8.3.3.1.10 PP_CABLE UVLO

If the PP5V pin voltage falls below its undervoltage lock out threshold (V_{PP5V_UVLO}), then the PP_CABLE switch is automatically disabled within $t_{PP\_CABLE\_off}$.

8.3.3.2 PP_EXT External Sink Path Control

The TPS65992SBG has two N-ch gate drivers designed to control a sinking path from VBUS to VSYS. The charge pump for these gate drivers requires VBUS to be above V_{VBUS_UVLO}. Figure 8-11 shows a diagram of the sink path. When a sink path is enabled, the circuitry includes a slew rate control loop to ensure that external switches do not turn on too quickly (SS). The TPS65992SBG senses the VSYS and VBUS voltages to control the gate voltages to enable or disable the external FETs.

The sink-path control includes overvoltage protection (OVP), and reverse current protection (RCP). Adding resistance in series with a GATE pin of the TPS65992SBG and the gate pin of the N-ch MOSFET will slow down the turn off time when OVP or RCP occurs. Any such resistance should be minimized, and not allowed to exceed 3 Ω

.

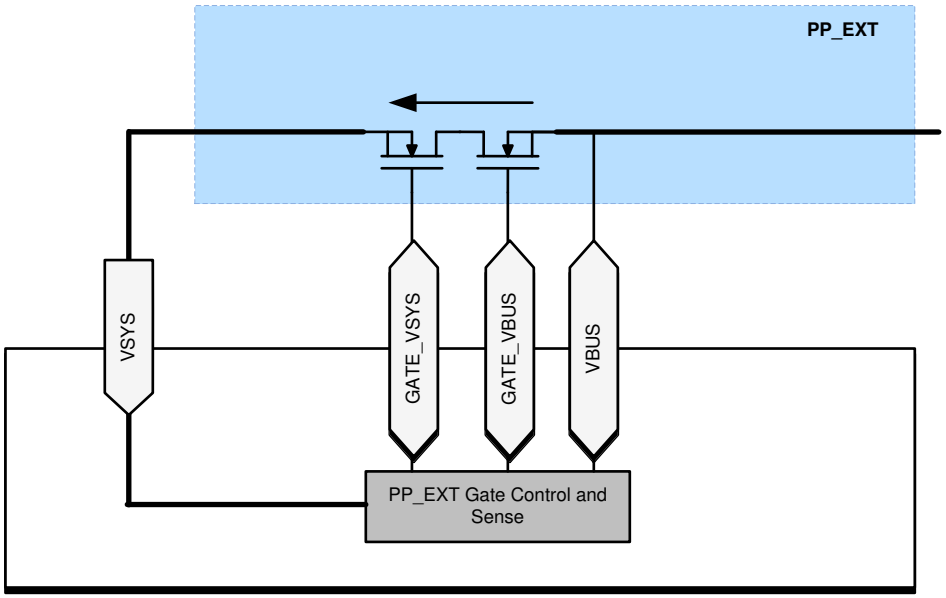


Figure 8-11. Sink Path Control

The following figure shows the GATE_VSYS gate driver in more detail.

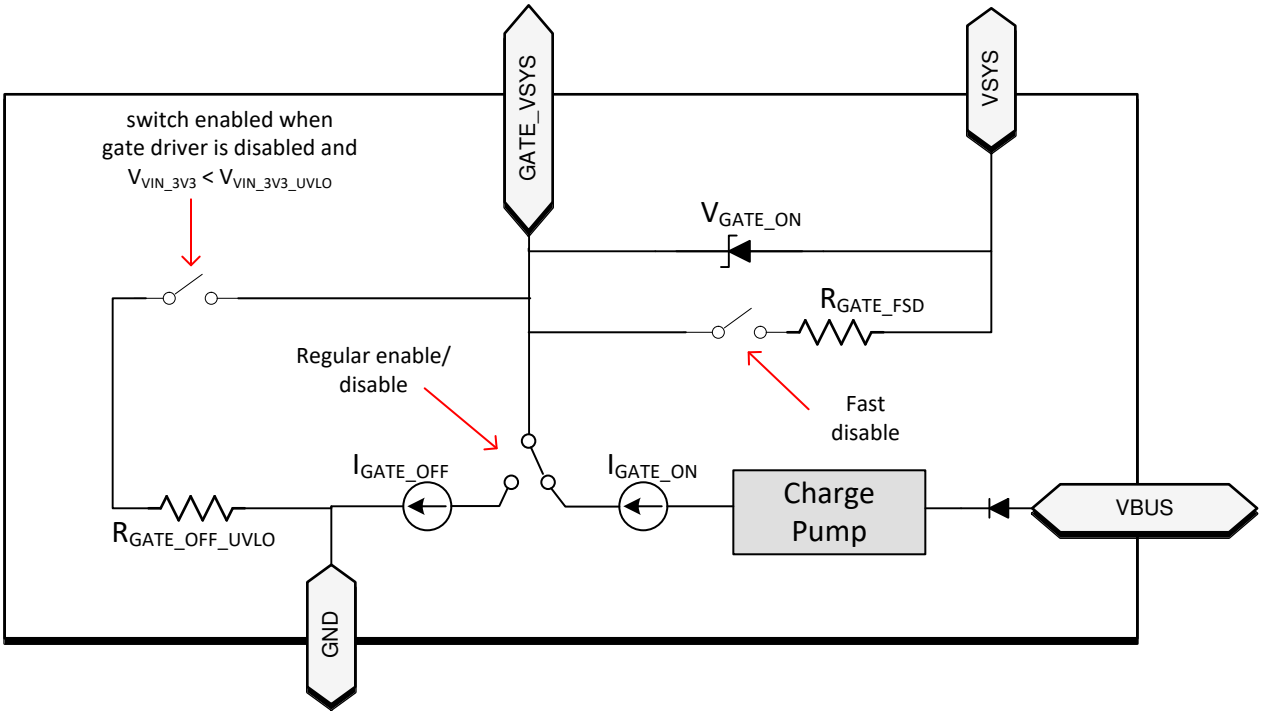


Figure 8-12. Details of the GATE_VSYS gate driver.

8.3.3.2.1 Overvoltage Protection (OVP)

The application firmware enables the OVP and configures it based on the expected VBUS voltage. If the voltage on VBUS surpasses the configured threshold $V_{OVP4VSYS} = V_{OVP4RCP}/r_{OVP}$, then GATE_VSYS is automatically disabled within $t_{GATE\_VSYS\_FSD}$ to protect the system. If the voltage on VBUS surpasses the configured threshold $V_{OVP4RCP}$ then GATE_VBUS is automatically disabled within $t_{GATE\_VBUS\_OVP}$. When V_{VBUS} falls below $V_{OVP4RCP}$ - $V_{OVP4RCPH}$ GATE_VBUS is automatically re-enabled within $t_{GATE\_VBUS\_ON}$ since the OVP condition has cleared. This allows two sinking power paths to be enabled simultaneously and GATE_VBUS will be disabled when necessary to ensure that V_{VBUS} remains below $V_{OVP4RCP}$.

While the TPS65992SBG is in the BOOT mode in a dead-battery scenario (that is VIN_3V3 is low) it handles an OVP condition slightly differently. As long as the OVP condition is present GATE_VBUS and GATE_VSYS are disabled. Once the OVP condition clears, both GATE_VBUS and GATE_VSYS are re-enabled (unless ADCINx are configured in SafeMode). Since this is a dead-battery condition, the TPS65992SBG will be drawing approximately $I_{VIN\_3V3,ActSnk}$ from VBUS during this time to help discharge it.

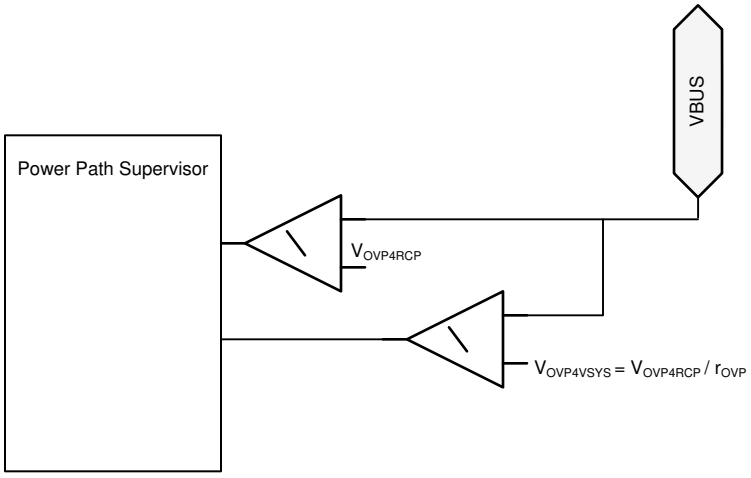


Figure 8-13. Diagram for OVP Comparators

8.3.3.2.2 Reverse-Current Protection (RCP)

The VSYS gate control circuit monitors the VSYS and VBUS voltages and detects reverse current when the V_{VSYS} surpasses V_{VBUS} by more than V_{RCP}. When the reverse current condition is detected, GATE_VBUS is disabled within $t_{GATE\_VBUS\_RCP}$. When the reverse current condition is cleared, GATE_VBUS is re-enabled within $t_{GATE\_VBUS\_ON}$. This limits the amount of reverse current that may flow from VSYS to VBUS through the external N-ch MOSFETs.

In reverse current protection mode, the power switch controlled by GATE_VBUS is allowed to behave resistively until the current reaches V_{RCP}/ R_{ON} and then blocks reverse current from VSYS to VBUS , where R_{ON} is the resistance of the external back-to-back N-ch MOSFET. Figure 8-14 shows the behavior of the switch.

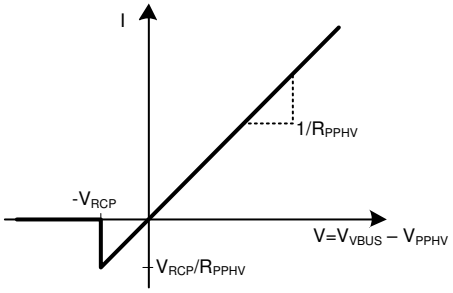


Figure 8-14. Switch I-V Curve for RCP on Sink-path Switches.

8.3.3.2.3 VBUS UVLO

The TPS65992SBG monitors VBUS voltage and detects when it falls below V_{VBUS_UVLO}. When the UVLO condition is detected, GATE_VBUS is disabled within $t_{GATE\_VBUS\_RCP}$. When the UVLO condition is cleared, GATE_VBUS is re-enabled within $t_{GATE\_VBUS\_ON}$.

8.3.3.2.4 Discharging VBUS to Safe Voltage

The TPS65992SBG has an integrated active pull-down (I_{DSCH}) on VBUS for discharging from high voltage to VSAFE0V (0.8 V). This discharge is applied when it is in an Unattached Type-C state.

8.3.4 Cable Plug and Orientation Detection

Figure 8-15 shows the plug and orientation detection block at each CCy pin (CC1, CC2). Each pin has identical detection circuitry.

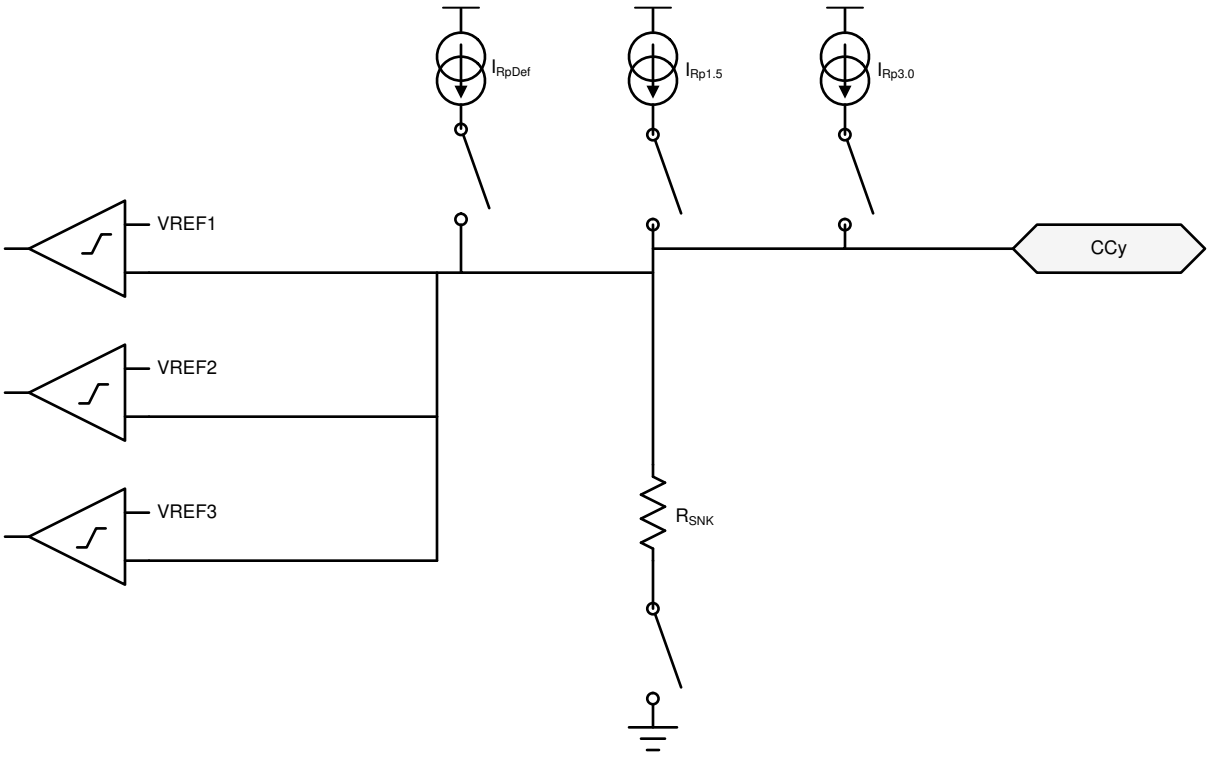


Figure 8-15. Plug and Orientation Detection Block

8.3.4.1 Configured as a Source

When configured as a source, the TPS65992SBG detects when a cable or a Sink is attached using the CC1 and CC2 pins. When in a disconnected state, the TPS65992SBG monitors the voltages on these pins to determine what, if anything, is connected. See *USB Type-C Specification* for more information.

Table 8-1 shows the Cable Detect States for a Source.

Table 8-1. Cable Detect States for a Source

CC1	CC2	CONNECTION STATE	RESULTING ACTION
Open	Open	Nothing attached	Continue monitoring both CCy pins for attach. Power is not applied to VBUS or VCONN.
Rd	Open	Sink attached	Monitor CC1 for detach. Power is applied to VBUS but not to VCONN (CC2).
Open	Rd	Sink attached	Monitor CC2 for detach. Power is applied to VBUS but not to VCONN (CC1).
Ra	Open	Powered Cable-No UFP attached	Monitor CC2 for a Sink attach and CC1 for cable detach. Power is not applied to VBUS or VCONN (CC1).
Open	Ra	Powered Cable-No UFP attached	Monitor CC1 for a Sink attach and CC2 for cable detach. Power is not applied to VBUS or VCONN (CC1).
Ra	Rd	Powered Cable-UFP Attached	Provide power on VBUS and VCONN (CC1) then monitor CC2 for a Sink detach. CC1 is not monitored for a detach.
Rd	Ra	Powered Cable-UFP attached	Provide power on VBUS and VCONN (CC2) then monitor CC1 for a Sink detach. CC2 is not monitored for a detach.
Rd	Rd	Debug Accessory Mode attached	Sense either CCy pin for detach.
Ra	Ra	Audio Adapter Accessory Mode attached	Sense either CCy pin for detach.

When a TPS65992SBG port is configured as a Source, a current I_{RpDef} is driven out each CCy pin and each pin is monitored for different states. When a Sink is attached to the pin a pull-down resistance of Rd to GND

exists. The current I_{RpDef} is then forced across the resistance Rd generating a voltage at the CCy pin. The TPS65992SBG applies I_{RpDef} until it closes the switch from PP5V to VBUS, at which time application firmware may change to $I_{Rp1.5A}$ or $I_{Rp3.0A}$.

When the CCy pin is connected to an active cable VCONN input, the pull-down resistance is different (Ra). In this case the voltage on the CCy pin will be lower and the TPS65992SBG recognizes it as an active cable.

The voltage on CCy is monitored to detect a disconnection depending upon which Rp current source is active. When a connection has been recognized and the voltage on CCy subsequently rises above the disconnect threshold for t_{CC}, the system registers a disconnection.

8.3.4.2 Configured as a Sink

When a TPS65992SBG port is configured as a Sink, the TPS65992SBG presents a pull-down resistance R_{SNK} on each CCy pin and waits for a Source to attach and pull-up the voltage on the pin. The Sink detects an attachment by the presence of VBUS. The Sink determines the advertised current from the Source based on the voltage on the CCy pin.

8.3.4.3 Configured as a DRP

When a TPS65992SBG port is configured as a DRP, the TPS65992SBG alternates the port's CCy pins between the pull-down resistance, R_{SNK}, and pull-up current source, I_{Rp}.

8.3.4.4 Fast Role Swap Signal Detection

The TPS65992SBG cable plug block contains additional circuitry that may be used to support the Fast Role Swap (FRS) behavior defined in the *USB Power Delivery Specification*. The circuitry provided for this functionality is detailed in Figure 8-16.

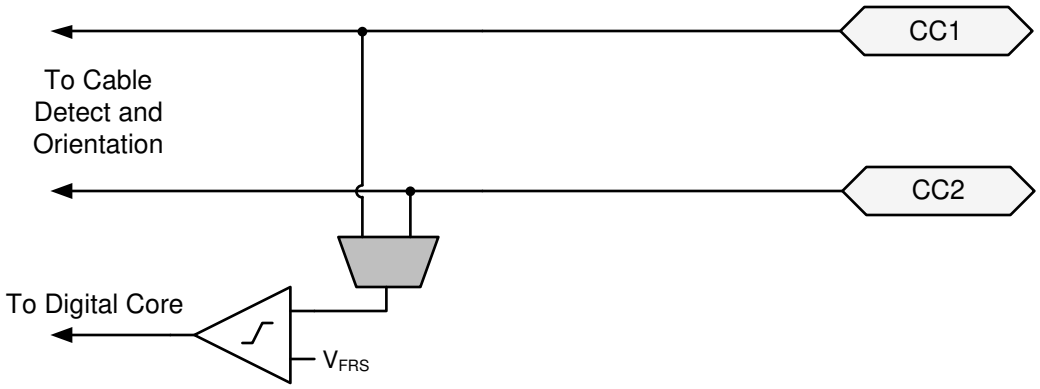


Figure 8-16. Fast Role Swap Detection and Signaling

When a TPS65992SBG port is operating as a sink with FRS enabled, the TPS65992SBG monitors the CC pin voltage. If the CC voltage falls below V_{FRS} for t_{FRS_DET} a fast role swap signal is detected and indicated to the digital core. When this signal is detected the TPS65992SBG ceases operating as a sink (disables GATE_VSYS and GATE_VBUS) and begins operating as a source.

8.3.4.5 Dead Battery Advertisement

The TPS65992SBG supports booting from no-battery or dead-battery conditions by receiving power from VBUS. Type-C USB ports require a sink to present Rd on the CC pin before a USB Type-C source provides a voltage on VBUS. TPS65992SBG hardware is configured to present this Rd during a dead-battery or no-battery condition. Additional circuitry provides a mechanism to turn off this Rd once the device no longer requires power from VBUS.

8.3.5 Overvoltage Protection (CC1, CC2)

The TPS65992SBG detects when the voltage on the CC1 or CC2 pin is too high or there is reverse current into the PP5V pin and takes action to protect the system. The protective action is to disable PP_CABLE within $t_{PP\_CABLE\_FSD}$ and disable the USB PD transmitter.

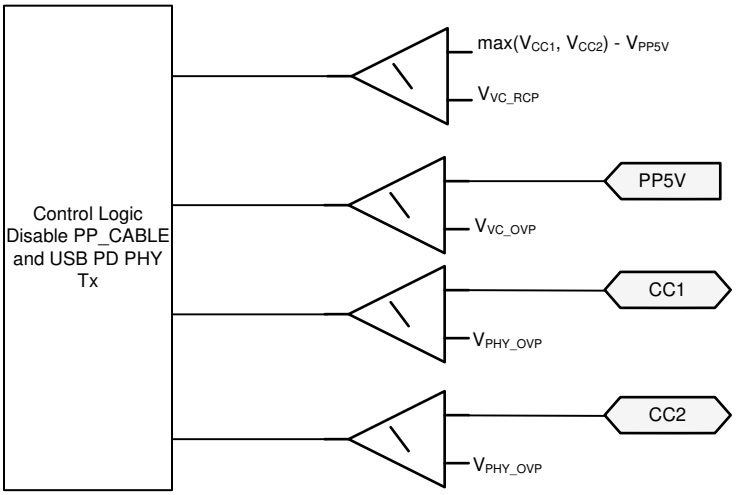


Figure 8-17. Overvoltage and Reverse Current Protection for CC1 and CC2

8.3.6 Default Behavior Configuration (ADCIN1, ADCIN2)

Note

This functionality is firmware controlled and subject to change.

The ADCINx inputs to the internal ADC control the behavior of the TPS65992SBG in response to VBUS being supplied when VIN_3V3 is low (that is the dead-battery scenario). The ADCINx pins must be externally tied to the LDO_3V3 pin via a resistive divider as shown in the following figure. At power-up the ADC converts the ADCINx voltage and the digital core uses these two values to determine start-up behavior. The available start-up configurations include options for I^2C slave address of I2C_EC_SCL/SDA, sink path control in dead-battery, and default configuration.

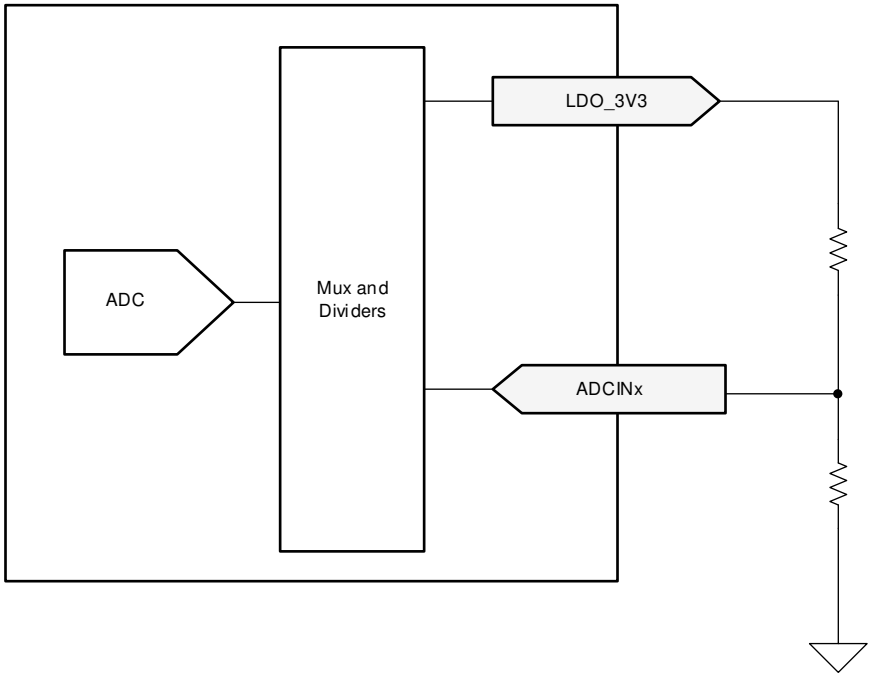


Figure 8-18. ADCINx Resistor Divider

The device behavior is determined in several ways depending upon the decoded value of the ADCIN1 and ADCIN2 pins. The following table shows the decoded values for different resistor divider ratios. See *Pin Strapping to Configure Default Behavior* for details on how the ADCINx configurations determine default device behavior. See *I²C Address Setting* for details on how ADCINx decoded values affects default I²C slave address.

Table 8-2. Decoding of ADCIN1 and ADCIN2 Pins

DIV = R_{DOWN} / (R_{UP} + R_{DOWN})(1)			Without using R_{UP} or R_{DOWN}	ADCINx decoded value
MIN	Target	MAX		
0	0.0114	0.0228	tie to GND	0
0.0229	0.0475	0.0722	N/A	1
0.0723	0.1074	0.1425	N/A	2
0.1425	0.1899	0.2372	N/A	3
0.2373	0.3022	0.3671	N/A	4
0.3672	0.5368	0.7064	tie to LDO_1V5	5
0.7065	0.8062	0.9060	N/A	6
0.9061	0.9530	1.0	tie to LDO_3V3	7

(1) External resistor tolerance of 1% is recommended. Resistor values must be chosen to yield a DIV value centered nominally between listed MIN and MAX values. For convenience, the Target column shows this value.

8.3.7 ADC

The TPS65992SBG ADC is shown in Figure 8-19. The ADC is an 8-bit successive approximation ADC. The input to the ADC is an analog input mux that supports multiple inputs from various voltages and currents in the device. The output from the ADC is available to be read and used by application firmware.

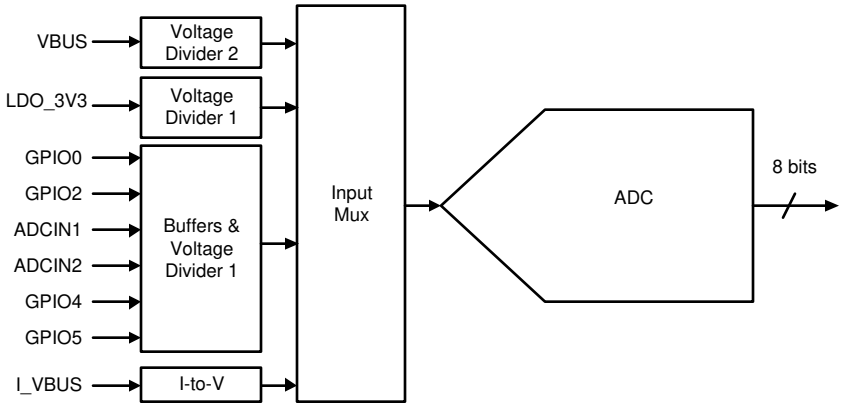


Figure 8-19. SAR ADC

8.3.8 BC 1.2 (USB_P, USB_N)

The TPS65992SBG supports BC 1.2 as a Portable Device or Downstream Port using the hardware shown in the following figure.

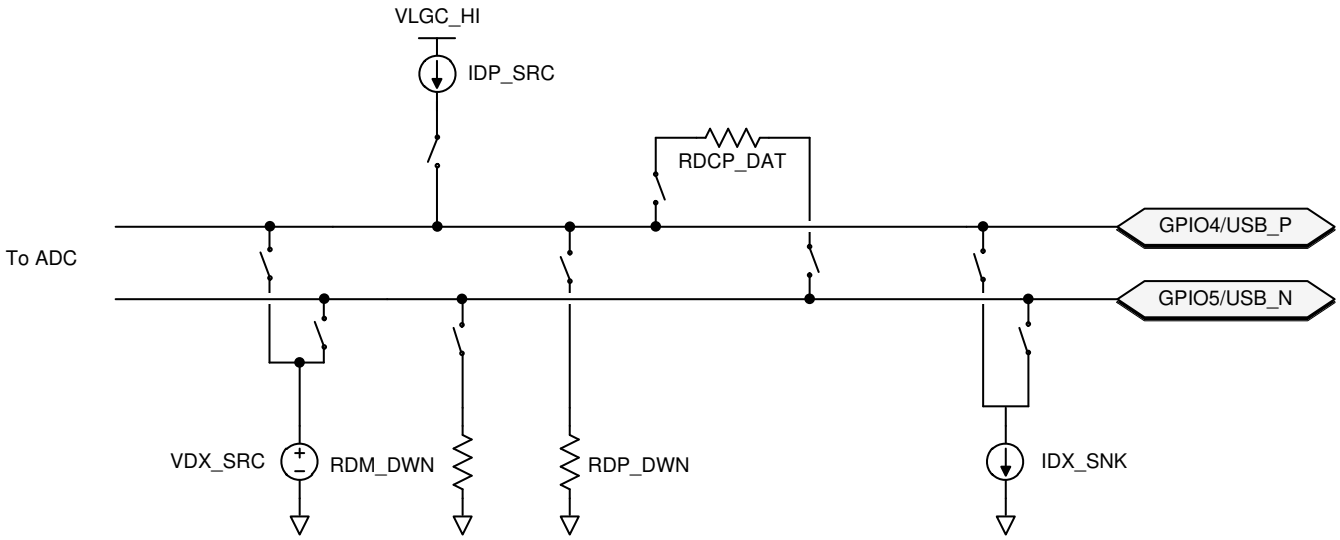


Figure 8-20. BC1.2 Hardware Components

8.3.9 DisplayPort Hot-Plug Detect (HPD)

The TPS65992SBG supports the DisplayPort alternate mode as a DP source or DP sink. It is recommended to use the virtual HPD functionality through I^2C. However, the TPS65992SBG also supports the HPD converter functions on GPIO pins (See Table 8-4). The core will translate PD messaging events onto the HPD pin(HPD_Tx), or detect HPD events and translate them into PD messaging (HPD_Rx).

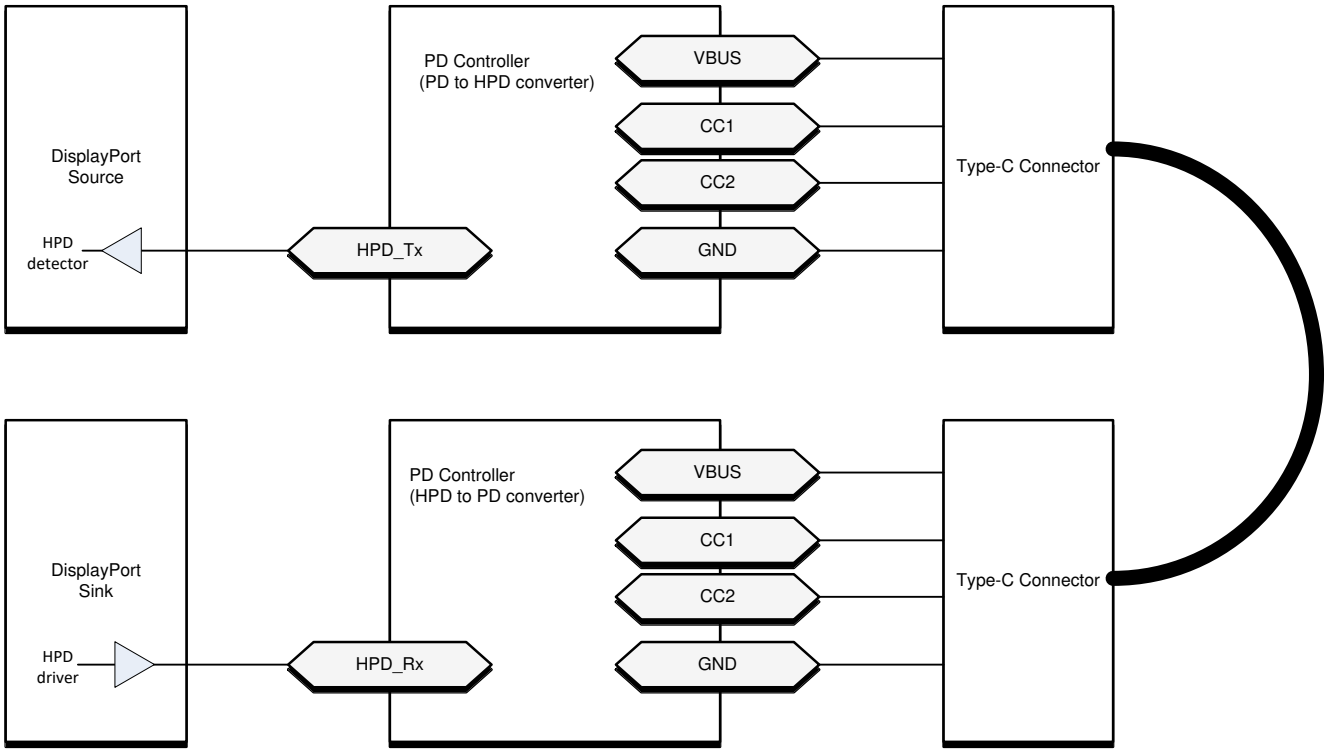


Figure 8-21. Illustration of how a PD-to-HPD Converter Passes the HPD Signal Along in a DisplayPort System

8.3.10 Digital Interfaces

The TPS65992SBG contains several different digital interfaces which may be used for communicating with other devices. The available interfaces include two I^2C Slaves and one I^2C Master, and additional GPIOs.

8.3.10.1 Battery Charging Control (CTL)

The system can control the mode of the BC 1.2 charging used. The TPS65992SBG will implement the Dedicated Charging Port (DCP) mode or the Charging Data Port (CDP) mode.

Table 8-3. BC 1.2 Mode Control (CTL)

CTL pin state	ADCIN2[0] Decoded Value	BC 1.2 Charging Mode
Low	0 or 1	CDP
High	0	DCP
High	1	DCP Auto Mode1

8.3.10.2 Debug Accessory Detection ($\overline{DEBUG}$)

If the TPS65992SBG detects the attachment of a Type-C debug accessory (Rd, Rd), then it will assert the $\overline{DEBUG}$ pin low. Otherwise this pin is Hi-Z.

8.3.10.3 Disable the Port (EN)

The system may force the TPS65992SBG to disable the port by forcing the EN pin low. This forces the TPS65992SBG into the Type-C Error Recovery state. Note that the TPS65992SBG has an internal pull-down on this pin (GPIO_RPD).

8.3.10.4 General GPIO

GPIOn pins can be mapped to USB Type-C, USB PD, and application-specific events to control other ICs, interrupt a host processor, or receive input from another IC. This buffer is configurable to be a push-pull output, a weak push-pull, or open drain output. When configured as an input, the signal can be a de-glitched digital input or an analog input to the ADC (only a subset of the GPIO's are ADC inputs see table below). The push-pull output is a simple CMOS output with independent pull-down control allowing open-drain connections. The weak push-pull is also a CMOS output, but with GPIO_RPU resistance in series with the drain. The supply voltage to the output buffer is LDO_3V3 and LDO_1V5 to the input buffer. When interfacing with non 3.3-V I/O devices the output buffer may be configured as an open drain output and an external pull-up resistor attached to the GPIO pin. The pull-up and pull-down output drivers are independently controlled from the input and are enabled or disabled via application code in the digital core.

Table 8-4. GPIO Functionality Table

Pin Name	Type	Special Functionality
GPIO0	I/O	ADC Input,
GPIO1	I/O	HPD_Tx
GPIO2	I/O	PROCHOT#, ADC Input,
GPIO3	I/O	HPD_Rx
GPIO4	I/O	ADC Input, D+,
GPIO5	I/O	ADC Input, D-,
GPIO6	I/O	
GPIO7	I/O	
$\overline{I2C\_EC\_IRQ}$(GPIO10)	O	IRQ for I2C_EC, or used as a general-purpose output
$\overline{I2C2s\_IRQ}$(GPIO11)	O	IRQ for I2C2, or used as a general-purpose output
$\overline{I2C3m\_IRQ}$(GPIO12)	I	IRQ for I2C3, or used as a general-purpose input

8.3.10.5 I^2C Interface

The TPS65992SBG features three I^2C interfaces that each use an I^2C I/O driver like the one shown in Figure 8-22. This I/O consists of an open-drain output and in input comparator with de-glitching.

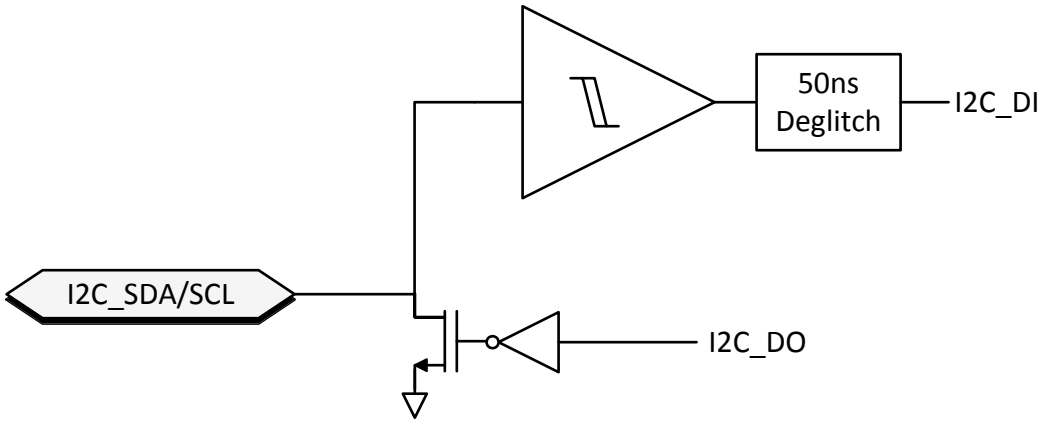


Figure 8-22. I²C Buffer

8.3.11 Digital Core

Figure 8-23 shows a simplified block diagram of the digital core.

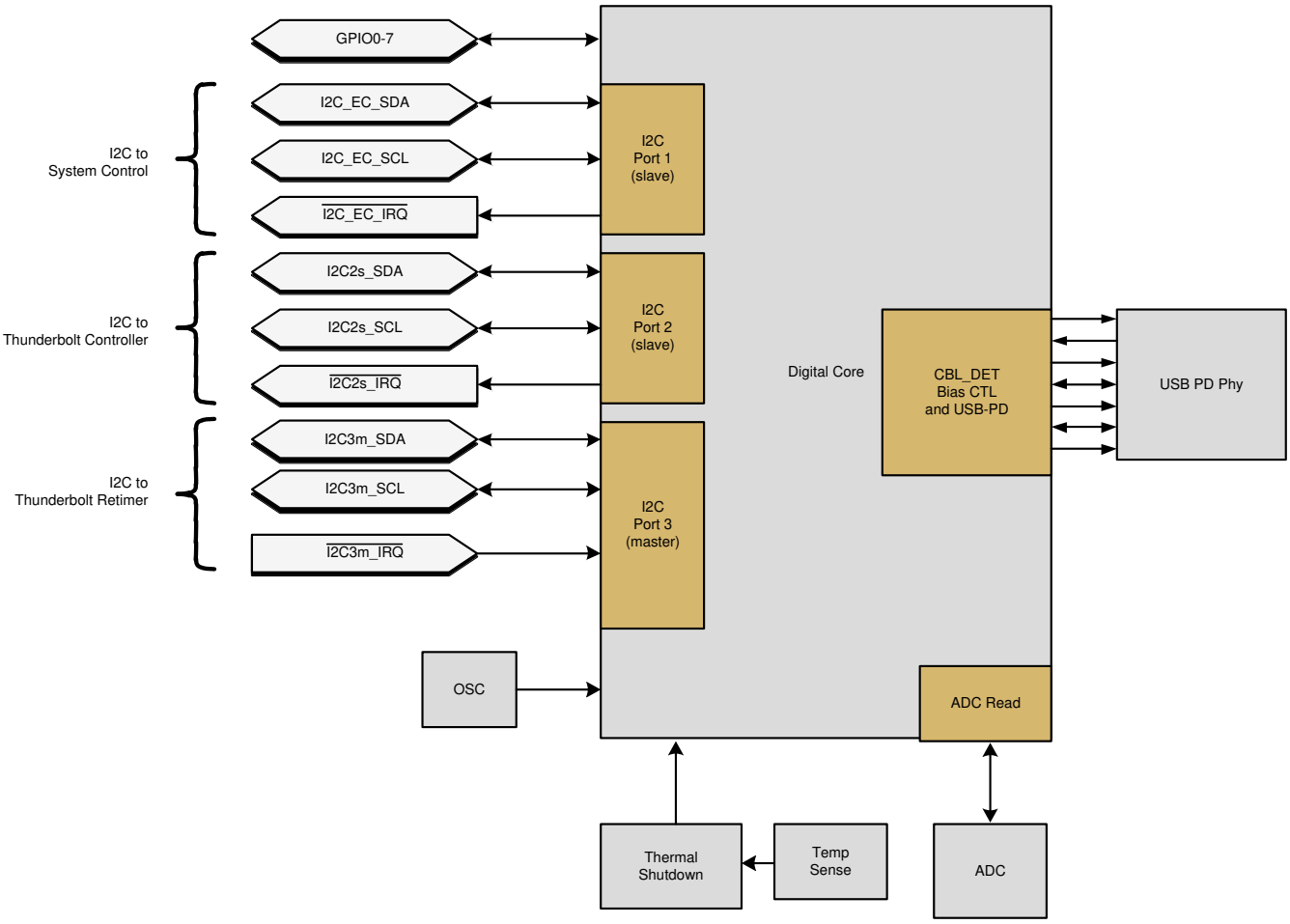


Figure 8-23. Digital Core Block Diagram

8.3.12 I²C Interface

The TPS65992SBG has two I²C slave interface ports: I2C_EC and I2C2s. I²C port I2C_EC is comprised of the I2C_EC_SDA, I2C_EC_SCL, and $\overline{\text{I2C\_EC\_IRQ}}$ pins. I²C I2C2s is comprised of the I2C2s_SDA, I2C2s_SCL, and $\overline{\text{I2C2s\_IRQ}}$ pins. These interfaces provide general status information about the TPS65992SBG, as well as

the ability to control the TPS65992SBG behavior, supporting communications to/from a connected device and/or cable supporting BMC USB-PD, and providing information about connections detected at the USB-C receptacle.

When the TPS65992SBG is in 'APP ' mode it is recommended to use Standard Mode or Fast Mode (that is a clock speed no higher than 400 kHz). However, in the 'BOOT' mode when a patch bundle is loaded Fast Mode Plus may be used (see f_{SCLS}).

The TPS65992SBG has one I²C master interface port: I2C3m. I2C3m is comprised of the I2C3m_SDA, I2C3m_SCL, and $\overline{\text{I2C3m\_IRQ1}}$ pins. This interface can be used to read from or write to external slave devices. During boot the TPS65992SBG attempts to read patch and Application Configuration data from an external EEPROM with a 7-bit slave address of 0x50. The EEPROM should be at least kilo-bytes.

Table 8-5. I²C Summary

I2C Bus	Type	Typical Usage
I2C_EC	Slave	Connect to an Embedded Controller (EC). Used to load the patch and application configuration.
I2C2s	Slave	Connect to a TBT controller or second master.
I2C3m	Master	Connect to a TBT retimer, USB Type-C mux, I²C EEPROM, or other slave. Use the LDO_3V3 pin as the pull-up voltage. Multi-master configuration is not supported.

8.3.12.1 I²C Interface Description

The TPS65992SBG supports Standard and Fast mode I²C interfaces. The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a supply through a pull-up resistor. Data transfer may be initiated only when the bus is not busy.

A master sending a Start condition, a high-to-low transition on the SDA input and output, while the SCL input is high initiates I²C communication. After the Start condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (R/W).

After receiving the valid address byte, this device responds with an acknowledge (ACK), a low on the SDA input/output during the high of the ACK-related clock pulse. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period as changes in the data line at this time are interpreted as control commands (Start or Stop). The master sends a Stop condition, a low-to-high transition on the SDA input and output while the SCL input is high.

Any number of data bytes can be transferred from the transmitter to receiver between the Start and the Stop conditions. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit. The device that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. Setup and hold times must be met to ensure proper operation.

A master receiver signals an end of data to the slave transmitter by not generating an acknowledge (NACK) after the last byte has been clocked out of the slave. The master receiver holding the SDA line high does this. In this event, the transmitter must release the data line to enable the master to generate a Stop condition.

Figure 8-24 shows the start and stop conditions of the transfer. Figure 8-25 shows the SDA and SCL signals for transferring a bit. Figure 8-26 shows a data transfer sequence with the ACK or NACK at the last clock pulse.

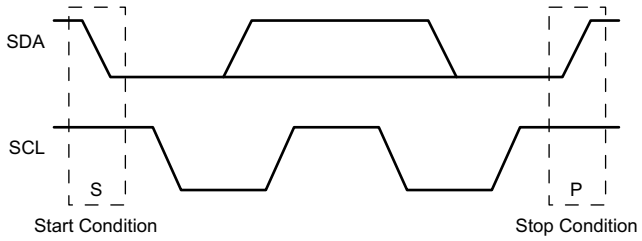


Figure 8-24. I²C Definition of Start and Stop Conditions

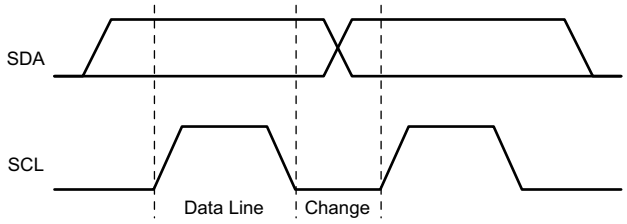


Figure 8-25. I²C Bit Transfer

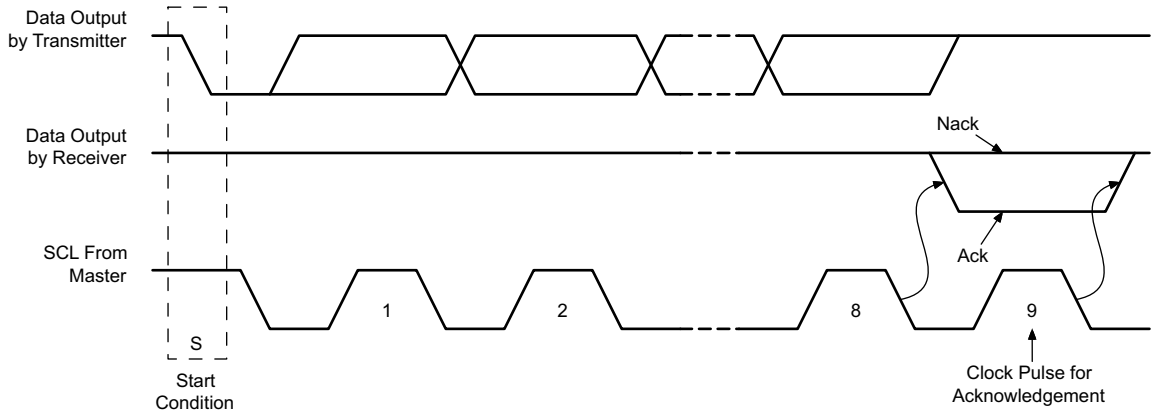


Figure 8-26. I²C Acknowledgment

8.3.12.2 I²C Clock Stretching

The TPS65992SBG features clock stretching for the I²C protocol. The TPS65992SBG slave I²C port may hold the clock line (SCL) low after receiving (or sending) a byte, indicating that it is not yet ready to process more data. The master communicating with the slave must not finish the transmission of the current bit and must wait until the clock line actually goes high. When the slave is clock stretching, the clock line remains low.

The master must wait until it observes the clock line transitioning high plus an additional minimum time (4 µs for standard 100-kbps I²C) before pulling the clock low again.

Any clock pulse may be stretched but typically it is the interval before or after the acknowledgment bit.

8.3.12.3 I²C Address Setting

The host should only use I2C_EC_SCL/SDA for loading a patch bundle. Once the boot process is complete, each port has a unique slave address on the I2C_EC_SCL/SDA bus as selected by the ADCINx pins. The slave address used by each port on the I2C2s bus are determined from the application configuration. The Port A slave address should be used for pushing the patch bundle since the Port B slave address is not available during the BOOT mode.

Table 8-6. I²C Default Slave Address for I2C_EC_SCL/SDA.

I²C address index (decoded from ADCIN1 and ADCIN2)(1)		Slave Address								Available During BOOT
		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
#1		0	1	0	0	0	0	0	R/W	Yes
#2		0	1	0	0	0	0	1	R/W	Yes
#3		0	1	0	0	0	1	0	R/W	Yes
#4		0	1	0	0	0	1	1	R/W	Yes

(1) See Table 8-2 details about ADCIN1 and ADCIN2 decoding.

8.3.12.4 I²C2s Address Setting during BOOT/PTCH

During BOOT/PTCH the slave address is set by the I²C address index (decoded from ADCIN1 and ADCIN2) When in APP, the slave address used by each port on the I2C2s bus are determined from the application configuration.

Table 8-7. I²C Default Slave Address for I2C2s_SCL/SDA during BOOT/PTCH

I²C address index (decoded from ADCIN1 and ADCIN2)(1)	I²C2s Address
#1	0x38
#2	0x48
#3	0x48
#4	0x48

8.3.12.5 Unique Address Interface

The Unique Address Interface allows for complex interaction between an I²C master and a single TPS65992SBG. The I²C Slave sub-address is used to receive or respond to Host Interface protocol commands. Figure 8-27 and Figure 8-28 show the write and read protocol for the I²C slave interface, and a key is included in Figure 8-29 to explain the terminology used. The key to the protocol diagrams is in the SMBus Specification and is repeated here in part.

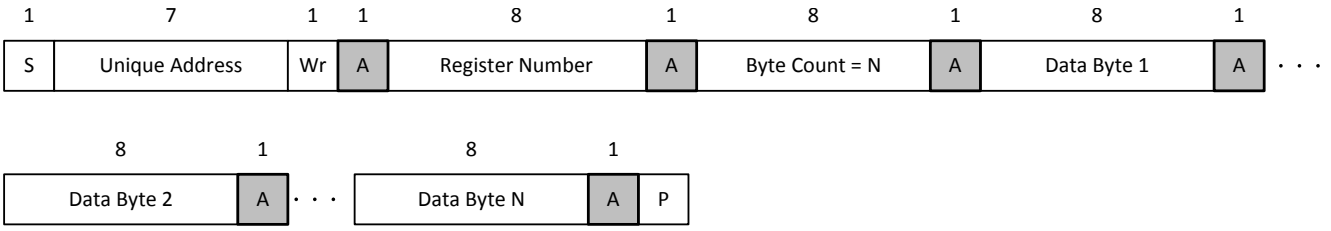


Figure 8-27. I²C Unique Address Write Register Protocol

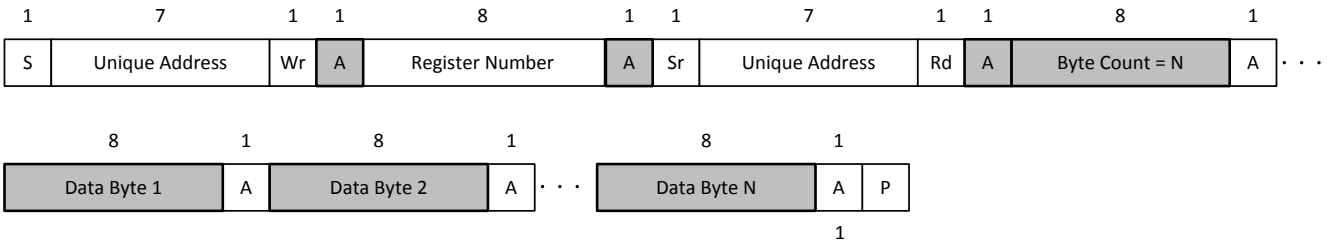


Figure 8-28. I²C Unique Address Read Register Protocol

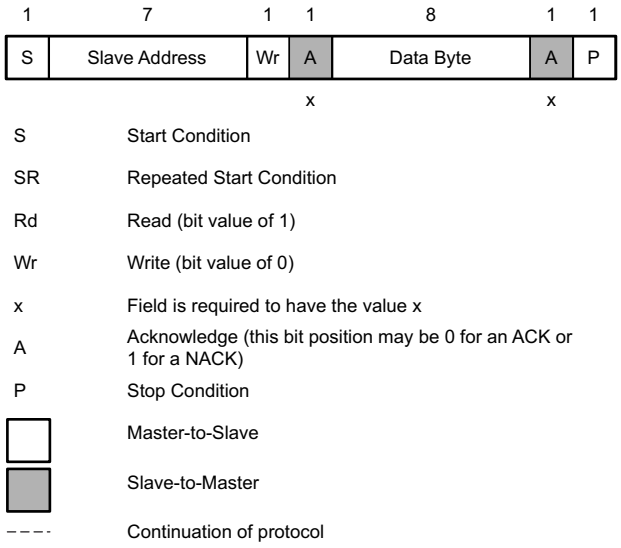


Figure 8-29. I²C Read/Write Protocol Key

8.4 Device Functional Modes

8.4.1 Pin Strapping to Configure Default Behavior

During the boot procedure, the device will read the ADCINx pins and set the configurations based on the table below. Then it will attempt to load a configuration from an external EEPROM on the I2C3m bus. If no EEPROM is detected, then the device will wait for an EC to load a configuration.

When an external EEPROM is used, each device is connected to a unique EEPROM, it cannot be shared for multiple devices. The external EEPROM shall be at 7-bit slave address 0x50.

Table 8-8. Device Configuration using ADCIN1 and ADCIN2

ADCIN1 decoded value (2)	ADCIN2 decoded value (2)	I²C address Index (1)	Dead Battery Configuration
7	5	#1	AlwaysEnableSink: The device always enables the sink path regardless of the amount of current the attached source is offering. USB PD is disabled until configuration is loaded.
5	5	#2	
2	0	#3	
1	7	#4	
7	4	#1	SinkRequires_3.0A: The device only enables the sink path if the attached source is offering at least 3.0A. USB PD is disabled until configuration is loaded.
4	4	#2	
3	0	#3	
2	7	#4	
7	6	#1	SinkRequires_1.5A: The device only enables the sink path if the attached source is offering at least 1.5A. USB PD is disabled until configuration is loaded.
6	6	#2	
6	5	#3	
6	7	#4	
7	3	#1	NegotiateHighVoltage: The device always enables the sink path during the initial implicit contract regardless of the amount of current the attached source is offering. The PD controller will enter the 'APP ' mode, enable USB PD PHY and negotiate a contract for the highest power contract that is offered up to 20 V. This cannot be used when a patch is loaded from EEPROM.
3	3	#2	
4	0	#3	
3	7	#4	
7	0	#1	SafeMode: The device does not enable the sink path. USB PD is disabled until configuration is loaded. Note that the configuration could put the device into a source-only mode. This is recommended when the application loads the patch from EEPROM.
0	0	#2	
6	0	#3	
5	7	#4	

(1) See Table 8-6 to see the exact meaning of I²C Address Index.
(2) See Table 8-2 for how to configure a given ADCINx decoded value.

8.4.2 Power States

The TPS65992SBG may operate in one of three different power states: Active, Idle, or Sleep. The Modern Standby mode is a special case of the Idle mode. The functionality available in each state is summarized in the following table. The device will automatically transition between the three power states based on the circuits that are active and required, see the following figure. In the Sleep State the TPS65992SBG will detect a Type-C connection. Transitioning between the Active mode to the Idle mode requires a period of time (T) without any of the following activity:

- Incoming USB PD message.
- Change in CC status.
- GPIO input event.
- I²C transactions.
- Voltage alert.
- Fault alert.

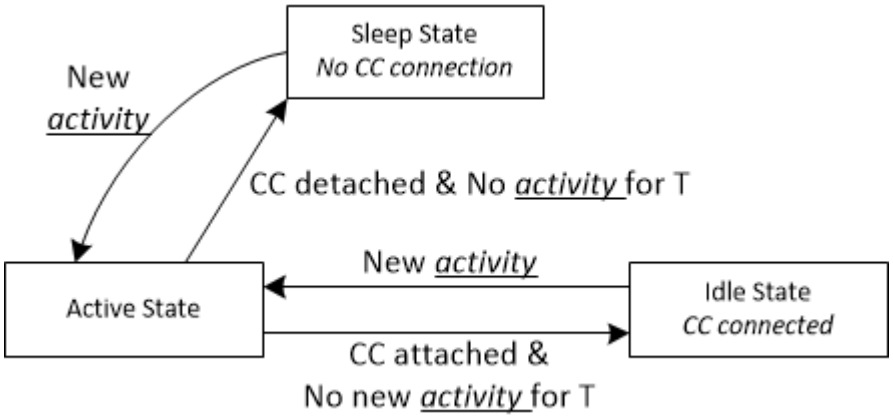


Figure 8-30. Flow Diagram For Power States

Table 8-9. Power Consumption States

	Active Source Mode(1)	Active Sink Mode(6)	Idle Source Mode(2)	Idle Sink Mode(7)	Modern Standby Source Mode(4)	Modern Standby Sink Mode(5)	Sleep Mode(3)
PP_5V	enabled	disabled	enabled	disabled	enabled	disabled	disabled
PP_EXT	disabled	enabled	disabled	enabled	disabled	disabled	disabled
PP_CABLE	enabled	enabled	enabled	enabled	disabled	disabled	disabled
external CC1 termination	Rd	Rp 3.0A	Rd	Rp 3.0A	Rd	Rp 3.0A	open
external CC2 termination	open	open	open	open	open	open	open

(1) This mode is used for: $I_{VIN\_3V3,ActSrc}$.
(2) This mode is used for: $I_{VIN\_3V3,IdlSrc}$
(3) This mode is used for: $I_{VIN\_3V3,Sleep}$
(4) This mode is used for: $P_{MstbySrc}$
(5) This mode is used for: $P_{MstbySnk}$
(6) This mode is used for: $I_{VIN\_3V3,ActSnk}$
(7) This mode is used for: $I_{VIN\_3V3,IdlSnk}$

8.4.3 Schottky for Current Surge Protection

To prevent the possibility of large ground currents into the TPS65992SBG during sudden disconnects due to inductive effects in a cable, it is recommended that a Schottky diode be placed from VBUS to ground as shown in Figure 8-31.

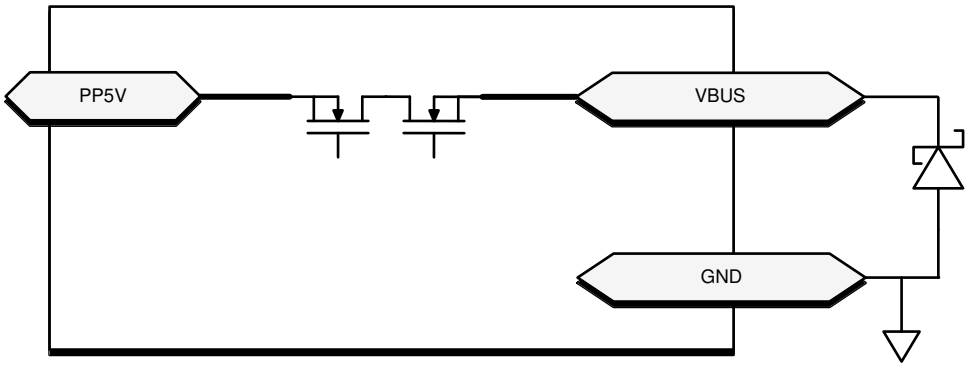


Figure 8-31. Schottky for Current Surge Protection

8.4.4 Thermal Shutdown

The TPS65992SBG features a central thermal shutdown as well as independent thermal sensors for each internal power path. The central thermal shutdown monitors the overall temperature of the die and disables all functions except for supervisory circuitry when die temperature goes above a rising temperature of T_{SD_MAIN}. The temperature shutdown has a hysteresis of T_{SDH_MAIN} and when the temperature falls back below this value, the device resumes normal operation.

The power path thermal shutdown monitors the temperature of each internal PP5V-to-VBUS power path and disables both power paths and the VCONN power path when either exceeds T_{SD_PP5V}. Once the temperature falls by at least T_{SDH_PP5V} the path can be configured to resume operation or remain disabled until re-enabled by firmware.

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

9.2 Typical Application

9.2.1 Design Requirements - Extended Power Range

The table below shows the Power Design parameters for the USB4 device application. For the UFP port 28V, 36V, and 48 V, Extended Power Range (EPR) is supported.

Table 9-1. Power Design Parameters

POWER DESIGN PARAMETER	VALUE	CURRENT PATH
UFP Source Port A	5 V/9 V/15 V/20 V/**28 V/36 V/48 V** @ 5 A	Host Charging VBUS
DFP Source Port B/C/D	5 V @ 9 A (3 A per port)	DFP VBUS
VCONN Port A/B/C/D	5V @ 2 A (500 mA per port)	VCONN Source
VIN_3V3 PD Controller & DMC	3.3 V @ 100 mA (50 mA per device)	PD Controller & DMC Power

9.2.2 Design Requirements - Supported Data Modes

USB4 Hub controllers may vary on the data supported on the UFP and DFP ports. In this specific example the USB4 Hub Controller supports USB3, DisplayPort, Thunderbolt, and USB4 on the UFP port. The DFP ports will also support these modes when connected to other Type-C & PD devices.

Table 9-2. Supported Data Modes

MODE OF OPERATION	DATA	DATA ROLE
USB Data	USB3.1 Gen2	UFP: Device, DFP: Host
DisplayPort	DP Video	UFP: UFP_D, DFP: DFP_D
Thunderbolt	PCIe/DP Video	UFP: Host/Device, DFP: Host
USB4	Tunneled USB3/PCIe/DP	UFP: Device, DFP: Host

9.2.3 Detailed Design Procedure

9.2.3.1 Extended Power Range VBUS PMOS Protection & Sense

For an EPR source application, the VBUS pin of the PD controller must be protected from the EPR voltages. In order to protect VBUS pin on the PD controller and sense the VBUS voltage at EPR voltage ranges, two circuits should be implemented. The VBUS blocking MOSFET circuit will protect the VBUS pin on the PD controller and VBUS sensing BJT circuit will provide a divided voltage within the voltage tolerance of the PD controller. The VBUS sensing is achieved with NPN BJT Q3 with a voltage divider, resistors R1 and R2, and NMOS Q4 to disable/enable the R1 and R2 divider. When VBUS is operating in the SPR range Q4 is open where the VBUS_Divider GPIO is being driven low. When VBUS is operating in the EPR range Q4 is closed where the VBUS_Divider GPIO is being driven high. For the VBUS blocking PMOS Q1 implementation the gate is driven by a voltage divider R3 and R4 with the Q2 NMOS. The gate drive voltage divider is controlled by the inverted VBUS_Divider GPIO (nVBUS_Divider) on Q2. When VBUS is operating in the SPR range Q2 is closed where the nVBUS_Divider is being driven high. When VBUS is operating in the EPR range Q2 is open where the nVBUS_Divider is being driven low. The voltage divider R3 and R4 must be set to properly drive the PMOS Q1 gate at 5 V. To ensure that the PMOS Q1 gate is not damaged a Zener Diode D1 is used to clamp the gate voltage within the PMOS Q1 Gate Absolute Maximum Vgs. Since the EPR power path is providing all voltages on VBUS the PMOS Q1 must not be a high current capable but it must be able to tolerate the EPR voltage

range. To further protect the VBUS pin on the PD controller a TVS Diode D2 is recommended to absorb any transients above the PD controller's VBUS voltage range.

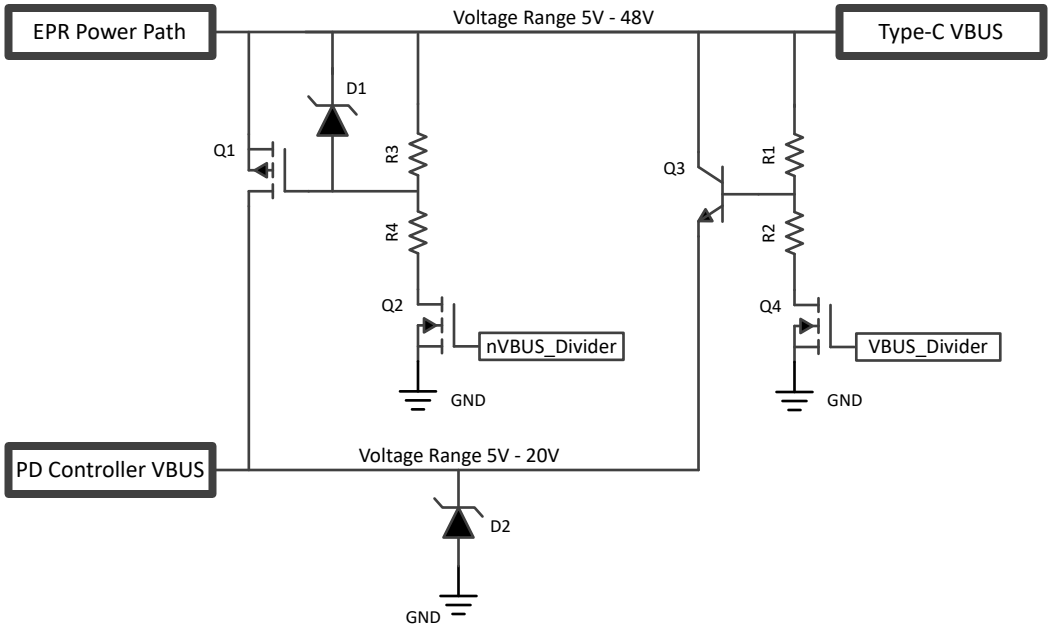


Figure 9-1. Source VBUS PMOS Protection & Sense

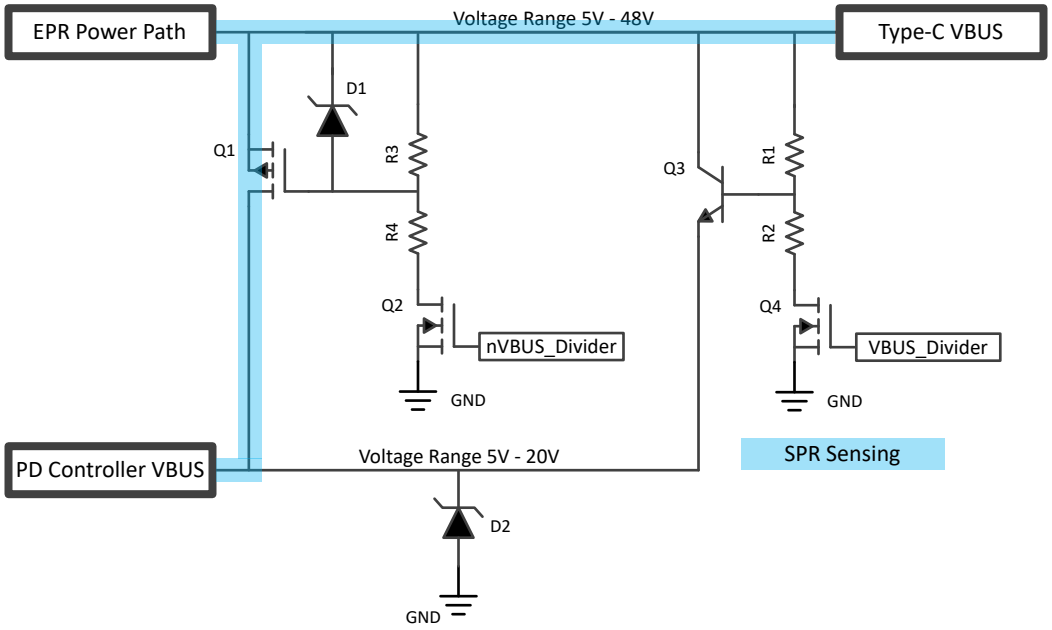


Figure 9-2. Source VBUS PMOS Protection & Sense - SPR

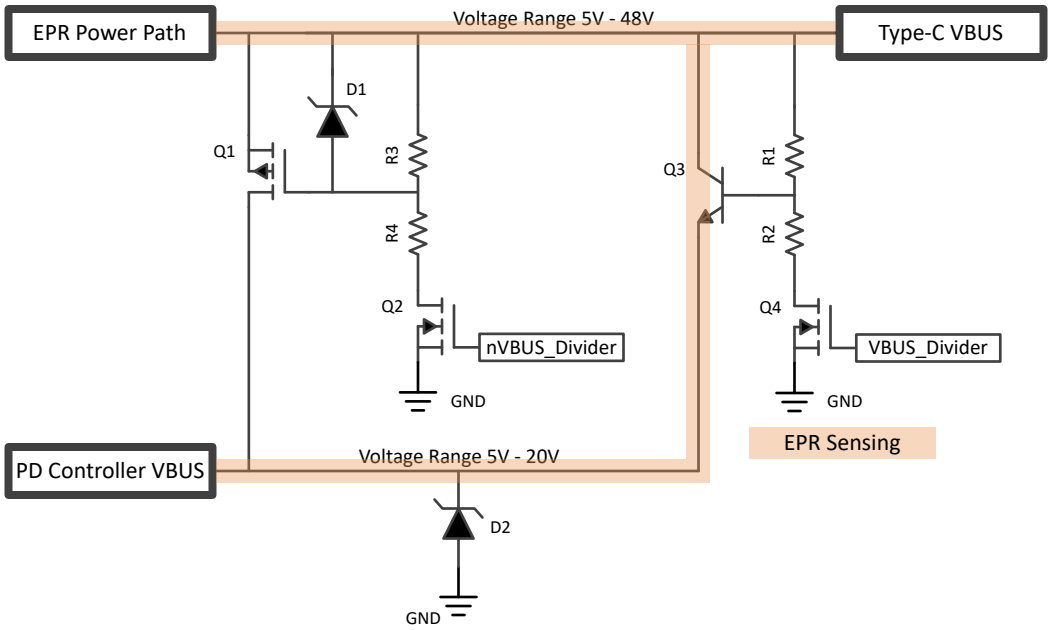


Figure 9-3. Source VBUS PMOS Protection & Sense - EPR

9.2.3.2 Extended Power Range VBUS PMOS Protection & Sense - DRP/Sink

For an EPR Dual Role Power and Sink applications that support dead battery, the VBUS pin of the PD controller must be protected from the EPR voltages but must be able to provide power to the PD Controller. In order to protect VBUS pin on the PD controller and sense the VBUS voltage at EPR voltage ranges, two circuits should be implemented. The VBUS blocking MOSFET circuit will protect the VBUS pin on the PD controller and VBUS sensing BJT circuit will provide a divided voltage within the voltage tolerance of the PD controller. The VBUS sensing is achieved with NPN BJT Q3 with a voltage divider, resistors R1 and R2, and NMOS Q4 to disable/enable the R1 and R2 divider. When VBUS is operating in the SPR range Q4 is open where the VBUS_Divider GPIO is being driven low. When VBUS is operating in the EPR range Q4 is closed where the VBUS_Divider GPIO is being driven high. For the VBUS blocking PMOS Q1 implementation the gate is driven by a voltage divider R3 and R4 with the Q2 NMOS. In order to drive the gate of NMOS Q2 in dead battery an additional circuit is needed. A voltage divider from VBUS R5 and R6 is used provide the gate voltage to Q2. The R5 and R6 voltage divider will be forced low through NMOS Q5 in an open drain configuration. The Q5 gate is controlled by the VBUS_Divider GPIO with a pull down R7 to ensure the Q5 gate does not float. The gate drive for Q2 is controlled by the VBUS_Divider GPIO when the PD controller powers up. When VBUS is operating in the SPR range Q2 is open where the VBUS_Divider is being driven low. When VBUS is operating in the EPR range Q2 is closed where the VBUS_Divider is being driven high. To ensure Q2's Gate Absolute Maximum Vgs is not violated, D3 Zener is used to clamp the gate voltage. The voltage divider R3 and R4 must be set to properly drive the PMOS Q1 gate at 5 V. To ensure that the PMOS Q1 gate is not damaged a Zener Diode D1 is used to clamp the gate voltage within the PMOS Q1 Gate Absolute Maximum Vgs. In an EPR sink only system, the PMOS Q1 must not be a high current capable but it must be able to tolerate the EPR voltage range. In an EPR DRP system where 5 V is provided by the PD controller's power path, PMOS Q1 must be a high current capable and must be able to tolerate the EPR voltage range. In an EPR DRP system, where VBUS is provided externally from the PD controller, the PMOS Q1 must not be a high current capable but it must be able to tolerate the EPR voltage range. To further protect the VBUS pin on the PD controller a TVS Diode D2 is recommended to absorb any transients above the PD controller's VBUS voltage range.

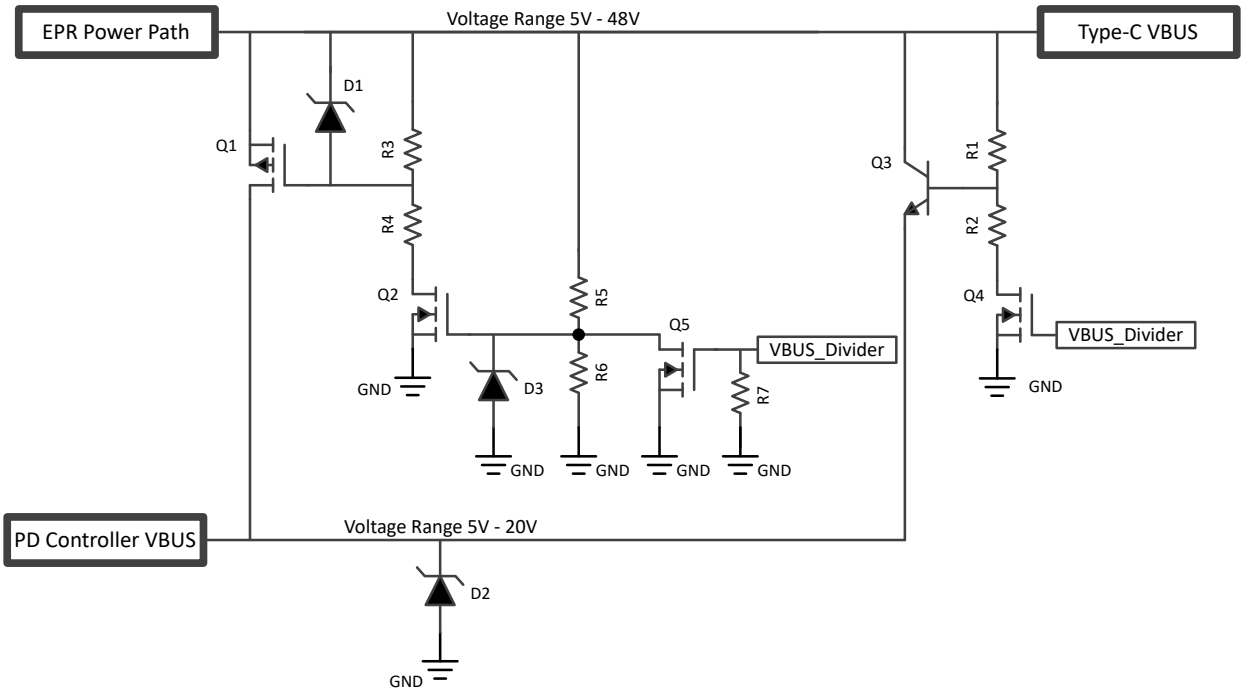


Figure 9-4. DRP & Sink VBUS PMOS Protection & Sense

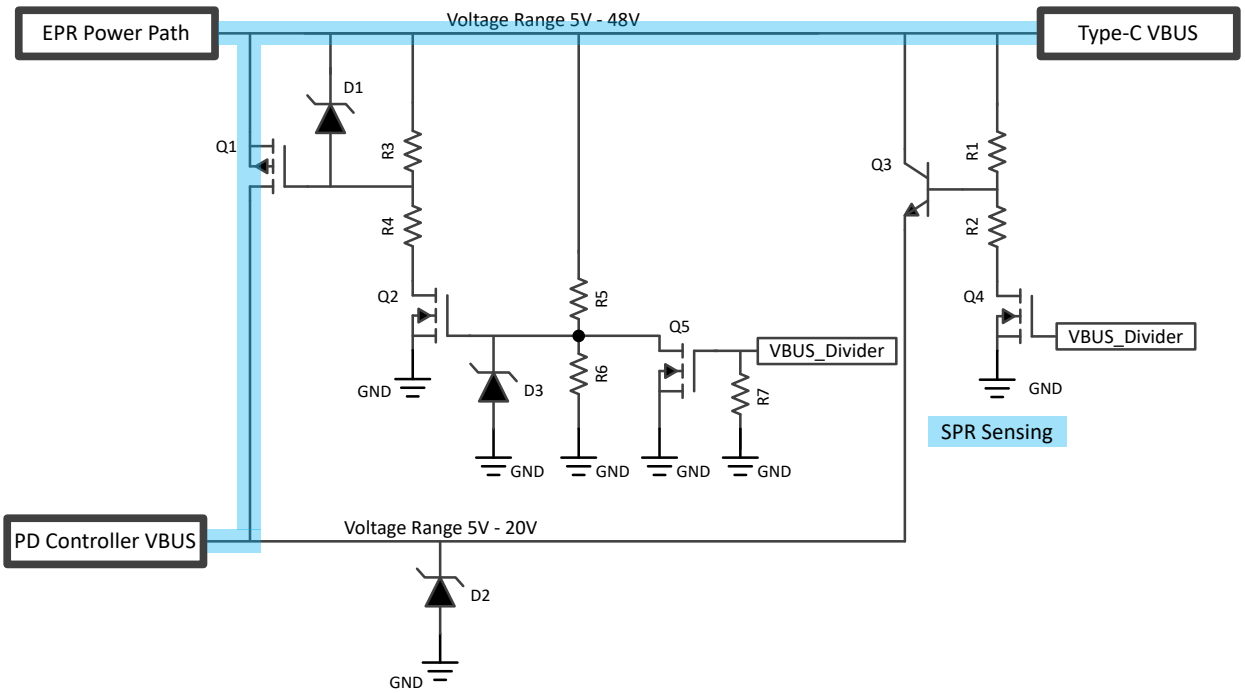


Figure 9-5. DRP & Sink VBUS PMOS Protection & Sense - SPR

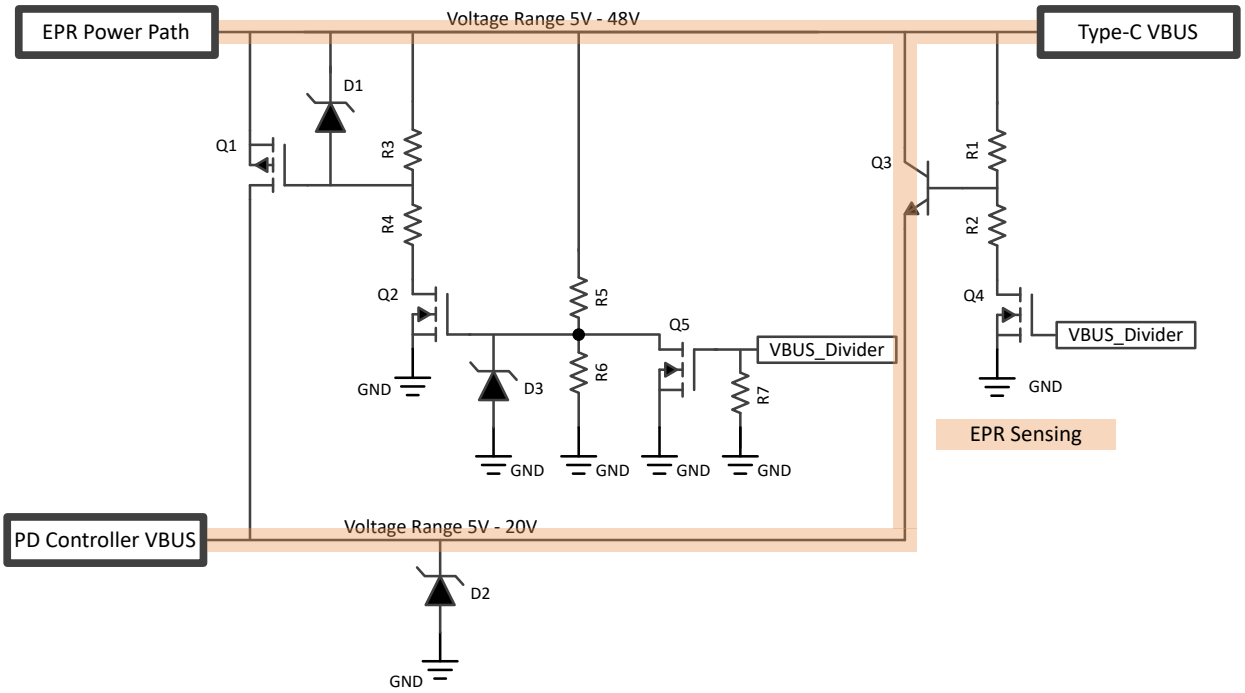


Figure 9-6. DRP & Sink VBUS PMOS Protection & Sense - EPR

9.2.3.3 Extended Power Range VBUS NMOS Protection & Sense

For an EPR source application, the VBUS pin of the PD controller must be protected from the EPR voltages.In order to protect VBUS pin on the PD controller and sense the VBUS voltage at EPR voltage ranges, two circuits should be implemented. The VBUS blocking MOSFET circuit will protect the VBUS pin on the PD controller and VBUS sensing BJT circuit will provide a divided voltage within the voltage tolerance of the PD controller. The VBUS sensing is achieved with NPN BJT Q3 with a voltage divider, resistors R1 and R2, and NMOS Q4 to disable/enable the R1 and R2 divider. When VBUS is operating in the SPR range Q4 is open where the VBUS_Divider GPIO is being driven low. When VBUS is operating in the EPR range Q4 is closed where the VBUS_Divider GPIO is being driven high. For the VBUS blocking NMOS Q1 implementation the gate is driven by Gate Driver Voltage with a series resistor R3 where the Gate Driver Voltage is controlled by a GPIO. When VBUS is operating in the SPR range Q1 is closed where the Gate Driver Voltage is enabled. When VBUS is operating in the EPR range Q2 is open where the Gate Driver Voltage is disabled. The Gate Driver Voltage must be sufficient enough to drive the gate of Q1 in the SPR range. Since the EPR power path is providing all voltages on VBUS the NMOS Q1 must not be a high current capable but it must be able to tolerate the EPR voltage range. To further protect the VBUS pin on the PD controller a TVS Diode D2 is recommended to absorb any transients above the PD controller's VBUS voltage range.

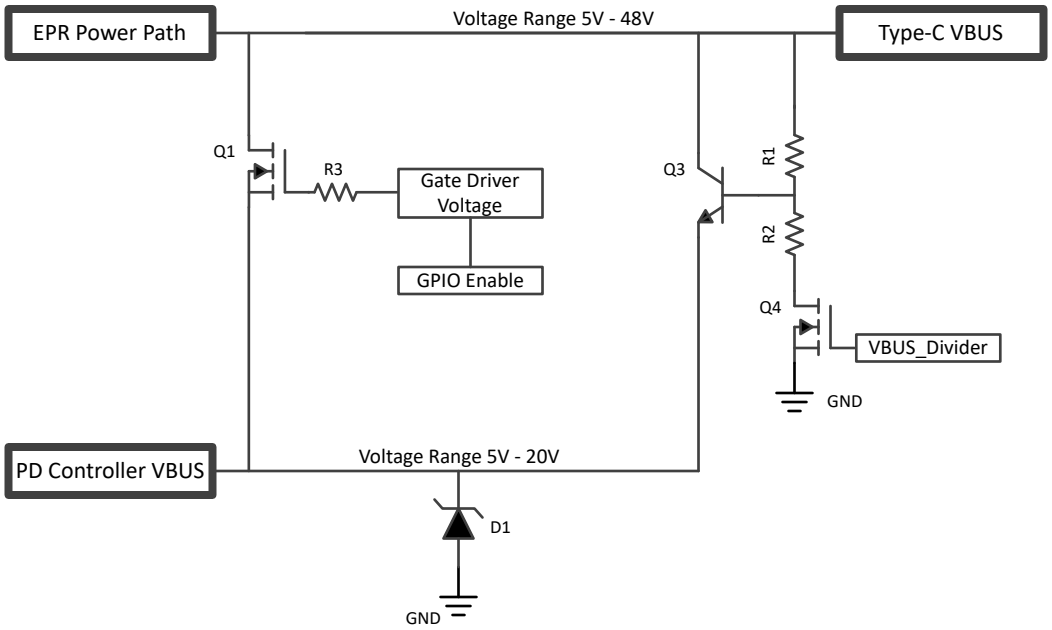


Figure 9-7. Source VBUS NMOS Protection & Sense

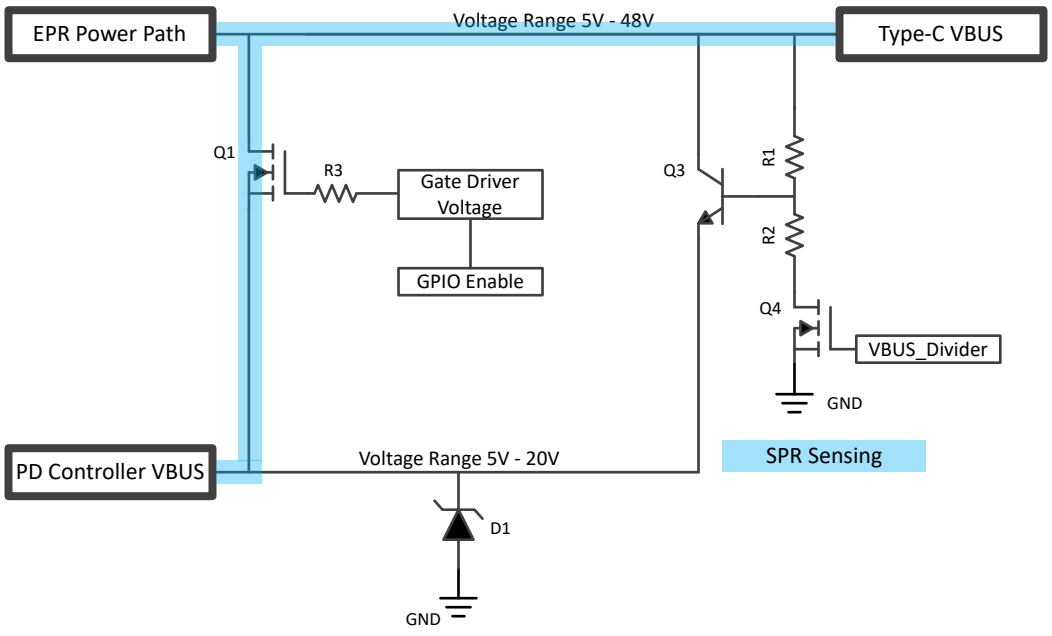


Figure 9-8. Source VBUS NMOS Protection & Sense - SPR

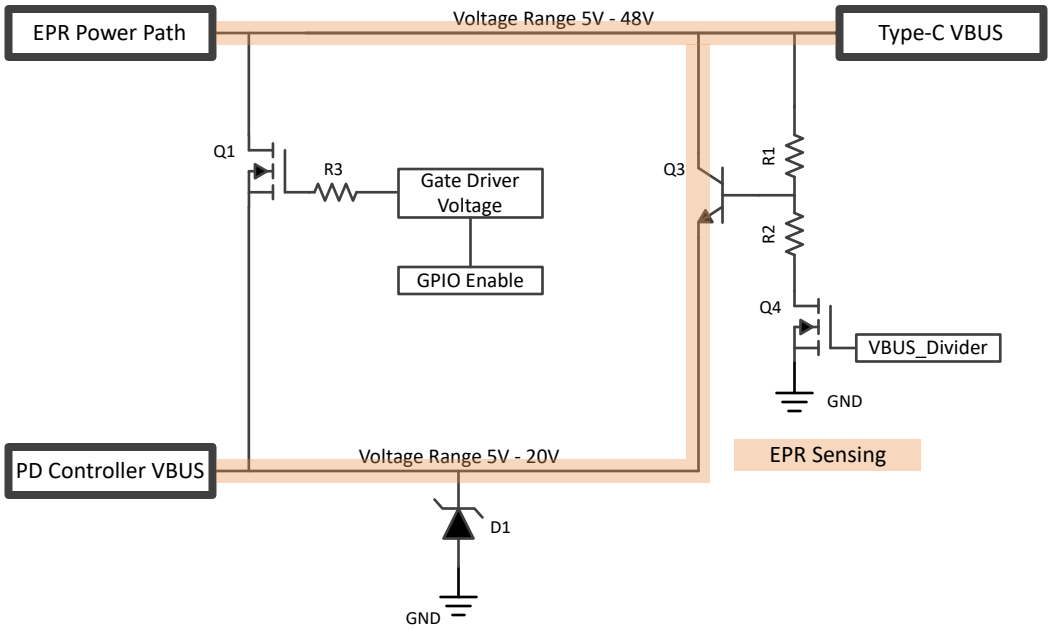


Figure 9-9. Source VBUS NMOS Protection & Sense - EPR

9.2.3.4 Extended Power Range VBUS NMOS Protection & Sense - DRP/Sink

For an EPR Dual Role Power and Sink applications that support dead battery, the VBUS pin of the PD controller must be protected from the EPR voltages but must be able to provide power to the PD Controller. In order to protect VBUS pin on the PD controller and sense the VBUS voltage at EPR voltage ranges, two circuits should be implemented. The VBUS blocking MOSFET circuit will protect the VBUS pin on the PD controller and VBUS sensing BJT circuit will provide a divided voltage within the voltage tolerance of the PD controller. The VBUS sensing is achieved with NPN BJT Q3 with a voltage divider, resistors R1 and R2, and NMOS Q4 to disable/ enable the R1 and R2 divider. When VBUS is operating in the SPR range Q4 is open where the VBUS_Divider GPIO is being driven low. When VBUS is operating in the EPR range Q4 is closed where the VBUS_Divider GPIO is being driven high. For the VBUS blocking NMOS Q1 implementation, the gate is driven by Gate Driver Voltage powered from VBUS with a series resistor R3 where the Gate Driver Voltage is controlled by a GPIO. The Gate Driver Voltage is generated from VBUS to provide the NMOS Q1 gate voltage in dead battery. When VBUS is operating in the SPR range Q1 is closed where the Gate Driver Voltage is enabled. When VBUS is operating in the EPR range Q2 is open where the Gate Driver Voltage is disabled. The Gate Driver Voltage must be sufficient enough to drive the gate of Q1 in the SPR range. In an EPR sink only system, the NMOS Q1 must not be a high current capable but it must be able to tolerate the EPR voltage range. In an EPR DRP system where 5 V is provided by the PD controller's power path, NMOS Q1 must be a high current capable and must be able to tolerate the EPR voltage range. In an EPR DRP system, where VBUS is provided externally from the PD controller, the NMOS Q1 must not be a high current capable but it must be able to tolerate the EPR voltage range. To further protect the VBUS pin on the PD controller a TVS Diode D2 is recommended to absorb any transients above the PD controller's VBUS voltage range.

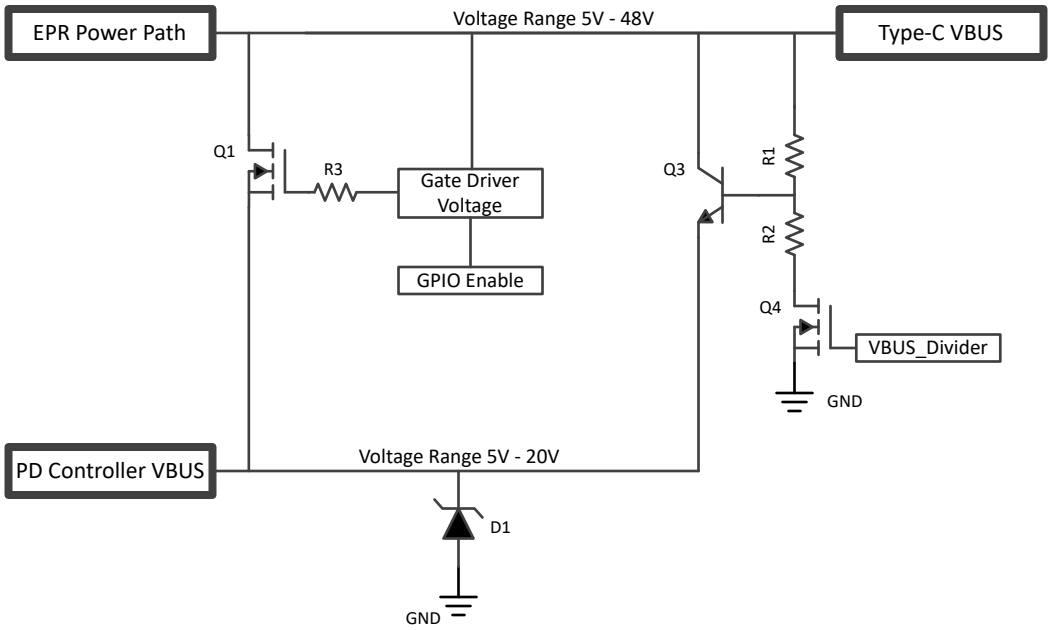


Figure 9-10. DRP & Sink VBUS NMOS Protection & Sense

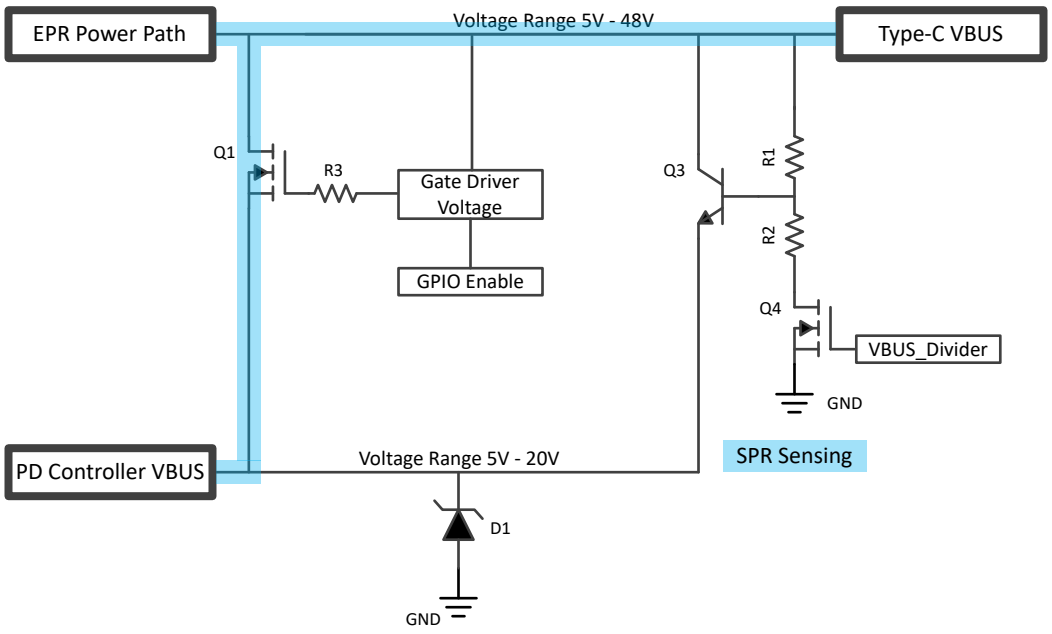


Figure 9-11. DRP & Sink VBUS PMOS Protection & Sense - SPR

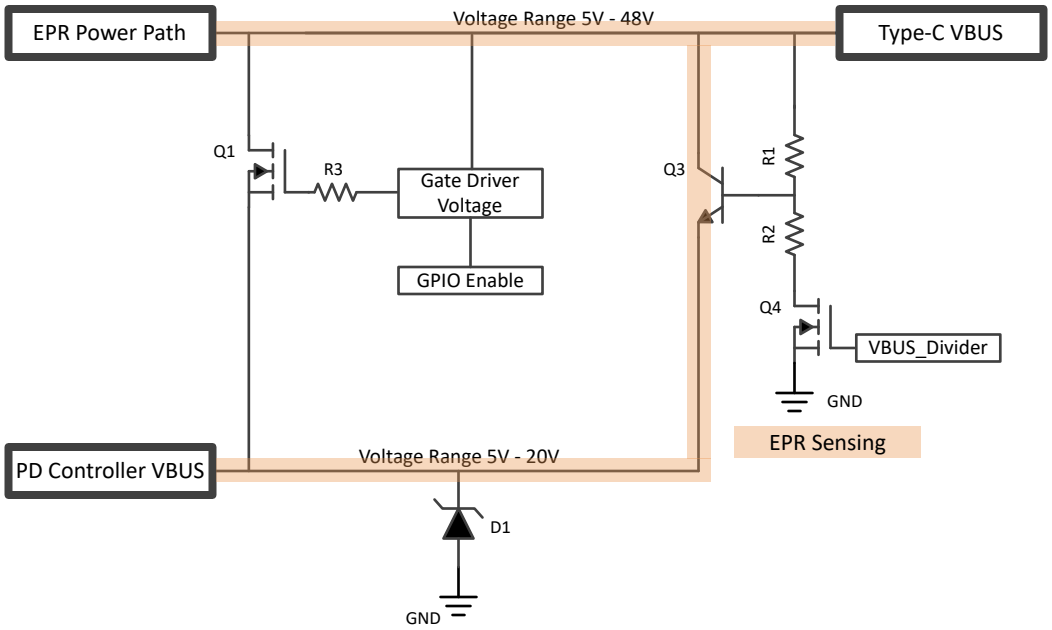


Figure 9-12. DRP & Sink VBUS PMOS Protection & Sense - EPR

9.2.3.5 Extended Power Range CC & SBU Protection

The SBU and CC pins are located next to the VBUS pins and are suspeptible to short to VBUS conditions when VBUS can be up to 48 V in EPR. To protect the PD controller and the system from a short to VBUS condition a blocking NMOS is used for each CC1/2 (Q1 & Q2) and SBU1/2 (Q3 & Q4). For CC1/2, the threshold must be set to allow for VCONN and minimize the impact of the NMOS Rdson. For SBU1/2, the threshold must be allowed to pass through AUX_P/N and SBTX/RX which is lower voltage than CC1/2. This requires two NMOS gate driver voltages needed to properly set the protection thresholds. To achieve this, a Gate Drive Supply is used with two voltage dividers to set the Vgs for the CC1/2 (R1||R2) and SBU1/2 (R3||R4) blocking NMOS gates. An optional capacitor can be used keep the voltage dividers more stable for CC1/2 (C1) and SBU1/2 (C2). The blocking NMOS Vds (Drain-to-Source Voltage) must be rated above the maximum VBUS voltage expected. The Vgs (Threshold Voltage) may vary since the votlage dividers can be adjusted to account for higher or lower Vgs. For the CC1/2 and SBU1/2 blocking NMOS, the added Rdson and Capacitance must be taken into account at the system level to meet impedance specifications. In additional to the blocking NMOS for CC1/2 and SBU1/2, it is recommended (but optional) to put an additional TVS (Transient Voltage Suppressor) between the blocking NMOS and system side. The TVS will absorb any voltage transients to further protect the system.

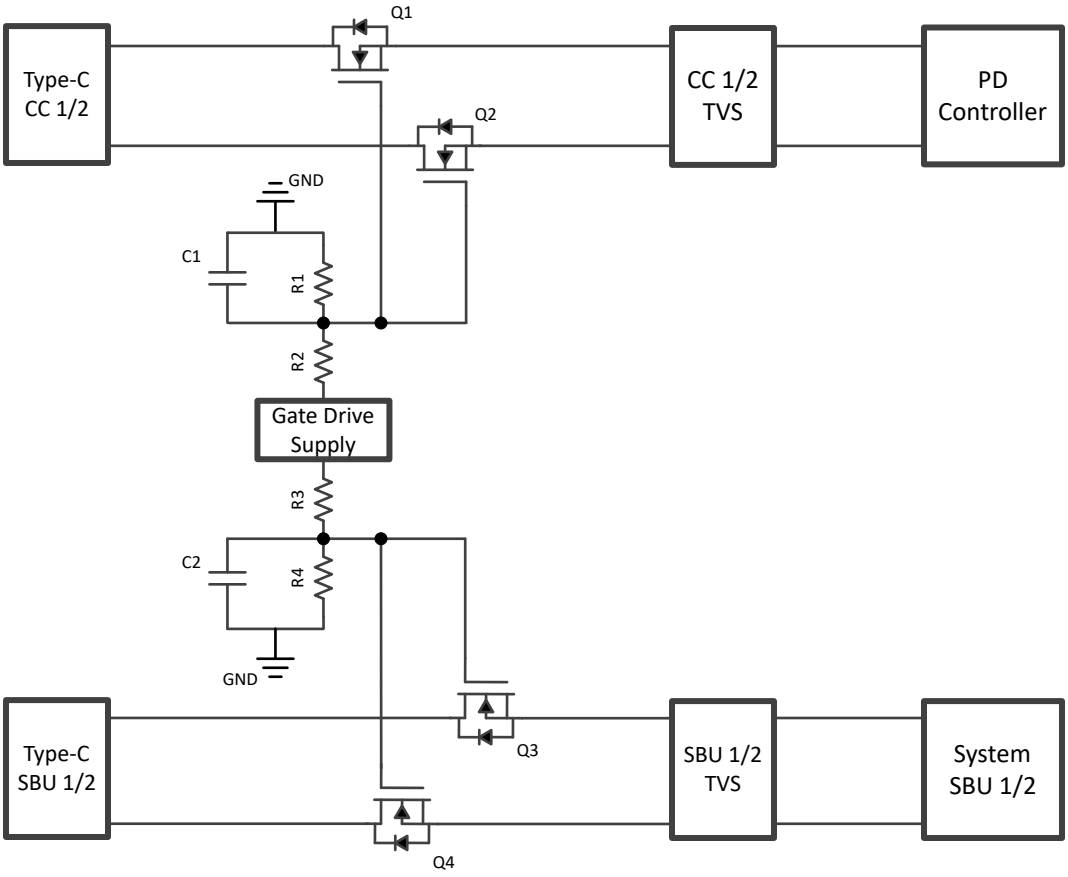


Figure 9-13. EPR CC & SBU Protection

9.2.3.6 Extended Power Range CC Dead Battery

The additional CC1/2 Extended Power Range (EPR) protection requires additional components to support dead battery conditions to place the CC Rd 5.1k Ohm termination. Rd1 and Rd1 are the dead battery CC pull downs that are asserted with Q1 (NMOS) and Q2 (NMOS) with R1 and R2 respectively. When a Rp is is connected through the Type-C cable, R1 or R2 will pull up the gate of Q1 or Q2, which will apply the Rd1 or Rd2 respectively. When the DFP provides VBUS the PD controller will power up and turn on the internal LDOs. The LDO output will drive the gate of Q3 pulling down the gates of Q1 and Q2 removing the Rd1 and Rd2 terminations. R3 is a weak pull down to ensure the gate of Q3 does not float. The zener diode D1 is used to prevent damage to the Q1 and Q2 gates in the event of a short to VBUS event. D1 should clamp above VCONN to not conduct when VCONN is sourced.

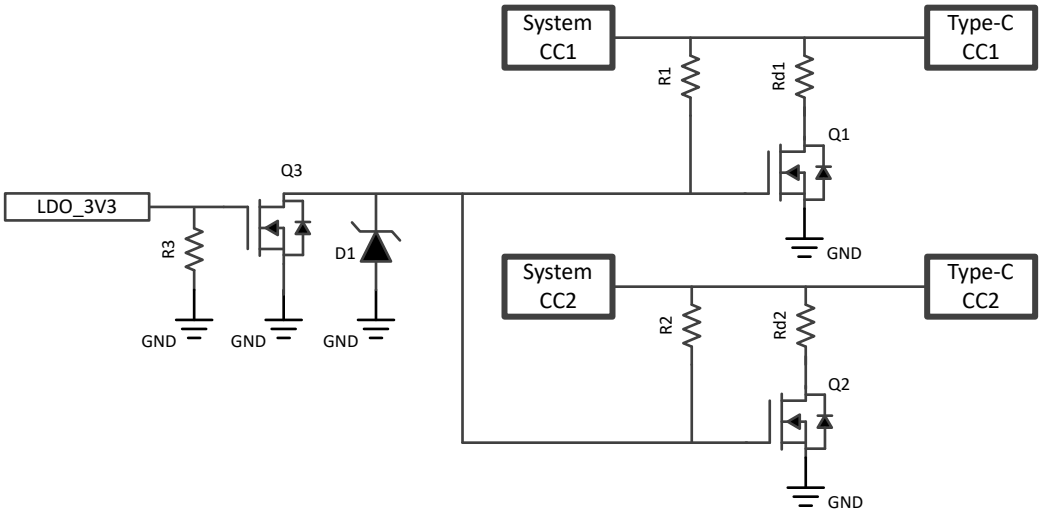


Figure 9-14. EPR CC Dead Battery

9.2.3.7 Extended Power Range Gate Driver Voltage for CC & SBU

The Gate Driver Voltage can be implemented in several was depending on the type of EPR system. This section provides guidance on several options. For a system that is a source only or will be externally powered, the Gate Driver Voltage for the CC and SBU protection can be generated from a charge pump from the VCONN 5 V rail. This would provide the rail for the voltage divider circuit for the SBU and CC protection NMOS. For a system that is a Dual Role Power or sink only that supports dead battery, two cascaded charge pumps can be used from LDO_3V3. This would provide the rail for the voltage divider circuit for the SBU and CC protection NMOS.

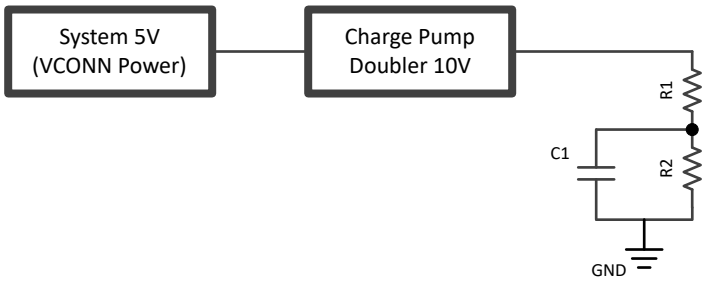


Figure 9-15. Gate Driver from VCONN Supply

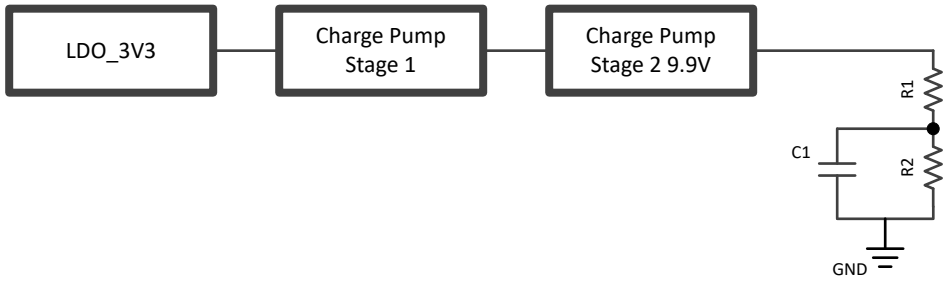


Figure 9-16. Gate Driver from LDO_3V3

9.2.3.8 USB4 Device Application

The figure below shows a USB4 Device application, where there are a total of four Type-C PD Ports. One port is the main connection to a USB4 Host, this is a UFP in terms of data and sources power. The other three ports are DFPs in terms of data and source power. Generally the main UFP source Type-C PD port provides the highest power to charge a USB4 Host. The key three devices in the system are the PD Controller(s), Dock Management Controller, and USB4 Hub Controller. In this application, two dual port PD controllers are used to determine the connection and provide power on the Type-C ports. The primary PD Controller manages Port A (UFP Source) and Port B (DFP Source). The secondary PD Controller manages the other two, Port C (DFP Source) and Port D (DFP Source). For systems that do not need all four ports or have different requirements, a combination of single and dual port PD Controllers may be used to scale for specific design requirements. The PD controllers have two I2C clients that are controlled by the Dock Management Controller and the USB4 Hub Controller. The Dock Management Controller (DMC), main functions are the Connection Manager, Power Manager (if applicable), Input Power Control (if applicable), Secure Firmware Update & booting of the PD controllers. The Connection Manager determines the capabilities of the UFP connection and sets the DFP capabilities accordingly. The Power Manager keeps the power allocated to each of the Type-C ports within a specific power budget and also monitors the entire system power to keep from over loading the Barrel Jack adapter supply. The DMC also controls the input power to the system and soft starts the power path to prevent large inrush currents when the Barrel Jack supply is connected. The Secure Firmware Update is accomplished over USB2, the DMC is connected to one of the USB2 DFP ports on the USB4 Hub Controller or USB2 Hub in the system. The DMC provides the Secure Firmware Update for itself and the PD controllers. The DMC will boot the PD controllers over the I2C connection. The I2C connection between the DMC and PD controllers also serves as communication channel for the Connection and Power Manager. The USB4 Hub Controller manages the data paths for all of the Type-C ports and determines the required data protocol by reading the PD controller status over I2C connection. The UFP port is the main connection to the USB4 Hub Controller from a USB4 host. The other DFP ports act as expansion ports to connect other USB Type-C & PD devices.

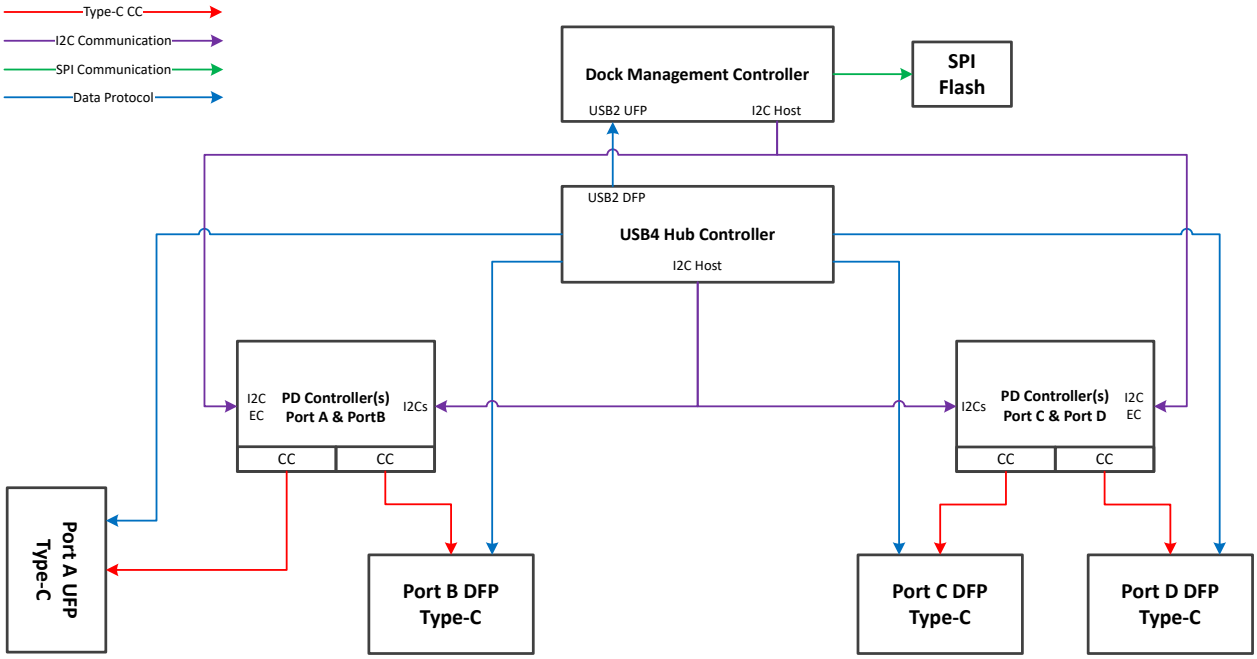


Figure 9-17. USB4 Device Application

9.2.3.9 UBS4 Hub Controller & PD Controller I2C Communication

The I2C connection from the PD controllers and the USB4 Hub Controller communicates the connection present at the Type-C Ports. The PD controllers have an option to use the shared interrupt for both ports or to have a separate interrupt for each port that is mapped to a GPIO in its configuration. In the shared interrupt case, the USB4 Hub Controller will query both port addresses and will determine which port has a data connection. For the dedicated interrupt the USB4 hub controller will only query the specific port address and determine the connection present.

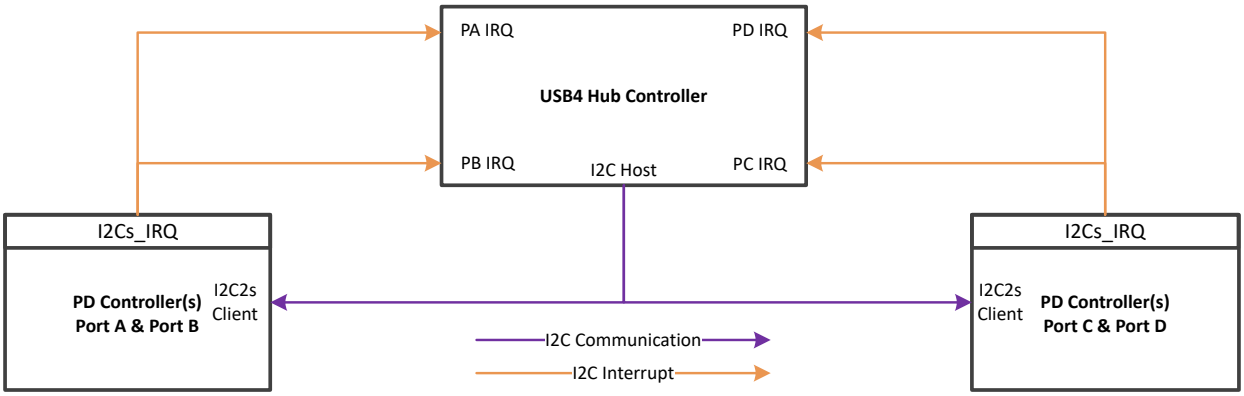


Figure 9-18. USB4 Hub Contoller & PD Controller Shared IRQ

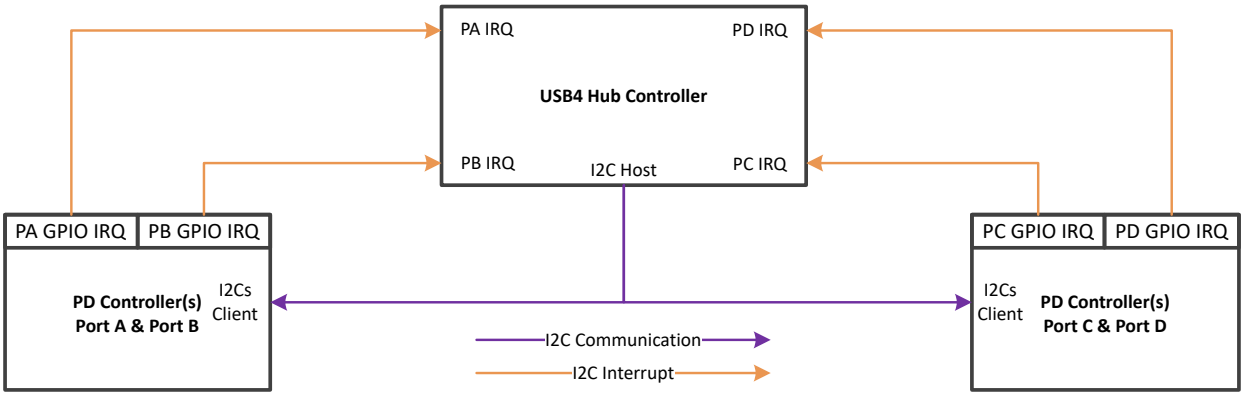


Figure 9-19. USB4 Hub Contoller & PD Controller Dedicated IRQ

The table below shows an exampl eof the port I2C address for each of the PD Controller ports.

Table 9-3. Recommended I2C Addresses - USB4 Hub Controller

PORT	I2C ADDRESS
Port A	0x38
Port B	0x3F
Port C	0x48
Port D	0x4F

9.2.3.10 Dock Management Controller & PD Controller I2C Communication

The I2C connection from the PD controllers and the Dock Management Controller communicates to boot up the PD controllers and enable the Connection & Power Manager functions. The DMC has two GPIOs dedicated for Port A/B and Port C/D interrupts. The shared interrupt connection to the DMC will query both port addresses and will determine which port has been updated.

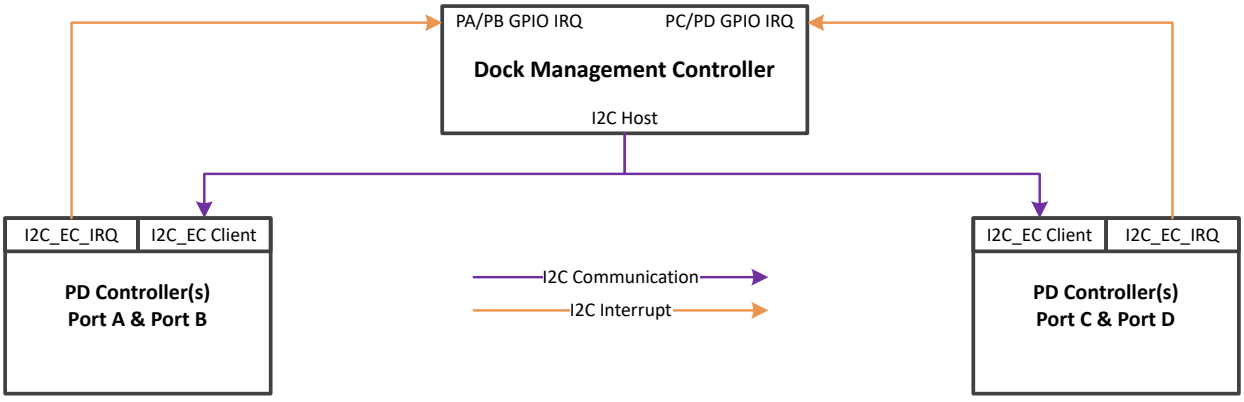


Figure 9-20. DMC & PD Controller I2C Communication

The table below shows an example of the I2C addresses for each of the PD controllers ports.

Table 9-4. Recommended I2C Addresses - DMC

PORT	I2C ADDRESS
Port A	0x20
Port B	0x24
Port C	0x21
Port D	0x25

9.3 VBUS Schottky and TVS Diodes

Schottky diodes are used on VBUS to help absorb large GND currents when a Type-C cable is removed while drawing high current. The inductance in the cable will continue to draw current on VBUS until the energy stored is dissipated. Higher currents could cause the body diodes on IC devices connected to VBUS to conduct. When the current is high enough it could damage the body diodes of IC devices. Ideally, a VBUS Schottky diode should have a lower forward voltage so it can turn on before any other body diodes on other IC devices. Schottky diodes on VBUS also help during hard shorts to GND which can occur with a faulty Type-C cable or damaged Type-C PD device. VBUS could ring below GND which could damage devices hanging off of VBUS. The Schottky diode will start to conduct once VBUS goes below the forward voltage. When the TPS25815 is the only device connected to VBUS, place the Schottky Diode close to the VBUS pin of the TPS25815.

TVS Diodes help suppress and clamp transient voltages. Most TVS diodes can fully clamp around 10 ns and can keep the VBUS at their clamping voltage for a period of time. Looking at the clamping voltage of TVS diodes after they settle during a transient will help decide which TVS diode to use. The peak power rating of a TVS diode must be able to handle the worst case conditions in the system.

9.4 Application Curves

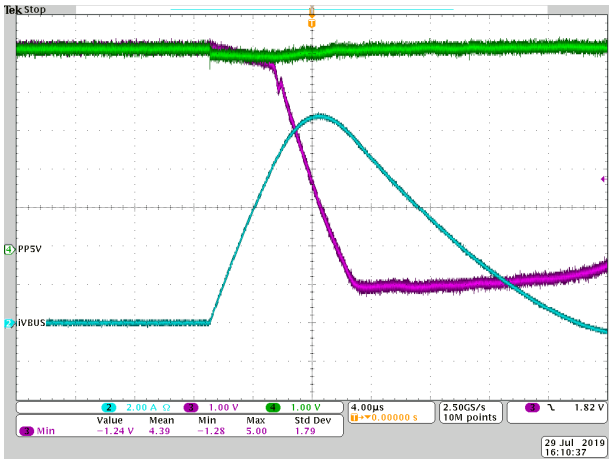


Figure 9-21. Px_VBUS Short with TVS2200, but Without Schottky Diode

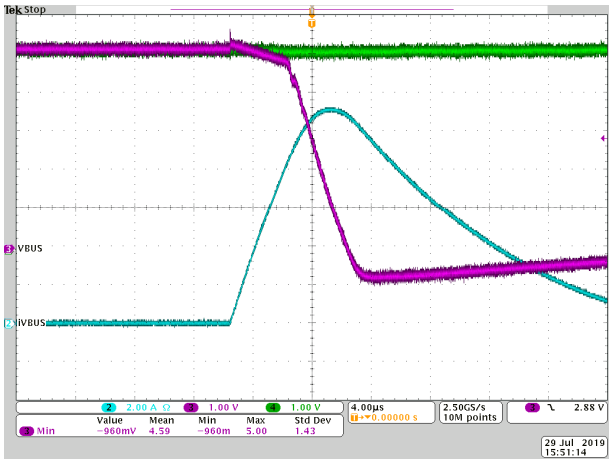


Figure 9-22. Px_VBUS Short with TVS2200 and Schottky Diode

10 Power Supply Recommendations

10.1 3.3-V Power

10.1.1 VIN_3V3 Input Switch

The VIN_3V3 input is the main supply of the TPS65992SBG device. The VIN_3V3 switch (see *Power Management*) is a uni-directional switch from VIN_3V3 to LDO_3V3, not allowing current to flow backwards from LDO_3V3 to VIN_3V3. This switch is on when the 3.3 V supply is available and the dead-battery flag is cleared. The recommended capacitance C_{VIN_3V3} (see the Recommended Capacitance in the *Specifications* section) should be connected from the VIN_3V3 pin to the GND pin).

10.1.2 VBUS 3.3-V LDO

The 3.3 V LDO from VBUS to LDO_3V3 steps down voltage from the VBUS pin to LDO_3V3 which allows the TPS65992SBG device to be powered from VBUS when VIN_3V3 is unavailable. This LDO steps down any recommended voltage on the VBUS pin. When VBUS reaches 20 V, which is allowable by USB PD, the internal circuitry of the TPS65992SBG device operates without triggering thermal shutdown; however, a significant external load on the LDO_3V3 pin or any GPIOx pin can increase temperature enough to trigger thermal shutdown. Keep the total load on LDO_3V3 within the limits from the *Recommended Operating Conditions* in the *Specifications* section. Connect the recommended capacitance C_{VBUS} (see *Recommended Capacitance* in the *Specifications* section) from the VBUS pin to the GND pin.

10.2 1.5-V Power

The internal circuitry is powered from 1.5 V. The 1.5-V LDO steps the voltage down from LDO_3V3 to 1.5 V. The 1.5-V LDO provides power to all internal low-voltage digital circuits which includes the digital core, and memory. The 1.5-V LDO also provides power to all internal low-voltage analog circuits. Connect the recommended capacitance C_{LDO_1V5} (see the Recommended Capacitance in the *Specifications* section) from the LDO_1V5 pin to the GND pin.

10.3 Recommended Supply Load Capacitance

The Recommended Capacitance in the *Specifications* section lists the recommended board capacitances for the various supplies. The typical capacitance is the nominally rated capacitance that must be placed on the board as close to the pin as possible. The maximum capacitance must not be exceeded on pins for which it is specified. The minimum capacitance is minimum capacitance allowing for tolerances and voltage derating ensuring proper operation.

11 Layout

11.1 Layout Guidelines

Proper routing and placement will maintain signal integrity for high speed signals and improve the heat dissipation from the TPS65992SBG power path. The combination of power and high speed data signals are easily routed if the following guidelines are followed. It is a best practice to consult with board manufacturing to verify manufacturing capabilities.

11.1.1 Top TPS65992SBG Placement and Bottom Component Placement and Layout

When the TPS65992SBG is placed on top and its components on bottom the solution size will be at its smallest.

11.2 Layout Example

Follow the differential impedances for Super / High Speed signals defined by their specifications (DisplayPort - AUXN/P and USB2.0). All I/O will be fanned out to provide an example for routing out all pins, not all designs will utilize all of the I/O on the TPS65992SBG.

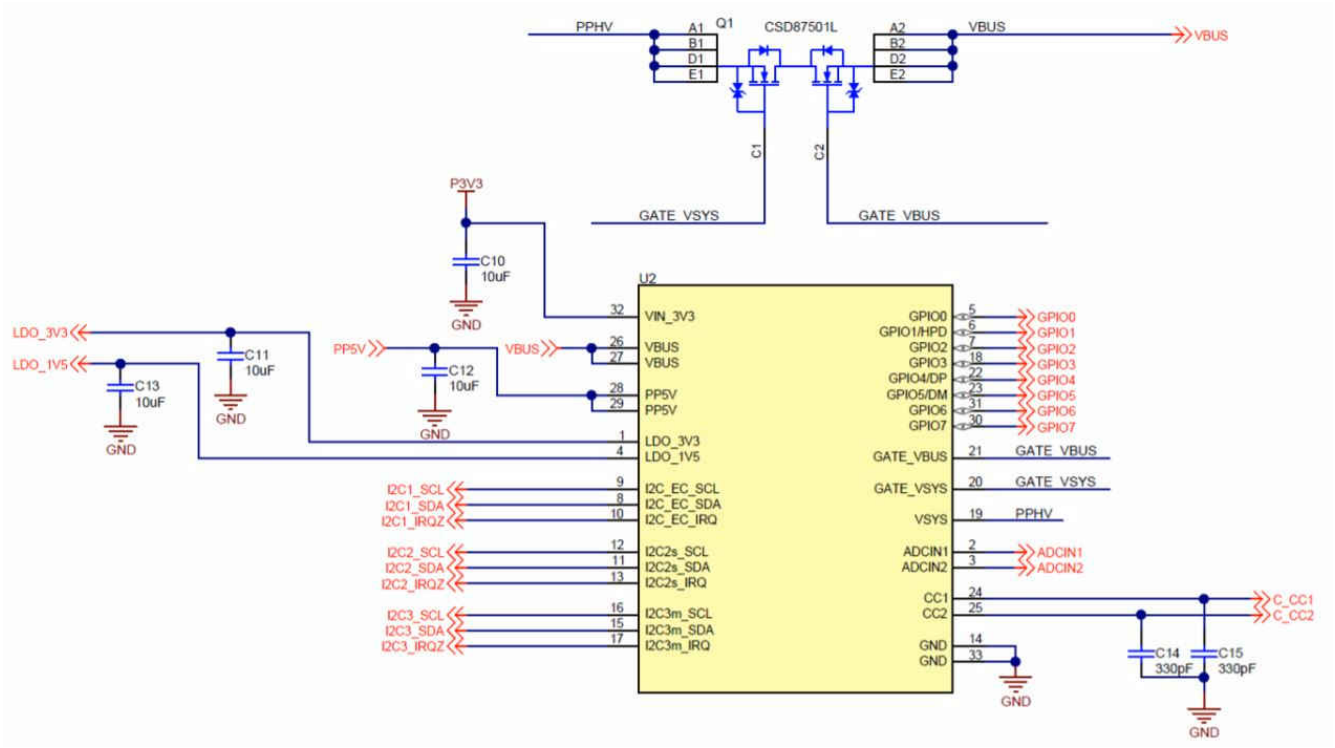


Figure 11-1. Example Schematic

11.3 Component Placement

Top and bottom placement is used for this example to minimize solution size. The TPS65992SBG is placed on the top side of the board and the majority of its components are placed on the bottom side. When placing the components on the bottom side, it is recommended that they are placed directly under the TPS65992SBG. When placing the PP5V capacitors it is easiest to place them with the GND terminal of the capacitors to face inward the TPS65992SBG or to the side. All other components that are for pins on the GND pad side of the TPS65992SBG should be placed where the GND terminal is underneath the GND pad.

The CC capacitors should be placed on the same side as the TPS65992SBG close to the respective CC1 and CC2 pins. Do NOT via to another layer in between the CC pins to the CC capacitor, placing a via after the CC capacitor is recommended.

The ADCIN1/2 voltage divider resistors can be placed where convenient.

The figures below show the placement in 2-D and 3-D.

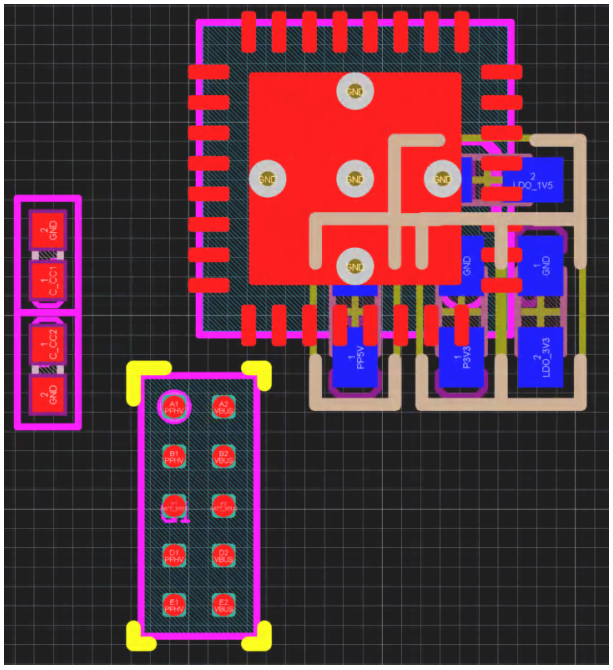


Figure 11-2. Top View Layout

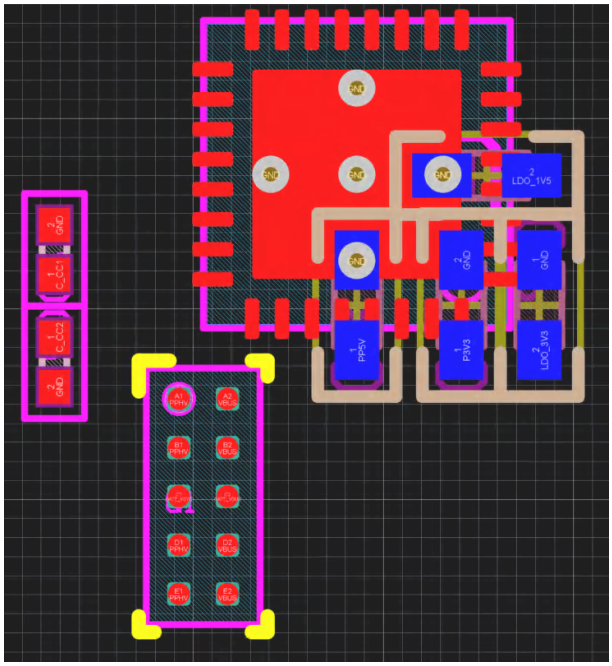


Figure 11-3. Bottom View Layout

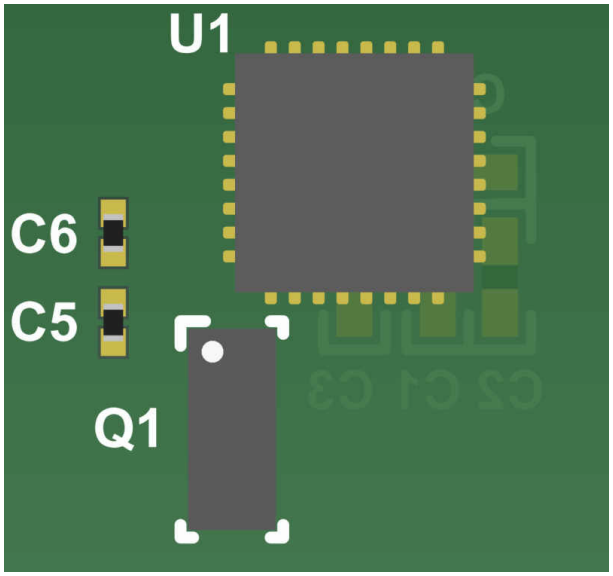


Figure 11-4. Top View 3-D

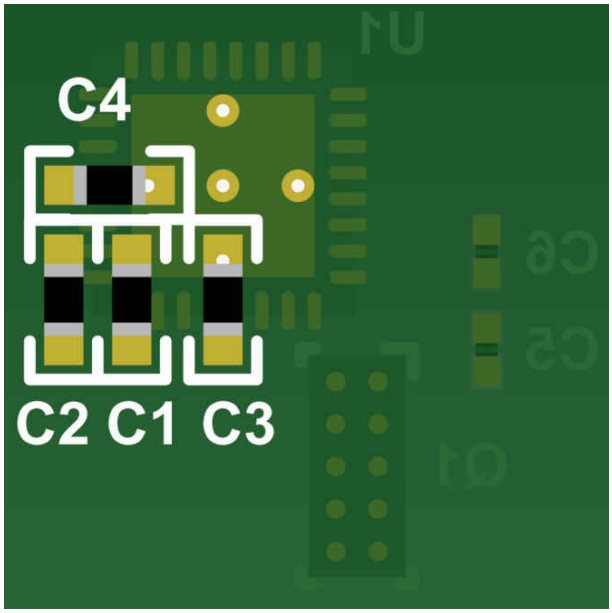


Figure 11-5. Bottom View 3-D

11.4 Routing PP5V, VBUS, PPHV, VIN_3V3, LDO_3V3, LDO_1V5

On the top side, create pours for PP5V, VBUS, and PPHV. Connect PP5V from the top layer to the bottom layer using at least 8, 8-mil hole and 16-mil diameter vias. Connect PPHV from the top layer to the bottom layer using at least 12, 8-mil hole and 16-mil diameter vias. See Figure 11-6 for the recommended via sizing. The via placement and copper pours are highlighted in Figure 11-7.

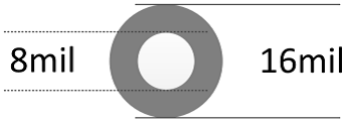


Figure 11-6. Recommended Minimum Via Sizing

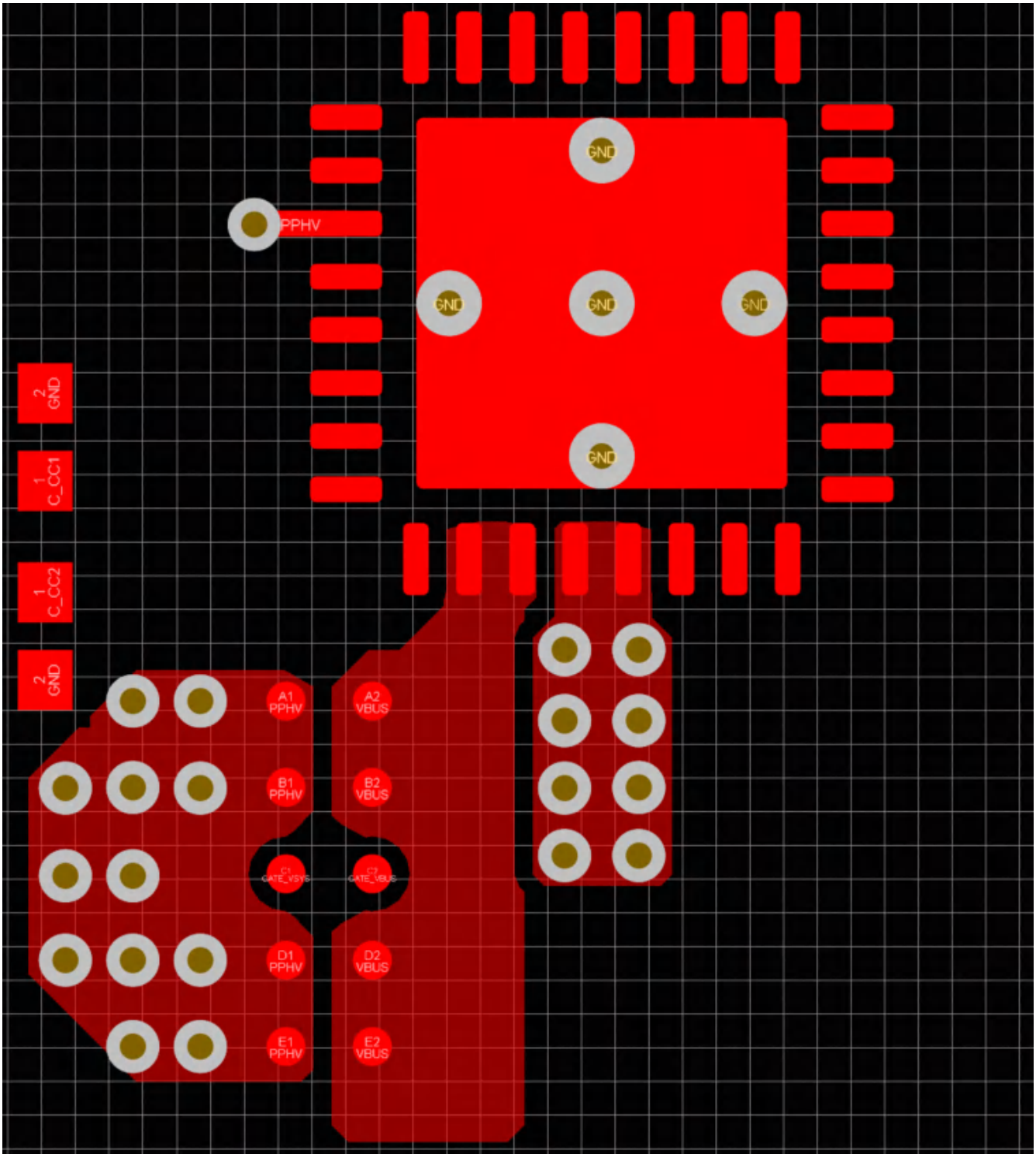


Figure 11-7. PP5V and VBUS1/2 Copper Pours and Via Placement

Next, VIN_3V3, LDO_3V3, and LDO_1V5 will be routed to their respective decoupling capacitors. Additionally, a copper pour on the bottom side is added to connect PP5V to the decoupling capacitors located on the bottom of the PCB. This is highlighted in Figure 11-8.

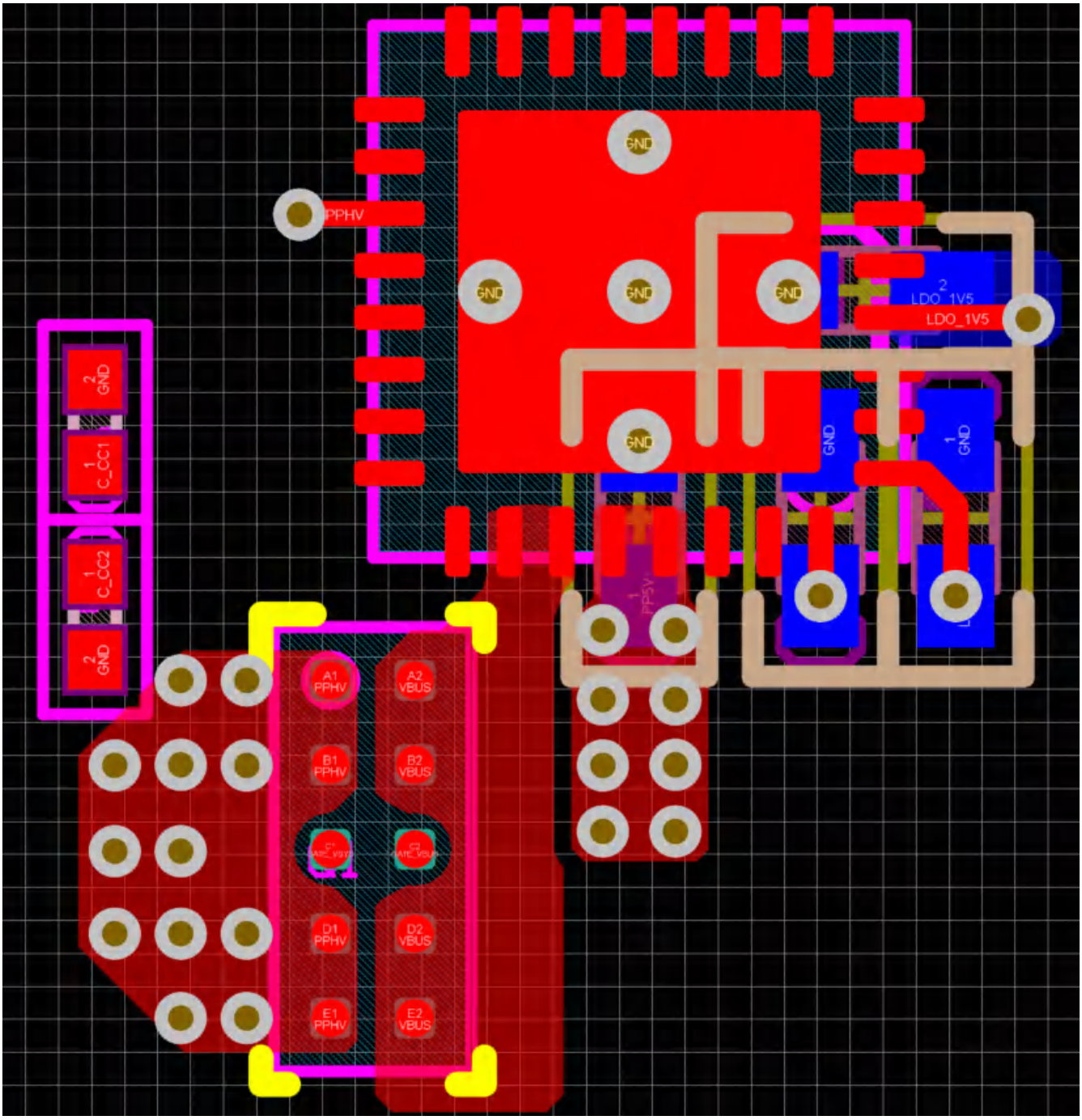


Figure 11-8. VIN_3V3, LDO_3V3, and LDO_1V5 Routing

The following figures show how to properly connect VSYS and the SYS_Gate control signals for the external N-FETs. The control signals can be routed on an internal layer using a 12-mil trace, and the trace going to VSYS should be as short as possible to minimize impedance, so placing a via directly on the high-voltage power path is ideal.

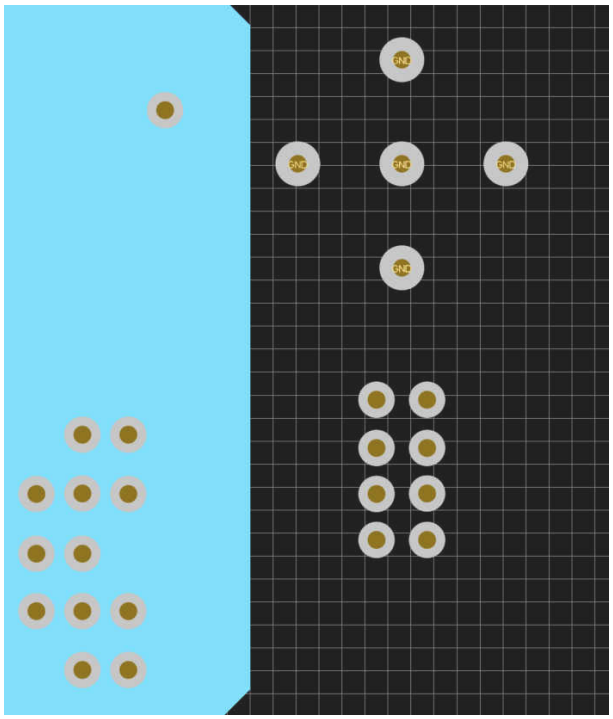


Figure 11-9. Top Polygon Pours

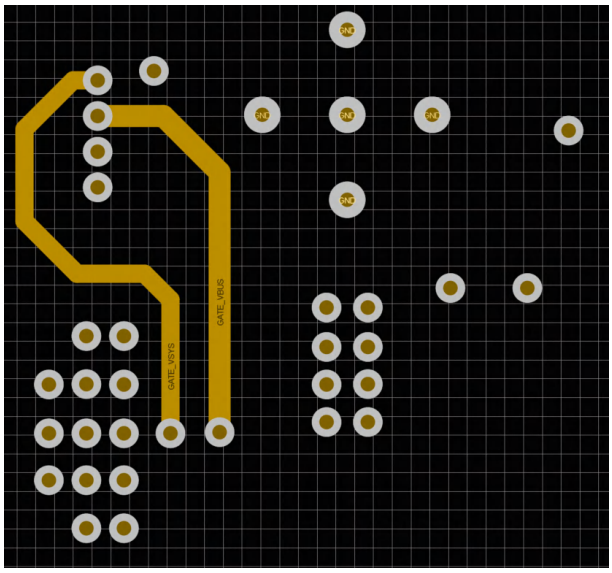


Figure 11-10. Bottom Polygon Pours

11.5 Routing CC and GPIO

Routing the CC lines with a 10-mil trace will ensure the needed current for supporting powered Type-C cables through VCONN. For more information on VCONN refer to the Type-C specification. For capacitor GND pin use a 16-mil trace if possible.

Most of the GPIO signals can be fanned out on the top or bottom layer using either a 8-mil trace or a 10-mil trace. The following images highlights how the CC lines and GPIO's are routed out.

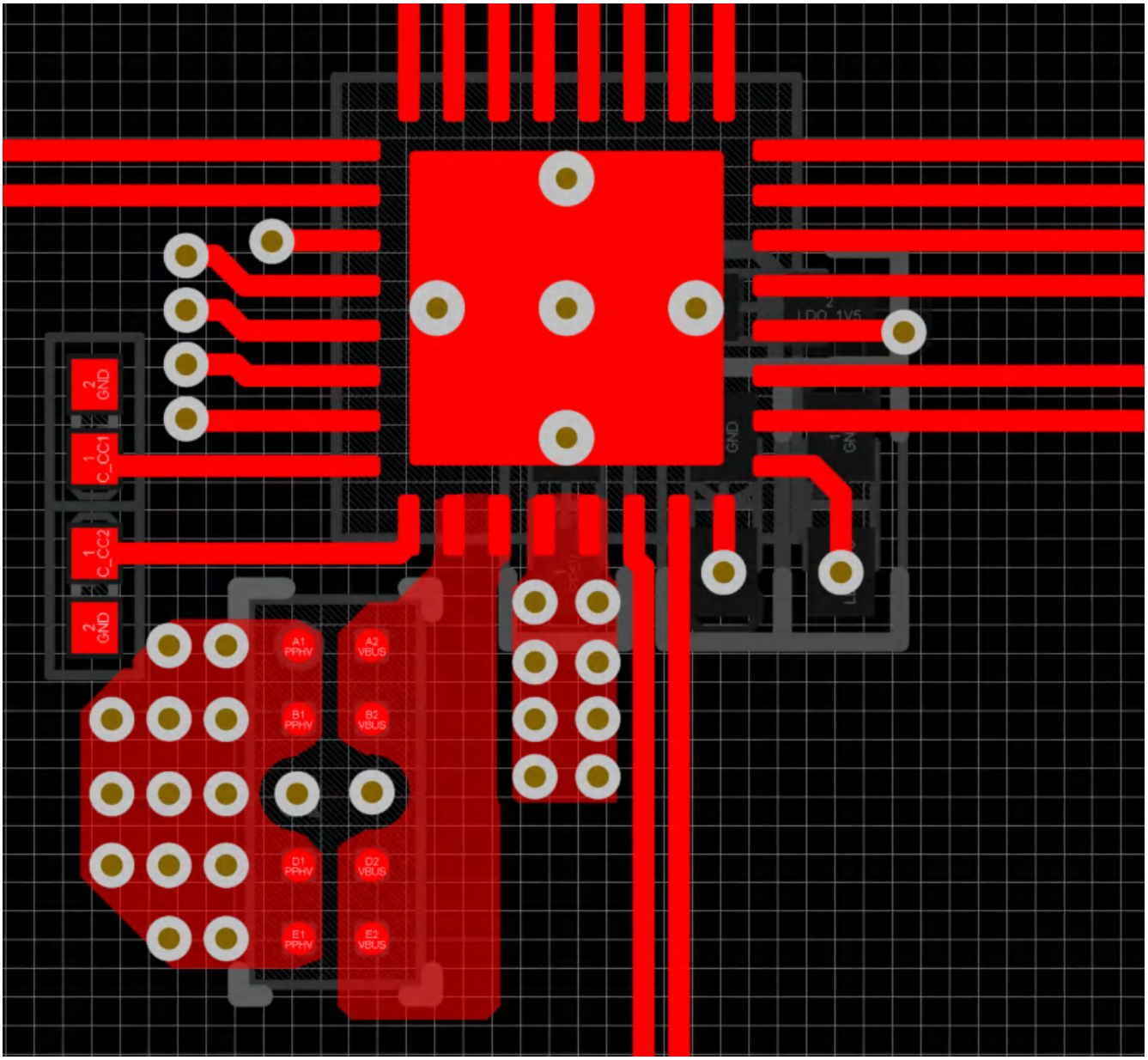


Figure 11-11. Top Layer GPIO Routing

Table 11-1. Routing Widths

ROUTE	WIDTH (mil minimum)
CC1, CC2	8
VIN_3V3, LDO_3V3, LDO_1V5	6
Component GND	10
GPIO	4

12 Device and Documentation Support

12.1 Device Support

12.1.1 Third-Party Products Disclaimer

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12.2 Documentation Support

12.2.1 Related Documentation

- *USB-PD Specifications*
- *USB Power Delivery Specification*

12.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

13.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(3)	MSL Peak Temp(4)	Op Temp	Device Marking(5) (6)
TPS65992SBGRSMR	ACTIVE	VQFN	RSM	32	3000	Green (RoHS& no Sb/Br)	NiPdAu / NiPdAuAg	Level-2-260C-1 YEAR	-40 to 125	T65992S BG

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

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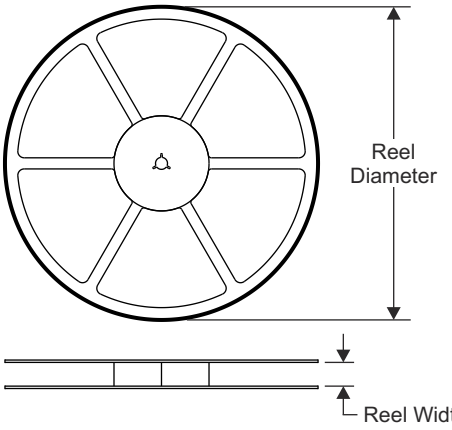
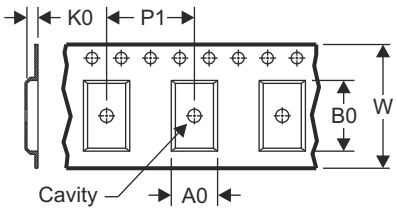
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

13.2 Tape and Reel Information

REEL DIMENSIONS

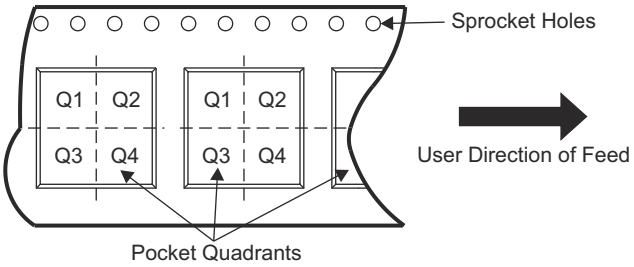


TAPE DIMENSIONS



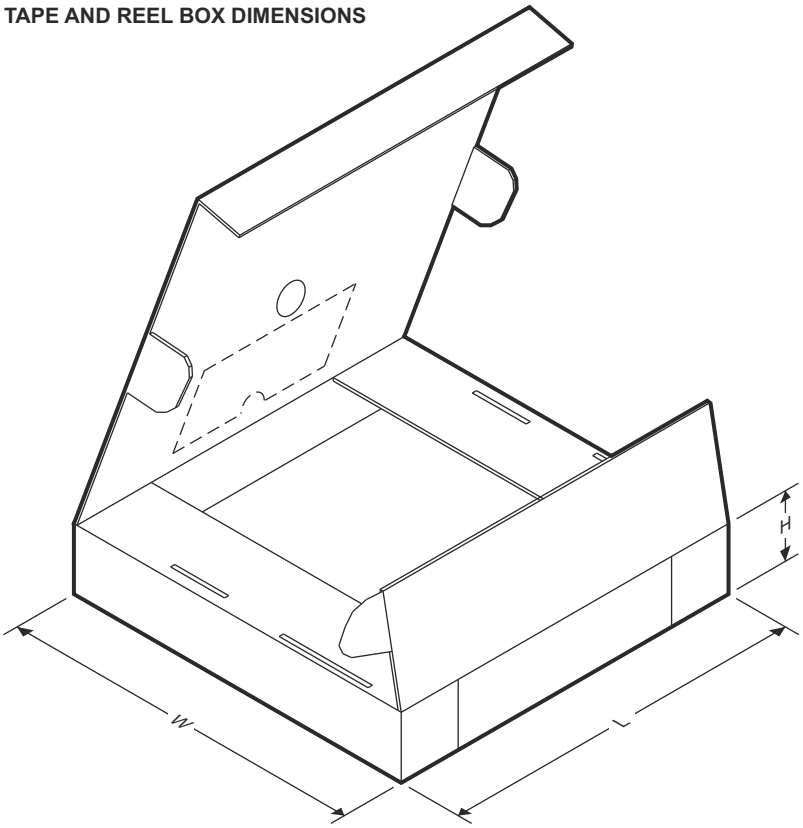
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS65992SBGRSMR	VQFN	RSM	32	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

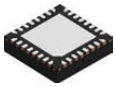
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS65992SBGRSMR	VQFN	RSM	32	3000	367.0	367.0	35.0

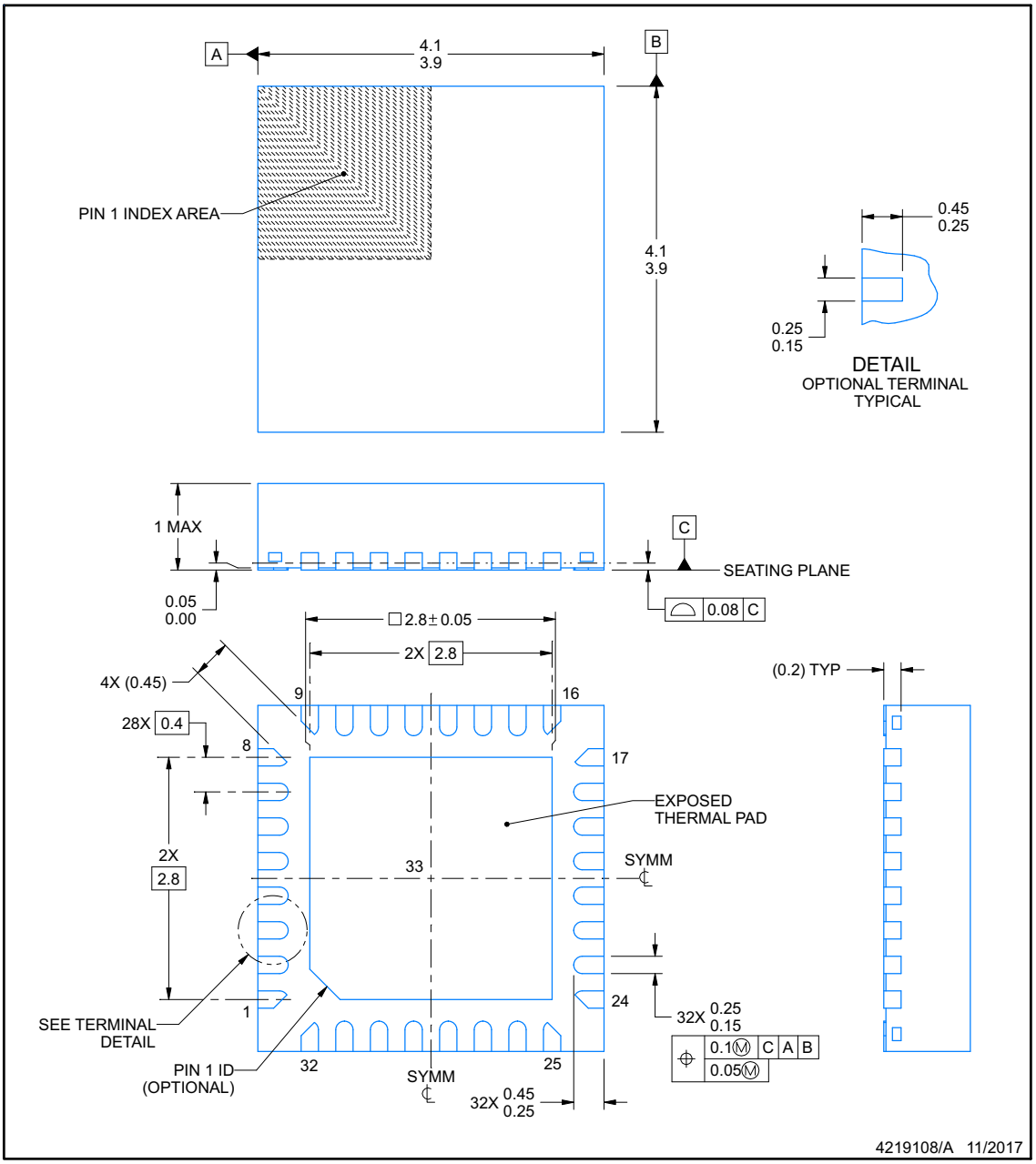
PACKAGE OUTLINE

RSM0032B



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

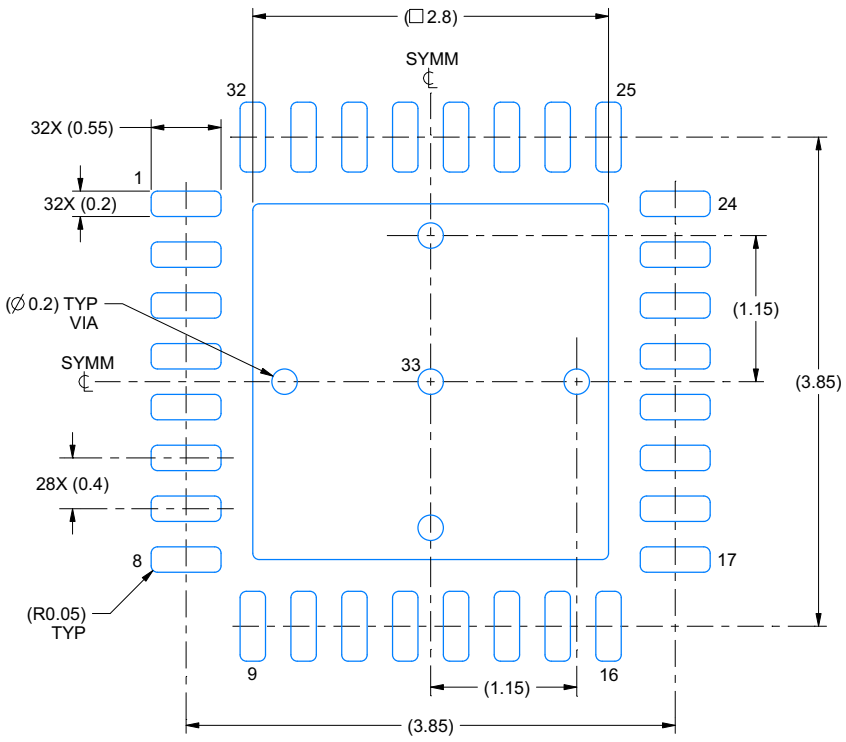
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

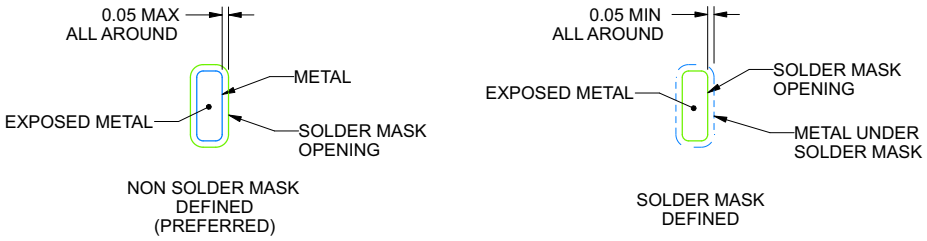
RSM0032B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4219108/A 11/2017

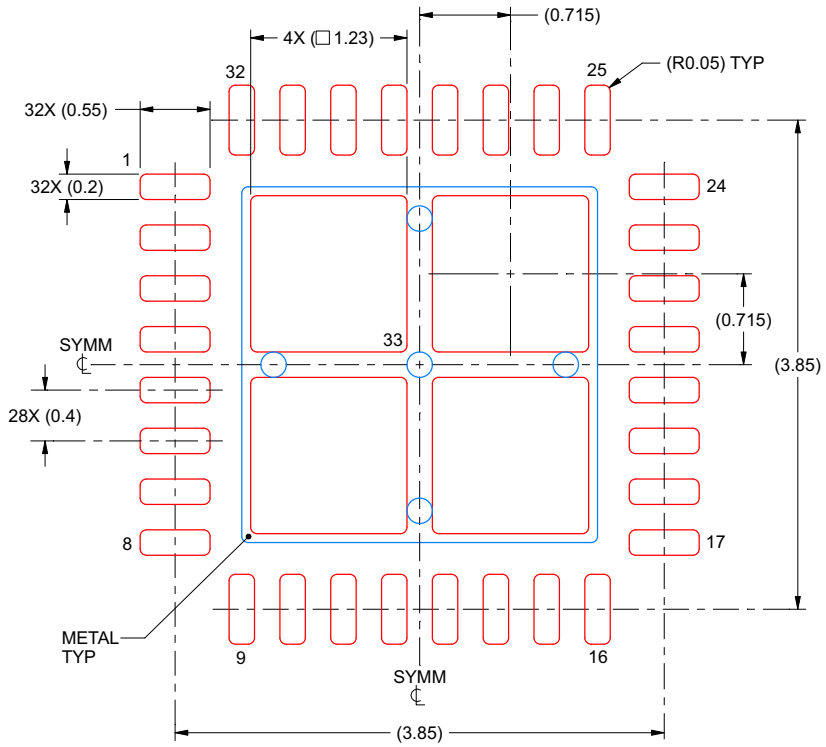
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RSM0032B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 33:
77% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219108/A 11/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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