



2017 Joint International EUROSIO Workshop and International Conference on Ultimate Integration on Silicon (ULIS)

April 3-5, 2017 - Athens, Greece

PROGRAM

SUNDAY, APRIL 2, 2017

16⁰⁰ – 19⁰⁰

Registration

**Divani Caravel Hotel,
Vassileos Alexandrou 2,
16121 Athens - Greece**

MONDAY, APRIL 3, 2017

09⁰⁰ – 09³⁰

Welcome

Conference Chairperson

Session 1: Nanoscale FETs

Session Chairs: Androula Nassiopoulou, Francis Balestra

09³⁰ – 10⁰⁰

Transistor architecture and channel materials for nanoscale FET

Dr. Anna Mocuta (Invited)

IMEC, Leuven, Belgium

10⁰⁰ – 10¹⁵

Modeling and Design Considerations for Negative Capacitance Field-Effect Transistors

Michael Hoffmann, Milan Pešić, Stefan Slesazeck, Uwe Schroeder, Thomas Mikolajick

NaMLab gGmbH, Noethnitzer Str. 64, D-01187 Dresden, Germany

10¹⁵ – 10³⁰

On quantum effects and Low Frequency Noise spectroscopy in Si Gate-All-Around Nanowire MOSFETs at cryogenic temperatures

D. Boudier¹, B. Cretu¹, E. Simoen², A. Veloso² and N. Collaert²

¹*Normandie Univ, UNICAEN, ENSICAEN, CNRS, GREYC, 14000 Caen, France,*

²*Imec, Kapeldreef 75, B-3001 Leuven, Belgium*

10³⁰ – 10⁴⁵

First SOI Tunnel FETs with Low-Temperature Process

C. Diaz Llorente¹, C. Le Royer¹, C-M. V. Lu¹, P. Batude¹, C. Fenouillet-Beranger¹, S. Martinie¹, F. Allain¹, S. Cristoloveanu², G. Ghibaudo², and M. Vinet¹

¹*CEA, LETI, MINATEC Campus, 17 rue des Martyrs, 38054 GRENOBLE Cedex 9, France,*

²*IMEP-LAHC, INP-Grenoble, MINATEC campus, 38016 Grenoble, France*

10⁴⁵ – 11⁰⁰

Impact of strain and traps on optimized n- and p-type TFETs

M. Visciarelli, E. Gnani, A. Gnudi, S. Reggiani, G. Baccarani

ARCES and DEI, University of Bologna, Bologna 40136, Italy

11⁰⁰ – 11³⁰

Coffee Break

Session 2: More than Moore devices and applications, Heterogeneous Integration, Other

Session Chairs: Mireille Mouis, Luca Selmi

11³⁰ – 12⁰⁰

Micro and Nano transducers for autonomous sensing applications

Dr. Cosmin Roman (Invited)

12⁰⁰ – 12¹⁵

Out-of-Equilibrium Body Potential Measurements in -MOSFET for Biosensing

Licinius Benea¹, Marylline Bawedin¹, Cécile Delacour², Sorin Cristoloveanu¹, Irina Ionica¹

¹IMEP-LAHC, Minatec, Grenoble INP, Univ. Grenoble Alpes, CNRS, 38016 Grenoble, France,

²Néel Inst., CNRS, 38042 Grenoble, France, France

12¹⁵ – 12³⁰

Electrical Characterization of Percolating Si-Nanonet FET for sensing applications

T. Cazimajou¹, M. Legallais^{1,2}, M.Mouis¹, C. Ternon^{2,3}, B.Salem³, G. Ghibaudo¹

¹Univ Grenoble Alpes, CNRS, Grenoble INP, IMEP-LaHC, F 38000 Grenoble, France,

²Univ Grenoble Alpes, CNRS, Grenoble INP, LMGP, F 38000 Grenoble, France,

³Univ Grenoble Alpes, CNRS, Grenoble INP, LTM, F 38000 Grenoble, France

12³⁰ – 12⁴⁵

Influence of Free Radical Surface Activation on Si/SiC Heterogeneous Integration by Direct Wafer Bonding at Room Temperature

P. Torchia¹, P. Pampili¹, J. O'Connell², J. O'Brien¹, M. White¹, M. Schmidt¹, B. Sheehan¹, F. Waldron¹, J. D. Holmes², S. Monaghan¹, R. Duffy¹, T. Trajkovic³, V. Kilchytska⁴, P. Gammon⁵, K. Cherkaoui¹, P. K. Hurley¹, and F. Gity¹

(1) Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork, Ireland,

(2) Chemistry Department, University College Cork, Cork, Ireland,

(3) Cambridge Microelectronics Limited, Cambridge, United Kingdom,

(4) Université Catholique de Louvain, Louvain-la-Neuve, Belgium,

(5) School of Engineering, University of Warwick, Coventry, CV4 7AL, United Kingdom

12⁴⁵ – 13⁰⁰

Hall-effect Mobility for a Selection of Natural and Synthetic 2D Semiconductor Crystals

Scott Monaghan¹, Farzan Gity¹, Jeffrey R. Lindemuth², Enrico Napolitani³, Ray Duffy¹, Gioele Mirabelli¹, Melissa McCarthy¹, Karim Cherkaoui¹, Ian M. Povey¹, Roger E. Nagle¹ and Paul K. Hurley¹

¹Tyndall National Institute, University College Cork, Lee Maltings, Cork, IRELAND,
²LakeShore Cryotronics, Inc., 575 McCorkle Blvd., Westerville, Ohio 43082-8888, USA.

³Dept. Physics & Astronomy, Uni. of Padova & CNR-IMM MATIS, Via Marzolo 8, I-35131 Padova, ITALY

13⁰⁰ – 14³⁰

Lunch Break

Session 3: Memory devices

Session Chairs: Francisco Gamiz, Marylin Bawedin

14³⁰ – 15⁰⁰

About the intrinsic resistance variability in HfO₂-based RRAM devices

C. Cagli¹, G. Piccolboni¹, D. Garbin¹, A. Grossi^{1,2}, G. Molas¹, E. Vianello¹, C. Zambelli², G. Reimbold¹ (Invited)

¹CEA-LETI, Minatec Campus, Grenoble, France,

²ENDIF, Univ. of Ferrara, Ferrara, Italy

15⁰⁰ – 15¹⁵

ReRAM ON/OFF Resistance Ratio Degradation Due to Line Resistance Combined with Device Variability in 28nm FDSOI technology

H. Aziza, P. Canet, J. Postel-Pellerin, M. Moreau, J.-M. Portal, M. Bocquet

Aix Marseille Univ., CNRS, IM2NP UMR 7334, 60 rue F. Joliot-Curie, 13453 Marseille Cedex 13, France

15¹⁵ – 15³⁰

Static Noise Margin Analysis of 8T TFET SRAM Cells Using a 2D Compact Model Adapted to Measurement Data of Fabricated TFET Devices

F. Horst^{1,2}, M. Graef^{1,2}, F. Hosenfeld^{1,2}, A. Farokhnejad^{1,2}, G. V. Luong³, Q. T. Zhao³, B. Iñíguez², A. Kloes¹

¹NanoP, TH Mittelhessen University of Applied Sciences, Giessen, Germany,

²DEEEA, Universitat Rovira i Virgili, Tarragona, Spain, 3PGI 9-IT and JARA-FIT, Forschungszentrum Jülich, Germany

15³⁰ – 15⁴⁵

Design and Implementation Methodology of Energy-Efficient Standard Cell Memory with Optimized Body-Bias Separation in Silicon-on-Thin-BOX

Yusuke YOSHIDA and Kimiyoshi USAMI

Shibaura Institute of Technology, 3-7-5 Toyosu, Koto-ku, Tokyo, Japan

15⁴⁵ – 16⁰⁰

Indium-Oxide Nanoparticles for Ox-RRAM in CMOS back-end-off-line

¹Edgar A. A. León Pérez, ¹Oumaïma Abouzaid, ¹Khaled Ayadi, ¹Nicolas Baboux, ¹Liviu Militaru, ¹Abdelkader Souifi, ²Jérémy Moeyaert, ²Thierry Baron

¹ Institute of Nanotechnologies of Lyon UMR CNRS 5270, INSA de Lyon, 69621 Villeurbanne Cedex, France,

² Laboratoire des Technologies de la Microélectronique, Centre National de la Recherche Scientifique, Grenoble, France

16³⁰ – 18³⁰

Poster Session

20⁰⁰ –

Reception

TUESDAY, APRIL 4, 2017

Session 4: Memory devices

Session Chairs: Carlo Cagli, Benjamin Iñíguez

09⁰⁰ – 09³⁰

The mystery of the Z²-FET 1T-DRAM memory
Prof. Maryline Bawedin (Invited)

IMEP - INP Grenoble MINATEC

09³⁰ – 09⁴⁵

Feasibility Demonstration of New e-NVM Cells Suitable for Integration at 28nm

S. Kalem¹ and R. Roelofs²

¹BILGEM Informatics and Information Security Research Center, TUBITAK, Gebze, Kocaeli, Turkey, ²ASM, Kapeldreef 75, Leuven 3001

09⁴⁵ – 10⁰⁰

Impact of carrier lifetime on Z²-FET operation

Mukta Singh Parihar¹, Kyung Hwa Lee¹, Maryline Bawedin¹, Joris Lacord², Sébastien Martinie², Jean-Charles Barbé², Yuan Taur³ and Sorin Cristoloveanu¹

¹Univ. Grenoble Alpes, IMEP-LAHC, Grenoble INP Minatec, CNRS, F-38000 Grenoble, France,

²CEA-LETI, Minatec Campus, 38054 Grenoble, France, ³Univ. of California, San Diego, USA

Session 5: Nanoscale devices

Session Chairs: Sorin Cristoloveanu, Qing-Tai Zhao

10⁰⁰ – 10¹⁵

Low temperature performance of proton irradiated strained SOI FinFET

L.F.V. Caparroz¹, C. C. M. Bordallo^{1,2}, J. A. Martino¹, E. Simoen², C. Claeys^{2,3} and P. G. D. Agopian^{1,4}

¹LSI/PSI/USP, University of Sao Paulo, Brazil,

²Imec, Leuven, Belgium,

³E.E. Dept., KU Leuven, Belgium,

⁴São Paulo State University (UNESP), Campus of São João da Boa Vista, Brazil

10¹⁵ – 10³⁰

The MSET Transistor as IC Building-Block

Assaf Peled, Ofer Amrani and Yossi Rosenwaks

t School of Electrical-Engineering, Tel-Aviv University, Tel-Aviv, Israel

10³⁰ – 10⁴⁵

A virtual SOI diode with electrostatic doping

Kyung Hwa Lee, Maryline Bawedin, Hyungjin Park, Mukta Singh Parihar and Sorin Cristoloveanu

Univ. Grenoble Alpes, IMEP-LAHC, Grenoble INP Minatec, CNRS, F-38000 Grenoble, France

10⁴⁵ – 11⁰⁰

MOSFETs in the VeSTIC process -fabrication and characterization

Daniel Tomaszewski, Krzysztof Domański, Grzegorz Głuszko, Andrzej Sierakowski, Dariusz Szmigiel

11⁰⁰ – 11³⁰

Coffee Break

Session 6: Nanoscale FETs

Session Chairs: Mikael Ostling, Cor Claeys

11³⁰ – 11⁴⁵

Silicon tunnel FET with average subthreshold slope of 55mV/dec at low drain currents

K. Narimani, S. Glass, T. Rieger, P. Bernardy, S. Mantl, Q.T.Zhao

Peter-Grünberg-Institute (PGI9-IT) ,JARA-Fundamentals for Future Technology, Forschungszentrum Jülich, 52428 Jülich, Germany

11⁴⁵ – 12⁰⁰

Performance and Transport Analysis of Vertically Stacked p-FET SOI Nanowires

B. C. Paz^a, M. Cassé^b, S. Barraud^b, G. Reimbold^b, M. Vinet^b, O. Faynot^b and M. A. Pavanello^a

^a Centro Universitário FEI, Av. Humberto de A. C. Branco, 3972, 09850-901 – São Bernardo do Campo – Brazil,

^b CEA-LETI Minatec, 17 Rue des Martyrs, 38054 – Grenoble – France

12⁰⁰ – 12¹⁵

Improved Analog Performance of SOI Nanowire nMOSFETs Self-Cascode through Back-Biasing

R. Assalti^a, M. Cassé^b, S. Barraud^b, G. Reimbold^b, M. Vinet^b, O. Faynot^b and M. de Souza^a

^a Department of Electrical Engineering, Centro Universitário FEI, São Bernardo do Campo, Brazil,

^b Département des Composants Silicium – SCME/LCTE, CEA-LETI Minatec, Grenoble, France

12¹⁵ – 12³⁰

Dependence of MOSFETs threshold voltage variability on channel dimensions

C. Couso¹, J. Diaz-Fortuny¹, J. Martin-Martinez¹, M. Porti¹, R. Rodriguez¹, M. Nafria¹, F.V. Fernandez², E. Roca², R. Castro-Lopez², E. Barajas³, D. Mateo³, X. Aragones³

¹Electronic Engineering Department (REDEC) group. Universidad Autónoma de Barcelona (UAB), Barcelona 08193, (Spain),

² Instituto de Microelectrónica de Sevilla, IMSE-CNM, CSIC and Universidad de Sevilla, (Spain),

³Dept. Enginyeria Electrònica, Universitat Politècnica de Catalunya (UPC), Edifici C4, 08034, Barcelona (Spain)

Session 7: Simulations / characterization

Session Chairs: Gérard Ghibaudo, Cosmin Roman

12³⁰ – 12⁴⁵

Mechanical simulations of BOX creep for strained FDSOI

R. Berthelon^{1,2,3}, F. Andrieu¹, B. Mathieu¹, D. Dutartre², C. Le Royer¹, M. Vinet¹, A. Claverie³

¹ CEA-LETI, Minatec campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France,

² STMicroelectronics, 850 rue Monnet, B.P. 16, F-38926 Crolles, France,

³ CEMES-CNRS, 29 rue Jeanne Marvig 31055 Toulouse Cedex 4

12⁴⁵ – 13⁰⁰

Impact of cryogenic temperature operation on static and low frequency noise behaviours of FD UTBOX nMOSFETs

B. Nafaa^{1,2}, B. Cretu¹, N. Ismail², O. Touayar², E. Simoen^{3,4}

¹Normandie University, UNICAEN, ENSICAEN, CNRS, GREYC, Caen, France,

² Carthage University, INSAT, MMA, Tunis, Tunisia,

³Imec, Kapeldreef 75, Leuven, Belgium,

⁴Solid-State Physics Department, Ghent University, Krijgslaan 281 S1, Gent, Belgium

13⁰⁰ – 14³⁰

Lunch Break

Session 8: Non-Si semiconductor materials and devices

Session Chairs: Max Lemme, Pierpaolo Palestri

14³⁰ – 15⁰⁰

Properties of III-V nanowires

Prof. Lars-Erik Wernersson (Invited)

Lund University, Sweden

15⁰⁰ – 15¹⁵

Vertically Stacked Lateral Si₈₀Ge₂₀ Nanowires Transistors for 5 nm CMOS Applications

T. Al-Ameri, A. Asenov

School of Engineering, University of Glasgow, Glasgow, G12 8LT, UK

15¹⁵ – 15³⁰

Static and LF noise characterization of ultra-thin body InAs MOSFETs

T.A. Karatsori^{1,3}, M. Pastorek², C.G Theodorou¹, A. Fadjie², N. Wichmann², L. Desplanque², X. Wallart², S. Bollaert², C.A. Dimitriadis³, G. Ghibaudo¹

¹IMEP-LAHC, Minatec, BP257, 38016 Grenoble, France,

² IEMN, University of Science and Technology, Lille, France,

³ Department of Physics, Aristotle University of Thessaloniki, Greece

15³⁰ – 15⁴⁵

Analysis of the transistor efficiency of Gas Phase Zn Diffusion In_{0.53}Ga_{0.47}As nTFETs at different temperatures

C. C. M. Bordallo^{1,2}, J. A. Martino¹, P. G. D. Agopian^{1,3}, A. Alian², Y. Mols², R. Rooyackers², A. Vandooren², A. Verhulst², E. Simoen², C. Claeys^{2,4}, N. Collaert²

¹LSI/PSI/USP, University of Sao Paulo, Brazil,

²Imec, Leuven, Belgium,

³São Paulo State University (UNESP), Campus of São João da Boa Vista, Brazil,

⁴E.E. Dept., KU Leuven, Belgium

15⁴⁵ – 16³⁰

Coffee Break

16³⁰ – 17⁰⁰

European Nanoelectronics Research

Dr Panagiotis Tsarchopoulos, EU Officer

CONFERENCE DINNER

WEDNESDAY, APRIL 5, 2017

Session 9: Novel materials and technologies

Session Chairs: Lars-Erik Wernersson, Viktor Sverdlov

09³⁰ – 10⁰⁰

The Prospects of 2D Materials for Ultimately-Scaled CMOS **Dr. Frank Schwierz (*Invited*)**

University of Ilmenau

10⁰⁰ – 10¹⁵

Charge Transport, Interface and Border Traps in Al₂O₃/InGaAs structures

Y.Y. Gomeniuk¹, Y.V. Gomeniuk¹, A.N. Nazarov¹, S. Monaghan², K. Cherkaoui², and P.K. Hurley²

¹*V. Lashkaryov Institute of Semiconductor Physics NAS of Ukraine, ISP NASU, Kyiv, Ukraine,*

²*Tyndall National Institute, University College Cork, Cork, Ireland*

10¹⁵ – 10³⁰

Evaluation of ONO compatibility with high-k metal gate stacks for future embedded flash products

Adam Dobri^{1,2,3}, Dann Morillon¹, Simon Jeannot¹, Fausto Piazza¹, Carine Jahan², Alain Toffoli², Luca Perniola², Francis Balestra³

¹ *STMicroelectronics, France*,

² *CEA-LETI, Grenoble, France*, ³ *IMEP-LAHC, Université Grenoble Alpes, Grenoble, France*

10³⁰ – 10⁴⁵

Hydrogen Silsesquioxane Tri-Dimensional Advanced Patterning Concepts for High Density of Integration in sub-7 nm Nodes

L. Gaben^{1,2,3}, S. Barraud², V. Balan², C. Euvrard², S. Pauliac², J.-A. Dallery^{2,4}, J. Bustos^{1,2}, R. Dechanoz², B. Hemard^{1,2}, L. Koscianski², X. Bossy^{1,2}, C. Arvet^{1,2}, C. Vizioz², S. Barnola², C. Perrot^{1,2}, J. Sturm², Y. Exbrayat², N. Daventure², V. Loup², P. Besson², B. Perrin², B. Previtali², M.-P. Samson^{1,2}, S. Monfray¹, F. Boeuf¹, T. Skotnicki¹, F. Balestra³, M. Vinet²

¹ *STMicroelectronics, 850 rue J. Monnet, 38920 Crolles, France,*

² *CEA-LETI, Minatec campus, 17 rue des Martyrs, 38054 Grenoble Cedex 9, France,*

³ *IMEP-LAHC, Université Grenoble Alpes, BP257, 38016 Grenoble Cedex 1, France,*

⁴ *Vistec Electron Beam GmbH, IlmestraBe 4. 07743 Jena, Germany*

10⁴⁵ – 11⁰⁰

Model 3D MOS capacitor system using regular arrays of vertical Si nanowires

E. Hourdakakis¹, A. Casanova², G. Larrieu², A.G. Nassiopoulou¹

¹ *NCSR Demokritos, INN, Patriarchou Grigoriou and Neapoleos, Aghia Paraskevi, 153 10 Athens, Greece,*

² *LAAS-CNRS, Université de Toulouse, CNRS, Toulouse, France*

11⁰⁰ – 11³⁰

Coffee Break

Session 10: Nanoscale MOSFETs

Session Chairs: Stephane Monfray, Jan Hoentschel

- 11³⁰ – 11⁴⁵** **Comparative study of non-linearities in 28 nm node FDSOI and Bulk MOSFETs**
V. Kilchytska¹, B. Kazemi Esfeh¹, C. Gimeno¹, B. Parvais², N. Planes³, M. Haond³, J.-P. Raskin¹, D. Flandre¹
¹ CTEAM, Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium,
² IMEC, Kapeldreef 75, 3001 Leuven, Belgium,
³ ST-Microelectronics, 850 rue J. Monnet, 38926 Crolles, France
- 11⁴⁵ – 12⁰⁰** **Sensitivity Analysis of C-V Global Variability for 28 nm FD-SOI**
Krishna Pradeep^{1,3}, Thierry Poiroux², Patrick Scheer¹, Gilles Gouget¹, André Juge¹ and Gérard Ghibaudo³
¹ STMicroelectronics, Crolles Site, 850 rue Jean Monnet, 38926 Crolles, France,
² CEA-LETI, MINATEC Campus, 38054 Grenoble Cedex 9, France,
³ IMEP-LAHC, MINATEC Campus, 3 Parvis Louis Néel, 38016 Grenoble, Cedex 1, France
- 12⁰⁰ – 12¹⁵** **Mass data analysis of Random Telegraph Noise in 22nm FDSOI back biased transistors**
Michael Otto, Maximilian Juettner, Jan Hoentschel
GLOBALFOUNDRIES Fab1 LLC & Co. KG, Dresden, Germany
- 12¹⁵ – 12³⁰** **Strain-induced increase of electron mobility in ultra-thin InGaAs-OI MOS transistors**
Sabina Krivec, Mirko Poljak and Tomislav Suligoj
Department of Electronics, Microelectronics, Computer and Intelligent Systems, Faculty of Electrical Engineering and Computing, University of Zagreb, HR-10000 Zagreb, Croatia

Session 11: Modelling and Characterization

Session Chairs: Enrico Sangiorgi, Asen Asenov

- 12³⁰ – 12⁴⁵** **Compact Modeling of Intrinsic Capacitances in Double-Gate Tunnel-FETs**
A. Farokhnejad^{1,2}, F. Horst^{1,2}, M. Graef^{1,2}, C. Liu³, Q.T. Zhao³, B. Iñiguez², F. Lime², A. Kloes¹
¹ NanoP, TH Mittelhessen University of Applied Sciences, Giessen, Germany,
² DEEEA, University Rovira i Virgili, Tarragona, Spain,
³ PGI 9-IT and JARA-FIT, Forschungszentrum Jülich, Germany
- 12⁴⁵ – 13⁰⁰** **Assessment of Gate Leakage Mechanism utilizing Multi-Subband Ensemble Monte Carlo**
C. Medina-Bailon¹, T. Sadi², C. Sampedro¹, A. Godoy¹, L. Donetti¹, V. Georgiev², F. Gamiz¹ and A. Asenov²
¹ Nanoelectronics Research Group - CITIC-UGR, Universidad de Granada, 18071 Granada, Spain,
² School of Engineering, University of Glasgow, Glasgow G12 8LT, Scotland, UK
- 13⁰⁰ – 13¹⁵** **De-embedding techniques for nanoscale characterization of semiconductor devices by scanning microwave microscopy**

Loukas Michalas¹, Enrico Brinciotti², Andrea Lucibello¹, Christopher Hardly Joseph¹, Ferry Kienberger², Emanuela Proietti¹ & Romolo Marcelli¹

¹National Research Council, Institute for Microelectronics and Microsystems (CNR-IMM), Rome, Italy

²Keysight Technologies Austria GmbH, Linz, Austria

13¹⁵ – 14³⁰

Lunch Break

Session 12: Non-Si semiconductor materials and devices

Session Chairs: Anda Mocuta, Siegfried Mantl

14³⁰ – 14⁴⁵

Investigation of InAs/GaSb tunnel diodes on SOI

¹C. Convertino, ¹D. Cutaia, ¹H. Schmid, ^{1,2}N. Bologna, ³P. Paletti, ⁴A.M. Ionescu, ¹H. Riel and ¹K. E. Moselund

¹IBM Research – Zurich, 8803 Rüschlikon, Switzerland,

²EMPA, Electron Microscopy Center, 8600 Dübendorf, Switzerland,

³University of Notre Dame, Department of Electrical Engineering IN 46556-5637, USA,

⁴Ecole Polytechnique Federal de Lausanne, EPFL, NanoLab, 1015 Lausanne, Switzerland

14⁴⁵ – 15⁰⁰

On the electron velocity-field relation in ultra-thin films of III-V compound semiconductors for advanced CMOS technology nodes

E. Caruso, A. Pin, P. Palestri, L. Selmi

DPIA, University of Udine, Via delle Scienze 206, 33100, Udine, Italy

15⁰⁰ – 15¹⁵

GaN-On-Insulator: From QDs to a new substrate

P. Dimitrakis¹, P. Normand¹, V. Ioannou-Sougleridis¹, C. Bonafos² and E. Iliopoulos^{3,4}

¹Institute of Nanoscience and Nanotechnology, National Centre for Scientific Research “Demokritos”, P.O. Box 60228, Aghia Paraskevi, 15310 Athens, Greece,

²CEMES-CNRS et Université de Toulouse, BP 94347, 31055 Toulouse, France,

³Physics Department, University of Crete, P.O. Box 2208, 71003 Heraklion, Greece,

⁴IESL-FORTH, P.O. Box 1527, 71110 Heraklion, Greece

15¹⁵ – 15³⁰

Modeling the Impact of 2D Hole Gas in a GaN/AlGaIn/GaN Heterostructure

J. Ghosh, S. Ganguly, D. Saha, and A. Laha

Department of Electrical Engineering, Indian Institute of Technology, Mumbai, India

15³⁰ : **CLOSING CEREMONY**



POSTER PROGRAM

Poster Session, Monday 3/04/2017, 16³⁰ – 18³⁰

- P1 S-shaped Gate-All-Around MOSFETs for High Density Design**
Ya-Chi Huang¹, Meng-Hsueh Chiang², and Shui-Jinn Wang¹
¹Institute of Microelectronics, National Cheng Kung University, Tainan 701, Taiwan,
²Department of Electrical Engineering, National Cheng Kung University, Tainan 701, Taiwan
- P2 C-shape silicon window nano MOSFET for reducing the short channel effects**
Mahsa Mehrad and Elmira Safarpour Ghadi
School of Engineering, Damghan University, Damghan, Iran
- P3 Improving on-state breakdown voltage and double hump substrate current of HV NMOS**
^{A, B}Dongil Park, ^ASungmin Kang, ^AYoungmok Kim, ^BYonghan Roh and ^AOhkyum Kwon
^ALSI TD Team, System LSI division, Samsung Electronics, 1, Samsung-ro, Giheung-gu, Yongin-si, Gyeonggi-do, 17113, Republic of Korea,
^BCollege of Information and Communication Engineering, Sungkyunkwan University, 2066, Seobu-ro, Jangan-gu, Suwon-City, Gyeonggi-do, 18448, Republic of Korea
- P4 Effects of Thermal Generation on Reliability of Z²-FET Device**
¹Sehyun Kwon, ¹Jinho Ahn, ²Francisco Gamiz, ³Sorin Cristoloveanu, ⁴Chunkeun Kim, ⁴Seong Il Kim, and ⁴Yong Tae Kim
¹Division of Materials Science and Engineering, Hanyang University, Seoul 04763, Korea ,
²Nanoelectronics Research Group, University of Granada, 18071 Granada, Spain,
³IMEP-LAHC, Grenoble INP MINATEC, 38016 Grenoble, France,
⁴Semiconductor Materials and Device Lab, Korea Institute of Science and Technology, Seoul 02792, Korea
- P5 Effects of non-stoichiometry of silicon oxide layers in double barrier structure on high temperature annealing of ultrathin silicon layer**
Romuald B. Beck^{1,2}, Paweł Korb¹
¹Institute of Microelectronics and Optoelectronics, Warsaw University of Technology, Warsaw, Poland,
²CEZAMAT PW, Warsaw, Poland

- P6 Experiments and simulation of multilevel resistive switching in forming free Ti/TiO_{2-x} RRAM devices**
P. Bousoulas, I. Giannopoulos, P. Asenov, I. Karageorgiou, and D. Tsoukalas
Department of Physics, School of Applied Sciences, National Technical University of Athens, Athens 15773, Greece
- P7 Z²-FinFET: 1T-DRAM operation**
Seong-II Kim^{1,3}, Yong Tae Kim¹, Do Hong Kim², F. Gamiz³, C. Navarro³, and S.Cristoloveanu⁴
¹*Nanophotonics Center, Korea Institute of Science and Technology, Seoul 136-791, South Korea,*
²*Department of Materials Science and Engineering, Korea University, Seoul 136-701, South Korea,*
³*Dept. de Electronica, University of Granada, 18071, Granada, Spain,*
⁴*Univ. Grenoble Alpes, IMEP-LAHC, Grenoble INP MINATEC, CNRS, F-38000 Grenoble, France*
- P8 Analog and RF analysis of gate all around silicon nanowire MOSFETs**
Qinghua Han¹, Linjie Liu¹, Sergej Makovejev², Stefan Trelenkamp¹, Jean-Pierre Raskin², Siegfried Mantl¹, Qing-Tai Zhao¹
¹*Peter Grünberg Institut (PGI-9), JARA-FIT, Forschungszentrum Jülich, 52428 Jülich, Germany.*
²*Institute of Information and Communication Technologies, Electronics and Applied Mathematics (ICTEAM), Université catholique de Louvain (UCL), B-1348 Louvain-la-Neuve, Belgium*
- P9 Experimental comparison between relaxed and strained Ge pFinFETs**
A.V. Oliveira¹, P. G. D. Agopian^{1,2}, J. A. Martino¹, E. Simoen^{3,4}, J. Mitard³, L. Witters³, N. Collaert³, and C. Claeys⁵
¹*LSI/PSI/EPUSP, University of Sao Paulo, Sao Paulo, Brazil;*
²*Sao Paulo State University (UNESP), Sao Joao da Boa Vista, Brazil;*
³*Imec, Leuven, Belgium;*
⁴*Dept. of Solid State Sciences, Ghent University, Ghent, Belgium;*
⁵*E. E. Dept., ESAT, KU Leuven, Belgium*
- P10 Layer Thickness Impact on Second Harmonic Generation Characterization of SOI Wafers**
D. Damianos,^a I. Ionica,^a J. Changala,^b M. Lei,^b A. Kaminski,^a D.B Pelissier,^c S. Cristoloveanu,^a G. Vitrant^a
^a*IMEP-LAHC, Minatec, Grenoble-INP, Univ. de Grenoble Alpes, 3 Parvis Louis Néel – CS 50257, F-38016 Grenoble, France,*
^b*FemtoMetrix, 1850 East Saint Andrew Place, Santa Ana, CA 92705, USA,*
^c*INL – UMR 5270, INSA de Lyon, 7 Avenue Jean Capelle, 69621 Villeurbanne, France*
- P11 FLEXIBLE PIEZOELECTRIC TRANSDUCERS BASED ON A PMMA/ZNO NANOWIRE COMPOSITE**
R. Tao, G. Ardila, M. Parmar and M. Mouis
Univ. Grenoble Alpes, CNRS, IMEP-LaHC, F-38000 Grenoble, France
- P12 Analog parameters on pMOS SOI Ω -gate nanowire down to 10 nm width for different back gate bias**
V. T. Itocazu¹, V. Sonnenberg^{1,2}, J. A. Martino¹, S. Barraud³, M. Vinet³ and O. Faynot³
¹*LSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil,*
²*FATEC/SP and FATEC/OSASCO / CEETEPS, Sao Paulo, Brazil,*
³*CEA, LETI, Minatec Campus and University Grenoble Alpes, 38054 Grenoble, France*
- P13 Quantum Confined Model for a Novel Tri-Material Gate Stack Engineered Double Gate MOSFET**
Dhriti Duggal¹, Rajnish Sharma², and Bhanu Kapoor³

¹ Department of ECE, Chitkara University, India/ Student Member, IEEE,

² Department of ECE, Chitkara University, India/ Senior Member, IEEE,

³ Mimasic, Richardson, TX, USA

- P14 Characterization of semiconductor structures using scanning microwave microscopy technique**
B. Abadlia Bagdad, F. Gamiz
Nanoelectronics Research Group - CITIC-UGR, Universidad de Granada, 18071 Granada, Spain
- P15 Back Enhanced (BE) SOI MOSFET under non-conventional bias conditions**
L.S.Yoyo, R.C. Rangel, K.R.A. Sasaki, J.A. Martino
LSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil
- P16 Improved Electrical Characteristics of Gate-Last FD-SOI TFETs with All ALD High-k/Metal Gate Stack Using D₂ Passivation**
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Division of Materials Science and Engineering, Hanyang University, Seoul 04763, Korea
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Meysam Zareiee, Milad Abtin
School of Engineering, Damghan University, Damghan, Iran
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H. J. Park^a, M. Bawedin^a, K. Sasaki^b, J-A. Martino^b, and S. Cristoloveanu^a
^aIMEP-LaHC, Minatec, Grenoble INP, University Grenoble Alpes, CNRS, Grenoble, France,
^bLSI/PSI/USP, University of Sao Paulo, Sao Paulo, Brazil
- P19 Nanoscale electrical characterization of a varistor-like device fabricated with oxydized CVD graphene**
S.Claramunt¹, B. Sempere², Q. Wu¹, A. Ruiz¹, M. Porti¹, C. Colominas², M. Nafria¹, X. Aymerich¹
¹Electronic Engineering Department, Universitat Autònoma de Barcelona, Cerdanyola del Vallès, Spain,
²Chemical Engineering and Materials Science Department, Institut Químic de Sarrià, Barcelona, Spain
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L. Donetti, C. Sampedro, F.G. Ruiz, A. Godoy, F. Gamiz
Departamento de Electrónica and CITIC, Universidad de Granada, Granada, Spain
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Daniel Tomaszewski^a, Grzegorz Głuszko^a, Lidia Łukasiak^b, Krzysztof Kucharski^a, Jolanta Malesińska^a
^a Division of Silicon Microsystem and Nanostructure Technology, Instytut Technologii Elektronowej (ITE), Al. Lotników 32/46, 02-668 Warsaw, Poland, ^b Institute of Microelectronics and Optoelectronics, Warsaw University of Technology (WUT), ul. Koszykowa 75, 00-662 Warsaw, Poland
- P22 Back-gate bias effect on FDSOI MOSFET RF Figures of Merits and Parasitic Elements**
B. Kazemi Esfeh¹, V. Kilchytska¹, B. Parvais², N. Planes³, M. Haond³, D. Flandre¹ and J.-P. Raskin¹
¹ICTEAM, Université catholique de Louvain, 1348 Louvain-la-Neuve, Belgium,
²Imec, IMEC, Kapeldreef 75, 3001 Leuven, Belgium,

³ST, ST-Microelectronics, 850 rue J. Monnet, 38926 Crolles, France

- P23** **Al₂O₃ coating of nanoparticle networks via ALD: effect on strain-sensing performance**
Evangelos Skotadis^a, Niovi Gialama^a, Lampros Patsiouras^a, S. Kennou^b, Dimitris Tsoukalas^a
^a Department of Applied Physics, National Technical University of Athens, Athens, Greece.,
^b Department of Chemical Engineering, University of Patras, Patras, Greece
- P24** **Toward the integration of Si nanonets into FETs**
M. Legallais^{1,2}, T. Nguyen^{1,3}, M. Mouis², B. Salem³, C. TERNON^{1,3}
¹Univ. Grenoble Alpes, CNRS, Grenoble INP*, LMGP, F-38000 Grenoble, France,
²Univ Grenoble Alpes, CNRS, Grenoble INP*, IMEP-LaHC, F-38000 Grenoble, France,
³Univ Grenoble Alpes, CNRS, LTM, F-38000 Grenoble, France,
*Institute of Engineering Univ. Grenoble Alpes
- P25** **Si measurements: SiO_x on Si**
S. Kalem, SB Tekin, ZE Kaya
BILGEM Informatics and Information Security Research Center, TDBY, TUBITAK, Gebze, Kocaeli, Turkey
- P26** **Design and fabrication of a novel power Si/SiC LDMOSFET for high temperature applications**
P.M. Gammon¹, F. Li¹, C.W. Chan¹, F. Gity², T. Trajkovic³, V. Kilchytska⁴, V. Pathirana³, N. Udugampola³, K. Ben Ali⁴, D. Flandre⁴, J.W. Gardner¹ and P.A. Mawby¹
¹ School of Engineering, University of Warwick, Coventry, CV4 7AL, UK,
² Tyndall National Institute, University College Cork, Lee Maltings, Dyke Parade, Cork, Ireland,
³ Cambridge Microelectronics Limited, Cambridge, United Kingdom,
⁴ Université catholique de Louvain, Louvain-la-Neuve, Belgium
- P27** **Gate capacitance performance of p-type InSb and GaSb nanowires**
C. Martínez-Blanco¹, F. G. Ruiz¹, L. Donetti¹, A. Toral¹, J. M. González-Medina¹, E. G. Marín², A. Godoy¹, and F. Gámiz¹
¹Departamento de Electrónica y Tec. Computadores, Universidad de Granada, Fac. Ciencias, Av. Fuentenueva S/N, 18071, Granada, Spain, ² Dipartimento di Ingegneria dell'Informazione, Università di Pisa, Via G. Caruso 16, 56122 Pisa, Italy