KGP-RISC Assignment

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Instruction Set Architecture:

Class	Instruction	Usage	Meaning
Arithmetic	Add	add rs,rt	$rs \leftarrow (rs) + (rt)$
	Comp	comp rs,rt	$rs \leftarrow$ 2's Complement (rs)
	Add immediate	addi rs,imm	$rs \leftarrow (rs) + imm$
	Complement Immediate	compi rs,imm	$rs \leftarrow$ 2's Complement (imm)
Logic	AND	and rs,rt	$rs \leftarrow (rs) \wedge (rt)$
	XOR	xor rs,rt	$rs \leftarrow (rs) \oplus (rt)$
Shift	Shift left logical	shll rs, sh	$rs \leftarrow (rs)$ left-shifted by sh
	Shift right logical	shrl rs, sh	$rs \leftarrow (rs)$ right-shifted by sh
	Shift left logical variable	shllv rs, rt	$rs \leftarrow (rs)$ left-shifted by (rt)
	Shift right logical	shrl rs, rt	$rs \leftarrow (rs)$ right-shifted by (rt)
	Shift right arithmetic	shra rs, sh	$rs \leftarrow (rs)$ arithmetic right-shifted by sh
	Shift right arithmetic variable	shrav rs, rt	$rs \leftarrow (rs)$ right-shifted by (rt)
Memory	Load Word	lw rt,imm(rs)	$rt \leftarrow mem[(rs) + imm]$
	Store Word	sw rt,imm,(rs)	$mem[(rs) + imm] \leftarrow (rt)$
Branch	Unconditional branch	b L	goto L
	Branch Register	br rs	goto (rs)
	Branch on less than 0	bltz rs,L	if$(rs) < 0$ then goto L
	Branch on flag zero	bz rs,L	if $(rs) = 0$ then goto L
	Branch on flag not zero	bnz rs,L	if$(rs) \neq 0$ then goto L
	Branch and link	bl L	goto L; 31 $\leftarrow$ (PC)+4
	Branch on Carry	bcy L	goto L if Carry = 1
	Branch on No Carry	bncy L	goto L if Carry = 0
Complex	Diff	diff rs, rt	$rs \leftarrow$ the LSB bit at which rs and rt differ

Instruction format and Encoding

OP Code:

We have used a 6 bit opcode format, with maximum accommodation of 64 classes, out of which in the current ISA, 10 are used.

OPCODE	Class	Functions
000001	Arithmetic	Add, Comp, And, XOR, Diff
000010	Arithmetic immediate	Addi, Compi

000011	Shift	Shift left logical, right logical, right arithmetic
000100	Shift with variable	left logical variable, right logical variable, right arithmetic value
000101	Memory	Load word
000110	Memory	Store Word
001000	Branch	Unconditional branch ,Branch on Carry ,Branch on No Carry
001010	Branch	Branch and link
001001	Branch	Branch Register
001011	Branch	Branch on less than 0,Branch on zero,Branch on not zero

Instruction architecture of all classes:

Function codes are 5 bit numbers and hence each class can accommodate 32 functions at max.

Arithmetic class

Usage: function RS RT Instructions: add, comp, and, xor

Op code	**RS**	**RT**	**Extra**	**Function**
6 bits	5 bits	5 bits	11 bits	5 bits

Instruction	**OP code**	**RS**	**RT**	**Extra**	**Function code**
Add	000001	5 bit	5 bit	11	00001
Comp	000001	5 bit	5 bit	11	00011
And	000001	5 bit	5 bit	11	00010
XOR	000001	5 bit	5 bit	11	00100
Diff	000001	5 bit	5 bit	11	01000

Arithmetic immediate class

Usage: function RS imm
Instructions: addi, compi

Op code	**RS**	**Immediate value**	**Function**
6 bits	5 bits	16 bits	5 bits

Instruction	**OP code**	**RS**	**Immediate value**	**Function code**
Addi	000010	5 bit	16 bit number	00001
Compi	000010	5 bit	16 bit number	00011

Shift arithmetic class

Usage: function RS Shift
Instructions: shll, shrl, shra

Op code	**RS**	**Shift**	**Function**
6 bits	5 bits	16 bits	5 bits

Instruction	**OP code**	**RS**	**Shift**	**Function code**
Shift Left Logical	000011	5 bit	16 bit	00101
Shift Right Logical	000011	5 bit	16 bit	00110
Shift right arithmetic	000011	5 bit	16 bit	00111

Shift arithmetic class

Usage: function RS RT
Instructions: shllv, shrlv, shrav

Op code	**RS**	**RT**	**Extra**	**Function**
6 bits	5 bits	5 bits	11 bits	**5 bits**

Instruction	OP code	RS	RT	Extra	Function code
Shift Left Logical variable	000100	5 bit	5 bit	11 bit	00101
Shift Right Logical variable	000100	5 bit	5 bit	11 bit	00110
Shift right arithmetic variable	000100	5 bit	5 bit	11 bit	00111

Load Word (Memory access)

Usage: function RS offset(RT)
Instructions: lw

Op code	RS	RT	Offset
6 bits	5 bits	5 bits	16 bits

Instruction	OP code	RS	RT	Offset
Load	000101	5 bit (destination)	5 bit (source)	16 bit constant

Store Word (Memory access)

Usage: function RS offset(RT)
Instructions: sw

Op code	RS	RT	Offset
6 bits	5 bits	5 bits	16 bits

Instruction	OP code	RS	RT	Offset
Store	000110	5 bit (destination)	5 bit (source)	16 bit constant

Flag (carry) based/ unconditional branch

Usage: unconditional branch/ branch on basis of carry flag set by ALU

Instructions: b, bcy, bncy

Op code	Extra	Destination address	function
6 bits	5 bits	16 bits	5 bits

Instruction	OP code	Destination address	Function code
Unconditional branch	001000	16 bit address	10001
Branch on carry	001000	16 bit address	10100
Branch on no carry	001000	16 bit address	10101

Branch and link

Usage: function calls

Instructions: bl

Op code	Extra	Destination address	function
6 bits	5 bits	16 bits	5 bits

Instruction	OP code	Destination address	Function code
Branch and link	001010	16 bit address	10001

Branch register

Usage: branch to register value

Instructions: br

Op code	RS	Extra	function
6 bits	5 bits	16 bits	5 bits

Instruction	OP code	RS	Function code
Branch Register	001001	5 bit register number	10001

Relational Branch

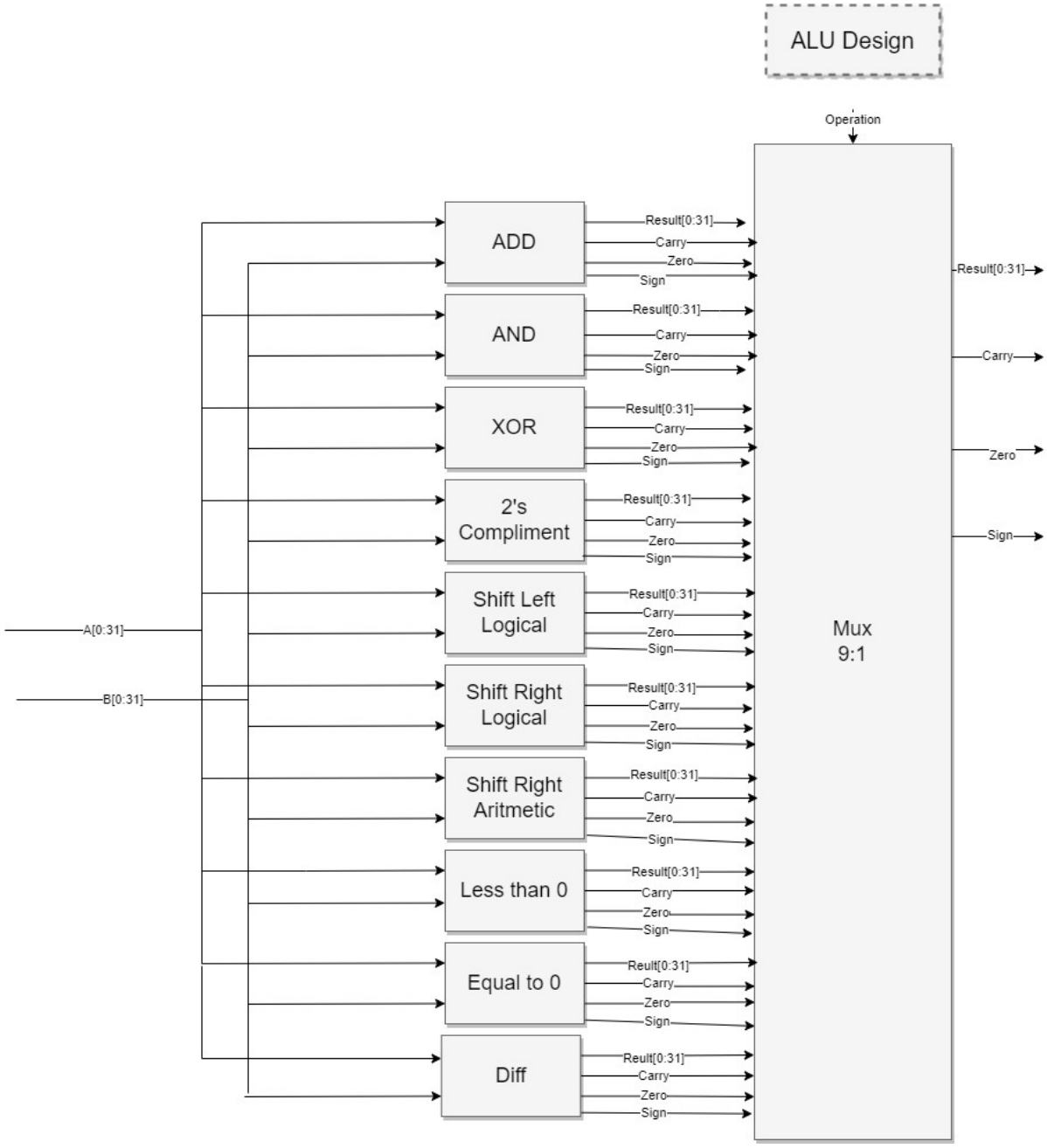
Usage: branch on basis of flags set by ALU (on basis of comparison)

Instructions: bltz, bz, bnz

Op code	**RS**	**Destination Address**	**function**
6 bits	5 bits	11 bits	5 bits

Instruction	**OP code**	**RS**	**Function code**
Branch on less than zero	001011	5 bit register number	11000
Branch on zero	001011	5 bit register number	10010
Branch on not zero	001011	5 bit register number	10011

ALU implementation:



ALU MUX CONTROL:

Instruction	**Operation (4 bit)**
And	0001

And	0010
Comp	0011
Xor	0100
Left logical shift	0101
Right Logical shift	0110
Right Arithmetic shift	0111
Diff	1000

Top level diagram