LEVELIZED LOGIC SIMULATION

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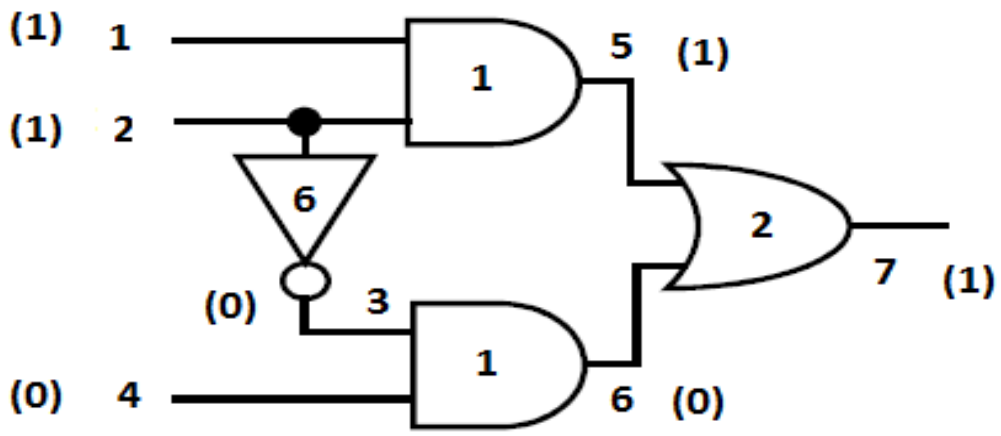
Idea:

In levelized simulation one starts by assigning binary values to the primary inputs, and proceeds by propagating those values through the gates to the primary outputs. A gate is not simulated until all of its input values are available.

The process of determining the correct gate-simulation order is called levelization. Levelization assigns a level number to each net in the circuit.
In the Logic simulator designed Breadth first search algorithm is used for levelization purpose, by considering the output node as the source node. Hence layer 0 will consist of the output node and the highest layer will consist of the primary inputs.

One the levelization is achieved; the simulation can be performed layer wise.

Advantages: Systematic automated simulation and time efficient.



Input format for the given circuit:

7 nodes
3 inputs
1 output

INPUT(1,1)
INPUT(2,1)
INPUT(4,0)

OUTPUT(7)

5 = AND(1,2)
6 = AND(3,4)
7 = OR(5,6)
3 = NOT(2)

NOTE: The format is case sensitive and hence should be followed strictly.

Gates Allowed:
AND, OR, NAND, NOR, NOT, XOR (Program can be extended to include other gates too)

OUTPUT:

The simulator gives as output the value of the node in interest and values of the subsequent nodes used in its evaluation.

For verification purpose the contents of the objects read from text document and layers as computed by Breadth first search algorithm are also presented.