Altera Complete Design Suite Version 13.1 Update Release Notes

This document provides information about the Altera® Complete Design Suite version 13.1 update 2.

You must either have previously installed the Quartus II software version 13.1 or must install the Quartus II software version 13.1 before installing this update. Otherwise, the update will not be installed correctly and the Quartus II software will not run properly.

For information about the Quartus II software version 13.1, refer to the *Quartus II Software and Device Support Release Notes Version 13.1*.

Altera Complete Design Suite updates are cumulative; update 2 includes update 1.

Issues Addressed in Update 2

The Altera Complete Design Suite version 13.1 update 2 addresses the following software issues:

Device Support

- Provides full compilation and programming support for the following Cyclone® V device: 5CGXFC5C6F23A7.
- Adds Serial Flash Loader support for the following Cyclone V devices: 5CSEA2, 5CSXC2, 5CSEA4, and 5CSXC4.
- Adds Hard Processor System (HPS) Loaner I/O timing support for Arria V SoCs and Cyclone V SoCs.

Qsys

- Fixes an issue that could cause incorrect information to be displayed in the Qsys Connections tab.
- For designs that target Arria V or Cyclone V SoCs, fixes an error that could prevent generation of Hard Processor System (HPS) Initial Software (**.isw**) files if a Quartus II IP file (**.qip**) assignment is in full path format. The error was:
  `Error (210006): Can't save or open file <filepath>/<filename>`

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Quartus II Compilation Flows

- Fixes an issue that could cause incorrect logic implementation in DSP blocks if you select the input cascade feature for signals using DATAA_X, DATAA_Z, DATAB_X, or DATAB_Z.
- For designs that target Cyclone IV E, Cyclone IV GX, and Cyclone V devices, the Quartus II software now honors Pad-to-Core delay chain **.qsf** settings in the Strict Preservation flow.
- For designs that target Arria V devices, this update adds an optional **quartus.ini** setting to improve Arria V hold timing closure performance. To use this setting, add `tis_increase_fitter_hold_pessimism=ON` to your **quartus.ini** file, put the **quartus.ini** into your project directory, and then restart the Quartus II software.
- For designs that target a Stratix® V device, modifies a default setting on the Stratix V CDR/CMU PLL block, providing additional margin for when the device operates in cold temperatures.
- Eliminates an error that could occur during compilation of a design that targets and Arria V SoC or Cyclone V SoC, if the design uses both the hard processor system (HPS) and LVDS.
- Eliminates an internal error that could occur during compilation when a LAB is configured such that an SLOAD signal is placed on an input port designated for a different signal type.
- Eliminates an internal error that could occur in the Assembler when an I/O pin with `ENABLE_STRICT_PRESERVATION` is not connected to logic with compatible preservation settings. Instead of an internal error, this condition now results in a regular error message during compilation.

Simulation

- For designs that target an Arria V, Cyclone V, or Stratix V device, fixes a Synopsis® VCS® compilation error that could occur when simulating a Hard IP (HIP) for PCIe Root Port (RP) device under test (DUT) configured with the Avalon Memory-Mapped interface.

Chip Planner

- Eliminates an internal error that could occur when you open the Chip Planner or Change Manager window.

Netlist Viewers

- Eliminates an internal error that could occur in Netlist Viewers when you view a SystemVerilog design that includes a bidirectional pin.
- Fixes a problem in the Netlist Viewer that might cause the constant value of a bus signal in reverse order

PowerPlay Power Analyzer

- Fixes an internal error that might occur during power analysis of a design that targets an Cyclone V device, includes a transceiver and the transceiver uses an fPLL as a transmitter PLL.

System Console

- Fixes an error that prevented the System Console GUI from opening if the file MSVCR71.dll is not present on your computer. The error message displayed was:

```
system-console.exe - System Error
The program can't start because MSVCR71.dll is missing from your
computer. Try reinstalling the program to fix this problem.
```

Transceiver Toolkit

- Fixes a problem in the Transceiver Toolkit that caused DFE adaptation values in the combined Autosweep + EyeQ mode to be nonoptimal.
- Fixes a fatal error in the Transceiver Toolkit that might occur when you open a custom link between two boards.

DSP Builder

- Fixes a problem with the DSP Builder Standard IO&Bus::AltBus block. In previous versions of DSP Builder, the block was producing functionally incorrect HDL for signed-to-unsigned conversions when saturation was enabled.
- Fixes a problem introduced in DSP Buider Advanced version 13.1 that affected designs that us the BusStimulusFileReader block in a subsystem that is not an ancestor to the DUT synthesized subsystem. The fix ensures that blocks that are enclosed in multiply nested subsystems are found and the appropriate test bench code is generated.
- Fixes a problem that prevented MathWorks MATLAB R2013b from simulating a design that uses the NCO ModelIP block.

IP

- IP cores released with the Altera Complete Design Suite version 13.1 update 2 have a version of

EMIF IP Cores

- Allows you to mask groups and ranks from calibration in UniPHY IP in the External Memory Interface (EMIF) Debug Toolkit. To use this feature, you need to regenerate the UniPHY IP after installing update 2.
- Corrects the initialization sequence for DDR3 LRDIMMs that use components with x4 DQS widths
- Fixes a migration issue from the Quartus II software version 13.0 SP1 DP5 to version 13.1. When a top-level EMIF wrapper generated in version 13.0 SP1 DP5 was opened in version 13.1, the parameter editor GUI was reset to its default values. This fix maintains your design-specific parameters from version 13.0 SP1 DP5.

HSSI IP

- Fixes an issue that affected designs that targeted 5CSXFC4 and 5CSXFC2 devices in the Cyclone V family when HSSI-related input ports are tied to logic `1` or logic `0`. This update ensures that the connectivity implied by the netlist is maintained.
- For designs that target Arria II GX, Arria II GZ, Cyclone IV GX, Stratix IV GX, and Stratix IV GT devices, allows the `inclk[0]` port of a HSSI PLL to be left open. Previous versions of the Quartus II software required the `inclk[0]` port of an HSSI PLL to be driven.

PCI Express®

- For designs that target Arria V, Cyclone V, and Stratix V devices, fixes a problem that prevented the MegaWizard Plug-In Manager from automatically launching an IP variant that had been created with the PCIe Hard IP MegaWizard.
- For designs that target Arria® V devices, fixes a problem that affected the LTSSM within the PHY MAC in the Hard IP (HIP). In previous versions of the Altera Complete Design Suite, the Clock Generation Block (CGB) in the PMA does not get reset by digital reset when there is a speed switch, causing the LTSSM to loop between `Detect` and `Polling.Active` and to not proceed to `Polling.Config`, leading to a time out in Gen2 PCI Express (PCIe®) designs on Arria V ES and production devices. To apply this fix, regenerate the IP and recompile after installing update 2.
- For designs that target Arria V, Cyclone V, and Stratix V devices, fixes an issue with the PCIe MegaWizard Plug-In Manager, allowing variants to be successfully regenerated.
- Fixes an issue with the PCIe HIP when using the Avalon Memory-Mapped (Avalon-MM) interface with fixed address translation enabled. The issue affected designs that target Arria II GX, Cyclone IV GX, and Stratix IV GX devices.

VIP Suite

- Updates some false paths for the clocked video input (CVI) that are necessary for timing closure. Without the update, designs using the CVI are prone to timing failure that results in non-operational designs. Whether the design synthesized will operate has been observed as intermittent without the update. If designs using the CVI consistently function when programmed, then the observed change from this update is cleaner TimeQuest Timing Analyzer results. If multiple synthesis runs are required to generate an operational design, this update removes that inconsistency.

Issues Addressed in Update 1

The Altera Complete Design Suite version 13.1 update 1 (included with update 2) addresses the following software issues:

Device Support

- Provides full compilation and programming support for the following Arria V devices: 5ASXMB3E4F31I3 and 5ASXMB5E4F31I3.
- Provides full compilation and programming support for the following Cyclone V devices: 5CSEMA2, 5CSEBA2, 5CSXFC2, 5CSEMA4, 5CSEBA4, 5CSXFC4.
- Fixes an issue in the Quartus II software version 13.1 related to minor temperature-related routing resistance variances for Cyclone V devices and reverts timing delays to match those in the Quartus II software version 13.0 SP1. The impact to designs compiled with version 13.1 was small and is unlikely to cause a silicon issue.

Nios II EDS

- Corrects an issue that caused some Nios II EDS utilities to fail with no error output or messages when run on a Windows PC. The affected utilities are: `sof2flash`, `elf2flash`, `elf2hex` and `bin2flash`.

Qsys

- Adds UART1 pin location information for Arria V SoCs to the Peripherals Pin Multiplexing tab in Qsys.

Quartus II Compilation Flows

- Fixes missing Arria V GZ Programmable Power Technology Optimization settings on the **More Settings** panel of the **Fitter Settings** dialog box in the Quartus II software.
- Fixes an internal error that was generated when a PLL clock is routed to external IO pin with a `create_generated_clock` SDC assignment.
- Prevents an internal error in Advanced Single Event Upset (SEU) Detection, CvP Update, and Partial Reconfiguration flows when Strictly Preserved logic is placed into a single 1x1 Logic Lock region with no preserved routes leaving or entering the region.

- Fixes an issue in the Fitter where LVDS input buffers are powered by VCCPD, but VCCIO was mistakenly assigned to LVDS input pins with differential OCT.
- Fixes a problem with the register packer where register banks could be accidentally merged within DSP inputs when the input to the Fitter came from third party synthesis tools.
- Fixes an issue in which the Quartus II Fitter fails to place one or more nodes, including at least one dual-regional clock driver, generating an Error message similar to
  `Error (175001): Could not place dual-regional clock driver`
  In previous versions of the Quartus II software, this error occurred after the Fitter indicated that it had successfully placed all clocks in the design through messages like
  `Info (11178): Promoted <x> clocks...` or
  `Info (11191): Automatically promoted <x> clocks...`
- Removes incorrect error messages that can occur when using the Engineering Change Order (ECO) Fitter flow.
- Fixes an issue with VCCIO, VCCPD, and VCCN voltage rail settings in Stratix V 5SGXMBBR2H40I2L devices. Previous versions of the Quartus II software ignored a Quartus II Settings File (.qsf) assignment of `set_global_assignment -name STRATIX_DEVICE_IO_STANDARD "1.8 V"` and the I/O banks remained at 2.5 V.

Transceiver Toolkit

- Fixes an issue in the Transceiver Toolkit that caused receiver-only autosweep to always report a bit error rate of 1.

Simulation

- In previous versions of the Quartus II software, simulation of a Stratix V example design with a VHDL testbench fails in NCSIM because:

  1. Multiple copies of same file were being generated. NCSIM is not able to bind the instance to the correct module.
  2. Port corresponding to the unused lanes were not terminated during file generation.

  In Update 1, the above mentioned issues are fixed. Regenerate the files to simulate the VHDL example design in NCSIM.
- Fixes a simulation mismatch at the outputs of an adder when performing multiple DSP chaining with 18x18+36 mode through HDL code (inferencing). In previous versions of the Quartus II software, there was a chance to have a functionality issue if the input is signed and the result width for each DSP blocks are different.
- Removes unnecessary notification messages during simulation. The removed messages are of the form:
  `Input frequency on DLL instance <name> now matches with specified clock frequency.`

DSP Builder

- Fixes DSP Builder Advanced incorrectly merging duplicate delays that have configuration differences:
  - between the status of the minimum delay checkbox
  - equivalence group, if minimum delay has been checked.
- Fixes the following issues in DSP Builder Advanced optimization of constant fixed-point sub-expressions:
  - Addition and subtraction of signals with differing fraction lengths
  - Comparing signals with 0
  - Adding and subtracting without word growth and comparing with a constant
  - Comparing signals with differing fraction lengths
  - Bitwise ANDing and ORing of signals with differing fraction length
  - Adding and subtracting of non-zero constants with non-constant signals

IP

Ethernet IP Cores

- Fixes a problem in the KR4 Configuration of the 40G/100G Ethernet Megacore where reads from the MAC RX Statistics Registers may return invalid data.
- Enables MAC 10/100 half duplex support in the 10/100Mb Small MAC variation of the Triple-Speed Ethernet IP core.

EMIF IP Cores

- Fixes the behavior of the timing counters used during the power-on memory initialization and reset period of DDR memory interfaces. In previous versions of the Quartus II software, these timers assumed an AFI clock period of 266 MHz, therefore interfaces with AFI clock frequencies faster than 266 MHz had slightly shorter reset and initialization periods than the JEDEC-required specification. This change now adjusts the counters according to the AFI frequency such that the initialization time remains constant irrespective of interface frequency or rate. This change also ensures that the `Tinit` value specified in the MegaWizard Plug-In Manager under the **Memory Timing** tab modifies the initialization counter accordingly. Previous versions of Quartus hard-coded the memory initialization time to 500 µs.
  - Device Families Affected: Arria V, Cyclone V, Stratix IV, and Stratix V
  - Protocols Affected: DDR2 and DDR3 (for AFI clock frequencies greater than 266 MHz).

- Previous versions of the Quartus II software did not properly configure the memory controller for the Hard Processor Subsystem (HPS) when an LPDDR2 memory interface is selected in Arria V SoC and Cyclone V SoC devices. This problem manifests as a calibration failure error during the memory initialization phase. This update fixes this issue and this fix is recommended for any customer using LPDDR2 on an HPS.
  - Device Families Affected: Arria V SoC and Cyclone V SoC
  - Protocols Affected: LPDDR2
- In the Altera Complete Design Suite version 13.1, EMIF IP cores incorrectly issued a warning to indicate that Cyclone V timing models are preliminary. However, the last Cyclone V (nonSoC) timing models became final in ACDS 13.1. This update removes the EMIF IP preliminary timing model warning.

Software Issues Resolved

The following Customer Service Requests were fixed or otherwise resolved in the Altera Complete Design Suite version 13.1 update 2:

Customer Service Request Numbers Resolved in the Quartus II Software Version 13.1 Update 2							
10900722	10954006	10992650	10992883	11001656	11003696	11004120	11004934
11005290	11006004	11007341	11007811	11008366	11009476	11009884	11012523
11012860	11013336	11014409	—	—	—	—	—

The following Customer Service Requests were fixed or otherwise resolved in the Altera Complete Design Suite version 13.1 update 1:

Customer Service Request Numbers Resolved in the Quartus II Software Version 13.1 Update 1							
10862388	10865226	10957886	10990717	10995942	11001820	11002391	11004954
11005496	11007025	11007465	—	—	—	—	—

Software Patches Included

The Altera Complete Design Suite version 13.1 update 2 includes the following patches released for previous versions of the Altera Complete Design Suite software:

Quartus II Software Version	Patch	Customer Service Request Number	Quartus II Software Version	Patch	Customer Service Request Number
13.1	0.44	11004120	13.1	0.15	10992883
13.1	0.37	—	13.0	0.47	10992650
13.1	0.36	11012860	13.0sp1	1.dp5s	11001656
13.1	0.28	11009884	—	—	—

The Altera Complete Design Suite version 13.1 update 1 includes the following patches released for previous versions of the Altera Complete Design Suite software:

Quartus II Software Version	Patch	Customer Service Request Number	Quartus II Software Version	Patch	Customer Service Request Number
13.1	0.24	10957886,10990717	13.1	0.04	11002391
13.1	0.20	—	13.1	0.02	10995942
13.1	0.16	10862388	13.0 SP1	1.dp5e	—
13.1	0.11	10845226	13.0 SP1	1.67	10957886
13.1	0.07	11004954	13.0 SP1	1.51	10865226
13.1	0.05	11001820	13.0	0.48	10957886

Latest Known Altera Complete Design Suite Issues

Description	Workaround
In the Quartus II software version 13.1 update 2, the IP Upgrade table incorrectly displays that an update is available for many IP cores. After you update an affected core, the IP Upgrade table continues to display that an update is available.	No action is required. The continuous display indicating that an update is available affects only the GUI. Even though the IP Upgrade table continues to display that an update is available, the IP core will be at the most current version.

For more information about known software issues, can find known issue information refer to the Knowledge Database page at the following URL:

http://www.altera.com/support/kdb/kdb-index.jsp

For technical support information about the Quartus II software, refer to the **Quartus II Software Support** page at the following URL:

http://www.altera.com/support/software/sof-quartus.html

Document Revision History

The following table shows the revision history for this document.

Document Revision History

Date	Version	Changes
January 2013	13.1.2.0	Added update 2 information.
December 2013	13.1.1.0	Initial release.