Implementing Matrix Algebra (*,+) for FPGA-AIE

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***Abstract*—The FPGA-AIE is a novel design of systolic architectures with a memory hierarchy and where communications and computations have to be designed tightly. We present two tools for the presentation and implementation of a matrix algebra (*,+) that we call tiling and code generation.**

Tiling is the science of choosing spatial and temporal locality in order to exploit parallelism and high throughput. As tiling is done, we represent the computation as a block computation (human understandable) and then as graph with DMA connections, loop and tiling information that we can use to create an HW implementation using FPGA-AIE and in particular the MLADF interface.

I. Introduction