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Architetture dei Sistemi di Elaborazione **02GOLOV [A-L]** **Laboratory 3**	Delivery date: Wednesday, November 6, 2019 Expected delivery of lab_03.zip must include: - `program_2_a.s`, `program_2_b.s` and `program_2_c.s` - this file compiled and if possible in pdf format.

Please, configure the winMIPS64 simulator with the *Base Configuration* provided in the following:

- Code address bus: 12
- Data address bus: 12
- Pipelined FP arithmetic unit (latency): 4 stages
- Pipelined multiplier unit (latency): 8 stages
- divider unit (latency): not pipelined unit, 12 clock cycles
- Forwarding is enabled
- Branch prediction is disabled
- Branch delay slot is disabled
- *Integer ALU: 1 clock cycle*
- *Data memory: 1 clock cycle*
- *Branch delay slot: 1 clock cycle*.

1) Starting from the assembly program you created in the previous lab called **`program_2.s`**,:

```
for (i = 0; i < 30; i++){
        v5[i] = (v1[i]*v2[i]) + v3[i];
        v6[i] =(v3[i]*v4[i])/v5[i]:

}
```

   a. Detect manually the different data, structural and control hazards that provoke a pipeline stall
   b. Optimize the program by re-scheduling the program instructions in order to eliminate as much hazards as possible. Compute manually the number of clock cycles the new program (**`program_2_a.s`**) requires to execute, and compare the obtained results with the ones obtained by the simulator.

   c. Starting from **`program_2_a.s`**, enable the *branch delay slot* and re-schedule again the code in order to positively exploit the branch delay slot, or add NOP operations that avoid the code to lost its functionalities. Compute manually the number of clock cycles the new program (**`program_2_b.s`**) requires to execute, and compare the obtained results with the ones obtained by the simulator.

d. Unroll 3 times the program (**`program_2_b.s`**), after unrolling the code, reschedule again the code in order to improve the program performance. Compute manually the number of clock cycles the new program (**`program_2_c.s`**) requires to execute, and compare the obtained results with the ones obtained by the simulator.

Complete the following table with the obtained results:

Program Clock cycle computation	program_2.s	program_2_a.s	program_2_b.s	program_2_c.s
By hand	936	908	879	735
By simulation	936	908	879	735

Compare the results obtained in the point 1, and provide some explanation in the case the results are different.

Eventual explanation:

Il calcolo dei clock cycle di program_2.s risulta differente da quanto calcolato nella precedente relazione di laboratorio siccome vengono utilizzate due differenti configurazioni.

È possibile che nelle precedenti due relazioni di laboratorio ci fossero calcoli errati tra quelli fatti a mano perché non consideravo correttamente gli stage della pipeline occupati durante gli stalli.