---------- Begin Simulation Statistics ----------

sim\_seconds 0.004277 # Number of seconds simulated

sim\_ticks 4277042500 # Number of ticks simulated

final\_tick 4277042500 # Number of ticks from beginning of simulation (restored from checkpoints and never reset)

sim\_freq 1000000000000 # Frequency of simulated ticks

host\_inst\_rate 120034 # Simulator instruction rate (inst/s)

host\_op\_rate 120034 # Simulator op (including micro ops) rate (op/s)

host\_tick\_rate 50633140 # Simulator tick rate (ticks/s)

host\_mem\_usage 630544 # Number of bytes of host memory used

host\_seconds 84.47 # Real time elapsed on the host

sim\_insts 10139380 # Number of instructions simulated

sim\_ops 10139380 # Number of ops (including micro ops) simulated

system.voltage\_domain.voltage 1 # Voltage in Volts

system.clk\_domain.clock 1000 # Clock period in ticks

system.mem\_ctrls.pwrStateResidencyTicks::UNDEFINED 4277042500 # Cumulative time (in ticks) in various power states

system.mem\_ctrls.bytes\_read::cpu.inst 2778944 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_read::cpu.data 52160 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_read::total 2831104 # Number of bytes read from this memory

system.mem\_ctrls.bytes\_inst\_read::cpu.inst 2778944 # Number of instructions bytes read from this memory

system.mem\_ctrls.bytes\_inst\_read::total 2778944 # Number of instructions bytes read from this memory

system.mem\_ctrls.bytes\_written::writebacks 2304 # Number of bytes written to this memory

system.mem\_ctrls.bytes\_written::total 2304 # Number of bytes written to this memory

system.mem\_ctrls.num\_reads::cpu.inst 43421 # Number of read requests responded to by this memory

system.mem\_ctrls.num\_reads::cpu.data 815 # Number of read requests responded to by this memory

system.mem\_ctrls.num\_reads::total 44236 # Number of read requests responded to by this memory

system.mem\_ctrls.num\_writes::writebacks 36 # Number of write requests responded to by this memory

system.mem\_ctrls.num\_writes::total 36 # Number of write requests responded to by this memory

system.mem\_ctrls.bw\_read::cpu.inst 649734951 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_read::cpu.data 12195343 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_read::total 661930294 # Total read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_inst\_read::cpu.inst 649734951 # Instruction read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_inst\_read::total 649734951 # Instruction read bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_write::writebacks 538690 # Write bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_write::total 538690 # Write bandwidth from this memory (bytes/s)

system.mem\_ctrls.bw\_total::writebacks 538690 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.bw\_total::cpu.inst 649734951 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.bw\_total::cpu.data 12195343 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.bw\_total::total 662468984 # Total bandwidth to/from this memory (bytes/s)

system.mem\_ctrls.readReqs 44237 # Number of read requests accepted

system.mem\_ctrls.writeReqs 42955 # Number of write requests accepted

system.mem\_ctrls.readBursts 44237 # Number of DRAM read bursts, including those serviced by the write queue

system.mem\_ctrls.writeBursts 42955 # Number of DRAM write bursts, including those merged in the write queue

system.mem\_ctrls.bytesReadDRAM 1484928 # Total number of bytes read from DRAM

system.mem\_ctrls.bytesReadWrQ 1346240 # Total number of bytes read from write queue

system.mem\_ctrls.bytesWritten 1820608 # Total number of bytes written to DRAM

system.mem\_ctrls.bytesReadSys 2831168 # Total read bytes from the system interface side

system.mem\_ctrls.bytesWrittenSys 2749120 # Total written bytes from the system interface side

system.mem\_ctrls.servicedByWrQ 21035 # Number of DRAM read bursts serviced by the write queue

system.mem\_ctrls.mergedWrBursts 14487 # Number of DRAM write bursts merged with an existing one

system.mem\_ctrls.neitherReadNorWriteReqs 0 # Number of requests that are neither read nor write

system.mem\_ctrls.perBankRdBursts::0 5141 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::1 481 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::2 6424 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::3 296 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::4 356 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::5 149 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::6 6839 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::7 561 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::8 87 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::9 133 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::10 158 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::11 82 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::12 1327 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::13 32 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::14 961 # Per bank write bursts

system.mem\_ctrls.perBankRdBursts::15 175 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::0 6714 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::1 385 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::2 6724 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::3 275 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::4 254 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::5 43 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::6 10128 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::7 595 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::8 40 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::9 8 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::10 8 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::11 25 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::12 1616 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::13 20 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::14 1033 # Per bank write bursts

system.mem\_ctrls.perBankWrBursts::15 579 # Per bank write bursts

system.mem\_ctrls.numRdRetry 0 # Number of times read queue was full causing retry

system.mem\_ctrls.numWrRetry 0 # Number of times write queue was full causing retry

system.mem\_ctrls.totGap 4277027500 # Total gap between requests

system.mem\_ctrls.readPktSize::0 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::1 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::2 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::3 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::4 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::5 0 # Read request sizes (log2)

system.mem\_ctrls.readPktSize::6 44237 # Read request sizes (log2)

system.mem\_ctrls.writePktSize::0 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::1 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::2 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::3 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::4 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::5 0 # Write request sizes (log2)

system.mem\_ctrls.writePktSize::6 42955 # Write request sizes (log2)

system.mem\_ctrls.rdQLenPdf::0 20609 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::1 2157 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::2 334 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::3 93 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::4 7 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::5 2 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::6 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::7 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::8 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::9 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::10 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::11 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::12 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::13 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::14 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::15 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::16 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::17 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::18 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::19 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::20 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::21 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::22 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::23 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::24 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::25 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::26 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::27 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::28 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::29 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::30 0 # What read queue length does an incoming req see

system.mem\_ctrls.rdQLenPdf::31 0 # What read queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::0 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::1 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::2 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::3 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::4 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::5 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::6 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::7 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::8 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::9 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::10 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::11 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::12 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::13 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::14 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::15 268 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::16 321 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::17 1431 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::18 1718 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::19 1836 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::20 1765 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::21 1771 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::22 1767 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::23 1933 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::24 1762 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::25 1746 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::26 1727 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::27 1788 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::28 1726 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::29 1726 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::30 1719 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::31 1718 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::32 1717 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::33 8 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::34 5 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::35 1 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::36 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::37 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::38 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::39 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::40 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::41 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::42 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::43 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::44 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::45 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::46 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::47 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::48 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::49 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::50 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::51 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::52 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::53 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::54 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::55 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::56 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::57 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::58 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::59 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::60 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::61 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::62 0 # What write queue length does an incoming req see

system.mem\_ctrls.wrQLenPdf::63 0 # What write queue length does an incoming req see

system.mem\_ctrls.bytesPerActivate::samples 10010 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::mean 329.820579 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::gmean 235.536964 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::stdev 264.513300 # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::0-127 1750 17.48% 17.48% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::128-255 2922 29.19% 46.67% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::256-383 1659 16.57% 63.25% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::384-511 1246 12.45% 75.69% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::512-639 896 8.95% 84.65% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::640-767 502 5.01% 89.66% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::768-895 362 3.62% 93.28% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::896-1023 286 2.86% 96.13% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::1024-1151 387 3.87% 100.00% # Bytes accessed per row activation

system.mem\_ctrls.bytesPerActivate::total 10010 # Bytes accessed per row activation

system.mem\_ctrls.rdPerTurnAround::samples 1717 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::mean 13.510775 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::gmean 12.837328 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::stdev 9.836870 # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::0-15 1362 79.32% 79.32% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::16-31 348 20.27% 99.59% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::32-47 4 0.23% 99.83% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::48-63 1 0.06% 99.88% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::112-127 1 0.06% 99.94% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::368-383 1 0.06% 100.00% # Reads before turning the bus around for writes

system.mem\_ctrls.rdPerTurnAround::total 1717 # Reads before turning the bus around for writes

system.mem\_ctrls.wrPerTurnAround::samples 1717 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::mean 16.567851 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::gmean 16.525099 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::stdev 1.254211 # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::16 1355 78.92% 78.92% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::17 59 3.44% 82.35% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::18 151 8.79% 91.15% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::19 42 2.45% 93.59% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::20 72 4.19% 97.79% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::21 28 1.63% 99.42% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::22 10 0.58% 100.00% # Writes before turning the bus around for reads

system.mem\_ctrls.wrPerTurnAround::total 1717 # Writes before turning the bus around for reads

system.mem\_ctrls.totQLat 450796750 # Total ticks spent queuing

system.mem\_ctrls.totMemAccLat 885834250 # Total ticks spent from burst creation until serviced by the DRAM

system.mem\_ctrls.totBusLat 116010000 # Total ticks spent in databus transfers

system.mem\_ctrls.avgQLat 19429.22 # Average queueing delay per DRAM burst

system.mem\_ctrls.avgBusLat 5000.00 # Average bus latency per DRAM burst

system.mem\_ctrls.avgMemAccLat 38179.22 # Average memory access latency per DRAM burst

system.mem\_ctrls.avgRdBW 347.19 # Average DRAM read bandwidth in MiByte/s

system.mem\_ctrls.avgWrBW 425.67 # Average achieved write bandwidth in MiByte/s

system.mem\_ctrls.avgRdBWSys 661.95 # Average system read bandwidth in MiByte/s

system.mem\_ctrls.avgWrBWSys 642.76 # Average system write bandwidth in MiByte/s

system.mem\_ctrls.peakBW 12800.00 # Theoretical peak bandwidth in MiByte/s

system.mem\_ctrls.busUtil 6.04 # Data bus utilization in percentage

system.mem\_ctrls.busUtilRead 2.71 # Data bus utilization in percentage for reads

system.mem\_ctrls.busUtilWrite 3.33 # Data bus utilization in percentage for writes

system.mem\_ctrls.avgRdQLen 1.05 # Average read queue length when enqueuing

system.mem\_ctrls.avgWrQLen 25.45 # Average write queue length when enqueuing

system.mem\_ctrls.readRowHits 17399 # Number of row buffer hits during reads

system.mem\_ctrls.writeRowHits 24228 # Number of row buffer hits during writes

system.mem\_ctrls.readRowHitRate 74.99 # Row buffer hit rate for reads

system.mem\_ctrls.writeRowHitRate 85.11 # Row buffer hit rate for writes

system.mem\_ctrls.avgGap 49052.98 # Average gap between requests

system.mem\_ctrls.pageHitRate 80.56 # Row buffer hit rate, read and write combined

system.mem\_ctrls\_0.actEnergy 59404800 # Energy for activate commands per rank (pJ)

system.mem\_ctrls\_0.preEnergy 31555425 # Energy for precharge commands per rank (pJ)

system.mem\_ctrls\_0.readEnergy 144563580 # Energy for read commands per rank (pJ)

system.mem\_ctrls\_0.writeEnergy 131115960 # Energy for write commands per rank (pJ)

system.mem\_ctrls\_0.refreshEnergy 185006640.000000 # Energy for refresh commands per rank (pJ)

system.mem\_ctrls\_0.actBackEnergy 405610290 # Energy for active background per rank (pJ)

system.mem\_ctrls\_0.preBackEnergy 4461600 # Energy for precharge background per rank (pJ)

system.mem\_ctrls\_0.actPowerDownEnergy 616604340 # Energy for active power-down per rank (pJ)

system.mem\_ctrls\_0.prePowerDownEnergy 21881280 # Energy for precharge power-down per rank (pJ)

system.mem\_ctrls\_0.selfRefreshEnergy 474779400 # Energy for self refresh per rank (pJ)

system.mem\_ctrls\_0.totalEnergy 2074983315 # Total energy per rank (pJ)

system.mem\_ctrls\_0.averagePower 485.144423 # Core power per rank (mW)

system.mem\_ctrls\_0.totalIdleTime 3376065500 # Total Idle time Per DRAM Rank

system.mem\_ctrls\_0.memoryStateTime::IDLE 2580000 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::REF 78290000 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::SREF 1966741000 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::PRE\_PDN 56963250 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::ACT 820107000 # Time in different power states

system.mem\_ctrls\_0.memoryStateTime::ACT\_PDN 1352361250 # Time in different power states

system.mem\_ctrls\_1.actEnergy 12152280 # Energy for activate commands per rank (pJ)

system.mem\_ctrls\_1.preEnergy 6432525 # Energy for precharge commands per rank (pJ)

system.mem\_ctrls\_1.readEnergy 21098700 # Energy for read commands per rank (pJ)

system.mem\_ctrls\_1.writeEnergy 17377380 # Energy for write commands per rank (pJ)

system.mem\_ctrls\_1.refreshEnergy 184392000.000000 # Energy for refresh commands per rank (pJ)

system.mem\_ctrls\_1.actBackEnergy 464170950 # Energy for active background per rank (pJ)

system.mem\_ctrls\_1.preBackEnergy 4632000 # Energy for precharge background per rank (pJ)

system.mem\_ctrls\_1.actPowerDownEnergy 431987610 # Energy for active power-down per rank (pJ)

system.mem\_ctrls\_1.prePowerDownEnergy 125182560 # Energy for precharge power-down per rank (pJ)

system.mem\_ctrls\_1.selfRefreshEnergy 476454900 # Energy for self refresh per rank (pJ)

system.mem\_ctrls\_1.totalEnergy 1743880905 # Total energy per rank (pJ)

system.mem\_ctrls\_1.averagePower 407.730553 # Core power per rank (mW)

system.mem\_ctrls\_1.totalIdleTime 3246917750 # Total Idle time Per DRAM Rank

system.mem\_ctrls\_1.memoryStateTime::IDLE 3646000 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::REF 78030000 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::SREF 1973723750 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::PRE\_PDN 325915750 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::ACT 948345000 # Time in different power states

system.mem\_ctrls\_1.memoryStateTime::ACT\_PDN 947382000 # Time in different power states

system.pwrStateResidencyTicks::UNDEFINED 4277042500 # Cumulative time (in ticks) in various power states

system.cpu.branchPred.lookups 1665759 # Number of BP lookups

system.cpu.branchPred.condPredicted 1232318 # Number of conditional branches predicted

system.cpu.branchPred.condIncorrect 47445 # Number of conditional branches incorrect

system.cpu.branchPred.BTBLookups 1175368 # Number of BTB lookups

system.cpu.branchPred.BTBHits 1068082 # Number of BTB hits

system.cpu.branchPred.BTBCorrect 0 # Number of correct BTB predictions (this stat may not work properly.

system.cpu.branchPred.BTBHitPct 90.872135 # BTB Hit Percentage

system.cpu.branchPred.usedRAS 138828 # Number of times the RAS was used to get a target.

system.cpu.branchPred.RASInCorrect 19 # Number of incorrect RAS predictions.

system.cpu.branchPred.indirectLookups 37992 # Number of indirect predictor lookups.

system.cpu.branchPred.indirectHits 36682 # Number of indirect target hits.

system.cpu.branchPred.indirectMisses 1310 # Number of indirect misses.

system.cpu.branchPredindirectMispredicted 126 # Number of mispredicted indirect branches.

system.cpu\_voltage\_domain.voltage 1 # Voltage in Volts

system.cpu\_clk\_domain.clock 500 # Clock period in ticks

system.cpu.dtb.fetch\_hits 0 # ITB hits

system.cpu.dtb.fetch\_misses 0 # ITB misses

system.cpu.dtb.fetch\_acv 0 # ITB acv

system.cpu.dtb.fetch\_accesses 0 # ITB accesses

system.cpu.dtb.read\_hits 1572316 # DTB read hits

system.cpu.dtb.read\_misses 1483 # DTB read misses

system.cpu.dtb.read\_acv 0 # DTB read access violations

system.cpu.dtb.read\_accesses 1573799 # DTB read accesses

system.cpu.dtb.write\_hits 916628 # DTB write hits

system.cpu.dtb.write\_misses 7 # DTB write misses

system.cpu.dtb.write\_acv 0 # DTB write access violations

system.cpu.dtb.write\_accesses 916635 # DTB write accesses

system.cpu.dtb.data\_hits 2488944 # DTB hits

system.cpu.dtb.data\_misses 1490 # DTB misses

system.cpu.dtb.data\_acv 0 # DTB access violations

system.cpu.dtb.data\_accesses 2490434 # DTB accesses

system.cpu.itb.fetch\_hits 1721594 # ITB hits

system.cpu.itb.fetch\_misses 520 # ITB misses

system.cpu.itb.fetch\_acv 0 # ITB acv

system.cpu.itb.fetch\_accesses 1722114 # ITB accesses

system.cpu.itb.read\_hits 0 # DTB read hits

system.cpu.itb.read\_misses 0 # DTB read misses

system.cpu.itb.read\_acv 0 # DTB read access violations

system.cpu.itb.read\_accesses 0 # DTB read accesses

system.cpu.itb.write\_hits 0 # DTB write hits

system.cpu.itb.write\_misses 0 # DTB write misses

system.cpu.itb.write\_acv 0 # DTB write access violations

system.cpu.itb.write\_accesses 0 # DTB write accesses

system.cpu.itb.data\_hits 0 # DTB hits

system.cpu.itb.data\_misses 0 # DTB misses

system.cpu.itb.data\_acv 0 # DTB access violations

system.cpu.itb.data\_accesses 0 # DTB accesses

system.cpu.workload.numSyscalls 7437 # Number of system calls

system.cpu.pwrStateResidencyTicks::ON 4277042500 # Cumulative time (in ticks) in various power states

system.cpu.numCycles 8554090 # number of cpu cycles simulated

system.cpu.numWorkItemsStarted 0 # number of work items this cpu started

system.cpu.numWorkItemsCompleted 0 # number of work items this cpu completed

system.cpu.fetch.icacheStallCycles 2794300 # Number of cycles fetch is stalled on an Icache miss

system.cpu.fetch.Insts 11521422 # Number of instructions fetch has processed

system.cpu.fetch.Branches 1665759 # Number of branches that fetch encountered

system.cpu.fetch.predictedBranches 1243592 # Number of branches that fetch has predicted taken

system.cpu.fetch.Cycles 3010393 # Number of cycles fetch has run and was not squashing or blocked

system.cpu.fetch.SquashCycles 98966 # Number of cycles fetch has spent squashing

system.cpu.fetch.MiscStallCycles 372 # Number of cycles fetch has spent waiting on interrupts, or bad addresses, or out of MSHRs

system.cpu.fetch.PendingTrapStallCycles 2887 # Number of stall cycles due to pending traps

system.cpu.fetch.IcacheWaitRetryStallCycles 37 # Number of stall cycles due to full MSHR

system.cpu.fetch.CacheLines 1721594 # Number of cache lines fetched

system.cpu.fetch.IcacheSquashes 25071 # Number of outstanding Icache misses that were squashed

system.cpu.fetch.rateDist::samples 5857472 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::mean 1.966962 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::stdev 2.832461 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::underflows 0 0.00% 0.00% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::0 3344711 57.10% 57.10% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::1 316722 5.41% 62.51% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::2 416706 7.11% 69.62% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::3 346916 5.92% 75.55% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::4 261690 4.47% 80.01% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::5 233717 3.99% 84.00% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::6 132298 2.26% 86.26% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::7 116289 1.99% 88.25% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::8 688423 11.75% 100.00% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::overflows 0 0.00% 100.00% # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::min\_value 0 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::max\_value 8 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.rateDist::total 5857472 # Number of instructions fetched each cycle (Total)

system.cpu.fetch.branchRate 0.194732 # Number of branch fetches per cycle

system.cpu.fetch.rate 1.346890 # Number of inst fetches per cycle

system.cpu.decode.IdleCycles 2428063 # Number of cycles decode is idle

system.cpu.decode.BlockedCycles 1140671 # Number of cycles decode is blocked

system.cpu.decode.RunCycles 1976710 # Number of cycles decode is running

system.cpu.decode.UnblockCycles 267139 # Number of cycles decode is unblocking

system.cpu.decode.SquashCycles 44889 # Number of cycles decode is squashing

system.cpu.decode.BranchResolved 1056195 # Number of times decode resolved a branch

system.cpu.decode.BranchMispred 4620 # Number of times decode detected a branch misprediction

system.cpu.decode.DecodedInsts 11191499 # Number of instructions handled by decode

system.cpu.decode.SquashedInsts 13818 # Number of squashed instructions handled by decode

system.cpu.rename.SquashCycles 44889 # Number of cycles rename is squashing

system.cpu.rename.IdleCycles 2534254 # Number of cycles rename is idle

system.cpu.rename.BlockCycles 48054 # Number of cycles rename is blocking

system.cpu.rename.serializeStallCycles 517275 # count of cycles rename stalled for serializing inst

system.cpu.rename.RunCycles 2136643 # Number of cycles rename is running

system.cpu.rename.UnblockCycles 576357 # Number of cycles rename is unblocking

system.cpu.rename.RenamedInsts 11068452 # Number of instructions processed by rename

system.cpu.rename.ROBFullEvents 10 # Number of times rename has blocked due to ROB full

system.cpu.rename.IQFullEvents 521630 # Number of times rename has blocked due to IQ full

system.cpu.rename.LQFullEvents 192 # Number of times rename has blocked due to LQ full

system.cpu.rename.SQFullEvents 1099 # Number of times rename has blocked due to SQ full

system.cpu.rename.RenamedOperands 8419052 # Number of destination operands rename has renamed

system.cpu.rename.RenameLookups 15812297 # Number of register rename lookups that rename has made

system.cpu.rename.int\_rename\_lookups 15678559 # Number of integer rename lookups

system.cpu.rename.fp\_rename\_lookups 117752 # Number of floating rename lookups

system.cpu.rename.CommittedMaps 7866705 # Number of HB maps that are committed

system.cpu.rename.UndoneMaps 552347 # Number of HB maps that are undone due to squashing

system.cpu.rename.serializingInsts 31498 # count of serializing insts renamed

system.cpu.rename.tempSerializingInsts 12498 # count of temporary serializing insts renamed

system.cpu.rename.skidInsts 1225255 # count of insts added to the skid buffer

system.cpu.memDep0.insertedLoads 1589707 # Number of loads inserted to the mem dependence unit.

system.cpu.memDep0.insertedStores 935070 # Number of stores inserted to the mem dependence unit.

system.cpu.memDep0.conflictingLoads 85230 # Number of conflicting loads.

system.cpu.memDep0.conflictingStores 31585 # Number of conflicting stores.

system.cpu.iq.iqInstsAdded 10661433 # Number of instructions added to the IQ (excludes non-spec)

system.cpu.iq.iqNonSpecInstsAdded 17451 # Number of non-speculative instructions added to the IQ

system.cpu.iq.iqInstsIssued 10496601 # Number of instructions issued

system.cpu.iq.iqSquashedInstsIssued 828 # Number of squashed instructions issued

system.cpu.iq.iqSquashedInstsExamined 539503 # Number of squashed instructions iterated over during squash; mainly for profiling

system.cpu.iq.iqSquashedOperandsExamined 337318 # Number of squashed operands that are examined and possibly removed from graph

system.cpu.iq.iqSquashedNonSpecRemoved 121 # Number of squashed non-spec instructions that were removed

system.cpu.iq.issued\_per\_cycle::samples 5857472 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::mean 1.792002 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::stdev 1.742380 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::underflows 0 0.00% 0.00% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::0 1785318 30.48% 30.48% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::1 1155053 19.72% 50.20% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::2 1178163 20.11% 70.31% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::3 792030 13.52% 83.83% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::4 476751 8.14% 91.97% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::5 256236 4.37% 96.35% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::6 114014 1.95% 98.29% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::7 62392 1.07% 99.36% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::8 37515 0.64% 100.00% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::overflows 0 0.00% 100.00% # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::min\_value 0 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::max\_value 8 # Number of insts issued each cycle

system.cpu.iq.issued\_per\_cycle::total 5857472 # Number of insts issued each cycle

system.cpu.iq.fu\_full::No\_OpClass 0 0.00% 0.00% # attempts to use FU when none available

system.cpu.iq.fu\_full::IntAlu 17111 14.20% 14.20% # attempts to use FU when none available

system.cpu.iq.fu\_full::IntMult 6798 5.64% 19.84% # attempts to use FU when none available

system.cpu.iq.fu\_full::IntDiv 0 0.00% 19.84% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatAdd 0 0.00% 19.84% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatCmp 0 0.00% 19.84% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatCvt 0 0.00% 19.84% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMult 12 0.01% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMultAcc 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatDiv 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMisc 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatSqrt 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdAdd 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdAddAcc 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdAlu 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdCmp 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdCvt 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdMisc 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdMult 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdMultAcc 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdShift 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdShiftAcc 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdSqrt 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatAdd 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatAlu 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatCmp 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatCvt 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatDiv 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatMisc 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatMult 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatMultAcc 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::SimdFloatSqrt 0 0.00% 19.85% # attempts to use FU when none available

system.cpu.iq.fu\_full::MemRead 37726 31.31% 51.16% # attempts to use FU when none available

system.cpu.iq.fu\_full::MemWrite 50179 41.65% 92.81% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMemRead 337 0.28% 93.09% # attempts to use FU when none available

system.cpu.iq.fu\_full::FloatMemWrite 8329 6.91% 100.00% # attempts to use FU when none available

system.cpu.iq.fu\_full::IprAccess 0 0.00% 100.00% # attempts to use FU when none available

system.cpu.iq.fu\_full::InstPrefetch 0 0.00% 100.00% # attempts to use FU when none available

system.cpu.iq.FU\_type\_0::No\_OpClass 2156 0.02% 0.02% # Type of FU issued

system.cpu.iq.FU\_type\_0::IntAlu 7863586 74.92% 74.94% # Type of FU issued

system.cpu.iq.FU\_type\_0::IntMult 66849 0.64% 75.57% # Type of FU issued

system.cpu.iq.FU\_type\_0::IntDiv 0 0.00% 75.57% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatAdd 31151 0.30% 75.87% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatCmp 4086 0.04% 75.91% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatCvt 8311 0.08% 75.99% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMult 8576 0.08% 76.07% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMultAcc 0 0.00% 76.07% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatDiv 1470 0.01% 76.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMisc 0 0.00% 76.08% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatSqrt 252 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdAdd 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdAddAcc 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdAlu 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdCmp 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdCvt 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdMisc 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdMult 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdMultAcc 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdShift 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdShiftAcc 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdSqrt 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatAdd 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatAlu 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatCmp 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatCvt 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatDiv 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatMisc 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatMult 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatMultAcc 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::SimdFloatSqrt 0 0.00% 76.09% # Type of FU issued

system.cpu.iq.FU\_type\_0::MemRead 1572720 14.98% 91.07% # Type of FU issued

system.cpu.iq.FU\_type\_0::MemWrite 897398 8.55% 99.62% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMemRead 16639 0.16% 99.78% # Type of FU issued

system.cpu.iq.FU\_type\_0::FloatMemWrite 23407 0.22% 100.00% # Type of FU issued

system.cpu.iq.FU\_type\_0::IprAccess 0 0.00% 100.00% # Type of FU issued

system.cpu.iq.FU\_type\_0::InstPrefetch 0 0.00% 100.00% # Type of FU issued

system.cpu.iq.FU\_type\_0::total 10496601 # Type of FU issued

system.cpu.iq.rate 1.227086 # Inst issue rate

system.cpu.iq.fu\_busy\_cnt 120492 # FU busy when requested

system.cpu.iq.fu\_busy\_rate 0.011479 # FU busy rate (busy events/executed inst)

system.cpu.iq.int\_inst\_queue\_reads 26775526 # Number of integer instruction queue reads

system.cpu.iq.int\_inst\_queue\_writes 11125402 # Number of integer instruction queue writes

system.cpu.iq.int\_inst\_queue\_wakeup\_accesses 10311989 # Number of integer instruction queue wakeup accesses

system.cpu.iq.fp\_inst\_queue\_reads 196468 # Number of floating instruction queue reads

system.cpu.iq.fp\_inst\_queue\_writes 95365 # Number of floating instruction queue writes

system.cpu.iq.fp\_inst\_queue\_wakeup\_accesses 93684 # Number of floating instruction queue wakeup accesses

system.cpu.iq.vec\_inst\_queue\_reads 0 # Number of vector instruction queue reads

system.cpu.iq.vec\_inst\_queue\_writes 0 # Number of vector instruction queue writes

system.cpu.iq.vec\_inst\_queue\_wakeup\_accesses 0 # Number of vector instruction queue wakeup accesses

system.cpu.iq.int\_alu\_accesses 10512367 # Number of integer alu accesses

system.cpu.iq.fp\_alu\_accesses 102570 # Number of floating point alu accesses

system.cpu.iq.vec\_alu\_accesses 0 # Number of vector alu accesses

system.cpu.iew.lsq.thread0.forwLoads 88137 # Number of loads that had data forwarded from stores

system.cpu.iew.lsq.thread0.invAddrLoads 0 # Number of loads ignored due to an invalid address

system.cpu.iew.lsq.thread0.squashedLoads 74738 # Number of loads squashed

system.cpu.iew.lsq.thread0.ignoredResponses 115 # Number of memory responses ignored because the instruction is squashed

system.cpu.iew.lsq.thread0.memOrderViolation 2390 # Number of memory ordering violations

system.cpu.iew.lsq.thread0.squashedStores 46522 # Number of stores squashed

system.cpu.iew.lsq.thread0.invAddrSwpfs 0 # Number of software prefetches ignored due to an invalid address

system.cpu.iew.lsq.thread0.blockedLoads 0 # Number of blocked loads due to partial load-store forwarding

system.cpu.iew.lsq.thread0.rescheduledLoads 5182 # Number of loads that were rescheduled

system.cpu.iew.lsq.thread0.cacheBlocked 78 # Number of times an access to memory failed due to the cache being blocked

system.cpu.iew.iewIdleCycles 0 # Number of cycles IEW is idle

system.cpu.iew.iewSquashCycles 44889 # Number of cycles IEW is squashing

system.cpu.iew.iewBlockCycles 47706 # Number of cycles IEW is blocking

system.cpu.iew.iewUnblockCycles 273 # Number of cycles IEW is unblocking

system.cpu.iew.iewDispatchedInsts 10887887 # Number of instructions dispatched to IQ

system.cpu.iew.iewDispSquashedInsts 27203 # Number of squashed instructions skipped by dispatch

system.cpu.iew.iewDispLoadInsts 1589707 # Number of dispatched load instructions

system.cpu.iew.iewDispStoreInsts 935070 # Number of dispatched store instructions

system.cpu.iew.iewDispNonSpecInsts 12465 # Number of dispatched non-speculative instructions

system.cpu.iew.iewIQFullEvents 8 # Number of times the IQ has become full, causing a stall

system.cpu.iew.iewLSQFullEvents 259 # Number of times the LSQ has become full, causing a stall

system.cpu.iew.memOrderViolationEvents 2390 # Number of memory order violations

system.cpu.iew.predictedTakenIncorrect 26671 # Number of branches that were predicted taken incorrectly

system.cpu.iew.predictedNotTakenIncorrect 17852 # Number of branches that were predicted not taken incorrectly

system.cpu.iew.branchMispredicts 44523 # Number of branch mispredicts detected at execute

system.cpu.iew.iewExecutedInsts 10434697 # Number of executed instructions

system.cpu.iew.iewExecLoadInsts 1573799 # Number of load instructions executed

system.cpu.iew.iewExecSquashedInsts 61904 # Number of squashed instructions skipped in execute

system.cpu.iew.exec\_swp 0 # number of swp insts executed

system.cpu.iew.exec\_nop 209003 # number of nop insts executed

system.cpu.iew.exec\_refs 2490434 # number of memory reference insts executed

system.cpu.iew.exec\_branches 1546414 # Number of branches executed

system.cpu.iew.exec\_stores 916635 # Number of stores executed

system.cpu.iew.exec\_rate 1.219849 # Inst execution rate

system.cpu.iew.wb\_sent 10415106 # cumulative count of insts sent to commit

system.cpu.iew.wb\_count 10405673 # cumulative count of insts written-back

system.cpu.iew.wb\_producers 6617437 # num instructions producing a value

system.cpu.iew.wb\_consumers 9312379 # num instructions consuming a value

system.cpu.iew.wb\_rate 1.216456 # insts written-back per cycle

system.cpu.iew.wb\_fanout 0.710606 # average fanout of values written-back

system.cpu.commit.commitSquashedInsts 547110 # The number of squashed insts skipped by commit

system.cpu.commit.commitNonSpecStalls 17330 # The number of times commit has been forced to stall to communicate backwards

system.cpu.commit.branchMispredicts 43197 # The number of times a branch was mispredicted

system.cpu.commit.committed\_per\_cycle::samples 5765068 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::mean 1.793675 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::stdev 2.168951 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::underflows 0 0.00% 0.00% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::0 2013290 34.92% 34.92% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::1 1203973 20.88% 55.81% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::2 1353592 23.48% 79.29% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::3 255535 4.43% 83.72% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::4 278294 4.83% 88.55% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::5 133448 2.31% 90.86% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::6 116408 2.02% 92.88% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::7 100192 1.74% 94.62% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::8 310336 5.38% 100.00% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::overflows 0 0.00% 100.00% # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::min\_value 0 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::max\_value 8 # Number of insts commited each cycle

system.cpu.commit.committed\_per\_cycle::total 5765068 # Number of insts commited each cycle

system.cpu.commit.committedInsts 10340658 # Number of instructions committed

system.cpu.commit.committedOps 10340658 # Number of ops (including micro ops) committed

system.cpu.commit.swp\_count 0 # Number of s/w prefetches committed

system.cpu.commit.refs 2403517 # Number of memory references committed

system.cpu.commit.loads 1514969 # Number of loads committed

system.cpu.commit.membars 4946 # Number of memory barriers committed

system.cpu.commit.branches 1505942 # Number of branches committed

system.cpu.commit.vec\_insts 0 # Number of committed Vector instructions.

system.cpu.commit.fp\_insts 93103 # Number of committed floating point instructions.

system.cpu.commit.int\_insts 9933385 # Number of committed integer instructions.

system.cpu.commit.function\_calls 130980 # Number of function calls committed.

system.cpu.commit.op\_class\_0::No\_OpClass 203010 1.96% 1.96% # Class of committed instruction

system.cpu.commit.op\_class\_0::IntAlu 7610239 73.60% 75.56% # Class of committed instruction

system.cpu.commit.op\_class\_0::IntMult 65686 0.64% 76.19% # Class of committed instruction

system.cpu.commit.op\_class\_0::IntDiv 0 0.00% 76.19% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatAdd 30763 0.30% 76.49% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatCmp 3934 0.04% 76.53% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatCvt 8299 0.08% 76.61% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMult 8547 0.08% 76.69% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMultAcc 0 0.00% 76.69% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatDiv 1468 0.01% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMisc 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatSqrt 248 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdAdd 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdAddAcc 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdAlu 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdCmp 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdCvt 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdMisc 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdMult 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdMultAcc 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdShift 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdShiftAcc 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdSqrt 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatAdd 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatAlu 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatCmp 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatCvt 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatDiv 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatMisc 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatMult 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatMultAcc 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::SimdFloatSqrt 0 0.00% 76.71% # Class of committed instruction

system.cpu.commit.op\_class\_0::MemRead 1503457 14.54% 91.25% # Class of committed instruction

system.cpu.commit.op\_class\_0::MemWrite 865163 8.37% 99.61% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMemRead 16458 0.16% 99.77% # Class of committed instruction

system.cpu.commit.op\_class\_0::FloatMemWrite 23386 0.23% 100.00% # Class of committed instruction

system.cpu.commit.op\_class\_0::IprAccess 0 0.00% 100.00% # Class of committed instruction

system.cpu.commit.op\_class\_0::InstPrefetch 0 0.00% 100.00% # Class of committed instruction

system.cpu.commit.op\_class\_0::total 10340658 # Class of committed instruction

system.cpu.commit.bw\_lim\_events 310336 # number cycles where commit BW limit reached

system.cpu.rob.rob\_reads 16341694 # The number of ROB reads

system.cpu.rob.rob\_writes 21868847 # The number of ROB writes

system.cpu.timesIdled 38337 # Number of times that the entire CPU went into an idle state and unscheduled itself

system.cpu.idleCycles 2696618 # Total number of cycles that the CPU has spent unscheduled due to idling

system.cpu.committedInsts 10139380 # Number of Instructions Simulated

system.cpu.committedOps 10139380 # Number of Ops (including micro ops) Simulated

system.cpu.cpi 0.843650 # CPI: Cycles Per Instruction

system.cpu.cpi\_total 0.843650 # CPI: Total CPI of All Threads

system.cpu.ipc 1.185325 # IPC: Instructions Per Cycle

system.cpu.ipc\_total 1.185325 # IPC: Total IPC of All Threads

system.cpu.int\_regfile\_reads 15119908 # number of integer regfile reads

system.cpu.int\_regfile\_writes 8032961 # number of integer regfile writes

system.cpu.fp\_regfile\_reads 116512 # number of floating regfile reads

system.cpu.fp\_regfile\_writes 59781 # number of floating regfile writes

system.cpu.misc\_regfile\_reads 46732 # number of misc regfile reads

system.cpu.misc\_regfile\_writes 9896 # number of misc regfile writes

system.cpu.dcache.tags.pwrStateResidencyTicks::UNDEFINED 4277042500 # Cumulative time (in ticks) in various power states

system.cpu.dcache.tags.replacements 161 # number of replacements

system.cpu.dcache.tags.tagsinuse 555.904980 # Cycle average of tags in use

system.cpu.dcache.tags.total\_refs 2365676 # Total number of references to valid blocks.

system.cpu.dcache.tags.sampled\_refs 815 # Sample count of references to valid blocks.

system.cpu.dcache.tags.avg\_refs 2902.669939 # Average number of references to valid blocks.

system.cpu.dcache.tags.warmup\_cycle 159000 # Cycle when the warmup percentage was hit.

system.cpu.dcache.tags.occ\_blocks::cpu.data 555.904980 # Average occupied blocks per requestor

system.cpu.dcache.tags.occ\_percent::cpu.data 0.542876 # Average percentage of cache occupancy

system.cpu.dcache.tags.occ\_percent::total 0.542876 # Average percentage of cache occupancy

system.cpu.dcache.tags.occ\_task\_id\_blocks::1024 654 # Occupied blocks per task id

system.cpu.dcache.tags.age\_task\_id\_blocks\_1024::0 12 # Occupied blocks per task id

system.cpu.dcache.tags.age\_task\_id\_blocks\_1024::3 642 # Occupied blocks per task id

system.cpu.dcache.tags.occ\_task\_id\_percent::1024 0.638672 # Percentage of cache occupancy per task id

system.cpu.dcache.tags.tag\_accesses 4735771 # Number of tag accesses

system.cpu.dcache.tags.data\_accesses 4735771 # Number of data accesses

system.cpu.dcache.pwrStateResidencyTicks::UNDEFINED 4277042500 # Cumulative time (in ticks) in various power states

system.cpu.dcache.ReadReq\_hits::cpu.data 1472638 # number of ReadReq hits

system.cpu.dcache.ReadReq\_hits::total 1472638 # number of ReadReq hits

system.cpu.dcache.WriteReq\_hits::cpu.data 883148 # number of WriteReq hits

system.cpu.dcache.WriteReq\_hits::total 883148 # number of WriteReq hits

system.cpu.dcache.LoadLockedReq\_hits::cpu.data 4944 # number of LoadLockedReq hits

system.cpu.dcache.LoadLockedReq\_hits::total 4944 # number of LoadLockedReq hits

system.cpu.dcache.StoreCondReq\_hits::cpu.data 4946 # number of StoreCondReq hits

system.cpu.dcache.StoreCondReq\_hits::total 4946 # number of StoreCondReq hits

system.cpu.dcache.demand\_hits::cpu.data 2355786 # number of demand (read+write) hits

system.cpu.dcache.demand\_hits::total 2355786 # number of demand (read+write) hits

system.cpu.dcache.overall\_hits::cpu.data 2355786 # number of overall hits

system.cpu.dcache.overall\_hits::total 2355786 # number of overall hits

system.cpu.dcache.ReadReq\_misses::cpu.data 1346 # number of ReadReq misses

system.cpu.dcache.ReadReq\_misses::total 1346 # number of ReadReq misses

system.cpu.dcache.WriteReq\_misses::cpu.data 454 # number of WriteReq misses

system.cpu.dcache.WriteReq\_misses::total 454 # number of WriteReq misses

system.cpu.dcache.LoadLockedReq\_misses::cpu.data 2 # number of LoadLockedReq misses

system.cpu.dcache.LoadLockedReq\_misses::total 2 # number of LoadLockedReq misses

system.cpu.dcache.demand\_misses::cpu.data 1800 # number of demand (read+write) misses

system.cpu.dcache.demand\_misses::total 1800 # number of demand (read+write) misses

system.cpu.dcache.overall\_misses::cpu.data 1800 # number of overall misses

system.cpu.dcache.overall\_misses::total 1800 # number of overall misses

system.cpu.dcache.ReadReq\_miss\_latency::cpu.data 96848000 # number of ReadReq miss cycles

system.cpu.dcache.ReadReq\_miss\_latency::total 96848000 # number of ReadReq miss cycles

system.cpu.dcache.WriteReq\_miss\_latency::cpu.data 27248490 # number of WriteReq miss cycles

system.cpu.dcache.WriteReq\_miss\_latency::total 27248490 # number of WriteReq miss cycles

system.cpu.dcache.LoadLockedReq\_miss\_latency::cpu.data 127500 # number of LoadLockedReq miss cycles

system.cpu.dcache.LoadLockedReq\_miss\_latency::total 127500 # number of LoadLockedReq miss cycles

system.cpu.dcache.demand\_miss\_latency::cpu.data 124096490 # number of demand (read+write) miss cycles

system.cpu.dcache.demand\_miss\_latency::total 124096490 # number of demand (read+write) miss cycles

system.cpu.dcache.overall\_miss\_latency::cpu.data 124096490 # number of overall miss cycles

system.cpu.dcache.overall\_miss\_latency::total 124096490 # number of overall miss cycles

system.cpu.dcache.ReadReq\_accesses::cpu.data 1473984 # number of ReadReq accesses(hits+misses)

system.cpu.dcache.ReadReq\_accesses::total 1473984 # number of ReadReq accesses(hits+misses)

system.cpu.dcache.WriteReq\_accesses::cpu.data 883602 # number of WriteReq accesses(hits+misses)

system.cpu.dcache.WriteReq\_accesses::total 883602 # number of WriteReq accesses(hits+misses)

system.cpu.dcache.LoadLockedReq\_accesses::cpu.data 4946 # number of LoadLockedReq accesses(hits+misses)

system.cpu.dcache.LoadLockedReq\_accesses::total 4946 # number of LoadLockedReq accesses(hits+misses)

system.cpu.dcache.StoreCondReq\_accesses::cpu.data 4946 # number of StoreCondReq accesses(hits+misses)

system.cpu.dcache.StoreCondReq\_accesses::total 4946 # number of StoreCondReq accesses(hits+misses)

system.cpu.dcache.demand\_accesses::cpu.data 2357586 # number of demand (read+write) accesses

system.cpu.dcache.demand\_accesses::total 2357586 # number of demand (read+write) accesses

system.cpu.dcache.overall\_accesses::cpu.data 2357586 # number of overall (read+write) accesses

system.cpu.dcache.overall\_accesses::total 2357586 # number of overall (read+write) accesses

system.cpu.dcache.ReadReq\_miss\_rate::cpu.data 0.000913 # miss rate for ReadReq accesses

system.cpu.dcache.ReadReq\_miss\_rate::total 0.000913 # miss rate for ReadReq accesses

system.cpu.dcache.WriteReq\_miss\_rate::cpu.data 0.000514 # miss rate for WriteReq accesses

system.cpu.dcache.WriteReq\_miss\_rate::total 0.000514 # miss rate for WriteReq accesses

system.cpu.dcache.LoadLockedReq\_miss\_rate::cpu.data 0.000404 # miss rate for LoadLockedReq accesses

system.cpu.dcache.LoadLockedReq\_miss\_rate::total 0.000404 # miss rate for LoadLockedReq accesses

system.cpu.dcache.demand\_miss\_rate::cpu.data 0.000763 # miss rate for demand accesses

system.cpu.dcache.demand\_miss\_rate::total 0.000763 # miss rate for demand accesses

system.cpu.dcache.overall\_miss\_rate::cpu.data 0.000763 # miss rate for overall accesses

system.cpu.dcache.overall\_miss\_rate::total 0.000763 # miss rate for overall accesses

system.cpu.dcache.ReadReq\_avg\_miss\_latency::cpu.data 71952.451709 # average ReadReq miss latency

system.cpu.dcache.ReadReq\_avg\_miss\_latency::total 71952.451709 # average ReadReq miss latency

system.cpu.dcache.WriteReq\_avg\_miss\_latency::cpu.data 60018.700441 # average WriteReq miss latency

system.cpu.dcache.WriteReq\_avg\_miss\_latency::total 60018.700441 # average WriteReq miss latency

system.cpu.dcache.LoadLockedReq\_avg\_miss\_latency::cpu.data 63750 # average LoadLockedReq miss latency

system.cpu.dcache.LoadLockedReq\_avg\_miss\_latency::total 63750 # average LoadLockedReq miss latency

system.cpu.dcache.demand\_avg\_miss\_latency::cpu.data 68942.494444 # average overall miss latency

system.cpu.dcache.demand\_avg\_miss\_latency::total 68942.494444 # average overall miss latency

system.cpu.dcache.overall\_avg\_miss\_latency::cpu.data 68942.494444 # average overall miss latency

system.cpu.dcache.overall\_avg\_miss\_latency::total 68942.494444 # average overall miss latency

system.cpu.dcache.blocked\_cycles::no\_mshrs 1370 # number of cycles access was blocked

system.cpu.dcache.blocked\_cycles::no\_targets 0 # number of cycles access was blocked

system.cpu.dcache.blocked::no\_mshrs 26 # number of cycles access was blocked

system.cpu.dcache.blocked::no\_targets 0 # number of cycles access was blocked

system.cpu.dcache.avg\_blocked\_cycles::no\_mshrs 52.692308 # average number of cycles each access was blocked

system.cpu.dcache.avg\_blocked\_cycles::no\_targets nan # average number of cycles each access was blocked

system.cpu.dcache.writebacks::writebacks 36 # number of writebacks

system.cpu.dcache.writebacks::total 36 # number of writebacks

system.cpu.dcache.ReadReq\_mshr\_hits::cpu.data 646 # number of ReadReq MSHR hits

system.cpu.dcache.ReadReq\_mshr\_hits::total 646 # number of ReadReq MSHR hits

system.cpu.dcache.WriteReq\_mshr\_hits::cpu.data 341 # number of WriteReq MSHR hits

system.cpu.dcache.WriteReq\_mshr\_hits::total 341 # number of WriteReq MSHR hits

system.cpu.dcache.demand\_mshr\_hits::cpu.data 987 # number of demand (read+write) MSHR hits

system.cpu.dcache.demand\_mshr\_hits::total 987 # number of demand (read+write) MSHR hits

system.cpu.dcache.overall\_mshr\_hits::cpu.data 987 # number of overall MSHR hits

system.cpu.dcache.overall\_mshr\_hits::total 987 # number of overall MSHR hits

system.cpu.dcache.ReadReq\_mshr\_misses::cpu.data 700 # number of ReadReq MSHR misses

system.cpu.dcache.ReadReq\_mshr\_misses::total 700 # number of ReadReq MSHR misses

system.cpu.dcache.WriteReq\_mshr\_misses::cpu.data 113 # number of WriteReq MSHR misses

system.cpu.dcache.WriteReq\_mshr\_misses::total 113 # number of WriteReq MSHR misses

system.cpu.dcache.LoadLockedReq\_mshr\_misses::cpu.data 2 # number of LoadLockedReq MSHR misses

system.cpu.dcache.LoadLockedReq\_mshr\_misses::total 2 # number of LoadLockedReq MSHR misses

system.cpu.dcache.demand\_mshr\_misses::cpu.data 813 # number of demand (read+write) MSHR misses

system.cpu.dcache.demand\_mshr\_misses::total 813 # number of demand (read+write) MSHR misses

system.cpu.dcache.overall\_mshr\_misses::cpu.data 813 # number of overall MSHR misses

system.cpu.dcache.overall\_mshr\_misses::total 813 # number of overall MSHR misses

system.cpu.dcache.ReadReq\_mshr\_miss\_latency::cpu.data 57655500 # number of ReadReq MSHR miss cycles

system.cpu.dcache.ReadReq\_mshr\_miss\_latency::total 57655500 # number of ReadReq MSHR miss cycles

system.cpu.dcache.WriteReq\_mshr\_miss\_latency::cpu.data 7573000 # number of WriteReq MSHR miss cycles

system.cpu.dcache.WriteReq\_mshr\_miss\_latency::total 7573000 # number of WriteReq MSHR miss cycles

system.cpu.dcache.LoadLockedReq\_mshr\_miss\_latency::cpu.data 125500 # number of LoadLockedReq MSHR miss cycles

system.cpu.dcache.LoadLockedReq\_mshr\_miss\_latency::total 125500 # number of LoadLockedReq MSHR miss cycles

system.cpu.dcache.demand\_mshr\_miss\_latency::cpu.data 65228500 # number of demand (read+write) MSHR miss cycles

system.cpu.dcache.demand\_mshr\_miss\_latency::total 65228500 # number of demand (read+write) MSHR miss cycles

system.cpu.dcache.overall\_mshr\_miss\_latency::cpu.data 65228500 # number of overall MSHR miss cycles

system.cpu.dcache.overall\_mshr\_miss\_latency::total 65228500 # number of overall MSHR miss cycles

system.cpu.dcache.ReadReq\_mshr\_miss\_rate::cpu.data 0.000475 # mshr miss rate for ReadReq accesses

system.cpu.dcache.ReadReq\_mshr\_miss\_rate::total 0.000475 # mshr miss rate for ReadReq accesses

system.cpu.dcache.WriteReq\_mshr\_miss\_rate::cpu.data 0.000128 # mshr miss rate for WriteReq accesses

system.cpu.dcache.WriteReq\_mshr\_miss\_rate::total 0.000128 # mshr miss rate for WriteReq accesses

system.cpu.dcache.LoadLockedReq\_mshr\_miss\_rate::cpu.data 0.000404 # mshr miss rate for LoadLockedReq accesses

system.cpu.dcache.LoadLockedReq\_mshr\_miss\_rate::total 0.000404 # mshr miss rate for LoadLockedReq accesses

system.cpu.dcache.demand\_mshr\_miss\_rate::cpu.data 0.000345 # mshr miss rate for demand accesses

system.cpu.dcache.demand\_mshr\_miss\_rate::total 0.000345 # mshr miss rate for demand accesses

system.cpu.dcache.overall\_mshr\_miss\_rate::cpu.data 0.000345 # mshr miss rate for overall accesses

system.cpu.dcache.overall\_mshr\_miss\_rate::total 0.000345 # mshr miss rate for overall accesses

system.cpu.dcache.ReadReq\_avg\_mshr\_miss\_latency::cpu.data 82365 # average ReadReq mshr miss latency

system.cpu.dcache.ReadReq\_avg\_mshr\_miss\_latency::total 82365 # average ReadReq mshr miss latency

system.cpu.dcache.WriteReq\_avg\_mshr\_miss\_latency::cpu.data 67017.699115 # average WriteReq mshr miss latency

system.cpu.dcache.WriteReq\_avg\_mshr\_miss\_latency::total 67017.699115 # average WriteReq mshr miss latency

system.cpu.dcache.LoadLockedReq\_avg\_mshr\_miss\_latency::cpu.data 62750 # average LoadLockedReq mshr miss latency

system.cpu.dcache.LoadLockedReq\_avg\_mshr\_miss\_latency::total 62750 # average LoadLockedReq mshr miss latency

system.cpu.dcache.demand\_avg\_mshr\_miss\_latency::cpu.data 80231.857319 # average overall mshr miss latency

system.cpu.dcache.demand\_avg\_mshr\_miss\_latency::total 80231.857319 # average overall mshr miss latency

system.cpu.dcache.overall\_avg\_mshr\_miss\_latency::cpu.data 80231.857319 # average overall mshr miss latency

system.cpu.dcache.overall\_avg\_mshr\_miss\_latency::total 80231.857319 # average overall mshr miss latency

system.cpu.icache.tags.pwrStateResidencyTicks::UNDEFINED 4277042500 # Cumulative time (in ticks) in various power states

system.cpu.icache.tags.replacements 42919 # number of replacements

system.cpu.icache.tags.tagsinuse 490.411652 # Cycle average of tags in use

system.cpu.icache.tags.total\_refs 1674068 # Total number of references to valid blocks.

system.cpu.icache.tags.sampled\_refs 43421 # Sample count of references to valid blocks.

system.cpu.icache.tags.avg\_refs 38.554340 # Average number of references to valid blocks.

system.cpu.icache.tags.warmup\_cycle 77000 # Cycle when the warmup percentage was hit.

system.cpu.icache.tags.occ\_blocks::cpu.inst 490.411652 # Average occupied blocks per requestor

system.cpu.icache.tags.occ\_percent::cpu.inst 0.957835 # Average percentage of cache occupancy

system.cpu.icache.tags.occ\_percent::total 0.957835 # Average percentage of cache occupancy

system.cpu.icache.tags.occ\_task\_id\_blocks::1024 502 # Occupied blocks per task id

system.cpu.icache.tags.age\_task\_id\_blocks\_1024::0 74 # Occupied blocks per task id

system.cpu.icache.tags.age\_task\_id\_blocks\_1024::2 14 # Occupied blocks per task id

system.cpu.icache.tags.age\_task\_id\_blocks\_1024::3 414 # Occupied blocks per task id

system.cpu.icache.tags.occ\_task\_id\_percent::1024 0.980469 # Percentage of cache occupancy per task id

system.cpu.icache.tags.tag\_accesses 3486609 # Number of tag accesses

system.cpu.icache.tags.data\_accesses 3486609 # Number of data accesses

system.cpu.icache.pwrStateResidencyTicks::UNDEFINED 4277042500 # Cumulative time (in ticks) in various power states

system.cpu.icache.ReadReq\_hits::cpu.inst 1674068 # number of ReadReq hits

system.cpu.icache.ReadReq\_hits::total 1674068 # number of ReadReq hits

system.cpu.icache.demand\_hits::cpu.inst 1674068 # number of demand (read+write) hits

system.cpu.icache.demand\_hits::total 1674068 # number of demand (read+write) hits

system.cpu.icache.overall\_hits::cpu.inst 1674068 # number of overall hits

system.cpu.icache.overall\_hits::total 1674068 # number of overall hits

system.cpu.icache.ReadReq\_misses::cpu.inst 47526 # number of ReadReq misses

system.cpu.icache.ReadReq\_misses::total 47526 # number of ReadReq misses

system.cpu.icache.demand\_misses::cpu.inst 47526 # number of demand (read+write) misses

system.cpu.icache.demand\_misses::total 47526 # number of demand (read+write) misses

system.cpu.icache.overall\_misses::cpu.inst 47526 # number of overall misses

system.cpu.icache.overall\_misses::total 47526 # number of overall misses

system.cpu.icache.ReadReq\_miss\_latency::cpu.inst 2295681500 # number of ReadReq miss cycles

system.cpu.icache.ReadReq\_miss\_latency::total 2295681500 # number of ReadReq miss cycles

system.cpu.icache.demand\_miss\_latency::cpu.inst 2295681500 # number of demand (read+write) miss cycles

system.cpu.icache.demand\_miss\_latency::total 2295681500 # number of demand (read+write) miss cycles

system.cpu.icache.overall\_miss\_latency::cpu.inst 2295681500 # number of overall miss cycles

system.cpu.icache.overall\_miss\_latency::total 2295681500 # number of overall miss cycles

system.cpu.icache.ReadReq\_accesses::cpu.inst 1721594 # number of ReadReq accesses(hits+misses)

system.cpu.icache.ReadReq\_accesses::total 1721594 # number of ReadReq accesses(hits+misses)

system.cpu.icache.demand\_accesses::cpu.inst 1721594 # number of demand (read+write) accesses

system.cpu.icache.demand\_accesses::total 1721594 # number of demand (read+write) accesses

system.cpu.icache.overall\_accesses::cpu.inst 1721594 # number of overall (read+write) accesses

system.cpu.icache.overall\_accesses::total 1721594 # number of overall (read+write) accesses

system.cpu.icache.ReadReq\_miss\_rate::cpu.inst 0.027606 # miss rate for ReadReq accesses

system.cpu.icache.ReadReq\_miss\_rate::total 0.027606 # miss rate for ReadReq accesses

system.cpu.icache.demand\_miss\_rate::cpu.inst 0.027606 # miss rate for demand accesses

system.cpu.icache.demand\_miss\_rate::total 0.027606 # miss rate for demand accesses

system.cpu.icache.overall\_miss\_rate::cpu.inst 0.027606 # miss rate for overall accesses

system.cpu.icache.overall\_miss\_rate::total 0.027606 # miss rate for overall accesses

system.cpu.icache.ReadReq\_avg\_miss\_latency::cpu.inst 48303.696924 # average ReadReq miss latency

system.cpu.icache.ReadReq\_avg\_miss\_latency::total 48303.696924 # average ReadReq miss latency

system.cpu.icache.demand\_avg\_miss\_latency::cpu.inst 48303.696924 # average overall miss latency

system.cpu.icache.demand\_avg\_miss\_latency::total 48303.696924 # average overall miss latency

system.cpu.icache.overall\_avg\_miss\_latency::cpu.inst 48303.696924 # average overall miss latency

system.cpu.icache.overall\_avg\_miss\_latency::total 48303.696924 # average overall miss latency

system.cpu.icache.blocked\_cycles::no\_mshrs 688 # number of cycles access was blocked

system.cpu.icache.blocked\_cycles::no\_targets 0 # number of cycles access was blocked

system.cpu.icache.blocked::no\_mshrs 8 # number of cycles access was blocked

system.cpu.icache.blocked::no\_targets 0 # number of cycles access was blocked

system.cpu.icache.avg\_blocked\_cycles::no\_mshrs 86 # average number of cycles each access was blocked

system.cpu.icache.avg\_blocked\_cycles::no\_targets nan # average number of cycles each access was blocked

system.cpu.icache.writebacks::writebacks 42919 # number of writebacks

system.cpu.icache.writebacks::total 42919 # number of writebacks

system.cpu.icache.ReadReq\_mshr\_hits::cpu.inst 4104 # number of ReadReq MSHR hits

system.cpu.icache.ReadReq\_mshr\_hits::total 4104 # number of ReadReq MSHR hits

system.cpu.icache.demand\_mshr\_hits::cpu.inst 4104 # number of demand (read+write) MSHR hits

system.cpu.icache.demand\_mshr\_hits::total 4104 # number of demand (read+write) MSHR hits

system.cpu.icache.overall\_mshr\_hits::cpu.inst 4104 # number of overall MSHR hits

system.cpu.icache.overall\_mshr\_hits::total 4104 # number of overall MSHR hits

system.cpu.icache.ReadReq\_mshr\_misses::cpu.inst 43422 # number of ReadReq MSHR misses

system.cpu.icache.ReadReq\_mshr\_misses::total 43422 # number of ReadReq MSHR misses

system.cpu.icache.demand\_mshr\_misses::cpu.inst 43422 # number of demand (read+write) MSHR misses

system.cpu.icache.demand\_mshr\_misses::total 43422 # number of demand (read+write) MSHR misses

system.cpu.icache.overall\_mshr\_misses::cpu.inst 43422 # number of overall MSHR misses

system.cpu.icache.overall\_mshr\_misses::total 43422 # number of overall MSHR misses

system.cpu.icache.ReadReq\_mshr\_miss\_latency::cpu.inst 2075659500 # number of ReadReq MSHR miss cycles

system.cpu.icache.ReadReq\_mshr\_miss\_latency::total 2075659500 # number of ReadReq MSHR miss cycles

system.cpu.icache.demand\_mshr\_miss\_latency::cpu.inst 2075659500 # number of demand (read+write) MSHR miss cycles

system.cpu.icache.demand\_mshr\_miss\_latency::total 2075659500 # number of demand (read+write) MSHR miss cycles

system.cpu.icache.overall\_mshr\_miss\_latency::cpu.inst 2075659500 # number of overall MSHR miss cycles

system.cpu.icache.overall\_mshr\_miss\_latency::total 2075659500 # number of overall MSHR miss cycles

system.cpu.icache.ReadReq\_mshr\_miss\_rate::cpu.inst 0.025222 # mshr miss rate for ReadReq accesses

system.cpu.icache.ReadReq\_mshr\_miss\_rate::total 0.025222 # mshr miss rate for ReadReq accesses

system.cpu.icache.demand\_mshr\_miss\_rate::cpu.inst 0.025222 # mshr miss rate for demand accesses

system.cpu.icache.demand\_mshr\_miss\_rate::total 0.025222 # mshr miss rate for demand accesses

system.cpu.icache.overall\_mshr\_miss\_rate::cpu.inst 0.025222 # mshr miss rate for overall accesses

system.cpu.icache.overall\_mshr\_miss\_rate::total 0.025222 # mshr miss rate for overall accesses

system.cpu.icache.ReadReq\_avg\_mshr\_miss\_latency::cpu.inst 47802.024319 # average ReadReq mshr miss latency

system.cpu.icache.ReadReq\_avg\_mshr\_miss\_latency::total 47802.024319 # average ReadReq mshr miss latency

system.cpu.icache.demand\_avg\_mshr\_miss\_latency::cpu.inst 47802.024319 # average overall mshr miss latency

system.cpu.icache.demand\_avg\_mshr\_miss\_latency::total 47802.024319 # average overall mshr miss latency

system.cpu.icache.overall\_avg\_mshr\_miss\_latency::cpu.inst 47802.024319 # average overall mshr miss latency

system.cpu.icache.overall\_avg\_mshr\_miss\_latency::total 47802.024319 # average overall mshr miss latency

system.membus.snoop\_filter.tot\_requests 87317 # Total number of requests made to the snoop filter.

system.membus.snoop\_filter.hit\_single\_requests 43081 # Number of requests hitting in the snoop filter with a single holder of the requested data.

system.membus.snoop\_filter.hit\_multi\_requests 0 # Number of requests hitting in the snoop filter with multiple (>1) holders of the requested data.

system.membus.snoop\_filter.tot\_snoops 0 # Total number of snoops made to the snoop filter.

system.membus.snoop\_filter.hit\_single\_snoops 0 # Number of snoops hitting in the snoop filter with a single holder of the requested data.

system.membus.snoop\_filter.hit\_multi\_snoops 0 # Number of snoops hitting in the snoop filter with multiple (>1) holders of the requested data.

system.membus.pwrStateResidencyTicks::UNDEFINED 4277042500 # Cumulative time (in ticks) in various power states

system.membus.trans\_dist::ReadResp 44123 # Transaction distribution

system.membus.trans\_dist::WritebackDirty 36 # Transaction distribution

system.membus.trans\_dist::WritebackClean 42919 # Transaction distribution

system.membus.trans\_dist::CleanEvict 125 # Transaction distribution

system.membus.trans\_dist::ReadExReq 113 # Transaction distribution

system.membus.trans\_dist::ReadExResp 113 # Transaction distribution

system.membus.trans\_dist::ReadCleanReq 43422 # Transaction distribution

system.membus.trans\_dist::ReadSharedReq 702 # Transaction distribution

system.membus.pkt\_count\_system.cpu.icache.mem\_side::system.mem\_ctrls.port 129762 # Packet count per connected master and slave (bytes)

system.membus.pkt\_count\_system.cpu.dcache.mem\_side::system.mem\_ctrls.port 1791 # Packet count per connected master and slave (bytes)

system.membus.pkt\_count::total 131553 # Packet count per connected master and slave (bytes)

system.membus.pkt\_size\_system.cpu.icache.mem\_side::system.mem\_ctrls.port 5525760 # Cumulative packet size per connected master and slave (bytes)

system.membus.pkt\_size\_system.cpu.dcache.mem\_side::system.mem\_ctrls.port 54464 # Cumulative packet size per connected master and slave (bytes)

system.membus.pkt\_size::total 5580224 # Cumulative packet size per connected master and slave (bytes)

system.membus.snoops 0 # Total snoops (count)

system.membus.snoopTraffic 0 # Total snoop traffic (bytes)

system.membus.snoop\_fanout::samples 44237 # Request fanout histogram

system.membus.snoop\_fanout::mean 0.000023 # Request fanout histogram

system.membus.snoop\_fanout::stdev 0.004755 # Request fanout histogram

system.membus.snoop\_fanout::underflows 0 0.00% 0.00% # Request fanout histogram

system.membus.snoop\_fanout::0 44236 100.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::1 1 0.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::2 0 0.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::overflows 0 0.00% 100.00% # Request fanout histogram

system.membus.snoop\_fanout::min\_value 0 # Request fanout histogram

system.membus.snoop\_fanout::max\_value 1 # Request fanout histogram

system.membus.snoop\_fanout::total 44237 # Request fanout histogram

system.membus.reqLayer0.occupancy 264152000 # Layer occupancy (ticks)

system.membus.reqLayer0.utilization 6.2 # Layer utilization (%)

system.membus.respLayer1.occupancy 223837987 # Layer occupancy (ticks)

system.membus.respLayer1.utilization 5.2 # Layer utilization (%)

system.membus.respLayer2.occupancy 4405250 # Layer occupancy (ticks)

system.membus.respLayer2.utilization 0.1 # Layer utilization (%)

---------- End Simulation Statistics ----------