Kleanthis Papachatzopoulos

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Last Updated:	06/2023

Personal Objective

Applying for the role of **Digital IC Design Engineer**; experienced in digital implementations of communication and signal processing algorithms for various ASIC and FPGA flows; accustomed to handling deadline-oriented responsibilities.

Education

Sept. 2019- End 2023 (exp.)	**PhD Cand.**, Electrical and Computer Engineering Dept., University of Patras, GR • **Thesis: "*Circuits and Systems in the Presence of Variability,*"** supervised by Prof. V. Paliouras, ECE Dept., University of Patras, GR • Contributed variation-aware statistical models for the performance of ripple-carry, borrow-save, and parallel-prefix adders [J1, J2] • Proposed borrow-save- and RNS-based arithmetic architectures as variation-tolerant alternatives to conventional binary counterparts [J4, C1, C2]
2016 - Oct. 2018	**MSc**, Hardware-Software Integrated Systems, Electrical and Computer Engineering Dept., and Computer Engineering and Informatics Dept., University of Patras, GR • GPA: 9.53/10
2010 - April 2016	**Diploma** (300 ECTS), Electrical and Computer Engineering Dept., Un. of Patras • GPA: 8.75/10 **(top 2%)** • Major: Electronics and Computers

Professional Experience

June 2021 - Jan. 2022	**IC Designer, Un. of Patras, Project: *"Firmware and digital design development of an FPGA tester for Mezzanine cards,"* funded by the industry** • Developed the PHY layer for a custom 8b10b protocol - asynchronous oversampling techniques at 640/320 Mbps based on SERDES for a Zynq-based (XILINX) SOM • Firmware development, connection of custom IPs with an integrated Cortex-A9 ARM CPU using various AXI interfaces • Configured DACs and ADCs peripherals using SPI and UART protocols, and verified using digital oscilloscope
Dec. 2018 - Dec. 2021	**Research Assistant, Un. of Patras, Project: "*HIDIT: Highly Integrated Digital Transmitter for System-on-Chip,*" funded by NSRF** • Developed a digital baseband DSP based on broadcast transmission scheme compatible with Bluetooth Low Energy v5.0

         • Synthesis, place and route of baseband DSP at 28-nm FDSOI Samsung technology
         • Proposed noise-shaping binary-to-stochastic converters for digital stochastic filtering applications

Jul. 2018 - Sept. 2018	**Research Assistant, Un. of Patras, Project:** *"Evaluation of FPGA interconnection techniques with a System-in Package that includes an array of chips,"* **funded by the industry** • Evaluated and extracted interconnections specifications for the system under study • Design verification and HDL testbenches development for the core sub-systems • Implemented a prototype in a HITECH GLOBAL HTG-V5-330-PCIE FPGA
Oct. 2016 - March 2017	**Research Assistant, Inria, Cairn Team, University of Rennes 1, France, funded by the French Defense Procurement Agency (DGA)** • Study of soft-error-resilient digital system architectures, mainly targeting soft-core processors • Classification of hardware and software soft-error-tolerance techniques concerning to digital circuits and systems

Additional Experience

Jan. 2020 - Sept. 2021	**IC Designer, VLSI Lab., ECE Dept., Un. of Patras, Project:** *"SmartPV"* • Led HDL lint checking, synthesis and implementation of various digital blocks at an 180-nm XFAB standard-cell library for several tapeouts • Managed floorplanning and interconnection of digital blocks with analog blocks • Verification of manufactured chips using digital logic analyzers • Cross-validation with an FPGA prototype
Sept. 2016- Present	**Researcher and Teaching Assistant, ECE Dept., Un. of Patras, GR** • *Teaching Assistant:* VLSI Design I/II, DSP lab courses • *Co-Author/Speaker:* IEEE ISCAS 2022-2020/2018/2016, MOCAST 2016 • *Reviewer*: IEEE TCAS–I, TCAS–II, IEEE TETC, IEEE VLSI SOC/ISCAS

Technical Skills

• Experienced with ASIC design and physical implementation using Cadence digital tool suite
• Skilled in Vivado digital design flow, synthesis-implementation-debugging with Hardware Manager, and familiarized with SoC architectures
• Engaged with digital filter design and fixed-point arithmetic optimizations on C6711 Board, TI

Programming Skills	Assembly (MIPS, Intel 8085, Intel 80x86 family, TI C67xx family), C, Python, MATLAB, Mathematica, TCL
HDL	VHDL, Verilog
Design/Sim. Tools	Vivado (XILINX), ModelSim (Mentor Graphics), Spice (Eldo, Spectre, NGSPICE), HDL Designer
Certifications	Advanced Synthesis with Genus Stylus Common UI v19.1 Exam Test Synthesis with Genus Stylus Common UI Genus v19.1 Exam Innovus Implementation System (Block) v19.1 Exam Innovus Implementation System (Hierarchical) v19.1 Exam Tempus Signoff Timing Analysis and Closure v19.1 Exam IBM Blockchain Essentials
Others	LaTeX, Microsoft Office, Libre Office

Languages

English	Certificate of Proficiency in English (ECPE) C2, University of Michigan, HAU
German	Goethe-Zertifikat B1, Zertifikat Deutsch, Goethe-Institut

Honors and Awards

2018	**Best student paper award finalist, IEEE ISCAS 2018**
2018	**Award of academic excellence** from the **Technical Chamber of Greece** for my performance during undergraduate studies
2017	**Award of academic excellence** from **Limmat Foundation** for the acquisition of 3rd highest GPA in 2016
2011-2012	**Scholarships** by the **Greek State Scholarships Foundation (IKY)** for my performance and conduct during the first and second academic years

Publications

International Journals

[J1] **K. Papachatzopoulos** and V. Paliouras, "Path-Based Delay Variation Models for Parallel-Prefix Adders," *IEEE Transactions on Emerging Topics in Computing*, 2023.

[J2] ——, "Static Delay Variation Models for Ripple-Carry and Borrow-Save Adders," *IEEE Transactions on Circuits and Systems—Part I: Regular Papers*, vol. 66, no. 7, pp. 2546–2559, 2019.

[J3] G. Dimitrakopoulos, **K. Papachatzopoulos**, and V. Paliouras, "Sum Propagate Adders," *IEEE Transactions on Emerging Topics in Computing, Special Section on Emerging and Impacting Trends on Computer Arithmetic*, no. 01, pp. 1–1, 2021.

[J4] **K. Papachatzopoulos** and V. Paliouras, "Low-Power Addition with Borrow-Save Adders under Threshold Voltage Variability," *IEEE Transactions on Circuits and Systems—Part II: Express Briefs*, vol. 65, no. 5, pp. 572–576, 2018, Journal Special Issue on IEEE ISCAS 2018.

[J5] ——, "Noise-Shaping Binary-to-Stochastic Converters for Reduced-Length Bit-Streams," *IEEE Transactions on Emerging Topics in Computing*, under review.

Conferences

[C1] **K. Papachatzopoulos**, I. Kouretas, and V. Paliouras, "Dynamic Delay Variation Behaviour of RNS Multiply-Add Architectures," in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*.   IEEE, 2016, pp. 1978–1981.

[C2] **K. Papachatzopoulos** and V. Paliouras, "Reduction of Delay Variations in Arithmetic Circuits Using a Redundant Representation," in *2016 5th International Conference on Modern Circuits and Systems Technologies (MOCAST)*.   IEEE, 2016, pp. 1–4.

[C3] ——, "Sensitivity to Threshold Voltage Variations of Exact and Incomplete Prefix Addition Trees," in *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*.   IEEE, 2022, pp. 924–928.

[C4] C. Andriakopoulos, **K. Papachatzopoulos**, and V. Paliouras, "A Novel Stochastic Polar Architecture for All-Digital Transmission," in *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*.   IEEE, 2021, pp. 1–5.

[C5] **K. Papachatzopoulos** and V. Paliouras, "Maximum Delay Models for Parallel-Prefix Adders in the Presence of Threshold Voltage Variations," in *2020 IEEE 27th Symposium on Computer Arithmetic (ARITH).* IEEE Computer Society, 2020, pp. 88–95.

[C6] **K. Papachatzopoulos**, C. Andriakopoulos, and V. Paliouras, "Novel Noise-Shaping Stochastic-Computing Converters for Digital Filtering," in *2020 IEEE International Symposium on Circuits and Systems (ISCAS).* IEEE, 2020, pp. 1–5.

References

Professor Vassilis Paliouras

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