

# KLEANTHIS PAPACHATZOPOULOS

---



Date of Birth: 23/04/1992  
Nationality: Greek  
Address: 5 Strimonos, 26442, Patras, GR  
Mobile: +30 6947839459  
E-mail: [papachatz@ece.upatras.gr](mailto:papachatz@ece.upatras.gr)  
LinkedIn: [www.linkedin.com/in/kleanthis-papachatzopoulos](https://www.linkedin.com/in/kleanthis-papachatzopoulos)  
Last Updated: 06/2023

## PERSONAL OBJECTIVE

Applying for the role of **Digital IC Design Engineer**; experienced in digital implementations of communication and signal processing algorithms for various ASIC and FPGA flows; accustomed to handling deadline-oriented responsibilities.

## EDUCATION

Sept. 2019- End 2023 (exp.)	<b>PhD Cand.</b> , Electrical and Computer Engineering Dept., University of Patras, GR • <b>Thesis:</b> “ <i>Circuits and Systems in the Presence of Variability</i> ,” supervised by Prof. V. Paliouras, ECE Dept., University of Patras, GR • Contributed variation-aware statistical models for the performance of ripple-carry, borrow-save, and parallel-prefix adders [J1, J2] • Proposed borrow-save and RNS-based arithmetic architectures as variation-tolerant alternatives to conventional binary counterparts [J4, C1, C2]
2016 - Oct. 2018	<b>MSc</b> , Hardware-Software Integrated Systems, Electrical and Computer Engineering Dept., and Computer Engineering and Informatics Dept., University of Patras, GR • GPA: 9.53/10
2010 - April 2016	<b>Diploma</b> (300 ECTS), Electrical and Computer Engineering Dept., Un. of Patras • GPA: 8.75/10 ( <b>top 2%</b> ) • Major: Electronics and Computers

## PROFESSIONAL EXPERIENCE

June 2021 - Jan. 2022	<b>IC Designer, Un. of Patras, Project:</b> “ <i>Firmware and digital design development of an FPGA tester for Mezzanine cards</i> ,” funded by the industry • Developed the PHY layer for a custom 8b10b protocol - asynchronous oversampling techniques at 640/320 Mbps based on SERDES for a Zynq-based (XILINX) SOM • Firmware development, connection of custom IPs with an integrated Cortex-A9 ARM CPU and DDR memory using various AXI interfaces and DMA controllers • Configured DACs and ADCs peripherals using SPI and UART protocols, and verified using digital oscilloscope
Dec. 2018 - Dec. 2021	<b>Research Assistant, Un. of Patras, Project:</b> “ <i>HIDIT: Highly Integrated Digital Transmitter for System-on-Chip</i> ,” funded by NSRF • Developed a digital baseband DSP based on broadcast transmission scheme compatible with Bluetooth Low Energy v5.0

	<ul style="list-style-type: none"> <li>• Synthesis, place and route of baseband DSP at 28-nm FDSOI Samsung technology</li> <li>• Proposed noise-shaping binary-to-stochastic converters for digital stochastic filtering applications</li> </ul>
Jul. 2018 - Sept. 2018	<b>Research Assistant, Un. of Patras, Project: “<i>Evaluation of FPGA interconnection techniques with a System-in Package that includes an array of chips</i>,” funded by the industry</b> <ul style="list-style-type: none"> <li>• Evaluated and extracted interconnections specifications for the system under study</li> <li>• Design verification and HDL testbenches development for the core sub-systems</li> <li>• Implemented a prototype in a HITECH GLOBAL HTG-V5-330-PCIE FPGA</li> </ul>
Oct. 2016 - March 2017	<b>Research Assistant, Inria, Cairn Team, University of Rennes 1, France, funded by the French Defense Procurement Agency (DGA)</b> <ul style="list-style-type: none"> <li>• Study of soft-error-resilient digital system architectures, mainly targeting soft-core processors</li> <li>• Classification of hardware and software soft-error-tolerance techniques concerning to digital circuits and systems</li> </ul>

## ADDITIONAL EXPERIENCE

Jan. 2020 - Sept. 2021	<b>IC Designer, VLSI Lab., ECE Dept., Un. of Patras, Project: “<i>SmartPV</i>”</b> <ul style="list-style-type: none"> <li>• Led RTL code linting, equivalence checking, synthesis and implementation of various digital blocks at an XFAB XH018 0.18um CMOS technology for several tapeouts</li> <li>• Managed floorplanning and interconnection of digital blocks with analog blocks</li> <li>• Verification of manufactured chips using digital logic analyzers</li> <li>• Cross-validation with an FPGA prototype</li> </ul>
Sept. 2016- Present	<b>Researcher and Teaching Assistant, ECE Dept., Un. of Patras, GR</b> <ul style="list-style-type: none"> <li>• <i>Teaching Assistant</i>: VLSI Design I/II, DSP lab courses</li> <li>• <i>Co-Author/Speaker</i>: IEEE ISCAS 2022-2020/2018/2016, MOCAS 2016</li> <li>• <i>Reviewer</i>: IEEE TCAS-I, TCAS-II, IEEE TETC, IEEE VLSI SOC/ISCAS</li> </ul>

## TECHNICAL SKILLS

	<ul style="list-style-type: none"> <li>• Experienced with ASIC design and physical implementation using Cadence digital tool suite</li> <li>• Skilled in Vivado digital design flow, synthesis-implementation-debugging with Hardware Manager, and familiarized with SoC architectures</li> <li>• Engaged with digital filter design and fixed-point arithmetic optimizations on C6711 Board, TI</li> </ul>
Programming	Assembly (MIPS, Intel 8085, Intel 80x86 family, TI C67xx family), C, Python,
Skills	MATLAB, Mathematica, TCL
HDL	VHDL, Verilog
Design/Sim.	Vivado (XILINX), ModelSim (Mentor Graphics), Spice (Eldo, Spectre,
Tools	NGSPICE), HDL Designer
Certifications	<a href="#">Advanced Synthesis with Genus Stylus Common UI v19.1 Exam</a> <a href="#">Test Synthesis with Genus Stylus Common UI Genus v19.1 Exam</a> <a href="#">Innovus Implementation System (Block) v19.1 Exam</a> <a href="#">Innovus Implementation System (Hierarchical) v19.1 Exam</a> <a href="#">Tempus Signoff Timing Analysis and Closure v19.1 Exam</a> <a href="#">IBM Blockchain Essentials</a>
Others	L <sup>A</sup> T <sub>E</sub> X, Microsoft Office, Libre Office

## LANGUAGES

English	Certificate of Proficiency in English (ECPE) C2, University of Michigan, HAU
German	Goethe-Zertifikat B1, Zertifikat Deutsch, Goethe-Institut

## HONORS AND AWARDS

2018	<b>Best student paper award finalist, IEEE ISCAS 2018</b>
2018	<b>Award of academic excellence</b> from the <b>Technical Chamber of Greece</b> for my performance during undergraduate studies
2017	<b>Award of academic excellence</b> from <b>Limmat Foundation</b> for the acquisition of 3 <sup>rd</sup> highest GPA in 2016
2011-2012	<b>Scholarships</b> by the <b>Greek State Scholarships Foundation (IKY)</b> for my performance and conduct during the first and second academic years

## PUBLICATIONS

### International Journals

- [J1] **K. Papachatzopoulos** and V. Paliouras, “[Path-Based Delay Variation Models for Parallel-Prefix Adders](#),” *IEEE Transactions on Emerging Topics in Computing*, 2023.
- [J2] —, “[Static Delay Variation Models for Ripple-Carry and Borrow-Save Adders](#),” *IEEE Transactions on Circuits and Systems—Part I: Regular Papers*, vol. 66, no. 7, pp. 2546–2559, 2019.
- [J3] G. Dimitrakopoulos, **K. Papachatzopoulos**, and V. Paliouras, “[Sum Propagate Adders](#),” *IEEE Transactions on Emerging Topics in Computing, Special Section on Emerging and Impacting Trends on Computer Arithmetic*, no. 01, pp. 1–1, 2021.
- [J4] **K. Papachatzopoulos** and V. Paliouras, “[Low-Power Addition with Borrow-Save Adders under Threshold Voltage Variability](#),” *IEEE Transactions on Circuits and Systems—Part II: Express Briefs*, vol. 65, no. 5, pp. 572–576, 2018, Journal Special Issue on IEEE ISCAS 2018.
- [J5] —, “[Noise-Shaping Binary-to-Stochastic Converters for Reduced-Length Bit-Streams](#),” *IEEE Transactions on Emerging Topics in Computing*, under review.

### Conferences

- [C1] **K. Papachatzopoulos**, I. Kouretas, and V. Paliouras, “[Dynamic Delay Variation Behaviour of RNS Multiply-Add Architectures](#),” in *2016 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2016, pp. 1978–1981.
- [C2] **K. Papachatzopoulos** and V. Paliouras, “[Reduction of Delay Variations in Arithmetic Circuits Using a Redundant Representation](#),” in *2016 5th International Conference on Modern Circuits and Systems Technologies (MOCAST)*. IEEE, 2016, pp. 1–4.
- [C3] —, “[Sensitivity to Threshold Voltage Variations of Exact and Incomplete Prefix Addition Trees](#),” in *2022 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2022, pp. 924–928.
- [C4] C. Andriakopoulos, **K. Papachatzopoulos**, and V. Paliouras, “[A Novel Stochastic Polar Architecture for All-Digital Transmission](#),” in *2021 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2021, pp. 1–5.

- [C5] **K. Papachatzopoulos** and V. Paliouras, “[Maximum Delay Models for Parallel-Prefix Adders in the Presence of Threshold Voltage Variations](#),” in *2020 IEEE 27th Symposium on Computer Arithmetic (ARITH)*. IEEE Computer Society, 2020, pp. 88–95.
- [C6] **K. Papachatzopoulos**, C. Andriakopoulos, and V. Paliouras, “[Novel Noise-Shaping Stochastic-Computing Converters for Digital Filtering](#),” in *2020 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE, 2020, pp. 1–5.

## REFERENCES

### Professor Vassilis Paliouras

Electrical and Computer Engineering Dept., University of Patras, Greece

Phone: +30.2610.996446, E-mail: [paliouras@ece.upatras.gr](mailto:paliouras@ece.upatras.gr)