A Novel Stochastic Polar Architecture for All-Digital Transmission

Chris Andriakopoulos, Kleanthis Papachatzopoulos, and Vassilis Paliouras
Electrical and Computer Engineering Department
University of Patras, Patras, Greece
Email: {chrisandriakopoulos, papachatz, paliuras}@ece.upatras.gr

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***Abstract*—A novel architecture of an all-digital transmitter is proposed in this paper, introducing stochastic computation to a single-bit polar topology. The proposed architecture exploits the benefits of stochastic computing to simplify the design of an all-digital transmitter and minimize hardware complexity. Complexity reduction is achieved by implementing a digital oscillator as a cosine function in the stochastic domain instead of resorting to LUT-based or CORDIC-based implementations. An evaluation of the introduced all-digital polar architecture shows that the power spectral density of the transmitted passband signal is similar to that of a conventional transmitter. Synthesis of the proposed stochastic-enabled transmitter at a 28-nm FDSOI technology node reveals its minimal complexity requirements and 87.13% area reduction compared to conventional implementations.**

***Index Terms*—stochastic computing, all-digital transmitters, GFSK modulation, Sigma-Delta modulation**

I. Introduction

Low-power and low-complexity techniques for wireless transceivers are getting crucially important for IoT devices and the corresponding applications [1]–[3]. Therefore, new architectures for all-digital transmitters constitute a large area of research. In this work, we propose a novel stochastic-based polar architecture for all-digital transmission, able to modulate and meet the basic power spectral density (PSD) specifications.

An all-digital transmitter architecture drives directly a RF power amplifier, with no requirements for high-speed and high-resolution RF DACs [4]. The passband signal at the transmitter output is traditionally constructed using analog components such as a voltage-controlled oscillator [1], [2] and a phase-locked loop; all-digital structures rely on digital components such as an all-digital phase-locked loop (ADPLL) [5] in direct digital synthesis (DDS) [3], [6]. Wang *et al.* [5] introduce an ultra-low power ADPLL that outputs a passband signal utilizing a digital-controlled oscillator, and corrects/modulates the phase error by a time-to-digital converter. The direct digital synthesizer (cf. [3], [6]) is an alternative of ADPLL. A DDS consists of a phase generator and a numerical oscillator, widely implemented as a look-up table (LUT). The phase generator is an accumulator, controlled by the frequency command word (FCW), that generates the phase of the carrier and is used to address the cosine LUT to derive the passband signal.

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Several transmitter architectures have been proposed in the literature aiming at improving the efficiency and reducing complexity. These transmitters are based on I/Q, polar or dynamic load [7] modulation techniques and all of them present trade-offs regarding to area complexity, power and bandwidth limitations. An I/Q modulator uses Cartesian modulation, while a polar modulator relies on baseband phase and magnitude to generate the transmit signal. The selection of the transmitter's architecture is guided by the passband signal specifications. For example, I/Q modulation technique is used in wide-band systems such as WCDMA and WLAN [8], while polar modulation is preferred in narrow-band systems such as GSM and EDGE [9]–[11].

In this paper, we propose a novel architecture for an all-digital polar transmitter employing GFSK modulation. The corresponding data are pre-modulated by a Gaussian low-pass filter (LPF), which reshapes the rectangle information pulses into frequency information. This paper builds on the simplicity of stochastic computing hardware to develop a low-complexity all-digital transmitter. In particular, the hardware-costly computation unit for the numerical oscillator, for example implemented as a sine function, is replaced by a stochastic-computation-based equivalent, which implements a stochastic cosine. Alternative architectures employ variations of the CORDIC algorithm [12], [13] for sine/cosine computation and the implementation of polar transmitters [9], [14]. Furthermore, a Sigma-Delta ($\Sigma\Delta$) modulator is eliminated from the proposed architecture, since the transmitted signal is already encoded in a single-bit sequence by the stochastic stream at the cost of increased transmission spectrum noise.

The remainder of the paper is organized as follows: Section II reviews the arithmetic representations in stochastic computing. Section III introduces the architecture of proposed stochastic all-digital transmitter. The transmission characteristics of the proposed architecture are discussed in Section IV, while the respective hardware complexity is discussed in Section V. Finally, conclusions are discussed in Section VI.

II. Stochastic Computing Basics

In stochastic computing, a number x is mapped to a stochastic bit stream $X = x_0x_1 \cdots x_{L-1}$, with $x_i \in \{0, 1\}$,

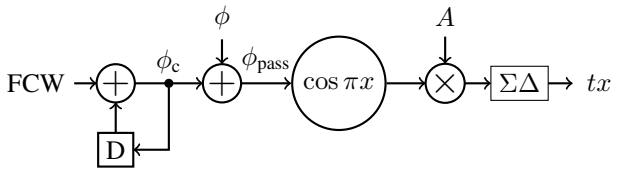

Fig. 1. Baseline all-digital polar transmitter based on direct digital synthesis.

$i = 0, 1, \ldots, L-1$ in such a way that

$$x = \frac{1}{L}\sum_{i=0}^{L-1} x_i, \tag{1}$$

where x is the percentage of bits in X that assume the value of one. Clearly, stochastic representation is non-positional and all bits in bit stream X are of equal weight [15]. Eq. (1) implies that $0 \leq x \leq 1$. The particular straightforward encoding is commonly referred to as *unipolar*. Assume the transformation

$$y = 2x - 1, \tag{2}$$

which maps the interval $[0, 1]$ to the interval $[-1, 1]$. By exploiting the inverse transformation

$$x = \frac{y+1}{2}, \tag{3}$$

a number y, $y \in [-1, 1]$, is initially mapped to x, $x \in [0, 1]$, and subsequently mapped to a stochastic stream, thus effectively encoding y in the so-called *bipolar* encoding. Therefore signed numbers can also be mapped to an appropriately defined bipolar stochastic stream.

Basic arithmetic operations are reduced to single-gate implementations, while efficient techniques have been proposed that allow the computation of more involved arithmetic functions based on polynomial approximations [16]. The particular digital implementations require only a few logic gates. Furthermore, stochastic computations can be performed with no accuracy loss when employing converters based on linear feedback shift registers [17]. Computational latency can also be efficiently reduced for certain digital signal processing systems when employing noise-shaping converters [18].

III. Proposed Stochastic Polar Transmitter

This section introduces the proposed transmitter architecture that constitutes a stochastic alternative of the DDS. Fig. 1 depicts a baseline all-digital transmitter where ϕ denotes the phase of the baseband signal computed by integrating the instantaneous frequency. The oversampled baseband phase ϕ is added to the phase of the carrier, ϕ_c, generated by integrating the FCW in Fig. 1, to form the passband phase, ϕ_{pass}. In a conventional polar architecture this phase is used to address a LUT that stores the corresponding cosine values.

Here, a novel stochastic approach is employed aiming to minimizing the hardware complexity. Specifically, we propose the use of a stochastic circuit that implements the $\cos \pi x$ function, instead of conventional LUT-based or other approximation-based solutions in the binary domain. For the implementation of the DDS, we propose the approximation of $\cos \pi x$. Function $\cos \pi x$ is selected here to implement the stochastic numerical oscillator, instead of the conventional choice of $\sin x$, due to the availability of approximation techniques with sufficient accuracy in the stochastic domain. The advantage of a stochastic implementation of $\cos \pi x$ over other trigonometric functions approximated in the stochastic domain, such as $\sin x$, is that the range offered by the approximation of $\cos \pi x$ is $[-1, 1]$ [16], which is convenient for the polar transmitter.

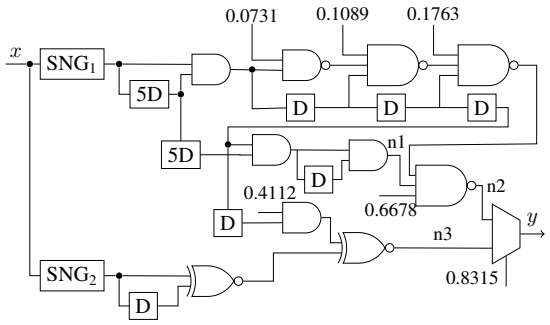

Fig. 2. The circuit diagram of stochastic implementation of $\cos(\pi x)$ using twelfth-order Maclaurin polynomial.

Parhi and Liu introduce approximations and architectures for nonlinear functions such as trigonometric, exponential and sigmoid functions, derived by truncated versions of Maclaurin series expansions [16]. The architecture proposed here, implements a truncated Maclaurin series for $\cos \pi x$, which includes terms up to the twelfth order, since more accuracy than the solution in [16] is required. The adopted approximation is

$$\begin{aligned}\cos \pi x \approx & 1 - \frac{\pi^2 x^2}{2!} + \frac{\pi^4 x^4}{4!} - \frac{\pi^6 x^6}{6!} + \frac{\pi^8 x^8}{8!} \\ & - \frac{\pi^{10} x^{10}}{10!} + \frac{\pi^{12} x^{12}}{12!}.\end{aligned} \tag{4}$$

Eq. (4) is re-expressed by defining $S(x)$ and $R(x)$, as follows

$$\begin{aligned}S(x) &= \frac{\pi^2 x^2}{2!}(2 \cdot \frac{\pi^2 x^2}{24} - 1) \\ &= 4.9348x^2(2 \cdot 0.4112x^2 - 1) = 4.9348 \cdot R(x),\end{aligned} \tag{5}$$

with $R(x) = x^2(2 \cdot 0.4112x^2 - 1)$ and $Q(x)$ as

$$\begin{aligned}Q(x) =& 1 - \frac{\pi^6 x^6}{6!} + \frac{\pi^8 x^8}{8!} - \frac{\pi^{10} x^{10}}{10!} + \frac{\pi^{12} x^{12}}{12!} \\ =& 1 - 2 \cdot 0.6678x^6\big(1 - 0.1763x^2(1 - 0.1089x^2) \cdot \\ & \cdot (1 - 0.0731x^2)\big).\end{aligned} \tag{6}$$

Using (5) and (6), approximation (4) is finally expressed as

$$\cos \pi x \approx Q(x) + 4.9348 \cdot R(x). \tag{7}$$

Using the technique by Parhi and Liu [16], the implementation of $R(x)$ exploits the resemblance to the unipolar-to-bipolar conversion (2). Fig. 2 depicts the corresponding circuit for the stochastic implementation of $\cos \pi x$ following (7). The *SNG* blocks are stochastic number generators which convert x to stochastic representation. Generator SNG_1 produces a unipolar stochastic bit stream, while SNG_2 generates a bipolar stochastic bit stream for the corresponding binary input x. As a result the stream at node *n3* is bipolar, while the stream

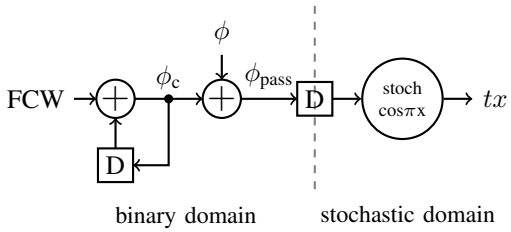

Fig. 3. Proposed implementation of stochastic transmitter.

at node *n2* is interpreted as converted from unipolar *n1* into bipolar format. The final output, y, is the scaled sum in bipolar format. Note that delay elements are used to decorrelate bit streams in the stochastic circuit; every path in Fig. 2 has a unique number of delay elements.

For every sample at the input of the stochastic cosine circuit in Fig. 2, n clock cycles in stochastic domain are required to output the corresponding stochastic word, where n is the length of the stochastic stream. In order to achieve sufficient accuracy of the corresponding stochastic information, the stochastic stream is required to be of sufficient length, namely $\{64, 128, 256, 512\}$ bits.

IV. Characteristics of the Proposed Transmitter

This section compares the proposed and conventional architectures in terms of power spectral estimation (PSE) and BER performance.

A. Power Spectrum for a Test Case

As an illustrative example of the proposed concept, a GFSK modulator front-end and back-end is implemented, the carrier frequency is 150 MHz, the frequency separator is 500 kHz and the sampling ratio is 8. In conventional transmitter architectures, the quantized passband signal is modulated by a $\Sigma\Delta$ modulator, amplified by Class-D amplifier and finally filtered by a bandpass filter (BPF) [4]. A $\Sigma\Delta$ modulator is used in order to transfer the quantization noise out of the band, while BPF removes that noise afterwards.

In the proposed polar transmitter architecture, the LUT is replaced by the unit of stochastic cosine. Furthermore, the $\Sigma\Delta$ modulator is removed, as a single-bit sequence for the transmitted signal is already produced by the stochastic unit. The stochastic stream, output of the stochastic cosine unit, is the transmitted signal, tx, in Fig. 3. The transmitted signal passes through a BPF in order to ensure the transmission remains within a pre-specified spectral mask. The stochastic encoding at the transmitter's output allows for a stochastic-based implementation of the BPF [19] that contributes further to area reduction. The stochastic signal contains a DC component resulting from the truncated polynomial approximation in stochastic domain, eliminated by the band-pass filter. Fig. 4 illustrates the normalized PSE of the transmitted signal when either the conventional or the proposed polar transmitter using the stochastic cosine is utilized. PSE estimation with the proposed transmitter refers to a stream length of 128 bits. Note that at the conventional transmitter, the quantized passband signal is noise-shaped and filtered afterwards.

It is necessary for the proposed transmitter to use a band-pass filter instead of a low-pass filter because the stochastic

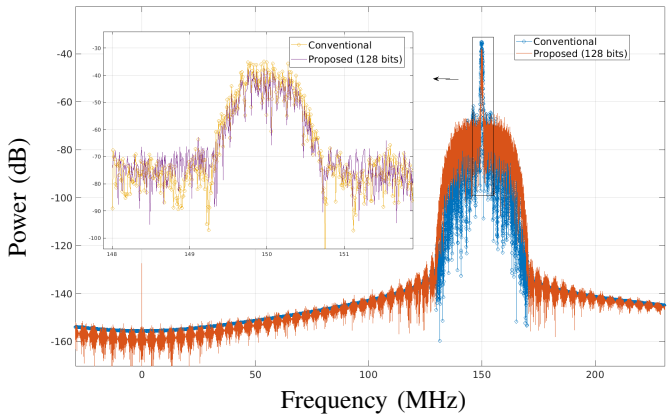

Fig. 4. Normalized power spectral estimation of band-pass-filtered stochastic stream and conventional modulated by a first-order $\Sigma\Delta$ structure.

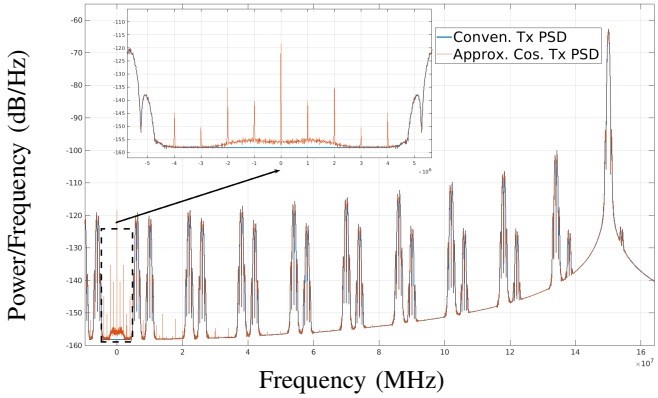

Fig. 5. Power spectral density of transmitted signal using a conventional implementation and an approximation for the $\cos \pi x$ function.

stream has a DC component in the corresponding PSD. Fig. 5 depicts PSDs of the passband signal generated by a conventional implementation for a cosine and the passband signal generated by the Maclaurin approximation of $\cos \pi x$. Fig. 5 proves that the DC component on the PSD of the reconstructed signal is effect of the approximation of *cosine*. Also note that *SNG* units in Fig. 2 introduce quantization error, depending on the length of the stochastic stream, that may lead to erroneous reconstructed value during conversion from stochastic to binary domain. The reconstruction of a long stochastic stream achieves better accuracy than relying on a short one, with the cost of different data rates for actual data and the stochastic stream.

B. BER Evaluation

In order to derive BER *vs.* noise plots, a passband AWGN channel model and an FSK non-coherent correlation demodulator [20, Fig. 2] are used. An AWGN is added to the band-pass-filtered stochastic stream of the stochastic cosine unit in Fig. 3. The noisy signal is demodulated by an FSK non-coherent correlation demodulator, which is proposed as an optimal FSK demodulator [20]. On the receiver side, the channel output, initially is down-converted to baseband by multiplying it with *sine* and *cosine* signals of carrier frequency and filtered by LPFs. The baseband *I* and *Q* branch are multiplied to *sine* and *cosine* signal, both with predefined frequency for bit

TABLE I
HARDWARE COMPLEXITY OF PROPOSED STOCHASTIC-BASED AND CONVENTIONAL LUT- AND CORDIC-BASED POLAR TRANSMITTER AT 28 nm

n	Proposed Stochastic Transmitter			LUT-Based Transmitter		CORDIC-Based Transmitter		
	logic cells	area (μm^2)	area red. (%)[1]	logic cells	area (μm^2)	cordic stages	logic cells	area (μm^2)
7	198	189	69.37	2174	1143	5	915	618
8	244	220	68.18	3952	2059	5	1067	692
9	321	251	66.57	6279	3250	5	1108	753
10	328	261	69.51	10928	5206	5	1313	858
11	366	282	82.74	19900	9377	8	2617	1640
12	361	299	83.53	35577	16 685	8	2822	1820
16	574	428	87.13	323544	135 366	10	5496	3331

[1]Area reduction with respect to CORDIC implementation. Area estimations do not comprise the band-pass filter.

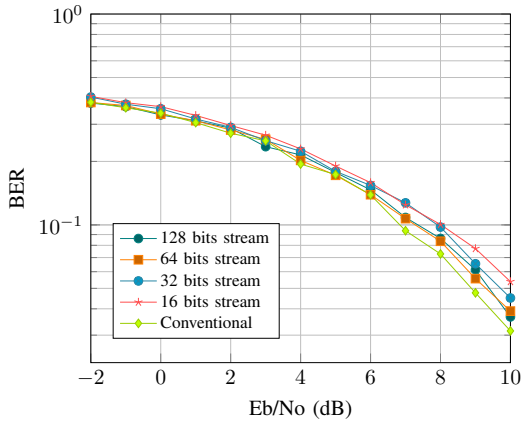

Fig. 6. BER comparison with certain stream lengths of the stochastic cosine.

values 0 and 1, respectively. The corresponding correlation values are integrated for symbol duration, while the decision unit compares the correlation values for 0 and 1, and makes a decision for the corresponding bit.

Fig. 6 illustrates the BER performance of the proposed transmitter for indicative stochastic stream lengths. Large-length streams for stochastic cosine representation asymptotically improve the BER performance, due to the accuracy of the reconstructed value to binary domain. Notice that the transmission is uncoded, while only data, without redundancy, are modulated and transmitted through an AWGN channel.

V. HARDWARE COMPLEXITY

Regarding the hardware complexity of examined architectures, the introduced stochastic-based and conventional LUT-based and CORDIC-based transmitter implementations are synthesized using Cadence Genus at a 28-nm FDSOI technology node. The LUT-based implementation resembles that of Fig. 1, where quantized values of cosine function are stored in a LUT and drive a first-order $\Sigma\Delta$ modulator [21]. In the CORDIC-based implementation, loop iterations corresponding to the estimation of cosine function are implemented in consecutive pipeline stages. The number of loop iterations, denoted as CORDIC stages, increase as computation precision increases. The output of last stage drives a $\Sigma\Delta$ modulator. The main difference between the proposed stochastic-based and conventional architecture is the elimination of LUT- or CORDIC-based approximation and $\Sigma\Delta$ modulator that relaxes significantly the requirements for hardware resources. The elimination of $\Sigma\Delta$ modulator is traded off by the requirement for a second clock domain, with a frequency that is a multiple of carrier frequency. Synthesis is performed for certain word-lengths, while LUT implementation outputs a 24-bit word [3]. Furthermore, conventional architectures for stochastic number generators that rely on primitive linear feedback shift registers are employed [15]. It is noted that the arithmetic accuracy of the stochastic approximation is controlled by the ratio of binary and stochastic domain operation frequencies. For a stochastic computation without an arithmetic accuracy loss, clock frequency of stochastic domain, f_{stoch}, should be $f_{\text{stoch}} = 2^n f_{\text{bin}}$, where f_{bin} is the operation frequency of binary domain that employs an n-bit fixed-point accuracy. Typically, it holds that $f_{\text{bin}} = 4f_{\text{carrier}}$ [4]. Increasing the parallelism and using N-parallel stochastic units, operation frequency reduces to $f_{\text{stoch}} = \frac{2^n}{N} f_{\text{bin}}$. A parallel implementation relaxes the requirement for a very high operation frequency in stochastic domain. In the proposed architecture, pipeline structures separate the binary and stochastic clock domains. Accordingly in a LUT-based architecture, a pipeline register precedes the LUT.

Table I demonstrates the occupied area for the investigated transmitter architectures. Table I reveals that the resources of stochastic-based implementation minimally increase as fixed-point accuracy increases. This happens because bit-stream length increase affects only the complexity of stochastic number generators and not the remainder implementation of Fig. 3. On the contrary, LUT-based implementations occupy the maximum area. The complexity reduction achieved by the stochastic implementation is significant, increases with the increase of fixed-point accuracy and reaches almost 87.13% reduction of the occupied area.

VI. CONCLUSIONS

In this paper we introduce a novel architecture for an all-digital GFSK transmitter, utilizing a stochastic cosine function. One of the main concerns for a transmitter is the hardware complexity, the performance in terms of power spectral density of the transmitted signal and the BER of the overall transmission. The proposed stochastic polar transmitter architecture achieves similar power spectrum with a corresponding conventional transmitter. Furthermore the BER performance improves asymptotically, as the length of the stochastic stream increases. Due to the availability of low-cost extremely simple stochastic filters, further processing of the passband signal becomes possible. Finally, this work shows that the stochastic transmitter is feasible and can be adopted in several low-cost resource-limited applications. The proposed architecture reduces area occupation by 87% at maximum.

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