Novel Noise-Shaping Stochastic-Computing Converters for Digital Filtering

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***Abstract*—Stochastic computing introduces massive parallelism in several practical applications by utilizing minimal-complexity processing elements, and provides inherent fault-tolerant features. However stochastic computation systems require long bit streams to achieve sufficient performance in terms of Signal to Noise Ratio. This paper proposes a first- and a second-order Noise-Shaping Binary-to-Stochastic Converter (NSBSC) for bipolar format. The proposed architecture schemes are compared with a baseline Binary-to-Stochastic Converter (BSC) in terms of Signal-to-Quantization-Noise Ratio (SQNR). It is shown that for certain test cases, the proposed architecture leads to 15.276 dB improved SQNR for the same bit stream length and, furthermore, achieves the same SQNR as the conventional converter using as much as 93.75% shorter stream lengths. Furthermore, the analysis includes area and power figures for the introduced hardware architectures for a 28-nm FDSOI technology. Finally, achieved NSBSC gains are shown to propagate at the output of a stochastic FIR filter, proving that the stochastic properties of the derived stream are maintained.**

I. Introduction

In emerging technologies, maintaining precise boolean functionality becomes even more costly as physical-level uncertainties are encountered with large design margins. Stochastic Computing is proposed as promising, inherently offering tolerance to transient errors as it relies on long pseudo-random bit streams to represent data [1]. Hence it can trade precision for energy reduction using shorter bit streams.

Stochastic bit streams permit complex computations to be realized using low-cost units in terms of hardware complexity. While a bit-serial stochastic stream may introduce long computational latency, parallel computations can be massively performed, as stream bits are of equal weight. Therefore massive parallelism becomes available, allowing the exploration of a substantial area, time, power, and fault tolerance design space. Decreased complexity due to minimal complexity of hardware per bit is accompanied with reduced power dissipation only for moderate data processing or in applications that demand bit streams of short lengths and, hence, moderate accuracy. Otherwise, the length of the bit stream acts counter-intuitively as the power dissipation of the respective processing unit surpasses that of the binary case [2].

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The potential of stochastic computing has been highlighted in a wide range of applications such as neural networks [3], FIR [4] and IIR [5] digital filtering, FFT computation [6], [7], and Error Correction Decoding [8]. In wideband RF transceivers Nguyen *et al.* replace complex digital functions by their stochastic counterparts derived by piece-wise linear approximations [9]. Furthermore complex arithmetic functions can be realized based on Finite-State Machines [3], and Bernstein polynomials [10]. As precise approximation of arithmetic functions demands high-degree Bernstein polynomials and hence increased complexity, their use is rendered inefficient from a hardware complexity perspective. Additionally, Parhi and Liu [11] propose complex arithmetic function approximations using Maclaurin series expansion and factorization.

A stochastic bit stream of length of $L = 2^N$ bits offers the theoretical precision of an N-bit binary word. Yuan and Parhi [12] study the effect of bit stream length on BER performance of stochastic Belief Propagation Polar Decoders. For JPEG Compression, stream lengths of 2^{16} bits are required to achieve sufficient Signal to Noise Ratio [2].

Given the need for long bit stream lengths in applications of practical interest, this paper focuses on minimizing stochastic stream length while maintaining sufficient quality of representation. Specifically we propose to utilize noise-shaping techniques in combination with stochastic computing. Combining bit-stream generation with noise shaping, bit stream length required to achieve a given SQNR is reduced. The proposed technique relieves the requirements of the subsequent stochastic system, by either reducing the number of parallel stochastic units in case of a parallel system or by reducing computational latency or operation frequency for the case of a bit-serial system. As far as hardware or time complexity escalates proportionally to bit stream length, noise shaping the bit stream reduces power dissipation footprints.

Stochastic representation relies on the fraction of 1's in the bit stream. Gaines [13] introduced stochastic computing using two interpretations, namely, unipolar and bipolar. A number x is mapped to a unipolar stochastic stream X so that

$$x = p(x_i = 1), \tag{1}$$

where $x_i \in \{0, 1\}$ is any bit in the bit stream X and $x \in [0, 1]$, as it is a probability. In other words, x is expressed as the probability of a bit in the stream X assuming the value of one.

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In the bipolar format, $y \in [-1, 1]$ is mapped to $x \in [0, 1]$,

$$y = 2x - 1 \Leftrightarrow x = \frac{y+1}{2}, \tag{2}$$

and x is subsequently mapped to a stochastic stream.

The conventional hardware implementation of conversion from binary arithmetic to stochastic representation is realized using a random number generator. The conversion circuit comprises a comparator and a pseudo-random source implemented using a Linear Feedback Shift Register (LFSR). The output of the conversion circuit is the stochastic stream formed by the decisions of a comparator that compares the input binary number and the (evolving) output of the LFSR in every clock cycle. Qian *et al.* report that random number generators contribute to almost 80% and 62% of total area and power consumption of a stochastic computation system [1]. These drawbacks can be entirely alleviated according to [14], where Asynchronous Sigma Delta Modulators are proposed as alternatives of stochastic stream converters that eliminate the use of pseudo-random number generators.

In this paper, principles of noise-shaping techniques are employed for binary to bipolar stochastic conversion, and the SQNR delivered by the respective fixed-point hardware architectures is quantified. The related analysis reveals that the introduced conversion architectures that employ noise shaping generate bit streams with increased SQNR compared with the conventional architecture, allowing for reduction of sampling frequency of the input signal or reduction of bit stream length. Furthermore, area and power estimations for the proposed architectures are reported for a 28-nm FDSOI technology.

The remainder of this paper is organized as follows. In Section II, the basic principles that govern noise shaping techniques are reviewed and the proposed Noise-Shaping Binary-to-Stochastic Converter (NSBSC) is presented in detail, while in Section III a quantitative comparison between the proposed and the baseline architecture is demonstrated in terms of SQNR. Finally, Section IV concludes this paper.

II. Proposed Stochastic Converter Architectures

This section revisits basic principles of noise shaping techniques employed in Sigma-Delta Modulators and introduces the architectures of proposed first- and second-order NSBSC.

Noise-shaping techniques are applied with Delta Sigma Modulators [15] to remove the quantization noise from the signal bandwidth, effectively allowing the reduction of required oversampling ratio given a certain SQNR, and are also employed in RF transmitters for baseband signal modulation [16].

In the context of Stochastic Computing, the structure of a first- and a second-order Delta Sigma Modulator is appropriately modified in order to produce a stochastic stream with noise-shaped characteristics, forming the proposed *NSBSC*. A Binary-to-Stochastic Converter (BSC) inserts quantization noise in the same way a Quantizer does in a conventional Sigma-Delta Modulator. A conventional Sigma-Delta Modulator with noise shaping, followed by a BSC would not produce the expected noise modulation, as the noise of the latter would be superimposed to an already modulated noise.

TABLE I
Area and Power Dissipation for Architectures @ 28 nm

Stream Length	Architecture	Area (μm^2)	Power Diss. (nW)	Max. Frequency (MHz)
2^5	Conventional	18.605	3747.256	2000.00
	First Order	122.400	33 082.299	1209.18
	Second Order	193.773	59 272.784	938.08
2^{12}	Conventional	43.520	8464.552	1270.64
	First Order	260.902	63 485.155	842.45
	Second Order	382.976	111 505.053	722.54

In the proposed architectures, the Quantizer is replaced by a conventional BSC. The proposed architectures feature a feedback part, where a Stochastic-to-Binary Converter (SBC) is introduced. SBC output is delayed and subtracted from system input. Specifically, Fig. 1 depicts the proposed first-order converter that comprises a subtractor, an integrator (dashed box), a BSC and a SBC. The BSC can either generate all bits of the stochastic bit stream in parallel in a single clock cycle or produce them sequentially. The later case requires a frequency that is L times greater than that of the input sample frequency, where L is the bit stream length. The inverse conversion is either performed with an adder tree or with an accumulator that works with an L times greater frequency. The proposed second-order NSBSC is depicted in Fig. 2 and comprises a second subtraction and an additional integrator. The proposed architectures resemble digital architectures for Sigma-Delta Modulators from [17]. The achieved performance of the proposed structures is evaluated by studying noise spectra. Fig. 3 depicts the noise spectrum of a signal with a bandwidth of 0-100 Hz for the cases of a conventional BSC, and the proposed first- and second-order NSBSC. Resembling practice in Sigma-Delta systems, the generated bit stream should be further low-pass filtered to remove the out-of-bandwidth noise.

Regarding the proposed fixed-point first-order architecture, two bits are employed for the integral part, so as to prevent overflows, and $\log_2 L$ bits for the fractional part for an an L-bit stream BSC. Furthermore, the second order architecture uses one more integral bit due to the use of a second integrator. The conventional stochastic converter and the proposed first- and second-order NSBSC are synthesized with Cadence Genus to a 28-nm FDSOI technology for 5- and 12-bit accuracy, *i.e.*, the length of bit stream is 32 and 4096. Table I reports the area, total power dissipation and maximum operating frequency of the examined conversion architectures, referring at a typical delay corner and 1.0 V supply voltage. Even if the respective first- and second-order NSBSC seems that occupy seven and ten times more area than the conventional BSC, respectively, area increase can be compensated for by the subsequent area reduction of the stochastic system that follows, based on the bit stream length reduction that the proposed converters offer.

III. SQNR Analysis of Proposed Converter

This section demonstrates quantitatively the benefits of the proposed NSBSC compared to the conventional BSC in terms of SQNR, defined as $\mathrm{SQNR} = 10 \log_{10} \frac{P_{\text{signal}}}{P_{\text{noise}}}$, where P_{signal}

TABLE II
SQNR AND NOISE POWER IN SIGNAL SPECTRUM OF CONV. AND PROPOSED CONVERTERS WITH A CHIP INPUT OF 0-100 HZ. OVERSAMPLING RATIO 5.

Stream Length	Conventional		First Order Noise Shaping				Second Order Noise Shaping			
	SQNR (dB)	Noise Power	SQNR (dB)	Gain (dB)	Gain (%)	Noise Power	SQNR (dB)	Gain (dB)	Gain (%)	Noise Power
2^4	16.7419	8.4967e-03	25.2891	8.5471	51.0520	1.1872e-03	21.0778	4.3358	25.8979	3.1309e-03
2^5	20.1081	3.9583e-03	28.9666	8.8584	44.0538	5.1483e-04	27.3508	7.2426	36.0186	7.4686e-04
2^6	23.2256	1.9271e-03	32.2606	9.0349	38.9006	2.4066e-04	34.2794	11.0537	47.5927	1.5119e-04
2^7	26.1707	9.7790e-04	35.3260	9.1552	34.9829	1.1878e-04	40.0298	13.8591	52.9565	4.0214e-05
2^8	29.3426	4.7107e-04	38.2642	8.9216	30.4051	6.0384e-05	44.2807	14.9381	50.9093	1.5110e-05
2^9	32.3481	2.3583e-04	41.2172	8.8691	27.4177	3.0597e-05	47.4567	15.1085	46.7061	7.2734e-06
2^{10}	35.3998	1.1679e-04	44.3503	8.9505	25.2840	1.4872e-05	50.6695	15.2697	43.1350	3.4709e-06
2^{12}	41.3963	2.9360e-05	50.3230	8.9266	21.5639	3.7592e-06	56.6729	15.2765	36.9031	8.7118e-07

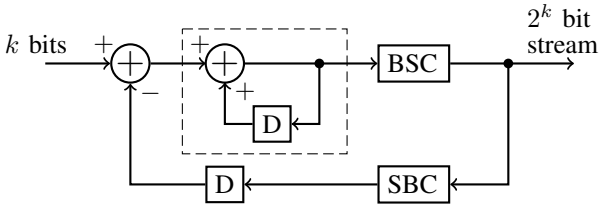

Fig. 1. Proposed first-order Noise-Shaping Binary-to-Stochastic Converter

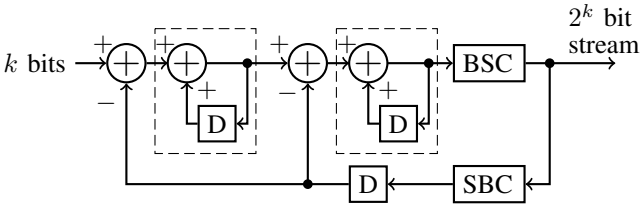

Fig. 2. Proposed second-order Noise-Shaping Binary-to-Stochastic Converter

is the signal power at the input of converter and P_{noise} is the quantization noise power in the signal bandwidth.

Specifically, the first experimental set-up investigates the behavior of SQNR for the conventional and proposed architectures for a chirp input signal with a bandwidth of 0–100 Hz. Note that frequencies chosen in the following are indicative and the reported results scale to general cases as well. An oversampling ratio 5 is assumed, *i.e.*, the sampling frequency is 1 kHz. A common fixed-point input is assumed for both proposed and conventional converters. Table II demonstrates that the SQNR of the proposed converter using the first-order noise-shaping system surpasses the SQNR of a conventional converter. Furthermore, it is evident that the SQNR difference between the conversion schemes, denoted as Gain in Table II, remains relatively constant as the stream length increases. However, the percentage Gain between the conversion architectures decreases. In addition, Table II reports the noise power in the signal bandwidth for the conventional and proposed architectures. For a 12-bit accuracy case, the proposed architectures reduce noise power in the signal bandwidth by as much as two orders of magnitude.

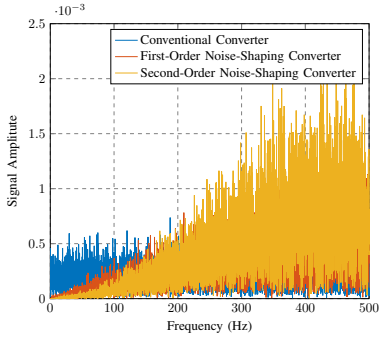

Fig. 3. Shaped Noise Power

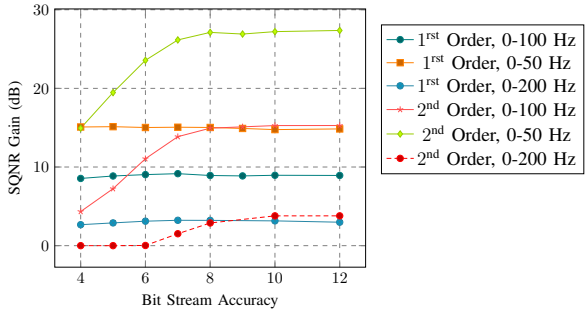

Fig. 4. SQNR Gain for first- and second-order NSBSC

Table II shows that a second-order NSBSC is not able to shape the quantization noise for 2^4 and 2^5 bit stream lengths. Increasing the fractional bits in the feedback part of the second-order NSBSC does not provide any benefit, as accuracy is primarily determined by the SBC. A second-order NSBSC with 2^7 bit stream length converters achieves a similar SQNR with a first-order NSBSC, and, for larger accuracy, the second-order NSBSC out weights in terms of achievable SQNR. It is further investigated whether the second-order NSBSC is able to shape quantization noise for larger values of oversampling ratio. Table III presents the SQNR of the second-order NSBSC and the noise power in the signal bandwidth for an oversampling ratio of 20. Table III reveals that oversampling improves the noise shaping behavior of the second-order NSBSC that achieves a 20.5735 dB Gain compared to the baseline converter for 2^4 stream length. Thus, achievable Gains are determined both by the employed oversampling ratio and the accuracy of SBC in the feedback part.

SQNR improvements are evaluated for chirp signals that occupy several bandwidths. Fig. 4 shows achieved SQNR Gains for chirp signals with bandwidth in ranges 0–50, 0–100, and 0–200 Hz, sampled at 1 kHz. Fig. 4 validates that the Gain remains relatively constant as stream accuracy increases. It is also shown that gain decreases as signal bandwidth increases, given a certain sampling frequency and stream length.

Furthermore, the reduction of bit stream length due to proposed noise shaping techniques is quantified for a given SQNR determined by the conventional BSC. Table IV reveals that second-order NSBSC is able to reduce the bit stream accu-

TABLE III
SQNR AND NOISE POWER IN SIGNAL SPECTRUM OF CONV. AND PROPOSED CONVERTER WITH A CHIP INPUT OF 0-100 HZ. OVERSAMPLING RATIO 20.

Stream Length	Conventional		First Order Noise Shaping				Second Order Noise Shaping			
	SQNR (dB)	Noise Power	SQNR (dB)	Gain (dB)	Gain (%)	Noise Power	SQNR (dB)	Gain (dB)	Gain (%)	Noise Power
2^4	21.9742	2.5470e-03	43.4491	21.4749	97.7277	1.8136e-05	42.5477	20.5735	93.6258	2.2319e-05
2^5	25.3825	1.1751e-03	46.9890	21.6065	85.1235	8.1179e-06	56.6646	31.2820	123.2423	8.7476e-07
2^6	28.8159	5.3198e-04	50.1528	21.3368	74.0455	3.9102e-06	64.7711	35.9551	124.7754	1.3501e-07

TABLE IV
MIN ACCURACY OF PROPOSED ARCHITECTURES FOR A GIVEN SQNR

Conventional		First Order		Second Order	
Stream Length	SQNR (dB)	Stream Length	SQNR (dB)	Stream Length	SQNR (dB)
2^4	16.7419	2^2	17.2331	-	-
2^5	20.1081	2^3	21.6825	-	-
2^6	23.2256	2^4	25.4562	-	-
2^7	26.1707	2^5	28.9610	-	-
2^8	29.3426	2^6	32.2807	2^6	34.3320
2^9	32.3481	2^7	35.2590	2^6	34.3320
2^{10}	35.3998	2^8	38.1917	2^7	40.1018
2^{12}	41.3963	2^{10}	44.2198	2^8	44.0730

TABLE V
MAXIMUM SAMPLING FREQUENCY REDUCTION FOR A GIVEN SQNR

Conventional		First Order			Second Order		
Stream Length	SQNR (dB)	SQNR (dB)	f_s (Hz)	f_s red	SQNR (dB)	f_s (Hz)	f_s red
2^4	16.741	16.902	510	49%	-	-	-
2^5	20.108	20.424	510	49%	-	-	-
2^6	23.225	23.530	510	49%	23.698	600	40%
2^7	26.170	26.680	510	49%	27.095	550	45%
2^8	29.342	29.772	510	49%	30.710	540	46%
2^9	32.348	32.729	510	49%	32.785	500	50%
2^{10}	35.399	35.807	510	49%	35.626	490	51%
2^{12}	41.396	41.645	500	50%	41.776	490	51%

racy by four bits compared with the conventional architecture, offering a bit stream length reduction from 2^{12} to 2^8. The particular achieved reduction is important. It means that it is possible to employ a stochastic computation system that uses streams with 93.75% shorter length when the stochastic bit stream is noise shaped. This potentially leads to a reduced-latency bit-serial system or, equivalently, a reduced-area parallel system, implementing stochastic computations and, consequently, reduced power dissipation. The proposed first-order NSBSC proves to be beneficial in cases of all stream lengths. Cases with a dash in Table IV do not provide any benefit as the second order architecture cannot shape noise for a stream accuracy shorter than that of the conventional.

Another aspect investigated here is the reduction of the oversampling ratio of the 0–100 Hz chirp input signal when employing noise shaping in order to achieve a certain SQNR determined by the conventional BSC. In more detail, Table V demonstrates the SQNR achieved by the first- and second-order NSBSC for the input chirp signal oversampled at a frequency f_s. Table V reveals that a stochastic converter and, consequently, the stochastic computation processing system that follows, when relying on noise shaping by using the proposed techniques, can operate at a working frequency that is as much as 51% lower than that of a conventional stochastic system without noise shaping.

A simple filtering example further validates the superiority

TABLE VI
SQNR (IN dB) AT A FOURTH ORDER FIR FILTER OUTPUT

Stream Length	Conventional		First Order		SQNR Gain
	SQNR	Noise Power	SQNR	Noise Power	
2^7	31.8860	2.5642e-04	42.7564	2.0985e-05	10.8704
2^8	34.8292	1.3073e-04	42.1106	2.4447e-05	7.2814
2^9	37.3735	7.2726e-05	44.0062	1.5791e-05	6.6327
2^{10}	39.6102	4.3443e-05	45.0984	1.2277e-05	5.4882

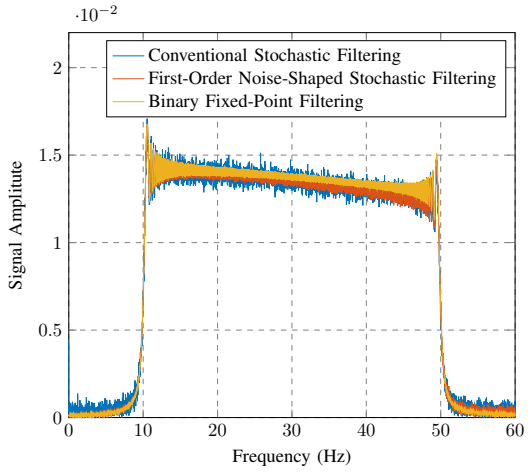

Fig. 5. Signal Spectrum at an eighth order FIR filter output

of noise-shaped stochastic stream delivered by the proposed NSBSC in terms of the introduced noise power in the signal bandwidth when the stream passes through a stochastic system. SQNR and noise power are estimated for a noise-shaped and a conventional bit stream processed by a low-pass stochastic filter which utilizes uneven-weighted-based adders [4] to mitigate the accuracy loss problem of conventional stochastic adders. Fig. 5 depicts spectra at the output of an eighth order filter and 2^7 stream length. Table VI presents SQNR Gains and Noise Power at a fourth order filter output for an input signal of 10–50 Hz bandwidth and shows that the Gains achieved by NSBSC are maintained at the output of a stochastic FIR filter. Employing a 2^5 length noise-shaped stream, an 32.4864 dB SQNR is achieved which is marginally greater than the SQNR achieved by a 2^7 length conventional stream at the output of the filter, leading to a 75% bit stream length reduction.

IV. CONCLUSIONS

This paper proposes a first- and a second-order NSBSC for the bipolar representation. The proposed fixed-point architectures outperform the conventional BSC in terms of SQNR for the same bit stream accuracy and oversampling ratio. Furthermore, the proposed architectures allow for stochastic bit stream length and oversampling rate reduction for a given SQNR with respect to the conventional BSC. Synthesis of respective fixed-pont architectures at 28-nm FDSOI technology are provided.

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