Low-Power Addition With Borrow-Save Adders Under Threshold Voltage Variability

Kleanthis Papachatzopoulos, *Student Member, IEEE*, and Vassilis Paliouras, *Member, IEEE*

***Abstract*—It is well known that reduced logic depth allows for operation at low voltages, therefore reducing power dissipation. However, such circuits are particularly susceptible to variations, which may compromise expected benefits. This brief presents a solution for low-power addition under variability, which successfully handles the challenge of increased threshold voltage variation. Specifically, we quantitatively compare the impact of variation on the performance of ripple-carry adder (RCA) and borrow-save adder (BSA), quantify the average power reduction achieved by BSA attained at low voltage values, at the cost of increased delay variation, and propose a technique that enhances BSA tolerance to variations. Using statistical timing evaluation at the 45-nm and 32-nm nodes, we estimate the maximum critical path delay variation and average power dissipation of BSA at different supply voltages. Our analysis reveals that BSA achieves three times smaller standard deviation of maximum delay than RCA at the same supply voltage. In addition, we show that it is possible to substantially reduce the supply voltage, decreasing by almost 60% the overall power dissipation of BSA in comparison to a counterpart operating at nominal voltage while keeping maximum delay less than that of RCA. Furthermore, simple design optimizations in the design of BSA are introduced that trade latency for variability, significantly reducing normalized standard deviation of the maximum delay.**

***Index Terms*—Borrow-save, Monte-Carlo simulations, timing analysis, variation-tolerant design, threshold voltage variation.**

I. Introduction

SIGNIFICANT delay uncertainties have arisen in the deep sub-micron IC design so that the adoption of statistical tools for Timing Analysis has become indispensable, as traditional methods for modeling electrical parameters render inefficient [1]. The fundamental atomic-level randomness encountered in modern semiconductor devices, coupled with difficulties in controlling manufacturing processes precisely, accounts for the fact that manufactured ICs present characteristics that dramatically differ from their initial specifications. In view of these challenges, the pronounced limitations of *Deterministic Static Timing Analysis* tools drive both academia and industry to seek efficient solutions considering multiple corner cases, which specify delay characteristics in extreme process and environmental conditions. In this context, *Statistical Timing Analysis* emerges as a viable solution [2], [3].

The complexity and increased number of stages involved in the manufacturing process make physical parameters prone to variations. When modeled statistically, parameters are distinguished into *inter-* and *intra-die* variations. The former, also termed as *die-to-die*, are due to mechanisms either in the manufacturing process or because of environmental factors, which cause global shifts, the same across a die, wafer or lot, and the latter, known also as *within-die*, model device parameters with different variations across a die. Although the contribution of intra-die variations on parameters was negligible in manufacturing process generations of long-channel devices, these variations are taken into account for contemporary digital designs in which low supply voltage values are used [4].

Extensive literature focuses on the modeling of delay uncertainty of simple structures due to environmental and manufacturing process variations. Alioto and Palumbo [5] derive an analytical model that describes the delay sensitivity of a Ripple-Carry Adder composed by Dual-Rail Domino or Mirror Full Adder cells. A model that describes the propagation delay variance of a CMOS inverter is presented in [6], taking into account within-die variations of threshold voltage and the value of input slew, showing that the propagation delay variance is proportional to threshold voltage variance. A great research effort has been focused on the evaluation of a range of Full Adder topologies (at the transistor level) [7] or of Ripple-Carry topologies [8] in terms of Power and Energy/Power Delay Product. Certain CMOS Full Adder architectures are investigated in [9] from a delay variation perspective, and the noise tolerance of CNFET technology on process variations is explored in [10]. Dorosti *et al.* [11] assess the mean delay and standard deviation of Adder structures working on sub-threshold operating region and propose the adoption of folded and deeply pipelined architectures to mitigate delay variations.

Furthermore, previous works employ alternative arithmetic encoding schemes in Digital Signal Processing (DSP) systems. Delay variation evaluation of FIR filters, which utilize processing units in Residue Number System (RNS), are introduced in [12] and compared with binary arithmetic counterparts in terms of normalized delay variance. The impact of delay variability on binary and RNS-based MACs, and adders pertaining to borrow-save encoding has been studied in [13] and [14], suggesting the use of RNS and borrow-save encoding for the cases where tolerance to delay variations is sought. A comparison of Ripple-Carry architecture with an adder based on a different encoding, such as a High-Radix Adder, in contemporary process technologies reveals interesting insights, because

Manuscript received March 2, 2018; revised March 28, 2018; accepted March 28, 2018. Date of publication April 2, 2018; date of current version May 1, 2018. This brief was recommended by Associate Editor J. M. de la Rosa. *(Corresponding author: Kleanthis Papachatzopoulos.)*

The authors are with the Department of Electrical and Computer Engineering, School of Engineering, University of Patras, 26504 Patras, Greece (e-mail: papachatz@ece.upatras.gr; paliuras@ece.upatras.gr).

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/TCSII.2018.2821905

of the presence of variations and their pronounced effect on timing and power violations.

Adders are fundamental in DSP systems and several other applications, and contribute significantly to the critical path delay of related hardware. This brief quantitatively compares binary arithmetic and borrow-save encoding for basic adder architectures in the presence of variations. The comparison is performed in terms of delay variation; voltage reduction is explored as a technique that leads to power efficiency. We focus mainly on estimating the variability of the maximum combinational delay caused by threshold voltage variations, neglecting the variability generated by other parameters that affect delay. Transient Timing Analysis is performed using BSIM 4 SPICE MOSFET models assuming 45-nm and 32-nm manufacturing processes [15]. Borrow-Save Adders are here proven suitable for low-power operation under variations. Additionally, two design techniques are introduced to reduce the normalized standard deviation of the delay.

The remainder of this brief is organized as follows: In Section II, an overview of threshold voltage variations is presented along with our modeling assumptions. The employed redundant encoding scheme and the structure of the examined adders are presented in Section III, while in Section IV the experimental evaluation and the introduced technique are detailed. Finally, conclusions are drawn in Section V.

II. Threshold Voltage Fluctuations and Employed Variation Model

One of the primary electrical parameters responsible for delay variability is the threshold voltage. A model that describes the relation between the threshold voltage, V_{th}, and the drain current, I_{n}, of an NMOS transistor, which discharges the output node, and, accordingly, defines the propagation delay, is given by

$$I_{\text{n}} = \begin{cases} k'_{\text{n}} \frac{W}{L} (V_{\text{GS}} - V_{\text{th}})^a, & V_{\text{GS}} \geq V_{\text{th}} \\ 0, & V_{\text{GS}} < V_{\text{th}}, \end{cases} \quad (1)$$

where k'_{n} is a technology-dependent parameter, W, L are the width and length of the transistor, respectively, V_{GS} is the gate-to-source voltage and a takes values in the interval $[1.4, 2]$ depending on the operating region of the transistor [16].

Concerning the sources of process variations affecting threshold voltage, the fluctuation of the number and placement of dopant atoms implanted in MOSFET channel, known as *Random Dopant Fluctuations* (RDF), causes significant deviation of the threshold value from its predicted value between different transistors [3]. The variation caused by the aforementioned manufacturing process results in a Gaussian spread of threshold voltage around its nominal value and its standard deviation is proportional to the inverse square root of MOSFET width and length, *i.e.,*

$$\sigma_{V_{\text{th,RDF}}} \propto \frac{1}{\sqrt{W_{\text{eff}} \cdot L_{\text{eff}}}}, \quad (2)$$

where W_{eff}, L_{eff} are the effective channel width and length for a transistor, respectively [17]. Furthermore, the use of light sources of optical lithography with wavelength that is quite larger than the minimum feature size leads to channel length distortions affecting the driving current and threshold voltage [3]. The latter presents an exponential relationship with the channel length for short-channel devices due to Drain-Induced Barrier Lowering (DIBL) and charge sharing [18]. Thus, from a design perspective, up-scaling device transistors helps mitigating variations. Secondary effects, such as Line-Edge Roughness, oxide thinness variation, aging and temperature, contribute to threshold voltage variability.

In addition, the aforementioned mechanisms cause a $3 \cdot \sigma_{V_{\text{th,total}}}$ threshold voltage variation that can be at most 10% of its nominal value [3]. In our analysis, we assume that, when variations are manifested, the final threshold voltage value can be approximated as a sum of three terms

$$V_{\text{th}} = V_{\text{th,nominal}} + V_{\text{th,inter}} + V_{\text{th,intra}}, \quad (3)$$

where $V_{\text{th,nominal}}$ is the nominal value of threshold voltage, $V_{\text{th,inter}}$ and $V_{\text{th,intra}}$ are Gaussian random variables with zero mean and standard deviations $\sigma_{V_{\text{th,inter}}}$ and $\sigma_{V_{\text{th,intra}}}$, respectively, which satisfy $3 \cdot (\sigma_{V_{\text{th,inter}}} + \sigma_{V_{\text{th,intra}}}) = 0.1 \cdot V_{\text{th,nominal}}$. Voltage component $V_{\text{th,inter}}$ is common for all MOSFETs of the examined circuits, referring to inter-die variations, such as channel length fluctuations, and $V_{\text{th,intra}}$ is completely independent across MOSFETs, modeling intra-die variations, such as those caused by RDF. Another basic assumption adopted here is that the threshold voltage is the main parameter that affects delay variability, presuming that channel length contributes to delay variability through DIBL effect and, hence, its effect is mapped to the threshold voltage [6].

III. Ripple-Carry and Borrow-Save Architectures

The investigation of Full-Adder timing margins is of paramount importance, as related timing violations impair severely operations at the core of every processing system. We focus on two architecturally simple adder structures, *i.e.,* the Ripple-Carry Adder (RCA) and Borrow-Save Adder (BSA). The RCA consists of a number of cascaded Full Adder (FA) cells, equal to its bit-length. Under nominal process and environmental conditions, its maximum critical path delay is defined by the path along its carry chain until the sum output of the Most Significant Bit position. However, when process fluctuations occur, the maximum critical path delay can be manifested through other sensitizable paths.

Departing from the conventional binary arithmetic, we study the delay characteristics of BSA that employs the radix-2 encoding over the digit set $S = \{-1, 0, 1\}$, also known as borrow-save (BS) encoding. In BS encoding, each digit, x_i, at the ith bit position is represented by a pair of bits, (x_i^n, x_i^p), with positive negative and positive weights, and $x_i = x_i^p - x_i^n \in S$. The addition of digits observing the radix-2 BS encoding is based on the *carry-free addition algorithm*, which consists of three steps: i) the computation of position sums $p_i = x_i + y_i$, ii) the decomposition of each p_i into a transfer t_{i+1} and an interim sum $w_i = p_i - r \cdot t_{i+1}$, where r is the radix of the representation, and iii) the addition of the incoming transfers to obtain the sum digits $s_i = w_i + t_i$ [19]. BSA consists of 4-to-2 compressors, composed of two FAs, implementing the *carry-free addition algorithm* [20]. The addition of operands, already expressed in BS encoding, resembles the

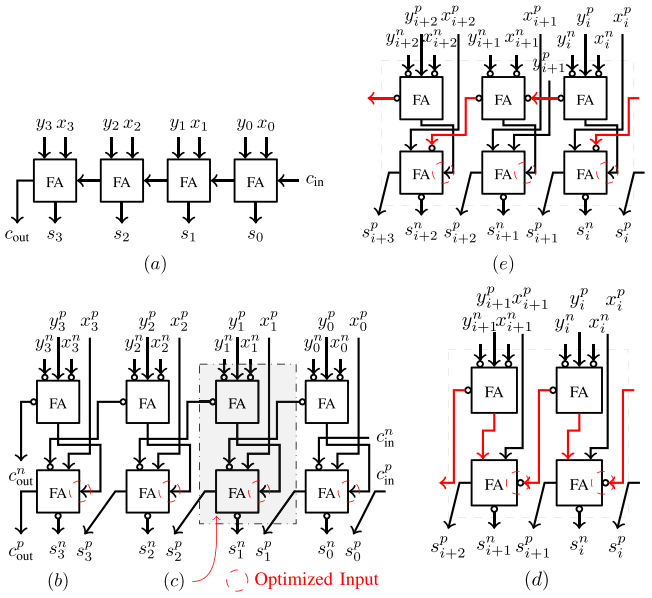

Fig. 1. The architecture of *a*) a 4-bit Ripple-Carry Adder, *b*) a Radix-16 Adder with borrow-save encoding, *c*) a 4-to-2 compressor implemented by two Full Adders (shaded in gray), *d*) first proposed modification of the baseline BSA architecture (BSA′) in which the slow sum-output drives a pin, not optimized to receive slow inputs and *e*) second proposed modification (BSA″) with a critical path of three Full Adders.

addition of operands expressed in carry-save encoding, with the exception of certain inversions in the beginning and at the end of the processing. BSA architecture demonstrates the advantage of reduced *ripple-effect* over RCA architecture. The architecture of the two adders is depicted in Fig. 1. In this implementation, the slow sum-output of FAs in the upper row drives the input-pin in a lower row FA, optimized to receive the slow-input. As an instance, the addition of seven and one with zero carry-in, expressed in conventional binary representation as $x = 0111$, $y = 0001$, respectively, mandates a carry to be propagated sequentially from the first to the fourth bit position through the carry chain in the RCA. The counterpart operation in BS domain, using the $x = \{(0,0),\ (0,1),\ (0,1),\ (0,1)\}_{\mathrm{BS}}$, $y = \{(0,0),\ (0,0),\ (0,0),\ (0,1)\}_{\mathrm{BS}}$ representation for seven and one, respectively, results to the sum $s = \{(0,1),\ (1,1),\ (1,1),\ (0,0)\}_{\mathrm{BS}}$, computed with a ripple-effect of t_i's only in a neighbor bit position.

Regarding the area occupied by the two architectures, the area of an n-bit RCA is $A_{\mathrm{RCA}} \approx n \cdot A_{\mathrm{FA}}$, and that of a BSA is $A_{\mathrm{BSA}} \approx 2n \cdot A_{\mathrm{FA}}$, where A_{FA} is the area of a FA. The techniques evaluated here do not use resizing/gate splitting [21] in order to control variation and optimize certain computational paths based on the respective architecture.

The cost associated with the conversion from binary to BS encoding and *vice versa* can be compensated when a sufficient amount of computations are performed in the encoded data domain. This is common in applications such as digital filtering, where conversions are required only in the beginning and at the end of processing [22]. Here, we do not take into account the effect of converters since their effect on delay variation can be significantly reduced using resizing, as they do not constitute a delay-critical component of the design.

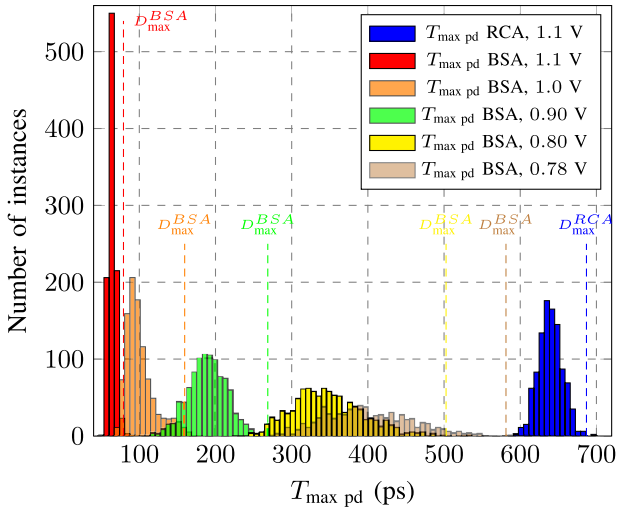

Fig. 2. Maximum propagation delay, $T_{\max\ \mathrm{pd}}$, histograms for an 8-bit RCA and an equal length BSA at certain supply voltages under inter-die V_{th} variations.

TABLE I
STANDARD DEVIATION OF MAXIMUM DELAY AND MAXIMUM DELAY, $D_{\max} = \mu + 3 \cdot \sigma$, FOR RCA AND BSA AT CERTAIN SUPPLY VOLTAGES

$V_{\mathrm{dd}}^{\mathrm{RCA}}$ (V)	inter-die		intra-die	
	σ_{RCA} (ps)	$D_{\mathrm{max}}^{\mathrm{RCA}}$ (ps)	σ_{RCA} (ps)	$D_{\mathrm{max}}^{\mathrm{RCA}}$ (ps)
1.1 (8 bit)	15.84	686.92	6.19	657.85
$V_{\mathrm{dd}}^{\mathrm{BSA}}$ (V)	σ_{BSA} (ps)	$D_{\mathrm{max}}^{\mathrm{BSA}}$ (ps)	σ_{BSA} (ps)	$D_{\mathrm{max}}^{\mathrm{BSA}}$ (ps)
1.1 (8 bit)	4.96	79.21	2.78	77.21
1.0 (8 bit)	19.50	159.54	10.46	148.29
0.9 (8 bit)	26.24	268.64	9.15	237.30
0.85 (8 bit)	35.76	361.98	12.54	315.39
0.8 (8 bit)	51.08	502.65	18.46	439.27
0.78 (8 bit)	59.64	581.28	22.16	512.20

IV. PERFORMANCE AND POWER ANALYSIS

A. Experimental Set-Up

This section investigates the impact of threshold voltage variability on the maximum delay of RCA and an equivalent length BSA using Monte-Carlo SPICE simulations. In more detail, we assume a 28-transistor FA cell [23] for both architectures. This cell is optimized for ripple-carry architectures, *i.e.,* the path from carry-in to carry-out is shorter than the path from carry-in to sum-out. In order to capture accurately the delay characteristics of nanometer MOSFETs, parameter values from a 45-nm and 32-nm low-power NMOS and PMOS Predictive Technology Model library [15] are used and introduced to a BSIM 4 model [24]. We also follow the threshold voltage variation modeling assumptions detailed in Section II and limit the number of iterations to 1000 to control the simulation time.

B. Statistical Evaluation

Initially, the standard deviation of maximum delay for RCA and BSA are estimated. As a first step, the input vector that sensitizes the maximum-delay path of the adder structures under nominal delay values is found and, for this vector, Transient Analysis simulations are performed. In Table I, the standard deviation of maximum delay is reported when only

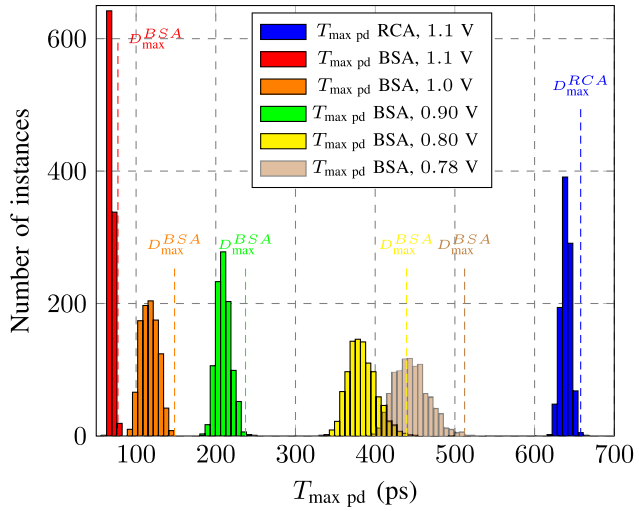

Fig. 3. Maximum propagation delay, $T_{\max\,pd}$, histograms for an 8-bit RCA and an equal length BSA at certain supply voltages under intra-die V_{th} variations.

intra- or only inter-die threshold variations take place, as well as the maximum delay, $D_{\max} = \mu + 3 \cdot \sigma$, where μ is the mean maximum delay and σ the corresponding standard deviation. The data refer to 8-bit architectures for the 45-nm technology. The supply voltage of RCA is kept constant at its nominal value, 1.1 V, while we examine BSA timing behavior in sub-nominal supply voltage values. Table I reveals that, for the nominal voltage value, a BSA exhibits smaller standard deviation of maximum delay than RCA, *i.e.,* 4.96 ps against 15.84 ps for inter-die variations and 2.78 ps against 6.39 ps for intra-die variations. In Figs. 2 and 3, histograms of the maximum propagation delay, $T_{\max\,pd}$, are depicted for inter- and intra-die variations of threshold voltage, respectively, at certain supply voltages. We also see that, in the presence of inter-die variations, the value of standard deviation of maximum delay for BSA is almost twice as great as that of intra-die variations at 1.1 V and the difference between the two grows as the supply voltage decreases. In addition, with the reduction of supply voltage, standard deviation is found to generally increase for both inter- and intra-die threshold variations (with an exception at 0.9 V for intra-die variations). As indicated by Table I, it is also possible to reduce the supply voltage at a value $V_{\text{sub-nom}}$ and, still, achieve $D^{\text{BSA}}_{\max}(V_{\text{sub-nom}}) < D^{\text{RCA}}_{\max}(V_{\text{nom}})$, although $\sigma^{\text{BSA}}_{\max}(V_{\text{sub-nom}}) > \sigma^{\text{RCA}}_{\max}(V_{\text{nom}})$. However, this increase of standard deviation does not affect timing yield as determined by $D^{\text{RCA}}_{\max}(V_{\text{nom}}) = 258.97$ ps, *i.e.,* the RCA worst-case performance.

Lowering supply voltage reduces power. In Table II, the mean sum of Dynamic and Static power dissipation of RCA and BSA and the difference of total power dissipation with respect to the one of nominal supply voltage case of BSA are demonstrated. The evaluation employs an extensive set of input vectors to assess the average power dissipation in the presence of inter-die voltage threshold fluctuations. For example, the supply voltage of BSA can be reduced from 1.1 V to 0.78 V achieving as much as 59% less than the total power dissipation of the nominal case, at the cost of increased delay variations. Table II also presents the Power Delay Product

TABLE II
AVERAGE RCA AND BSA POWER FOR A RANGE OF SUPPLY VOLTAGES

$V^{\text{RCA}}_{\text{dd}}$ (V)	P_{RCA} (fW)	Mean Max Delay (ps)	PDP (yJ)
1.1	94.14	639.4	60.19

$V^{\text{BSA}}_{\text{dd}}$ (V)	P_{BSA} (fW)	Mean Max Delay (ps)	PDP (yJ)	Pow Diff %	PDP Diff %
1.1	102.68	64.33	6.60	-	89.03
1.0	82.62	101.04	8.34	19.56	86.14
0.9	65.23	180.92	11.80	36.47	80.39
0.8	50.10	349.41	17.50	51.20	70.92
0.78	41.96	402.36	16.88	59.13	71.95

TABLE III
STANDARD DEVIATION OF MAXIMUM DELAY AND MAXIMUM DELAY, $D_{\max} = \mu + 3 \cdot \sigma$, FOR RCA AND BSA AT CERTAIN SUPPLY VOLTAGES FOR THE 32-nm TECHNOLOGY

$V^{\text{RCA}}_{\text{dd}}$ (V)	inter-die		intra-die	
	σ_{RCA} (ps)	$D^{\text{RCA}}_{\max}$ (ps)	σ_{RCA} (ps)	$D^{\text{RCA}}_{\max}$ (ps)
1.0 (8 bit)	18.52	623.96	7.17	590.15
$V^{\text{BSA}}_{\text{dd}}$ (V)	σ_{BSA} (ps)	$D^{\text{BSA}}_{\max}$ (ps)	σ_{BSA} (ps)	$D^{\text{BSA}}_{\max}$ (ps)
1.0 (8 bit)	17.21	140.29	5.18	117.04
0.9 (8 bit)	17.81	205.38	6.12	182.23
0.8 (8 bit)	38.87	391.89	13.64	341.16
0.78 (8 bit)	48.15	462.65	17.06	401.36
0.75 (8 bit)	65.16	602.86	25.10	527.11

(PDP) of RCA at the nominal supply voltage, the PDP of BSA at a range of sub-nominal supply voltages and its difference from the PDP of RCA. The difference between the two metrics ranges from almost 70% to 90%. Hence, significant savings related to PDP are revealed for the BSA architecture. Under no variability conditions, $V^{\text{BSA}}_{\text{dd}}$ can be reduced further to 0.723 V so as BSA has $D^{\text{BSA}}_{\max} = D^{\text{RCA}}_{\max}$, achieving a 68.11% (32.74 fW) Power and a 64.99% (21.07 yJ) PDP reduction. Thus, threshold voltage variations restrict the expected power benefits, but not considerably. However, their impact on delay is important enough and needs to be taken into account.

Furthermore, the performance characteristics of the RCA and BSA architectures are investigated for the 32-nm technology. Table III summarizes simulation results for the 32-nm technology under the same simulation scenarios studied for the 45-nm node. The nominal supply voltage for 32-nm is 1 V. Table III indicates that BSA architecture achieves smaller standard deviation of maximum delay, σ_{BSA}, than that of 45-nm node in the corresponding supply voltages. Still, in 32-nm node, it is possible to reduce the supply voltage of BSA from 1 V (*Power* = 72.07 fW, *PDP* = 6.39 yJ) to 0.75 V (*Power* = 36.79 fW, *PDP* = 14.98 yJ), achieving further power reduction (48.97%), and meeting the same delay constraints as RCA under inter-die threshold voltage variations. Although the power reduction benefits are expected to be smaller as nominal voltage supply declines following technology scaling, the absolute value of power decreases.

C. Proposed Reduction of BSA Normalized Delay Variation

Two simple interconnection modifications of a BSA are proposed here to improve tolerance to variations. Specifically, in the first one, BSA′, we drive an input pin, not optimized to receive slow inputs, with the slow sum-output and assess

TABLE IV
STANDARD DEVIATION OF MAXIMUM DELAY AND MAXIMUM DELAY, FOR THE THREE BSA ARCHITECTURES AT CERTAIN SUPPLY VOLTAGES

V_{dd} (V)	inter-die					
	σ_{BSA} (ps)	$\sigma_{BSA'}$ (ps)	$\sigma_{BSA''}$ (ps)	D_{max}^{BSA} (ps)	$D_{max}^{BSA'}$ (ps)	$D_{max}^{BSA''}$ (ps)
1.1 (8 bit)	4.96	6.68	7.39	79.21	182.20	266.59
0.9 (8 bit)	26.24	18.14	20.62	268.64	334.63	483.57
0.8 (8 bit)	51.08	42.23	45.34	502.65	578.41	812.05
V_{dd} (V)	intra-die					
	σ_{BSA} (ps)	$\sigma_{BSA'}$ (ps)	$\sigma_{BSA''}$ (ps)	D_{max}^{BSA} (ps)	$D_{max}^{BSA'}$ (ps)	$D_{max}^{BSA''}$ (ps)
1.1 (8 bit)	2.78	2.31	3.22	77.21	173.79	258.77
0.9 (8 bit)	9.15	6.83	8.62	237.30	313.47	458.49
0.8 (8 bit)	18.46	16.92	19.25	439.27	532.96	759.31

TABLE V
NORMALIZED STANDARD DEVIATION OF MAXIMUM DELAY FOR REFERENCE (BSA) AND PROPOSED (BSA′, BSA″) ARCHITECTURES

V_{dd} (V)	inter-die			intra-die		
	$\frac{\sigma_{BSA}}{\mu_{BSA}}$	$\frac{\sigma_{BSA'}}{\mu_{BSA'}}$	$\frac{\sigma_{BSA''}}{\mu_{BSA''}}$	$\frac{\sigma_{BSA}}{\mu_{BSA}}$	$\frac{\sigma_{BSA'}}{\mu_{BSA'}}$	$\frac{\sigma_{BSA''}}{\mu_{BSA''}}$
1.1	0.0729	0.0412	0.0302	0.0403	0.0138	0.0129
0.9	0.1450	0.0647	0.0489	0.0436	0.0233	0.0199
0.8	0.1461	0.0934	0.0670	0.0480	0.0350	0.0274

the standard deviation of maximum delay and D_{max}. In the second one, BSA″, we create a critical path of three FA stages. The connectivity between the FA cells of the new BSA architectures is depicted in Figs. 1(d) and 1(e). As shown in Table IV, the value of D_{max} increases compared to the 45-nm reference design, as expected; however, the standard deviation of BSA′ declines substantially for both intra- and inter-die variations compared to the baseline, while that of BSA″ presents smaller standard deviation only for specific supply voltage values. Finally, Table V presents the values of normalized standard deviation of maximum delay for the 45-nm reference and the two introduced BSA architectures. At the nominal supply voltage, the normalized standard deviation of the modified BSAs is almost one fourth of the reference for intra-die variations. In all cases, normalized standard deviation is smaller for the introduced BSAs. Hence, it follows that BSA′ achieves smaller standard deviation in both normalized and non-normalized terms and is therefore proposed as a delay-variation tolerant alternative. BSA″ is proposed for the cases where the normalized standard deviation is important.

V. CONCLUSION

We comparatively examine the effect of threshold voltage variability on the timing behavior of RCAs and BSAs. By modeling the behavior of threshold voltage under fluctuations and using BSIM 4 SPICE models, we estimate the standard deviation of maximum delay for the two aforementioned architectures. The evaluation shows that BSA achieves smaller delay variation than RCA at nominal supply voltage. Furthermore, it is possible to reduce the supply voltage of BSA, attaining the delay constraints imposed by the delay characteristics of RCA, as well as reducing significantly both power dissipation and PDP. The power reduction benefits are validated for both 32-nm and 45-nm technology nodes. Finally, simple introduced interconnection modifications lead to a reduced normalized and non-normalized delay variation for BSA.

REFERENCES

[1] R. Garg, *Analysis and Design of Resilient VLSI Circuits: Mitigating Soft Errors and Process Variations*. New York, NY, USA: Springer, 2009.

[2] A. Srivastava, D. Sylvester, and D. Blaauw, *Statistical Analysis and Optimization for VLSI: Timing and Power*. New York, NY, USA: Springer, 2006.

[3] M. Orshansky, S. Nassif, and D. Boning, *Design for Manufacturability and Statistical Design: A Constructive Approach*. New York, NY, USA: Springer, 2007.

[4] M. Eisele, J. Berthold, D. Schmitt-Landsiedel, and R. Mahnkopf, "The impact of intra-die device parameter variations on path delays and on the design for yield of low voltage digital circuits," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 5, no. 4, pp. 360–368, Dec. 1997.

[5] M. Alioto and G. Palumbo, "Impact of supply voltage variations on full adder delay: Analysis and comparison," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 14, no. 12, pp. 1322–1335, Dec. 2006.

[6] M. H. Abu-Rahma and M. Anis, "A statistical design-oriented delay variation model accounting for within-die variations," *IEEE Trans. Comput.-Aided Design Integr. Circuits Syst.*, vol. 27, no. 11, pp. 1983–1995, Nov. 2008.

[7] M. Alioto and G. Palumbo, "Analysis and comparison on full adder block in submicron technology," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 10, no. 6, pp. 806–823, Dec. 2002.

[8] M. Alioto and G. Palumbo, "High-speed/low-power mixed full adder chains: Analysis and comparison versus technology," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, New Orleans, LA, USA, 2007, pp. 2998–3001.

[9] K. Bernstein *et al.*, "High-performance CMOS variability in the 65-nm regime and beyond," *IBM J. Res. Develop.*, vol. 50, no. 4.5, pp. 433–449, 2006.

[10] Y. S. Mehrabani and M. Eshghi, "Noise and process variation tolerant, low-power, high-speed, and low-energy full adders in CNFET technology," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 11, pp. 3268–3281, Nov. 2016.

[11] H. Dorosti, A. Teymouri, S. M. Fakhraie, and M. E. Salehi, "Ultralow-energy variation-aware design: Adder architecture study," *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.*, vol. 24, no. 3, pp. 1165–1168, Mar. 2016.

[12] I. Kouretas and V. Paliouras, "Delay-variation-tolerant FIR filter architectures based on the residue number system," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Beijing, China, 2013, pp. 2223–2226.

[13] K. Papachatzopoulos and V. Paliouras, "Reduction of delay variations in arithmetic circuits using a redundant representation," in *Proc. 5th Int. Conf. Modern Circuits Syst. Technol. (MOCAST)*, Thessaloniki, Greece, 2016, pp. 1–4.

[14] K. Papachatzopoulos, I. Kouretas, and V. Paliouras, "Dynamic delay variation behaviour of RNS multiply-add architectures," in *Proc. IEEE Int. Symp. Circuits Syst. (ISCAS)*, Montreal, QC, Canada, 2016, pp. 1978–1981.

[15] *Predictive Technology Model*. Accessed: Sep. 15, 2017. [Online]. Available: http://ptm.asu.edu/

[16] T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 584–594, Apr. 1990.

[17] A. Asenov, S. Kaya, and J. H. Davies, "Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations," *IEEE Trans. Electron Devices*, vol. 49, no. 1, pp. 112–119, Jan. 2002.

[18] Y. Cao, *Predictive Technology Model for Robust Nanoelectronic Design*. New York, NY, USA: Springer, 2011.

[19] B. Parhami, *Computer Arithmetic: Algorithms and Hardware Designs*. New York, NY, USA: Oxford Univ. Press, 2009.

[20] P. Kornerup, "Reviewing high-radix signed-digit adders," *IEEE Trans. Comput.*, vol. 64, no. 5, pp. 1502–1505, May 2015.

[21] V. Agarwal, J. Sun, and J. M. Wang, "Delay uncertainty reduction by gate splitting," *IEEE Trans. Circuits Syst. II, Exp. Briefs*, vol. 56, no. 4, pp. 295–299, Apr. 2009.

[22] A. D. Re, A. Nannarelli, and M. Re, "Implementation of digital filters in carry-save residue number system," in *Proc. Rec. 35th Asilomar Conf. Signals Syst. Comput.*, vol. 2. Pacific Grove, CA, USA, 2001, pp. 1309–1313.

[23] N. H. Weste and D. Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*. Noida, India: Pearson Educ., 2015.

[24] A. M. Niknejad *et al.*, *BSIM4v4.7 MOSFET Model-User's Manual*, Univ. California, Berkeley, Berkeley, CA, USA, 2011, accessed: Sep. 10, 2017. [Online]. Available: https://bsim.berkeley.edu/models/bsim4/