



A Report
On

**Final Project
4-bit Calculator Design**

By

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Soumyadeep Choudhury (sxc180056)**

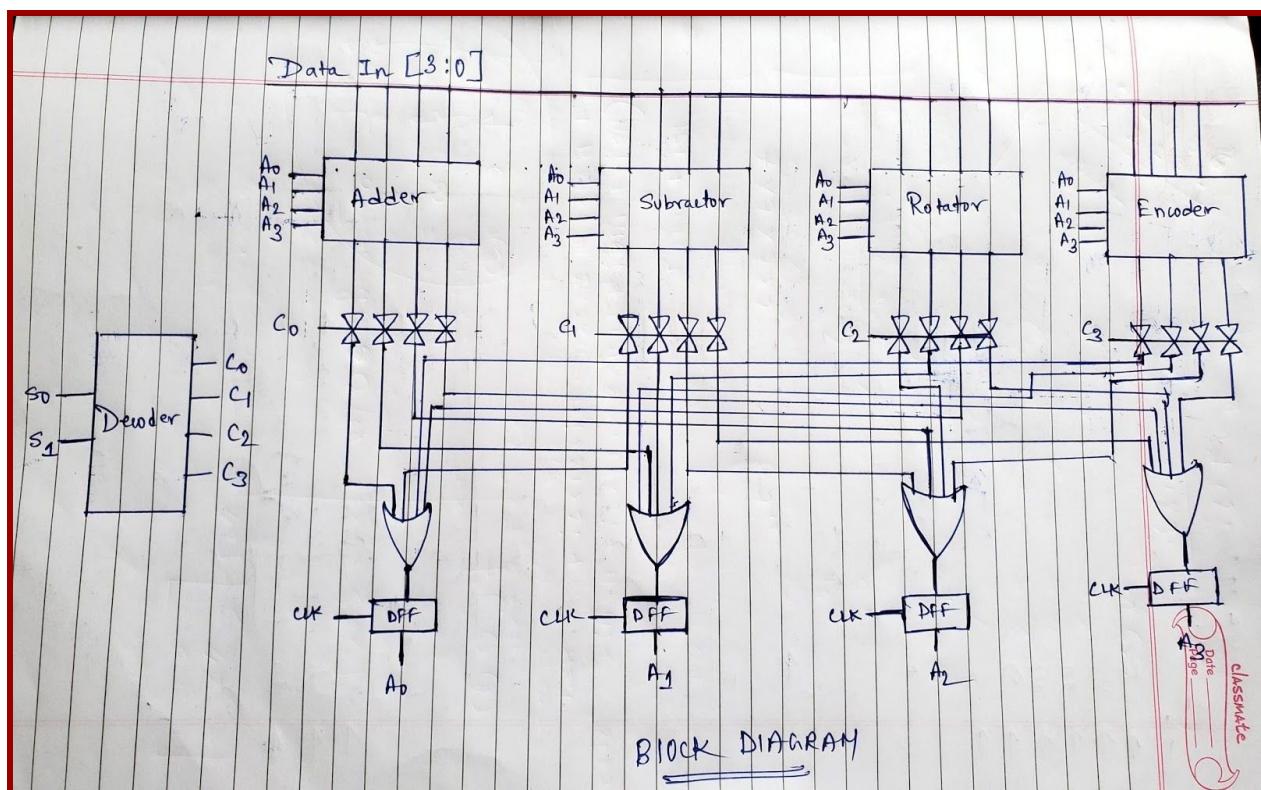
Objective :-

The objective of this project is to design a 4-bit Calculator in Cadence 6. It can perform the various mode arithmetic operations like - addition, subtraction and division. In order to design a 4-bit microprocessor - Calculator, we need to design and perform various computations and calculations modularly defining some specific operational functionality. Later, we need to integrate these modular operations to design a full 4-bit Calculator which can perform all the operations depending on the input control signals.

The various modular blocks performing specific arithmetic operations, are as follows -

1. Ripple Carry Adder-Subtractor
2. Full Adder and Half-Adder
3. Decoder
4. Encoder
5. Barrel Shifter
6. Buffer operation
7. D - Flip Flop
8. 2:1 Multiplexer
9. Transgate operation
10. AND and NAND operation
11. NOR and OR operation
12. XOR operation
13. Inverter operation

4-bit Microprocessor Block Diagram (Pencil Sketch)

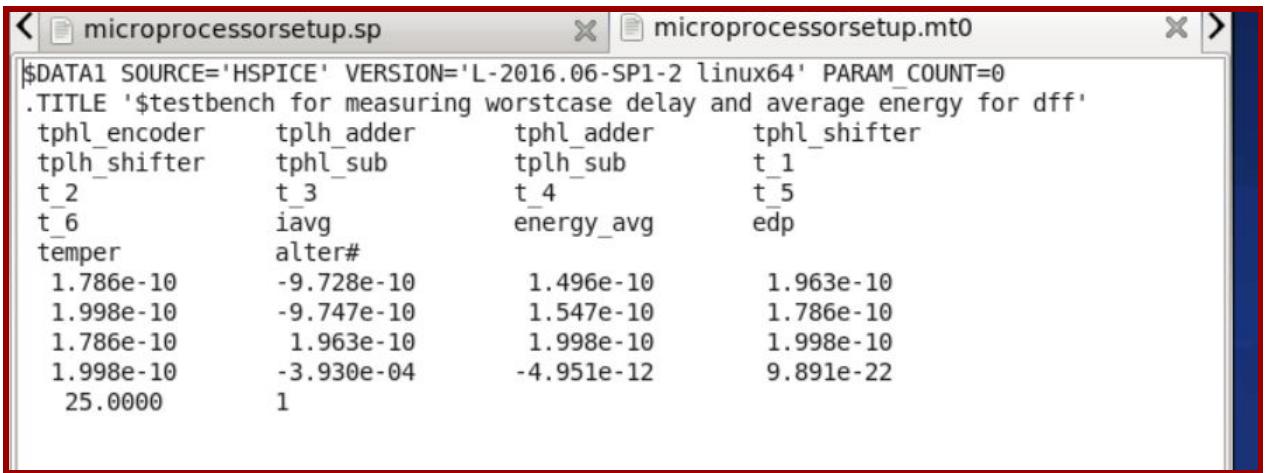


END

4-bit Microprocessor Design Analysis

minimum clock period TMIN	maximum clock period TMAX	Layout Width	Layout Height	
1ns	There is no max clock, Input signal must satisfy hold time.	69.82 um	68.36um	
delay	Energy over all transitions E	EDP	Area	AEDP (J um^2)
Encoder, adder,sub,shifter shown below(graph)	-4.951e-12J	9.891e-22	4772.8952 um^2	47208.7064e-22

HSPICE SIMULATION OF THE MICROPROCESSOR



The screenshot shows a terminal window with two tabs: 'microprocessorsetup.sp' and 'microprocessorsetup.mt0'. The 'sp' tab contains the SPICE script code, and the 'mt0' tab shows the simulation results.

```
$DATA1 SOURCE='HSPICE' VERSION='L-2016.06-SP1-2 linux64' PARAM_COUNT=0
.TITLE '$testbench for measuring worstcase delay and average energy for dff'
tphl_encoder tphl_adder tphl_adder tphl_shifter
tphl_shifter tphl_sub tphl_sub t_1
t_2 t_3 t_4 t_5
t_6 iavg energy_avg edp
temper alter#
1.786e-10 -9.728e-10 1.496e-10 1.963e-10
1.998e-10 -9.747e-10 1.547e-10 1.786e-10
1.786e-10 1.963e-10 1.998e-10 1.998e-10
1.998e-10 -3.930e-04 -4.951e-12 9.891e-22
25.0000 1
```

Working description :-

- Shifter** : we have 4 bits inputs. can only have 1 bit as 1, the others 3 bits should be all 0.
- Encoder** : if IN0 is 0, then will reset all, no matter what's the other inputs, only IN0 is 0, the others will work.
- Adder** : we have the last Cout float, don't affect 4 bits adder.
- Subtractor** : the output is **two's complement format**. For example, 1111-1110=0001, but the result is 1110.

END

Calculator Output Analysis : Truth Table

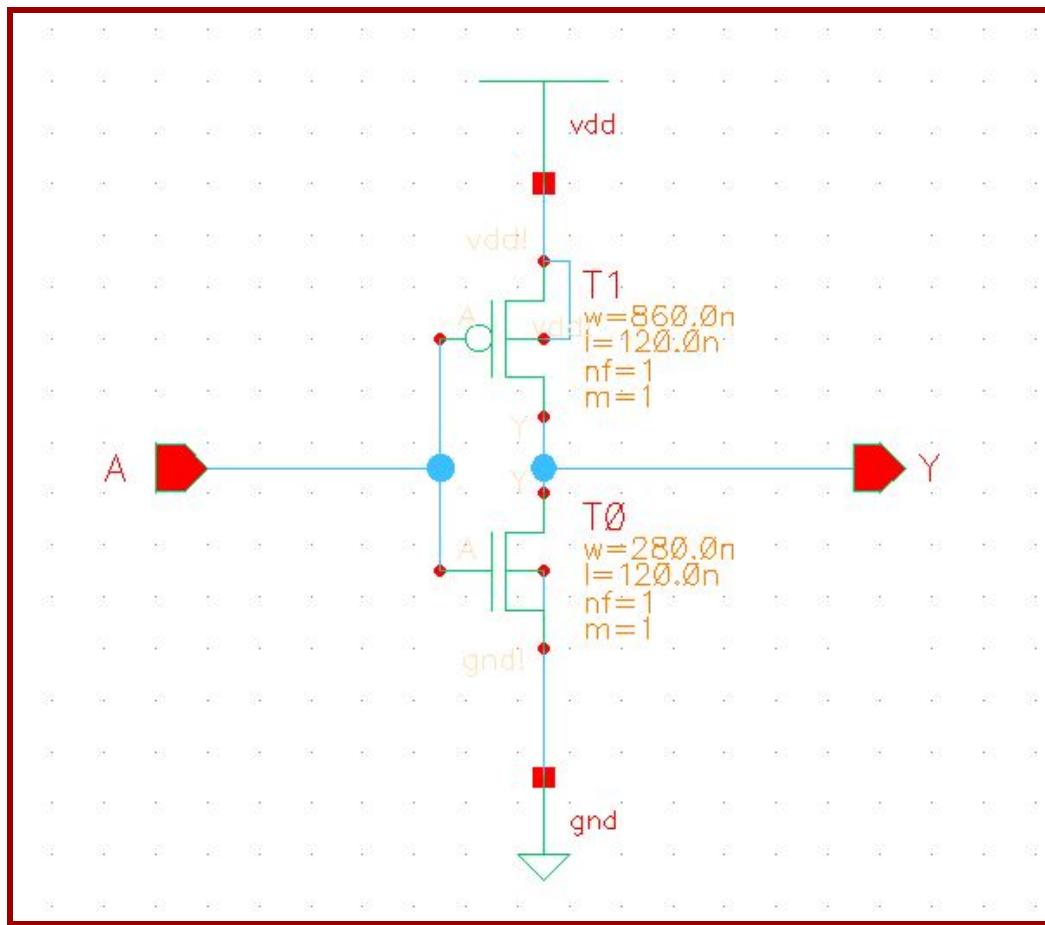
Operation	INPUT (4-BIT)	OUTPUT (4-BIT)
Encoder	1000	1111
Encoder	0010	0111
Encoder	0001	0101
Adder	0010	0000
Adder	1000	0010
Shifter	0010	1100
Shifter	0100	0110
Subtractor	0011	1100
Subtractor	0010	0111
Subtractor	0000	1011

END

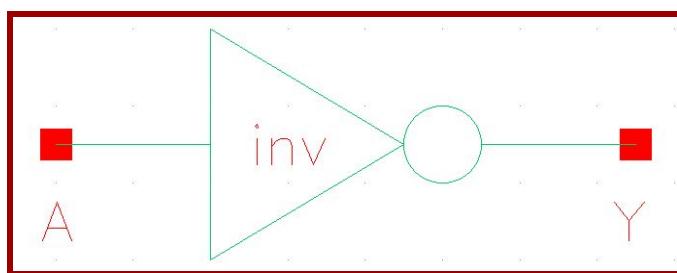
Design Analysis of Each Modular Block

1.) Inverter Operation

a) Schematic :-

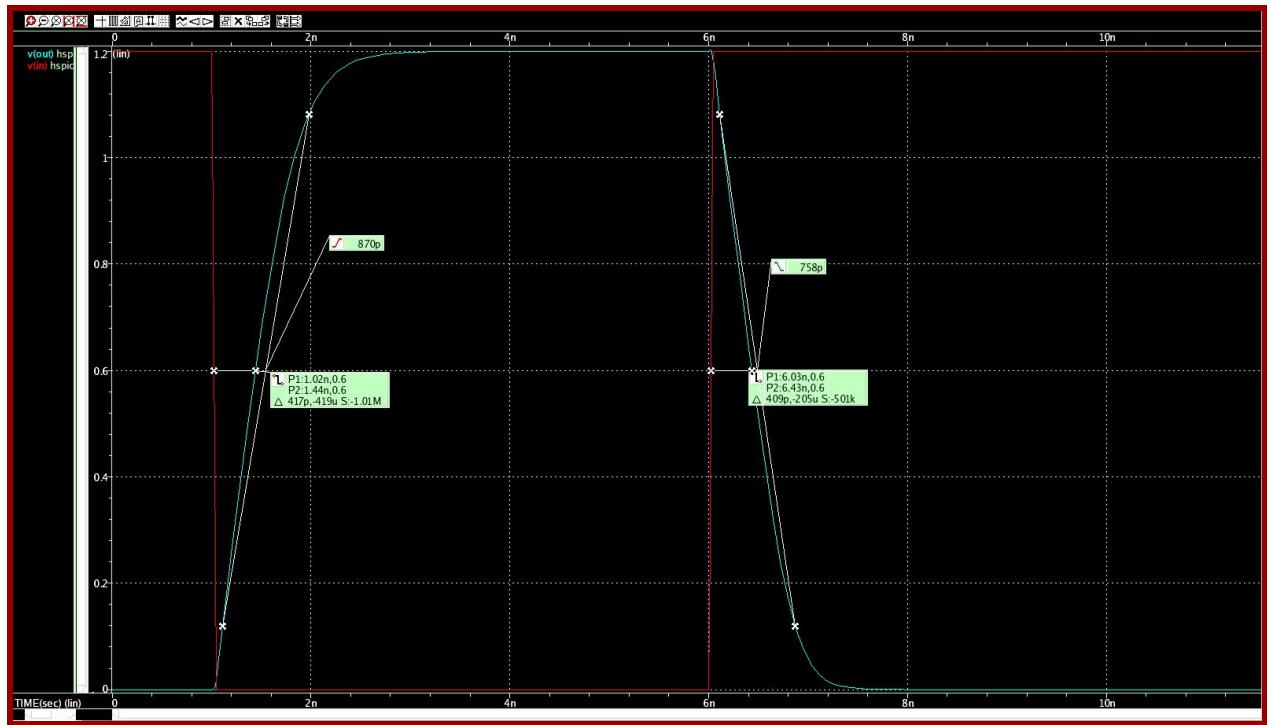


b) Symbol :-

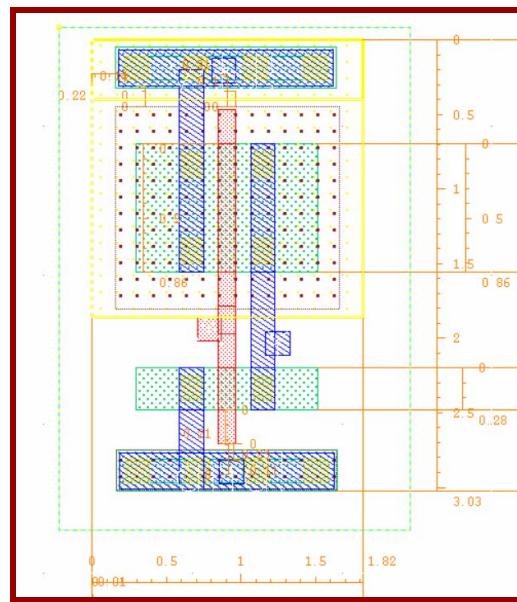


END

c) Simulation Waveform :-

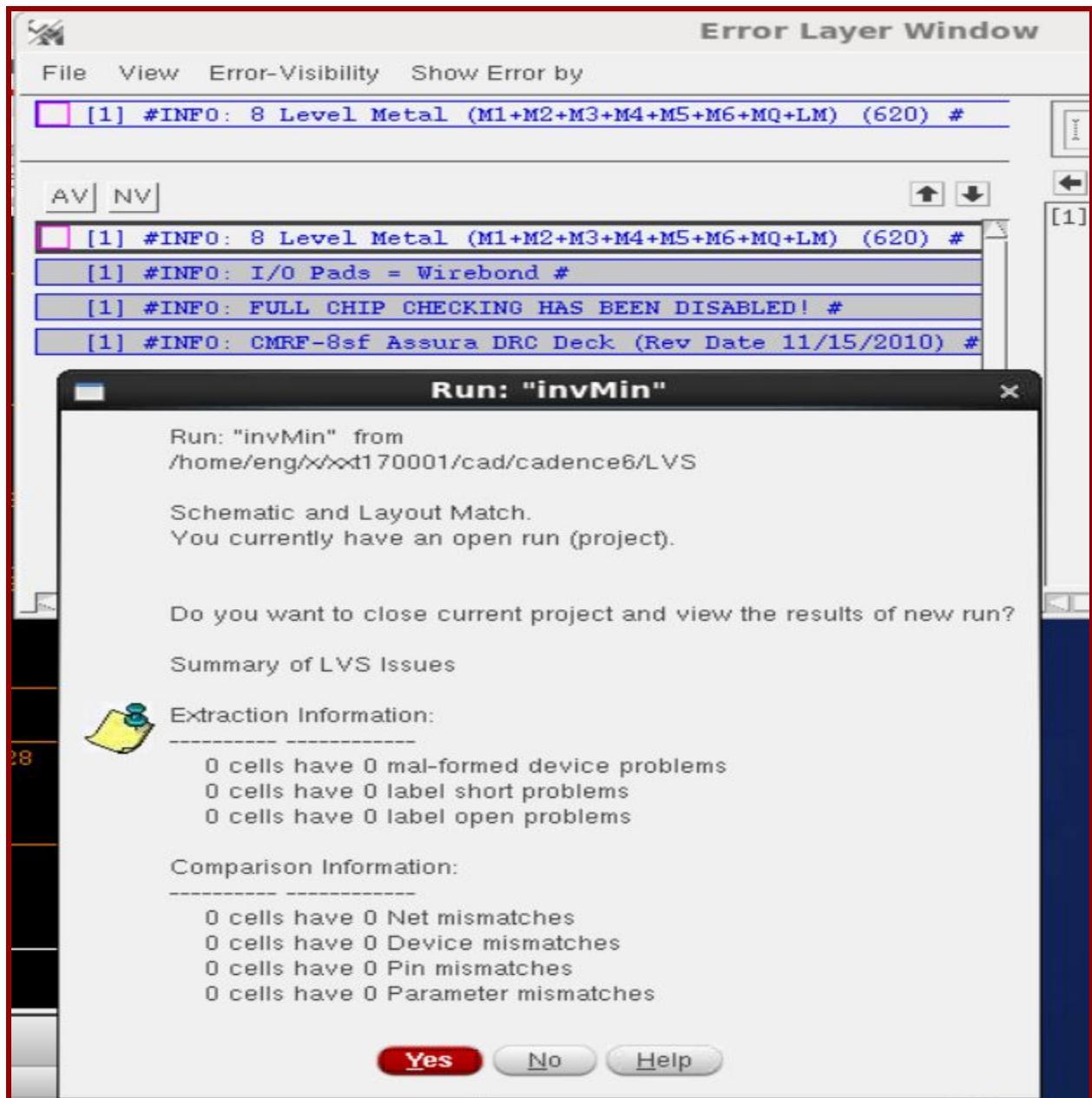


d) Layout



END

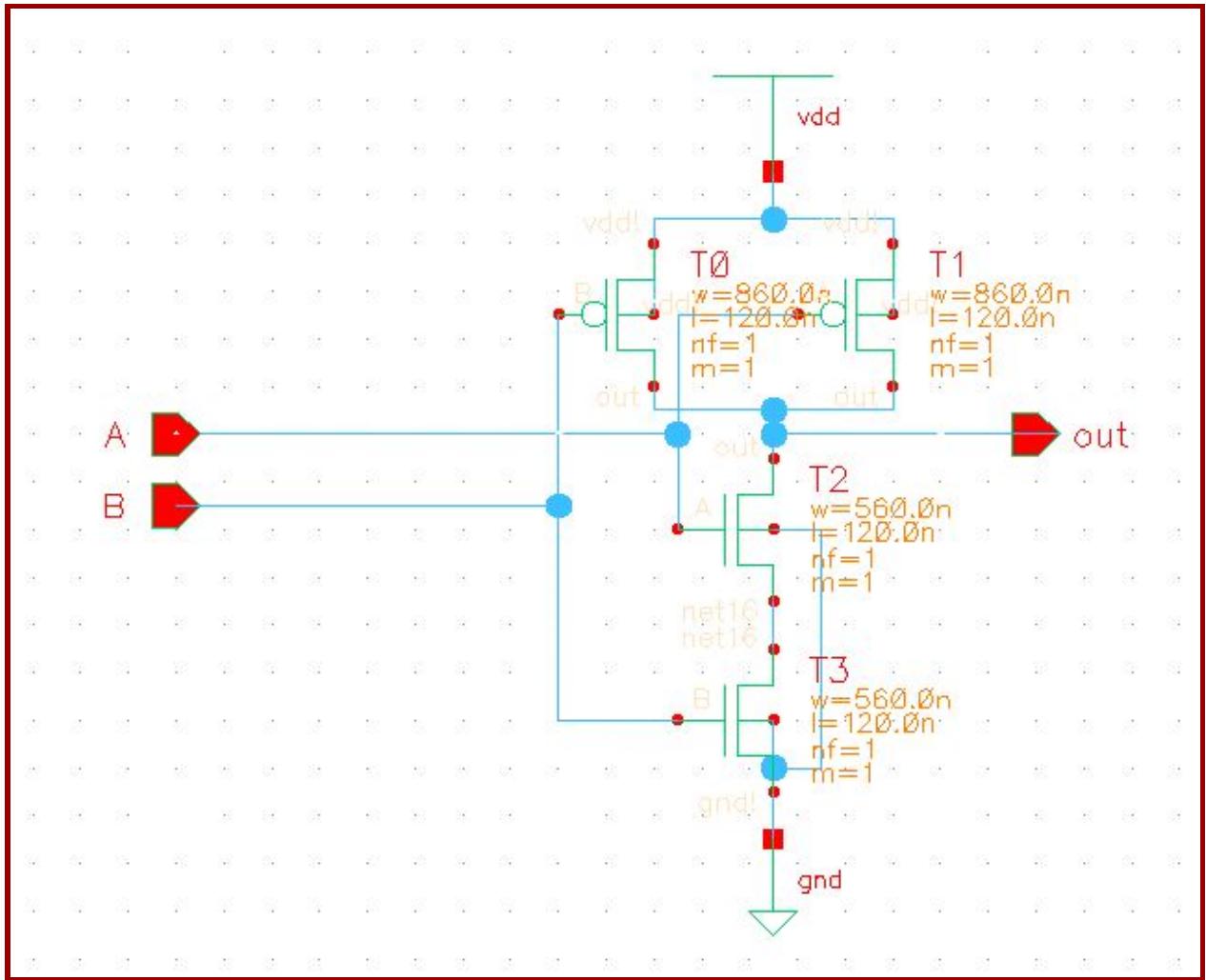
e) LVS Report



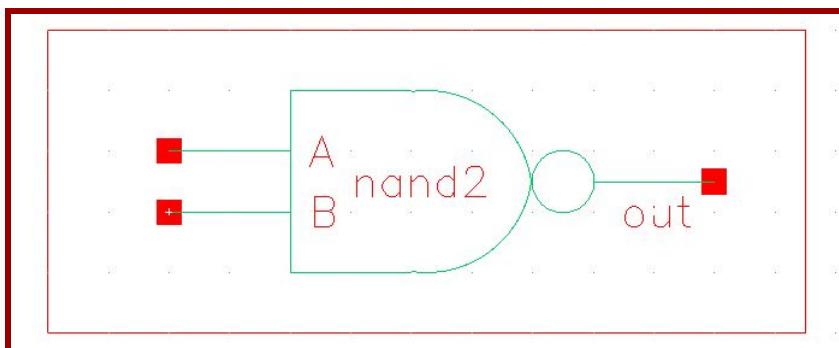
END

2.) NAND - 2 Operation

a) Schematic :-

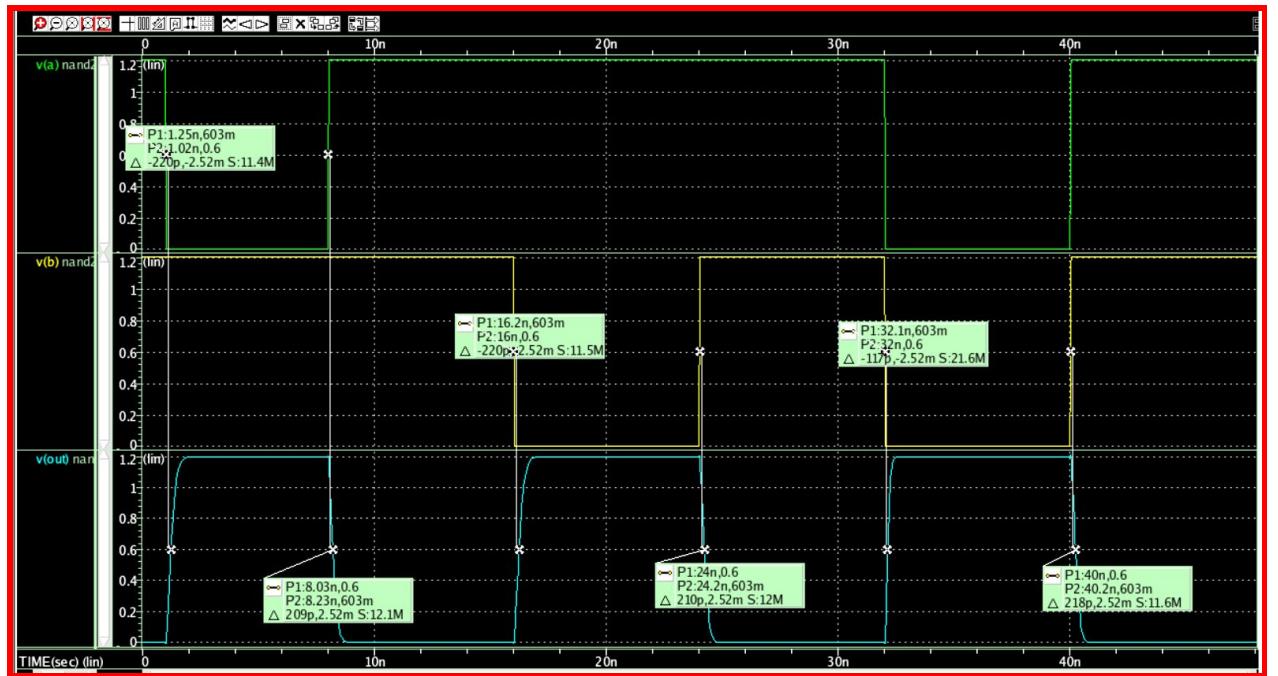


b) Symbol :-

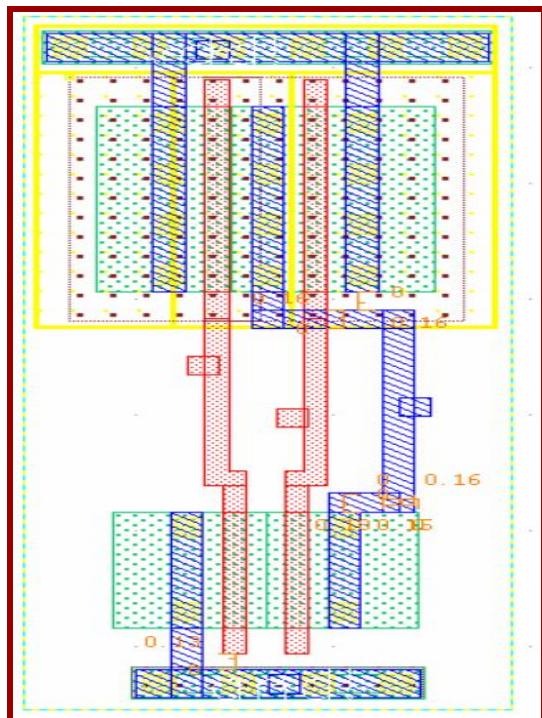


END

c) Simulation Waveform :-

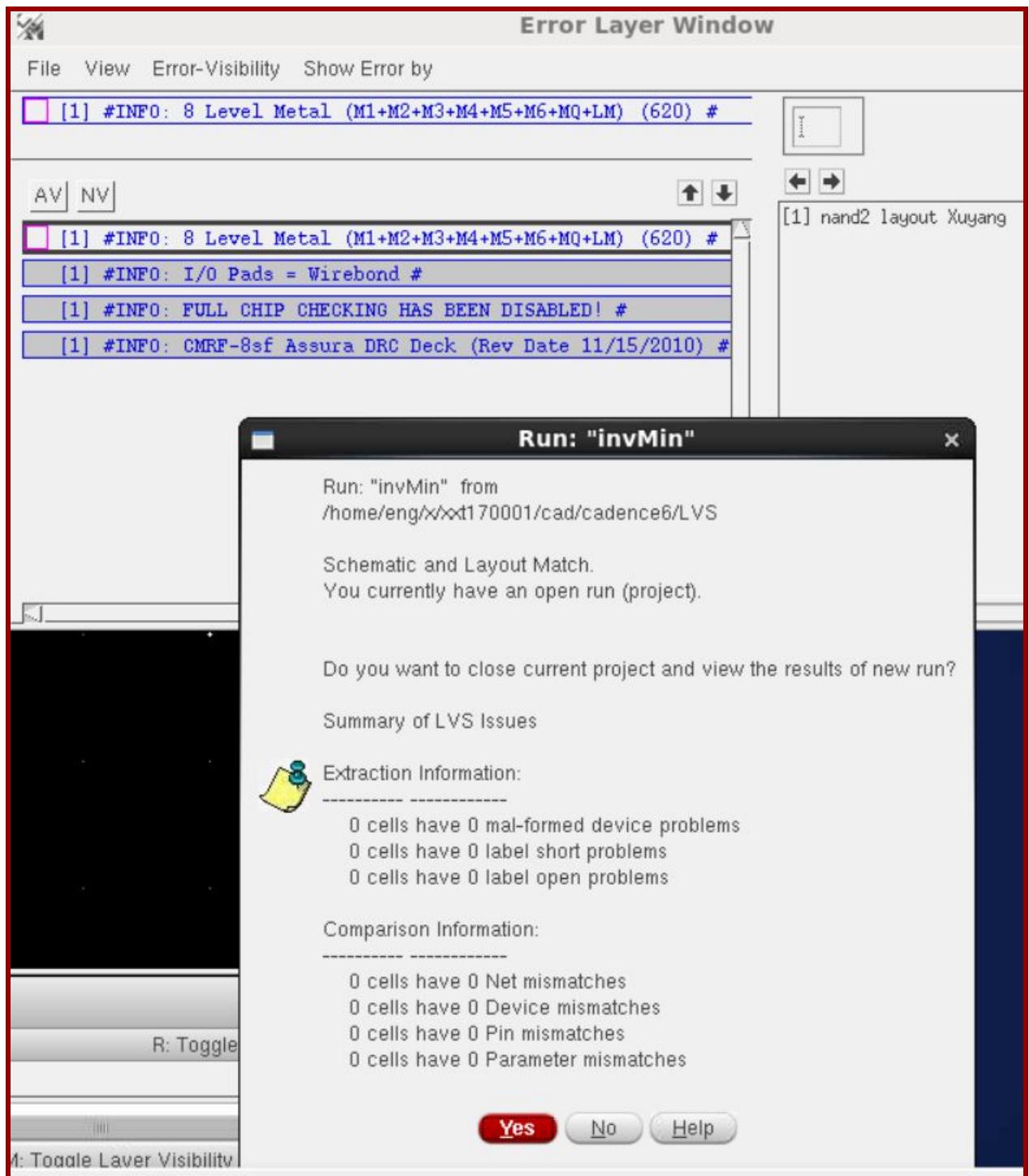


d) Layout :



END

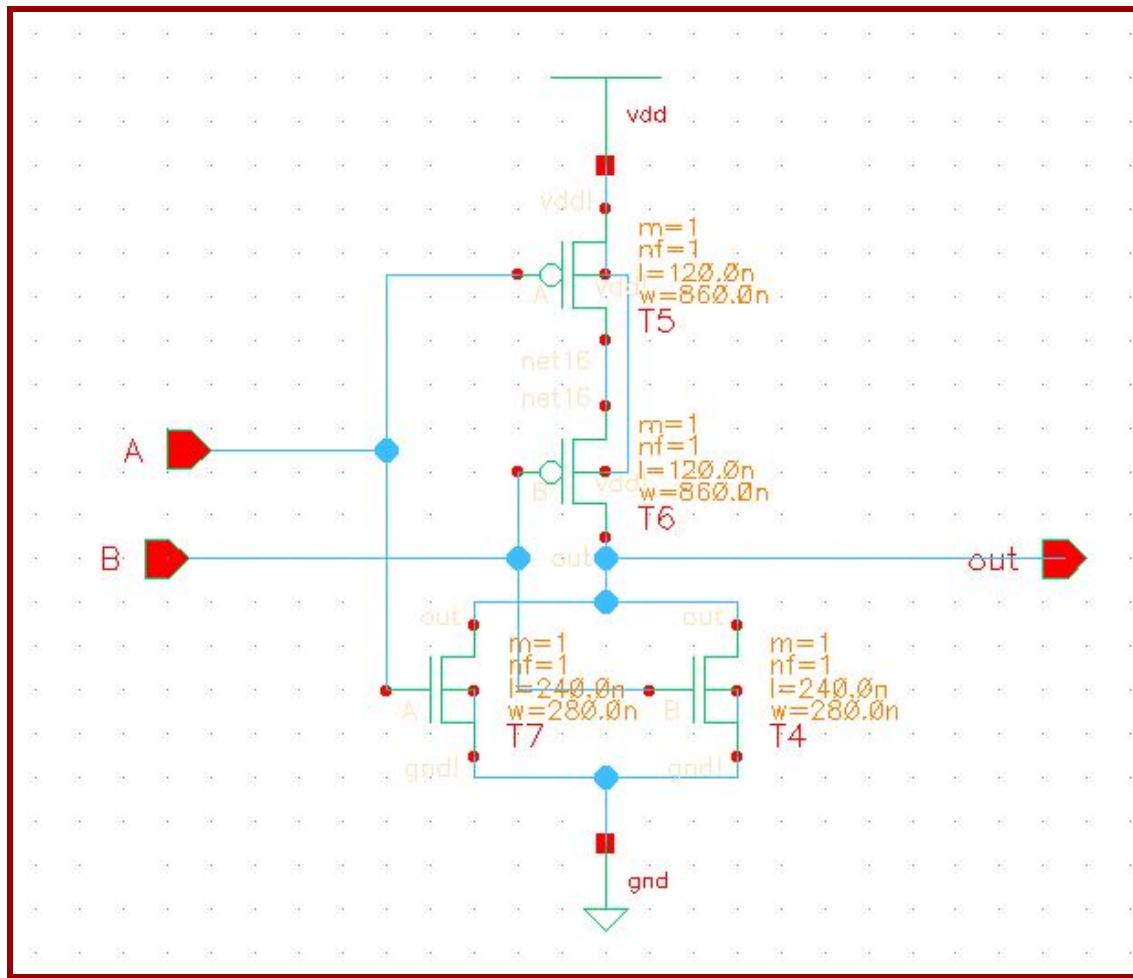
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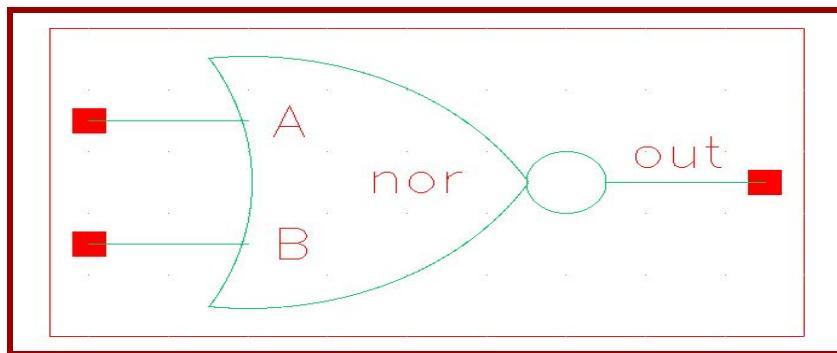
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3.) NOR - 2 Operation

a) Schematic :-

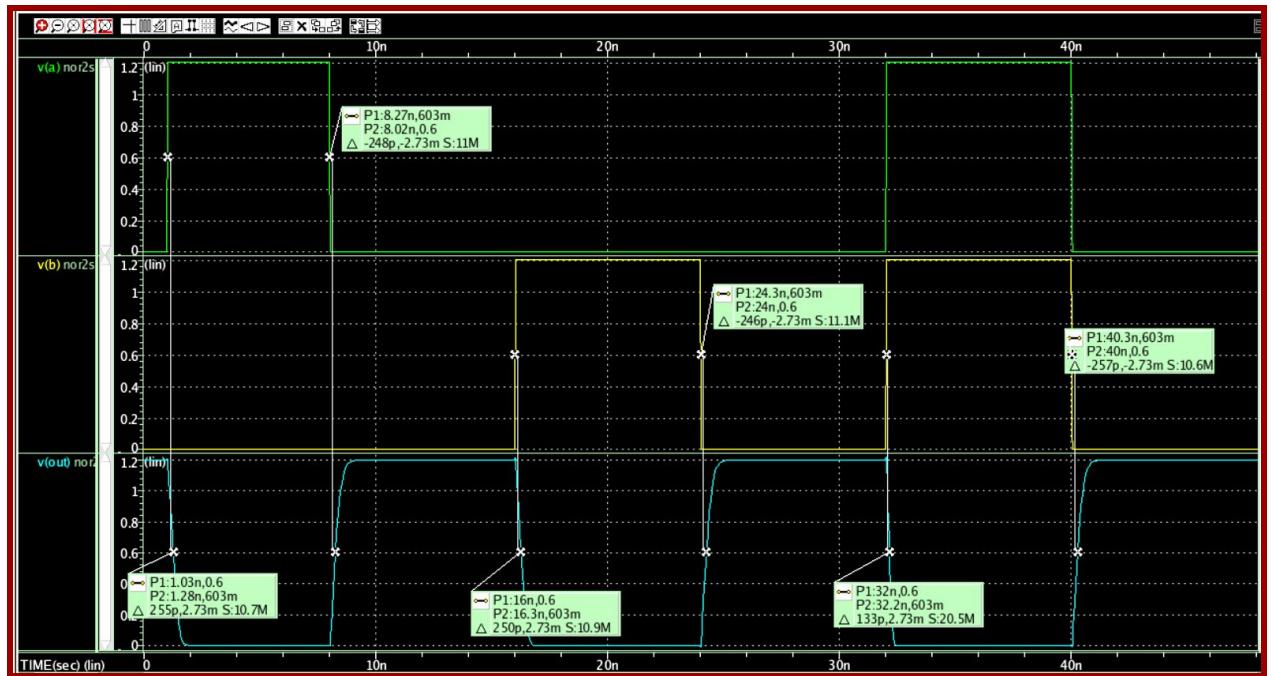


b) Symbol :-

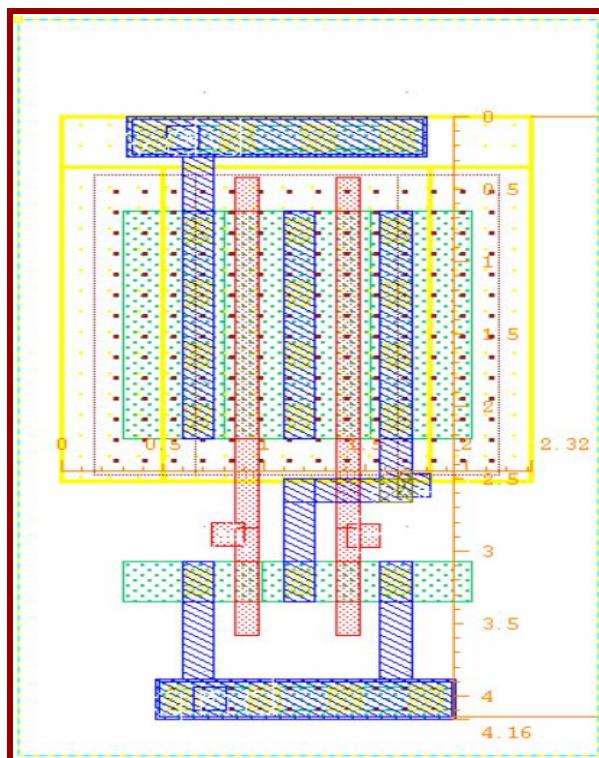


END

c) Simulation Waveform :-

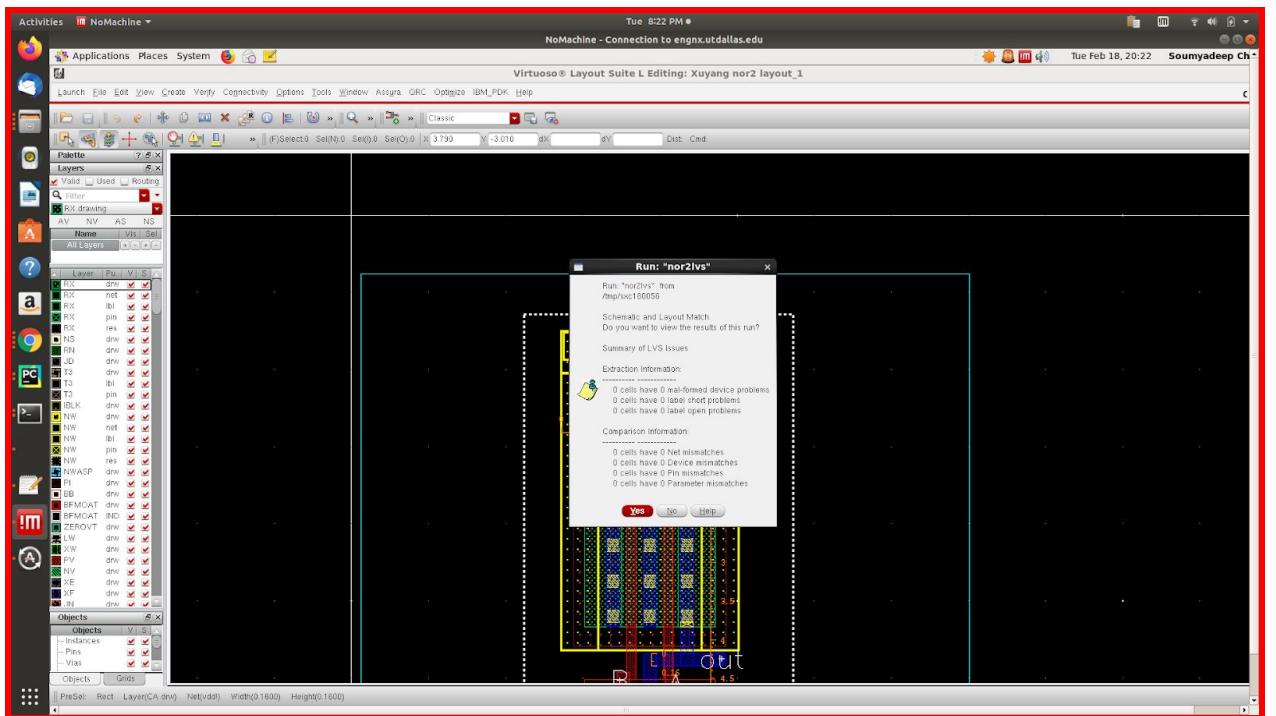


d) Layout



END

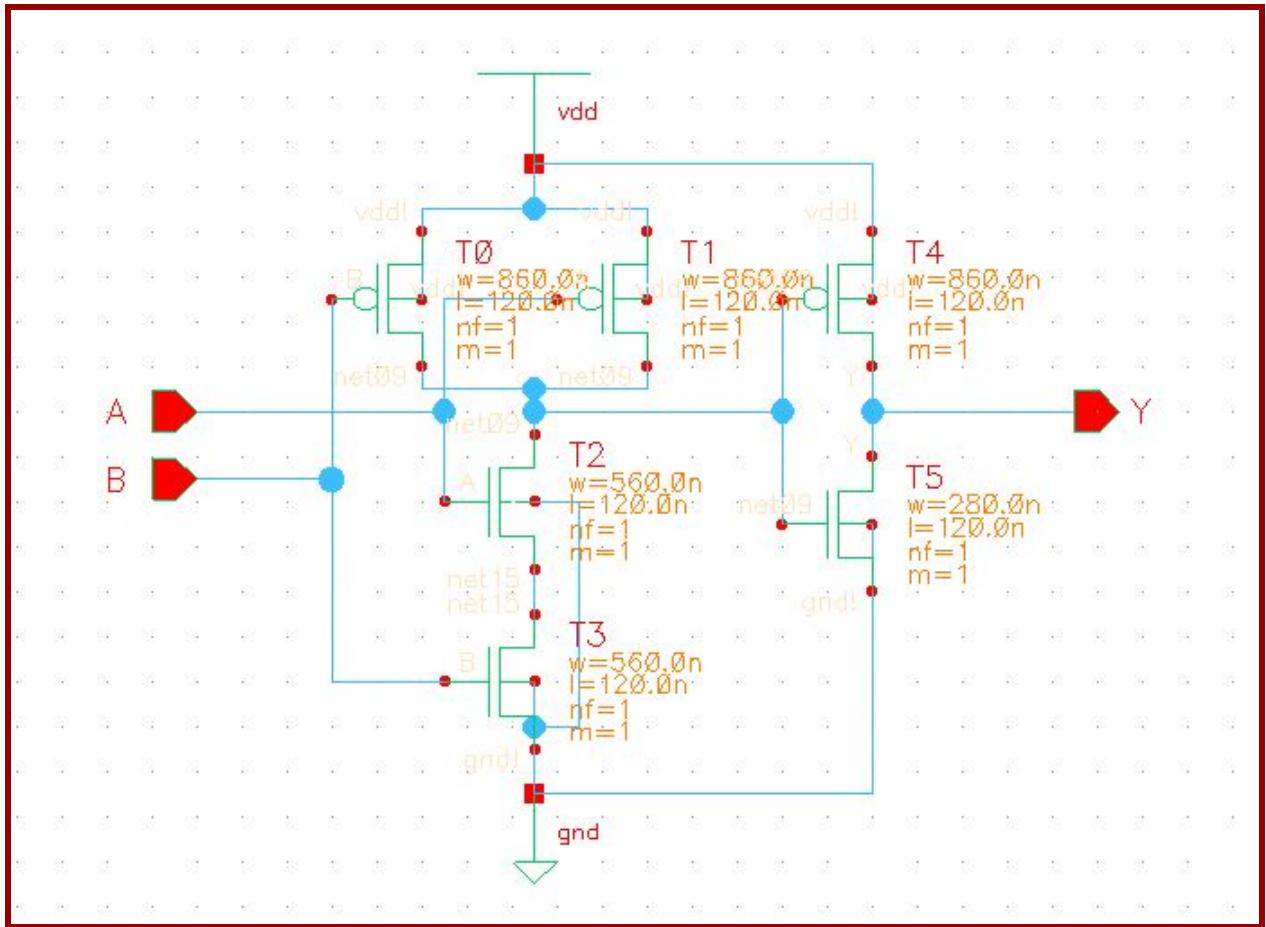
e) LVS Report



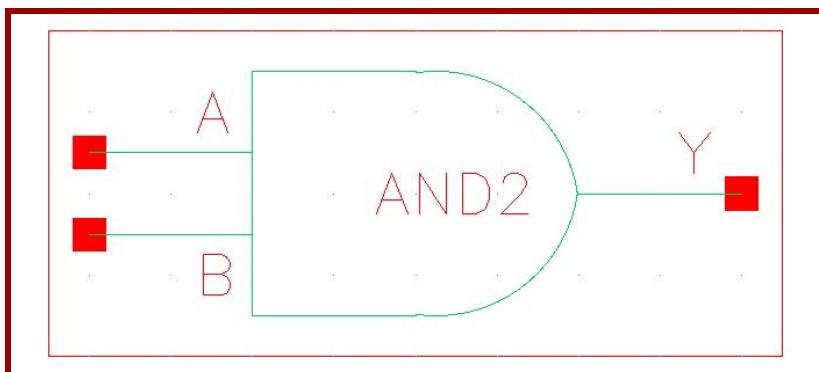
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4.) AND - 2 Operation

a) Schematic :-

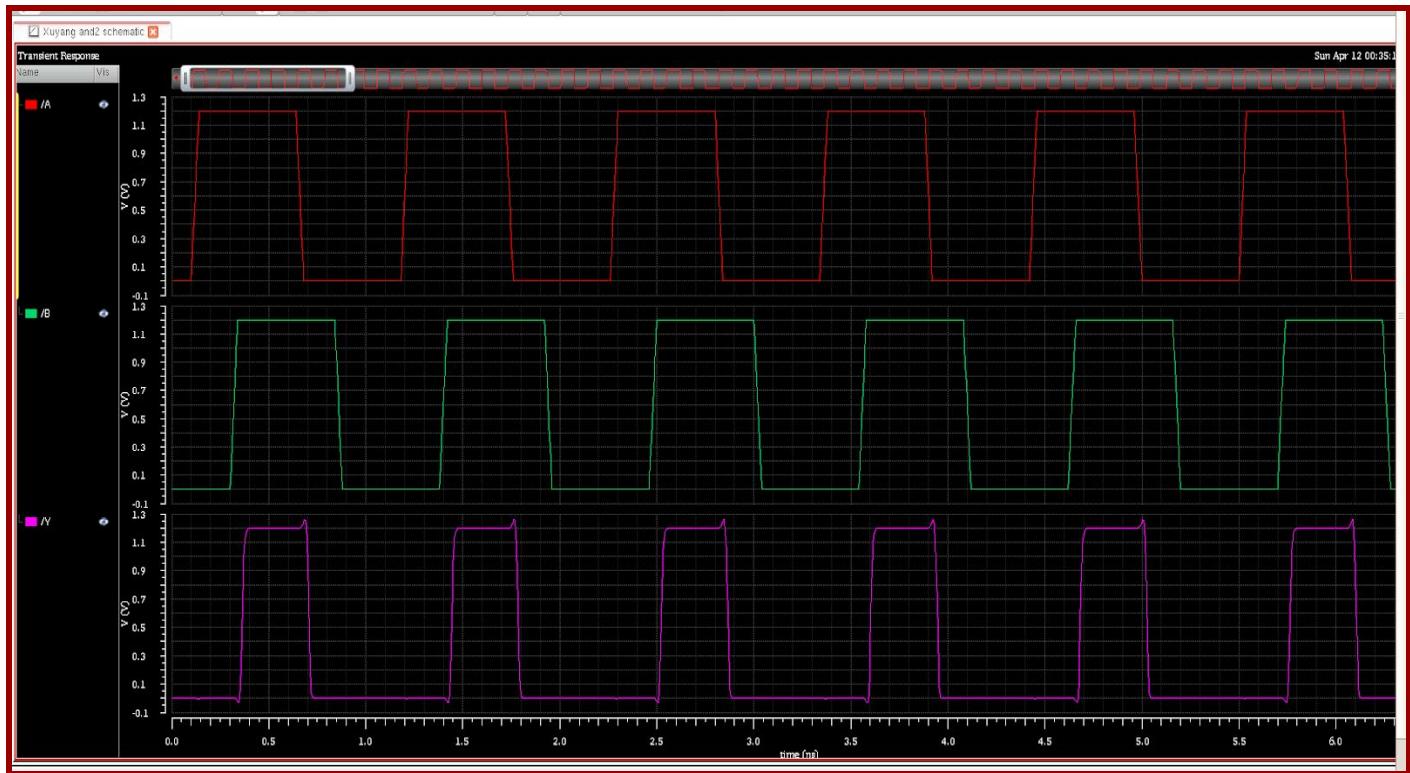


b) Symbol :-



END

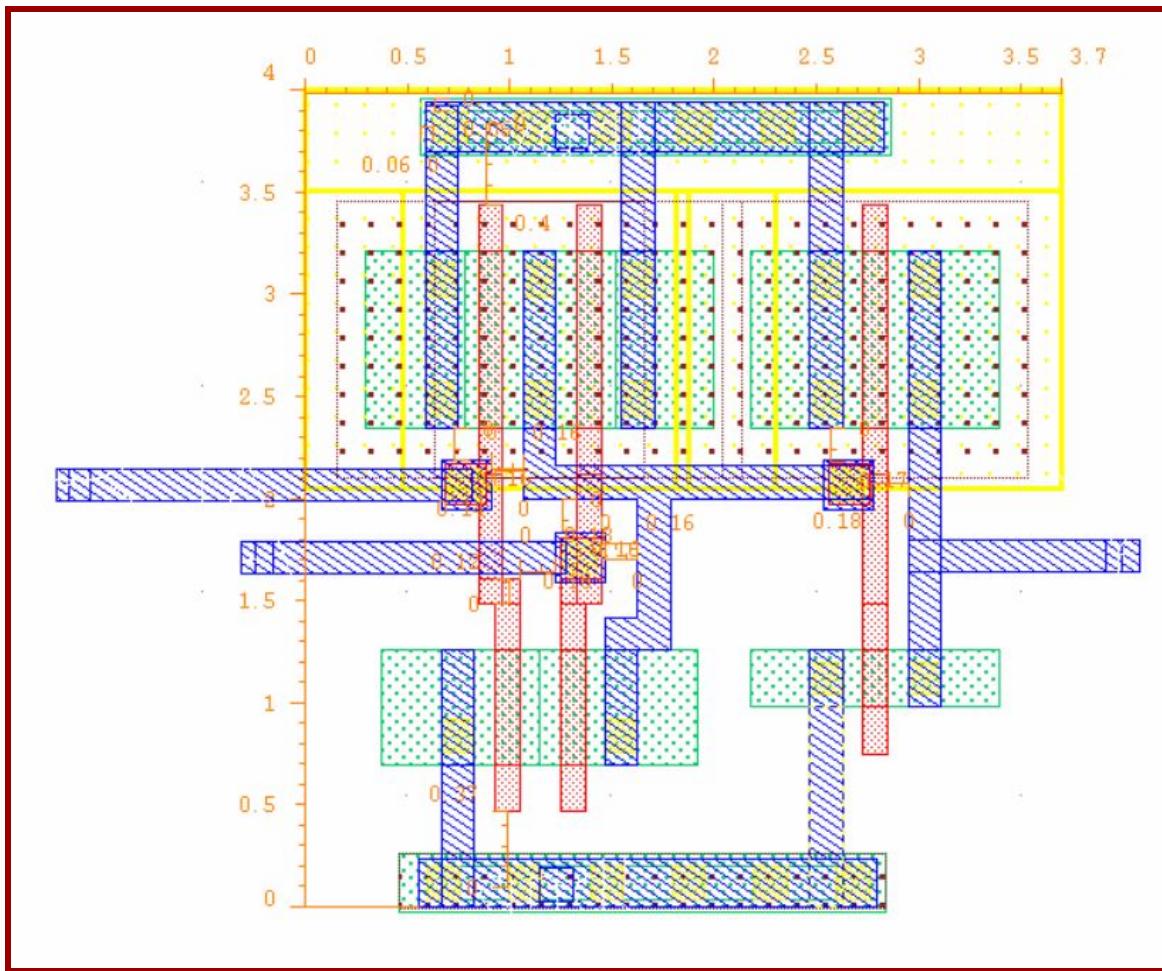
c) Simulation Waveform :-



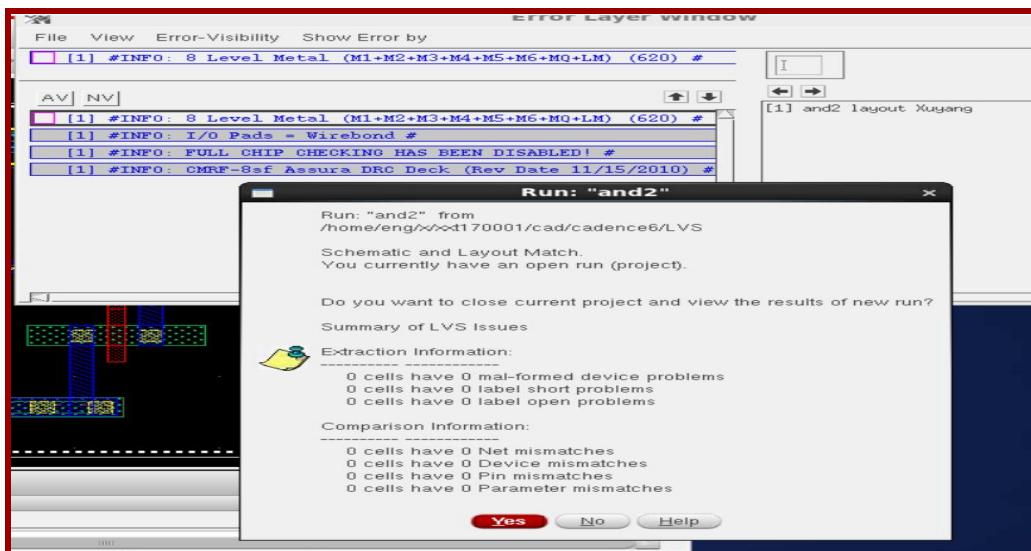
d) Layout

Next Page...

END



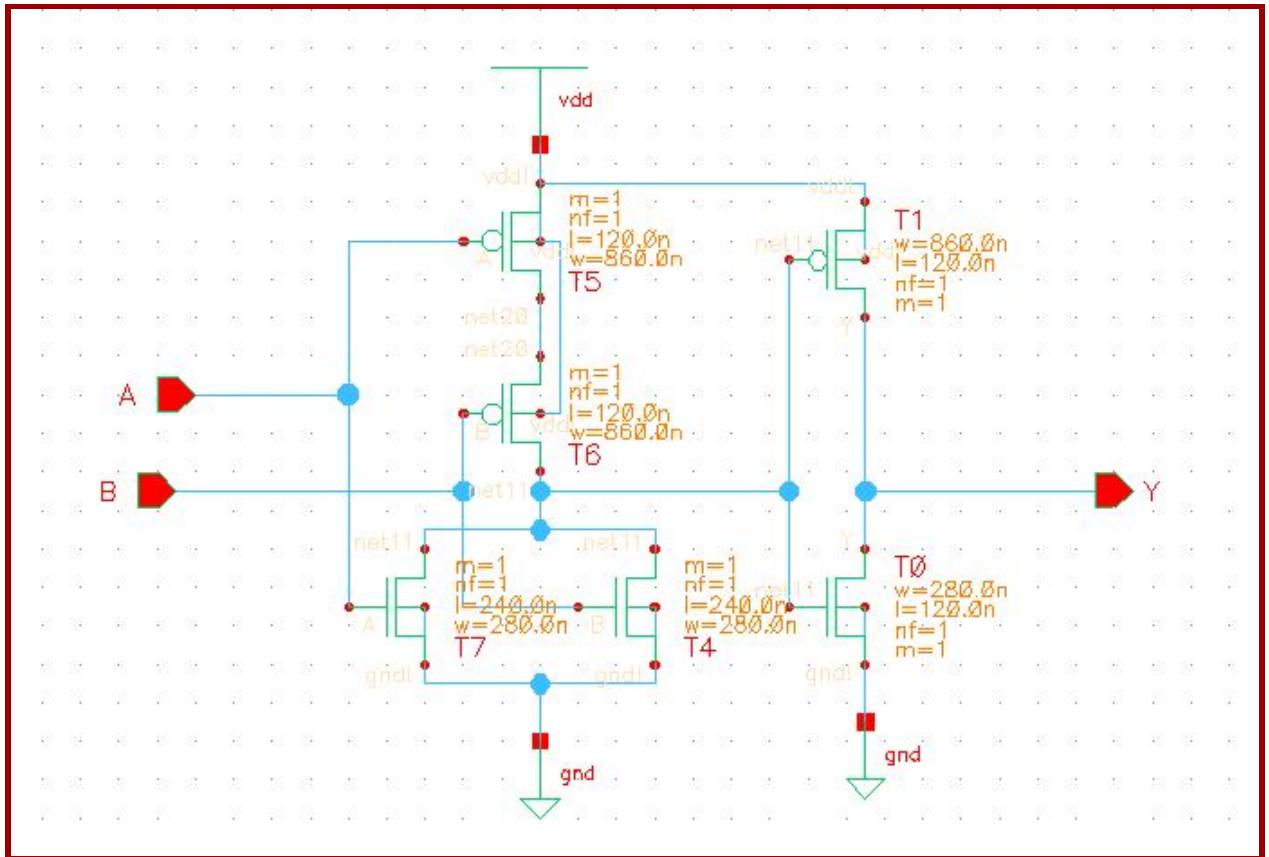
e) LVS Report



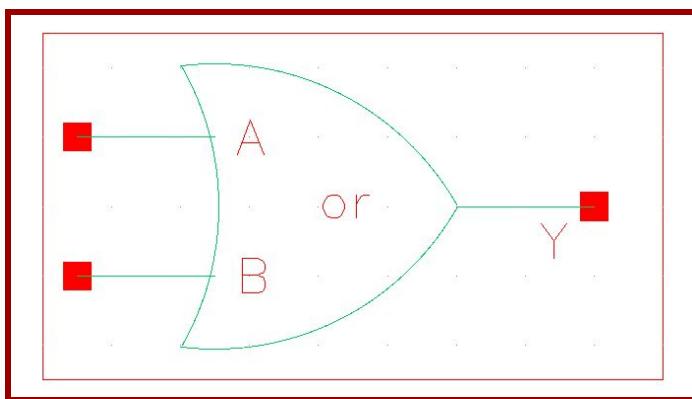
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5.) OR - 2 Operation

a) Schematic :-

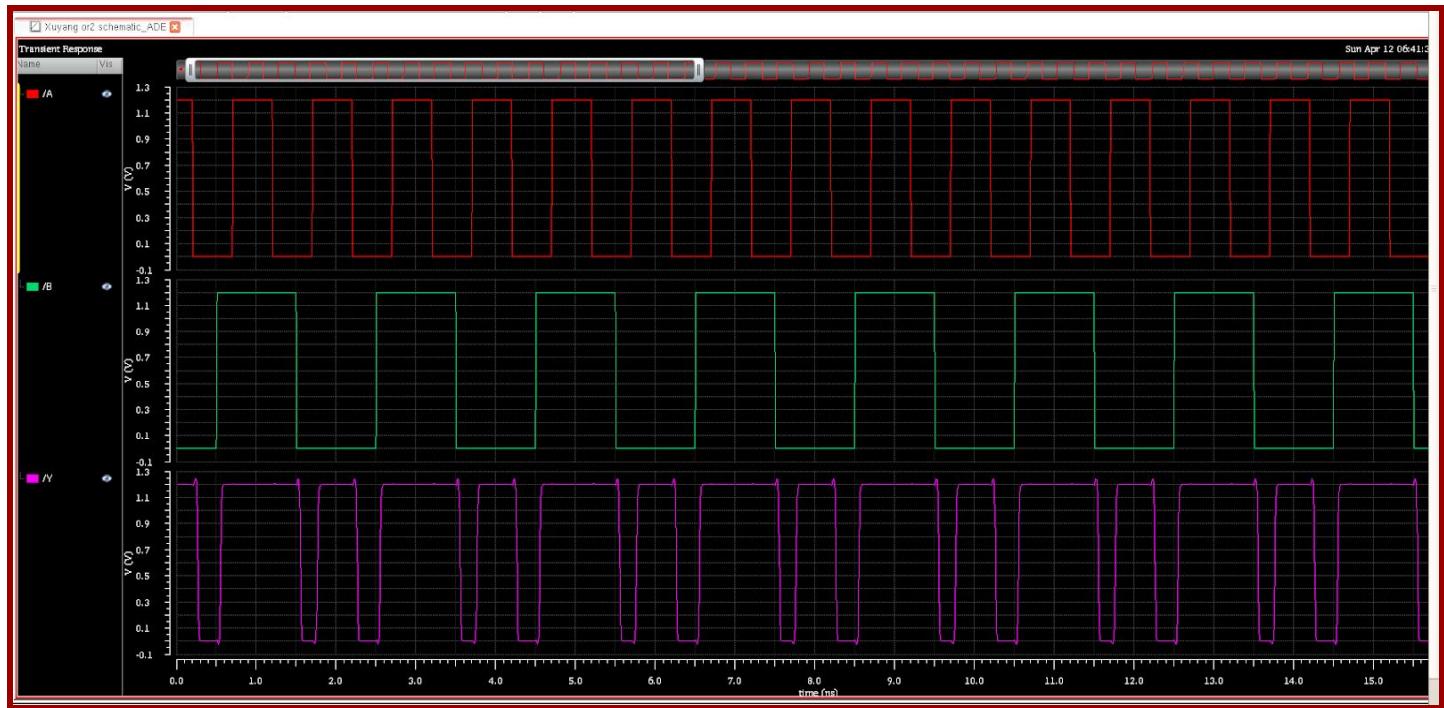


b) Symbol :-



END

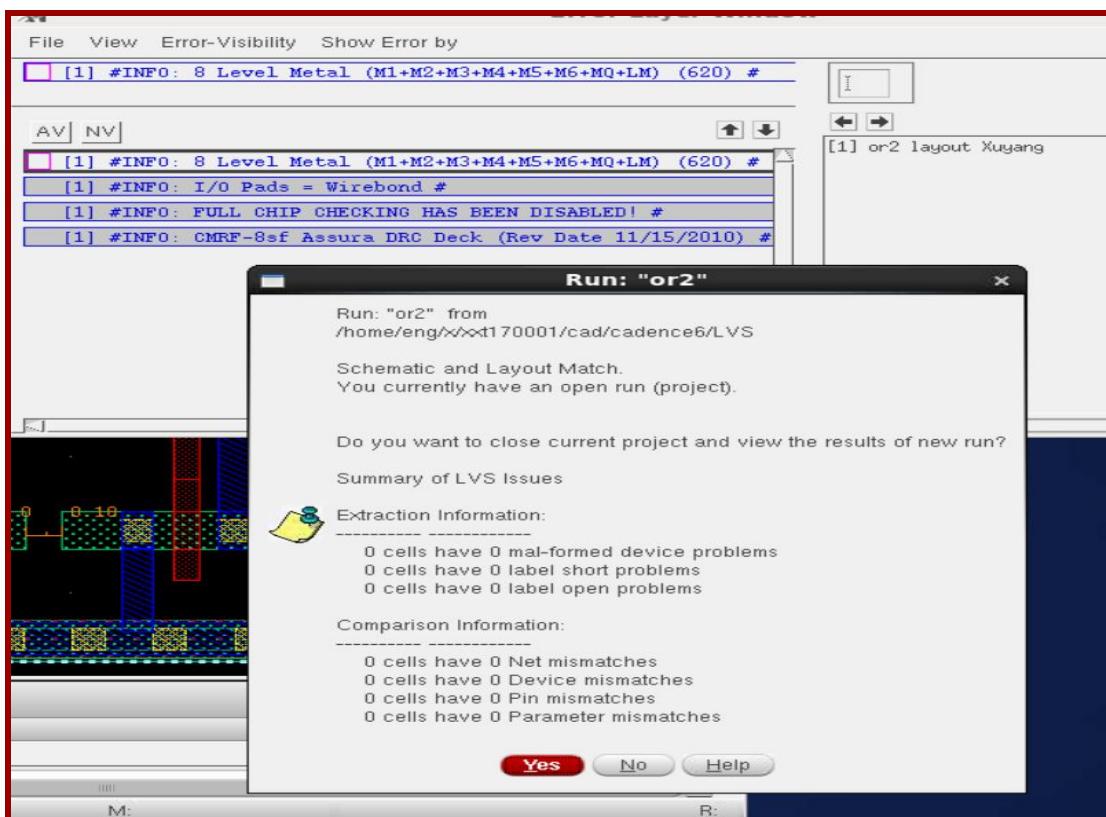
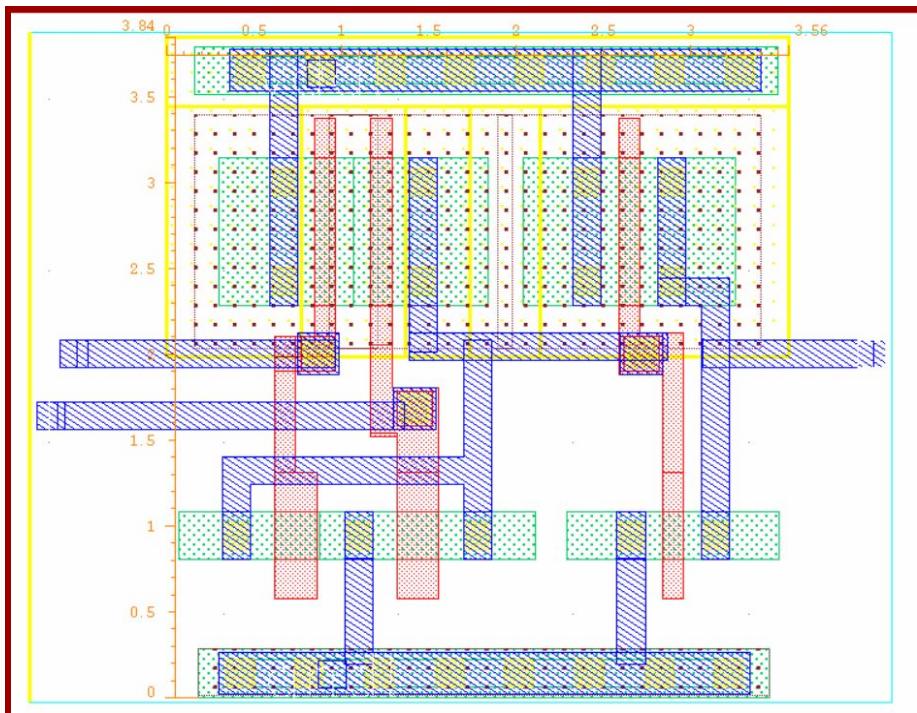
c) Simulation Waveform :-



d) Layout

Next Page

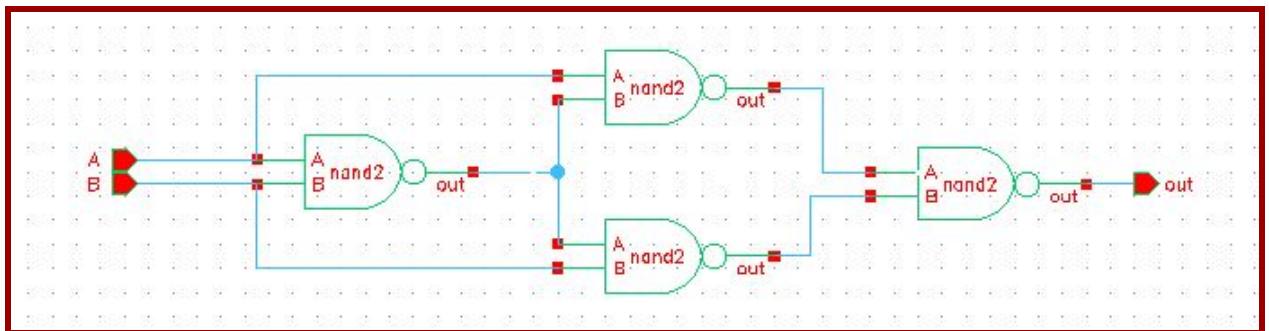
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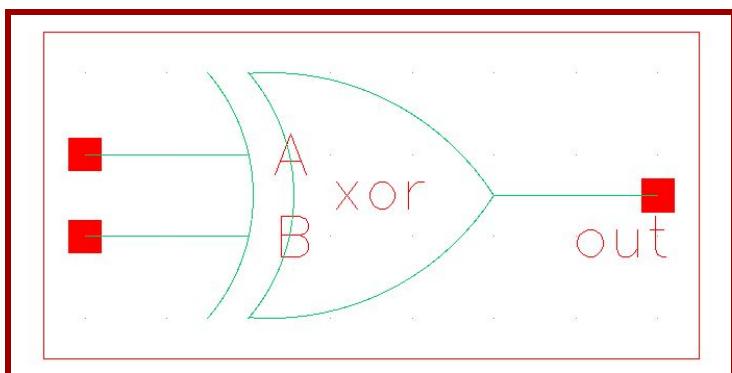
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6.) XOR - 2 Operation

a) Schematic :-



b) Symbol :-

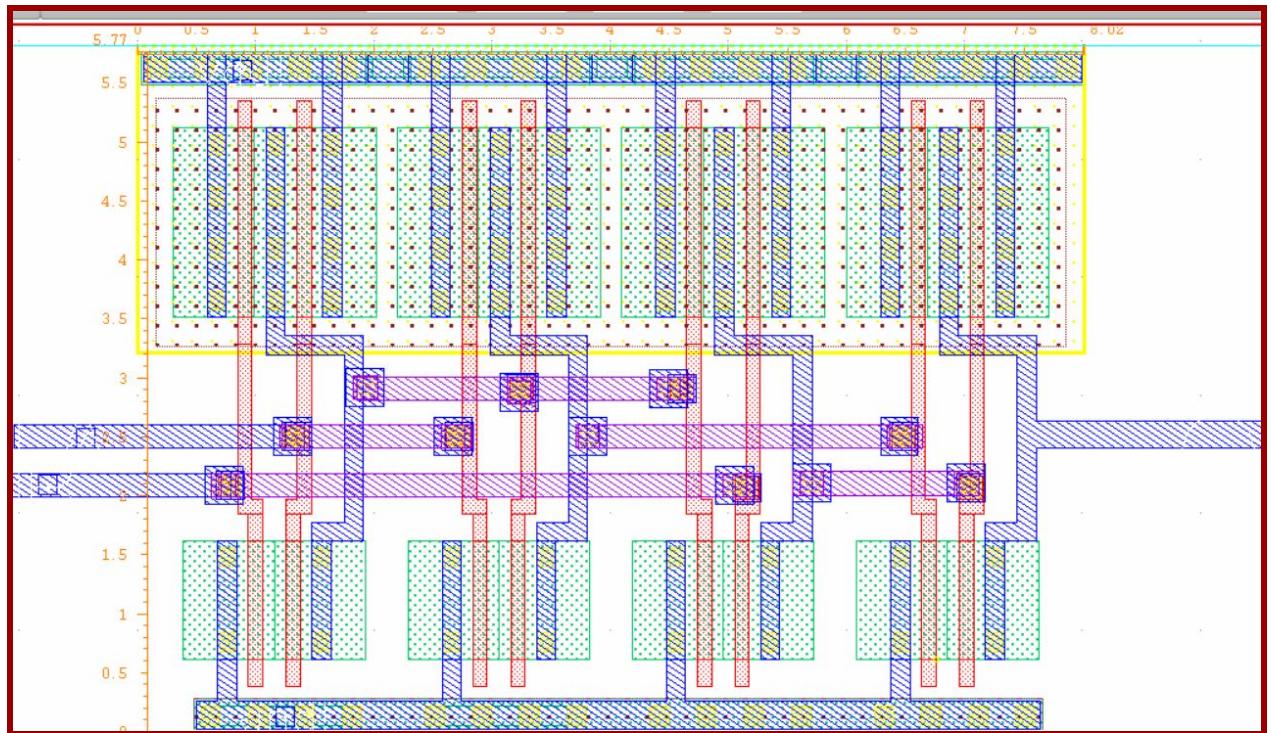


END

c) Simulation Waveform :-

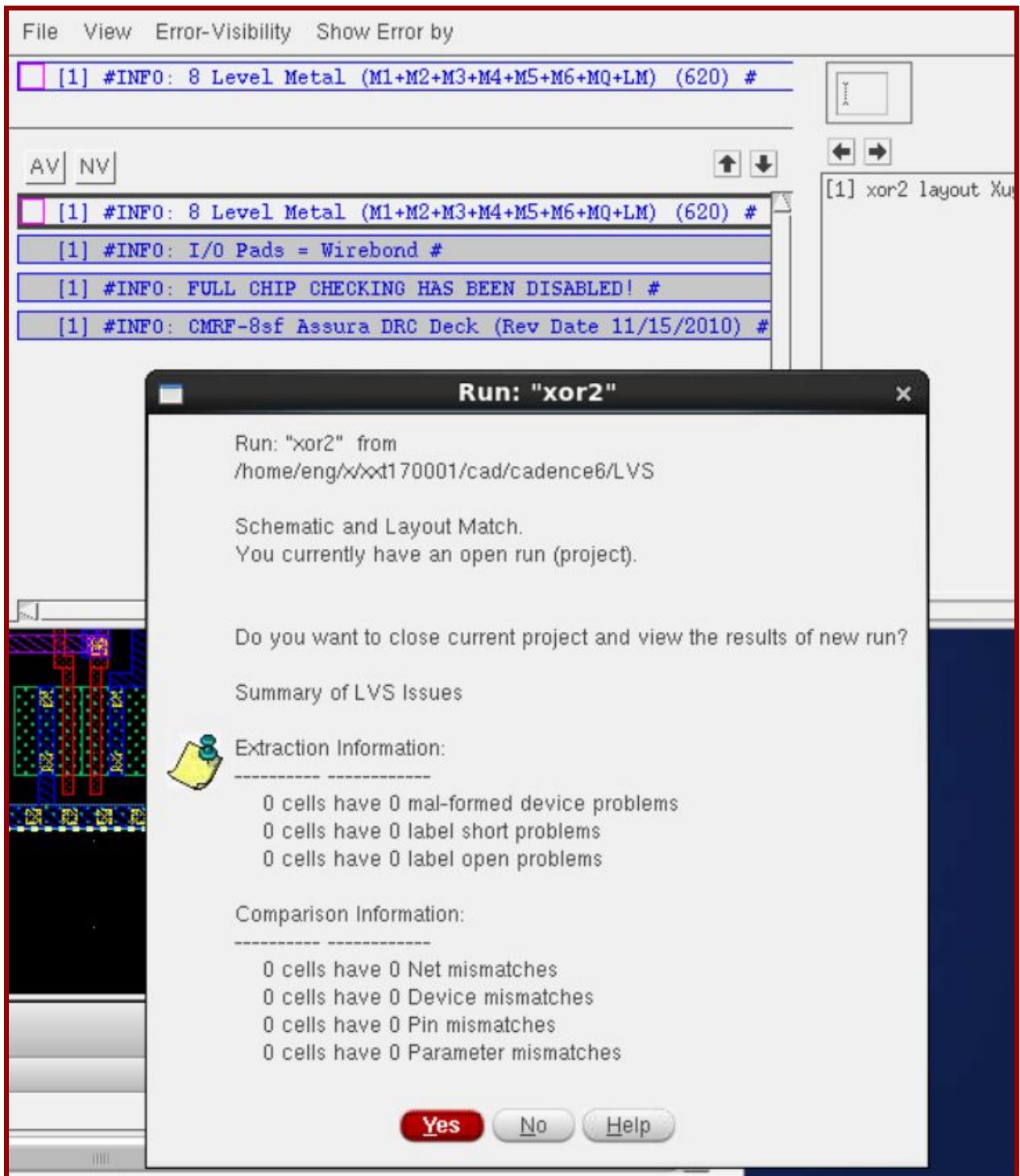


d) Layout



END

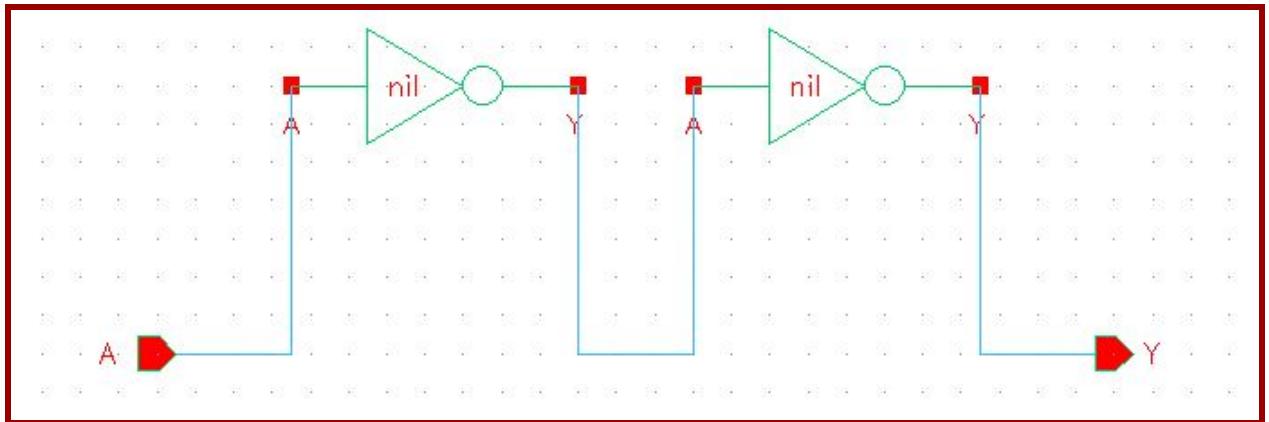
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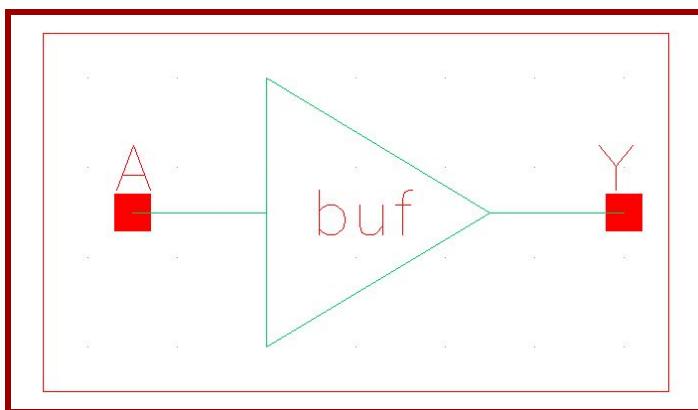
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7.) Buffer Operation

a) Schematic :-



b) Symbol :-



END

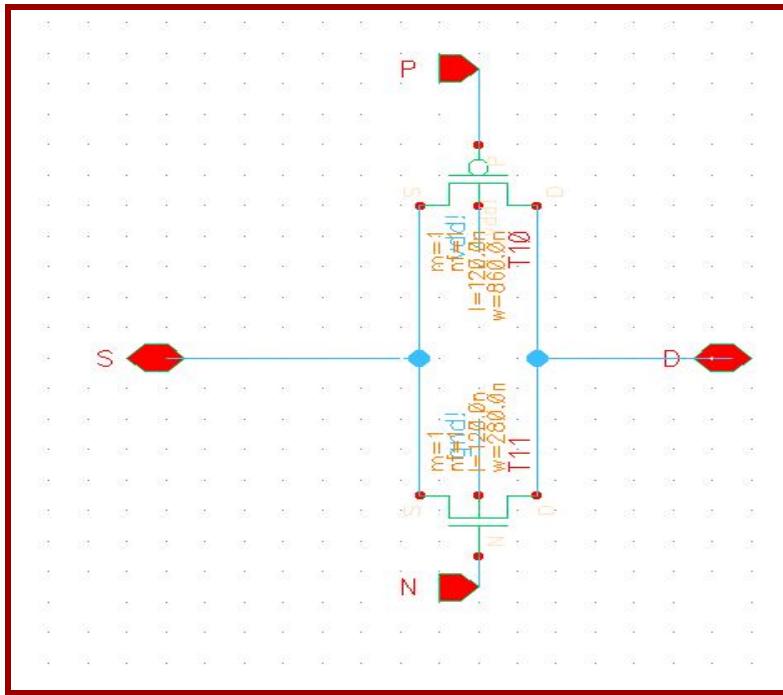
c) Simulation Waveform :-



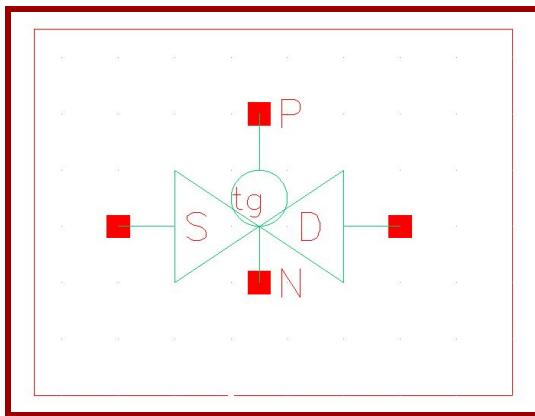
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8.) Transgate Operation

a) Schematic :-

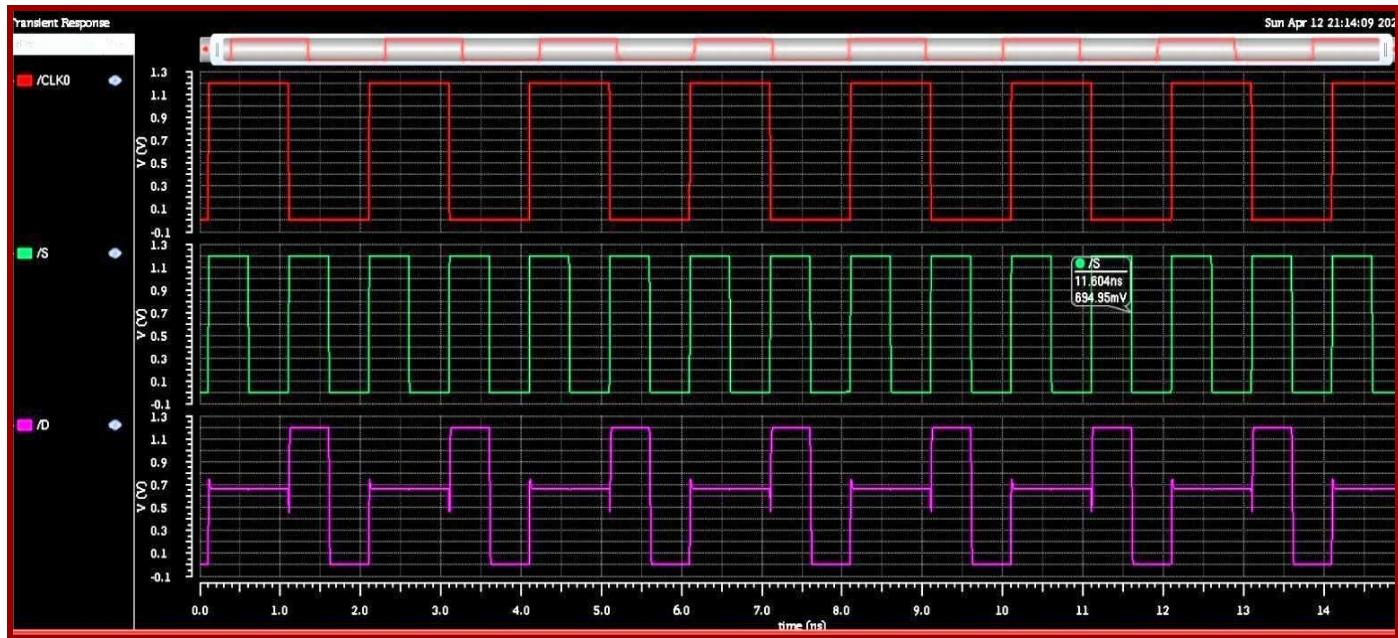


b) Symbol :-



END

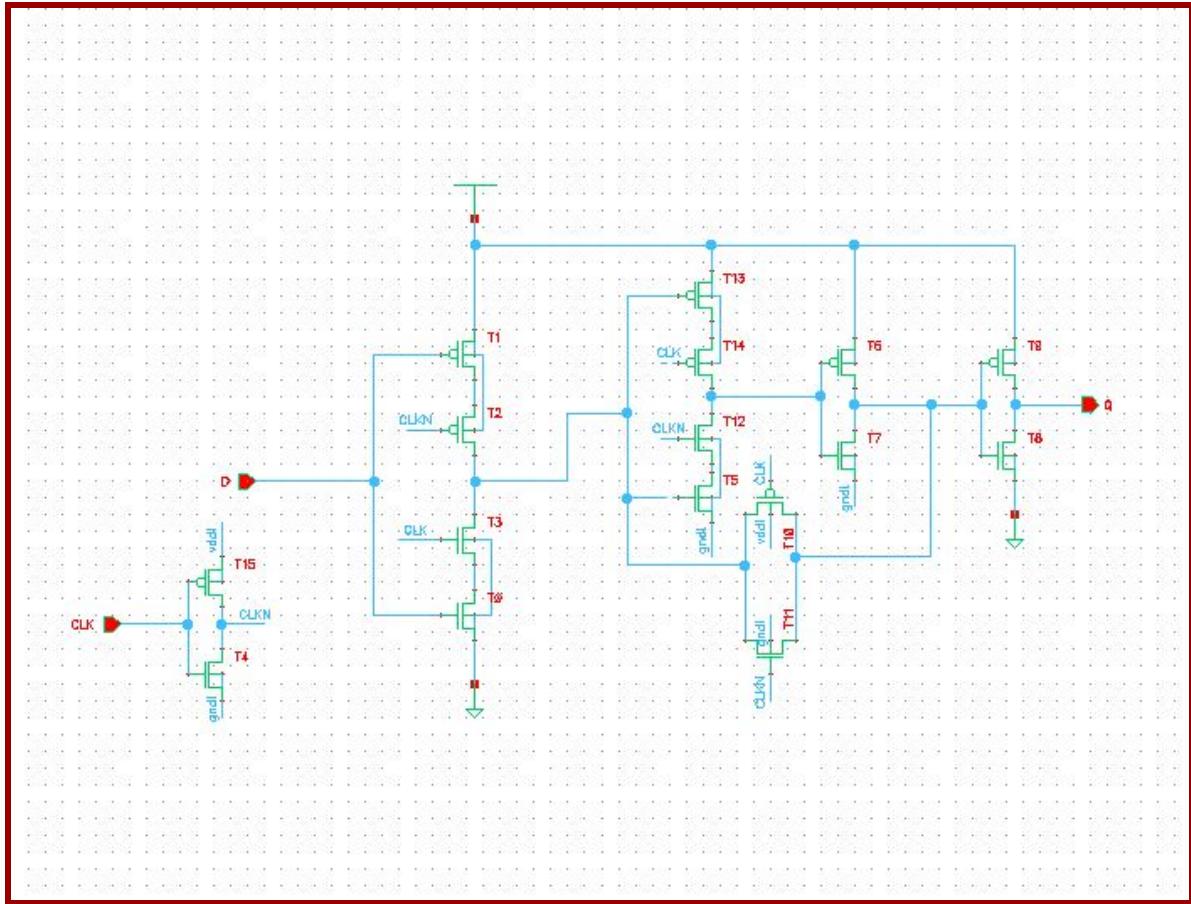
c) Simulation Waveform :-



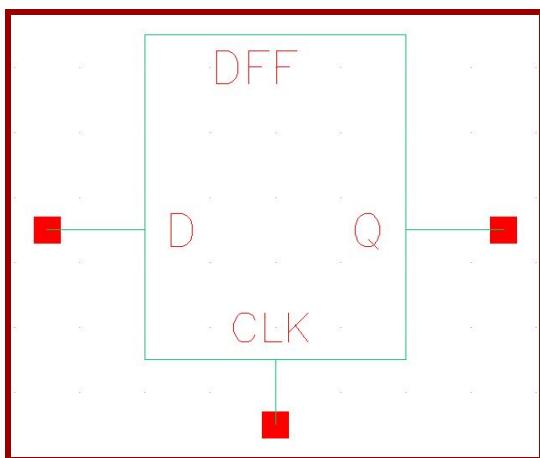
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9.) D - Flip Flop Operation

a) Schematic :-

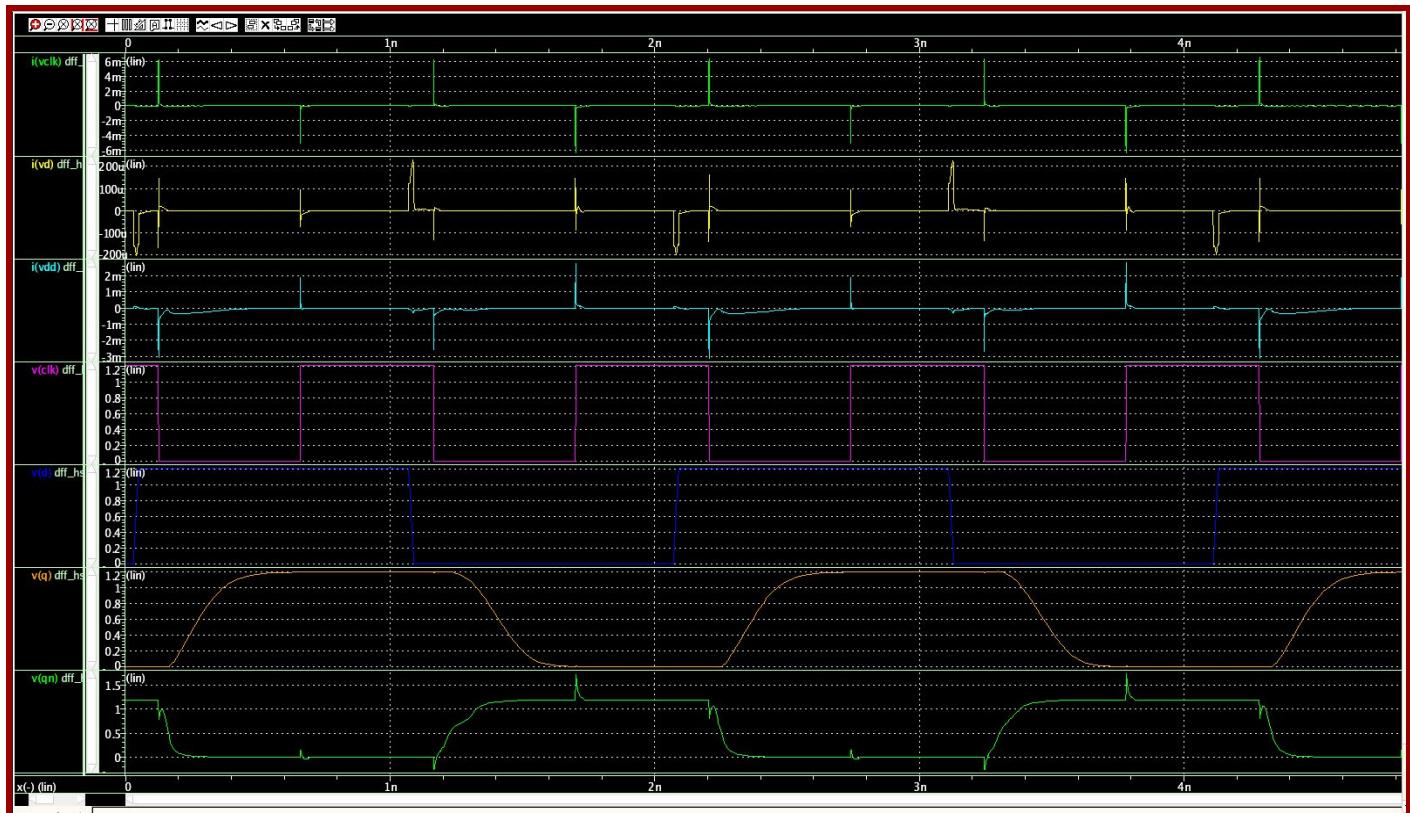


b) Symbol :-

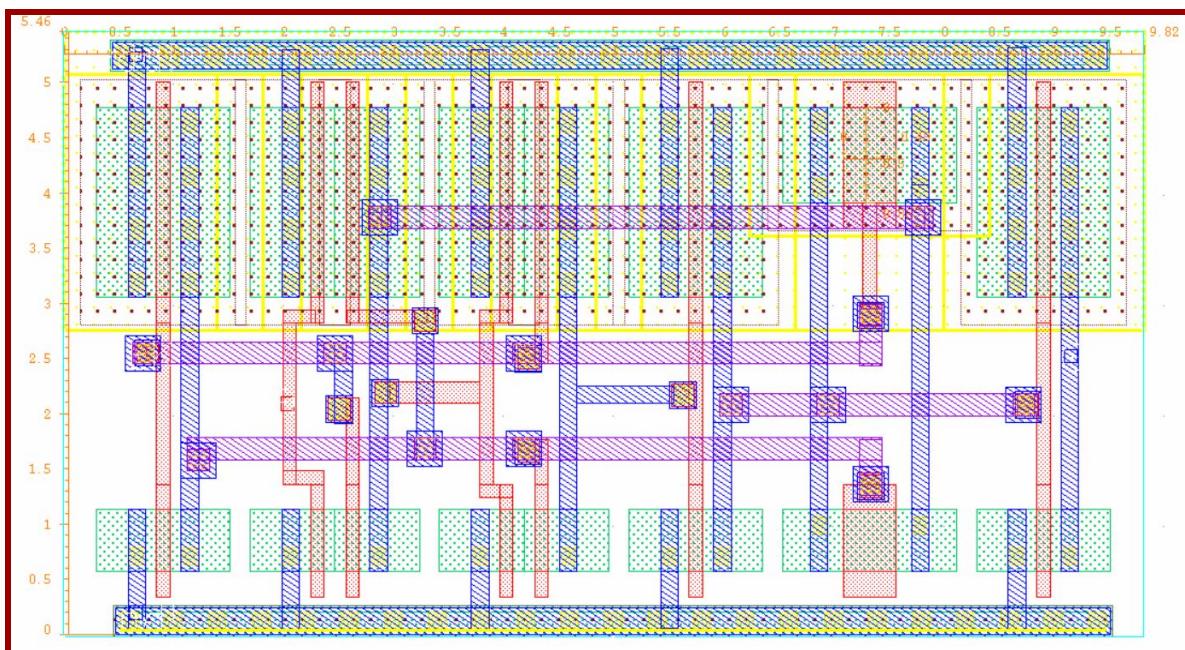


END

c) Simulation Waveform :-

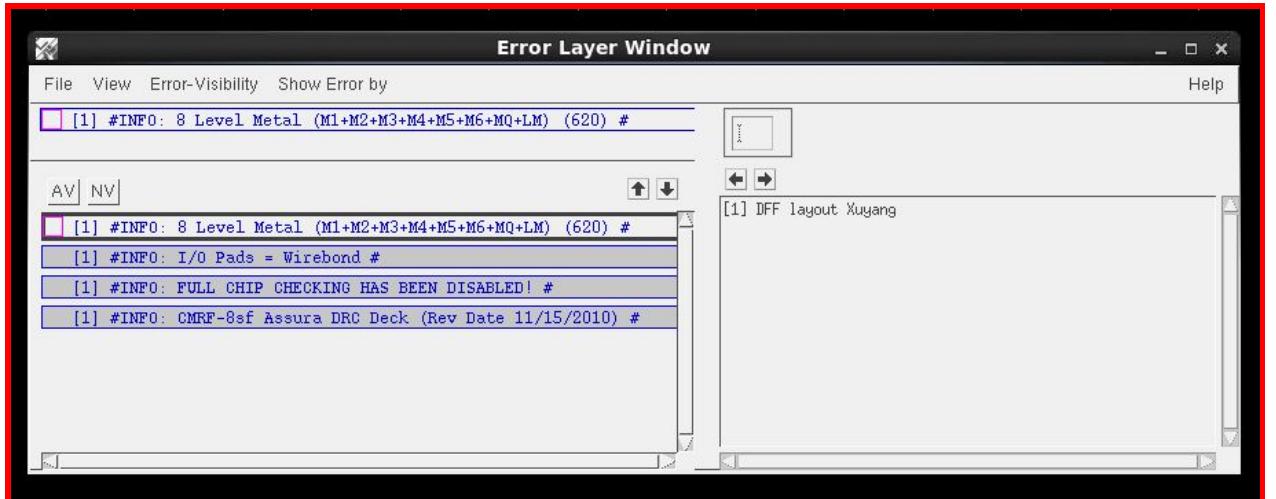


d) Layout



END

e) LVS Report



The image contains two side-by-side windows from the Cadence environment.

Left Window (Run: "dfflvs"):

Run: "dfflvs" from /tmp/sxc180056

Schematic and Layout Match.
You currently have an open run (project).

Do you want to close current project and view the results of new run?

Summary of LVS Issues

Extraction Information:

- 0 cells have 0 mal-formed device problems
- 0 cells have 0 label short problems
- 0 cells have 0 label open problems

Comparison Information:

- 0 cells have 0 Net mismatches
- 0 cells have 0 Device mismatches
- 0 cells have 0 Pin mismatches
- 0 cells have 0 Parameter mismatches

Buttons: Yes, No, Help

Right Window (LVS Debug - dfflvs):

File View Options Tools Help

cadence

Cell List (sch || lay) Extract Compare Summary (sch || lay)

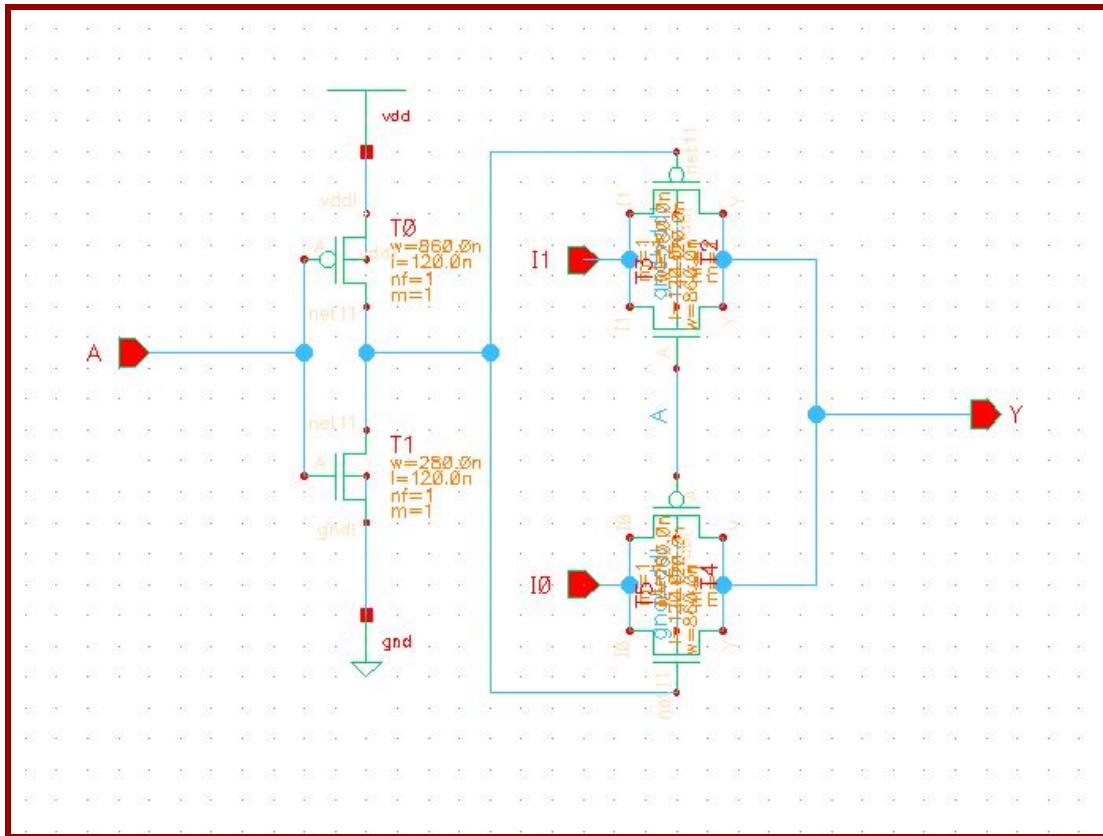
*** Schematic and Layout Match

Open Schematic Cell... Open Layout Cell... Open Tool...

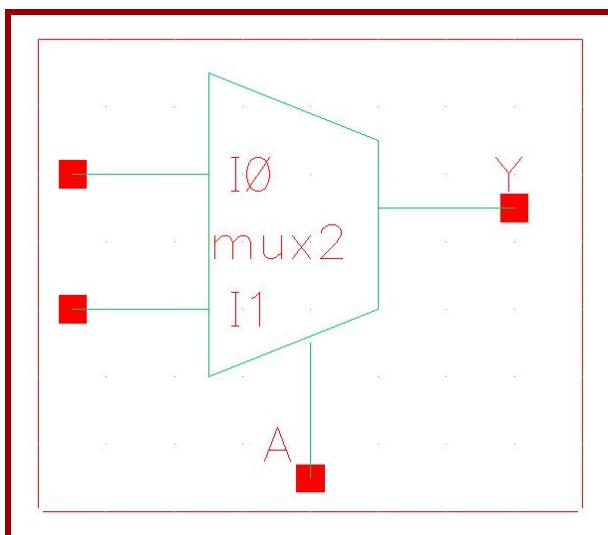
END

10.) 2:1 Multiplexer (MUX) Operation

a) Schematic :-

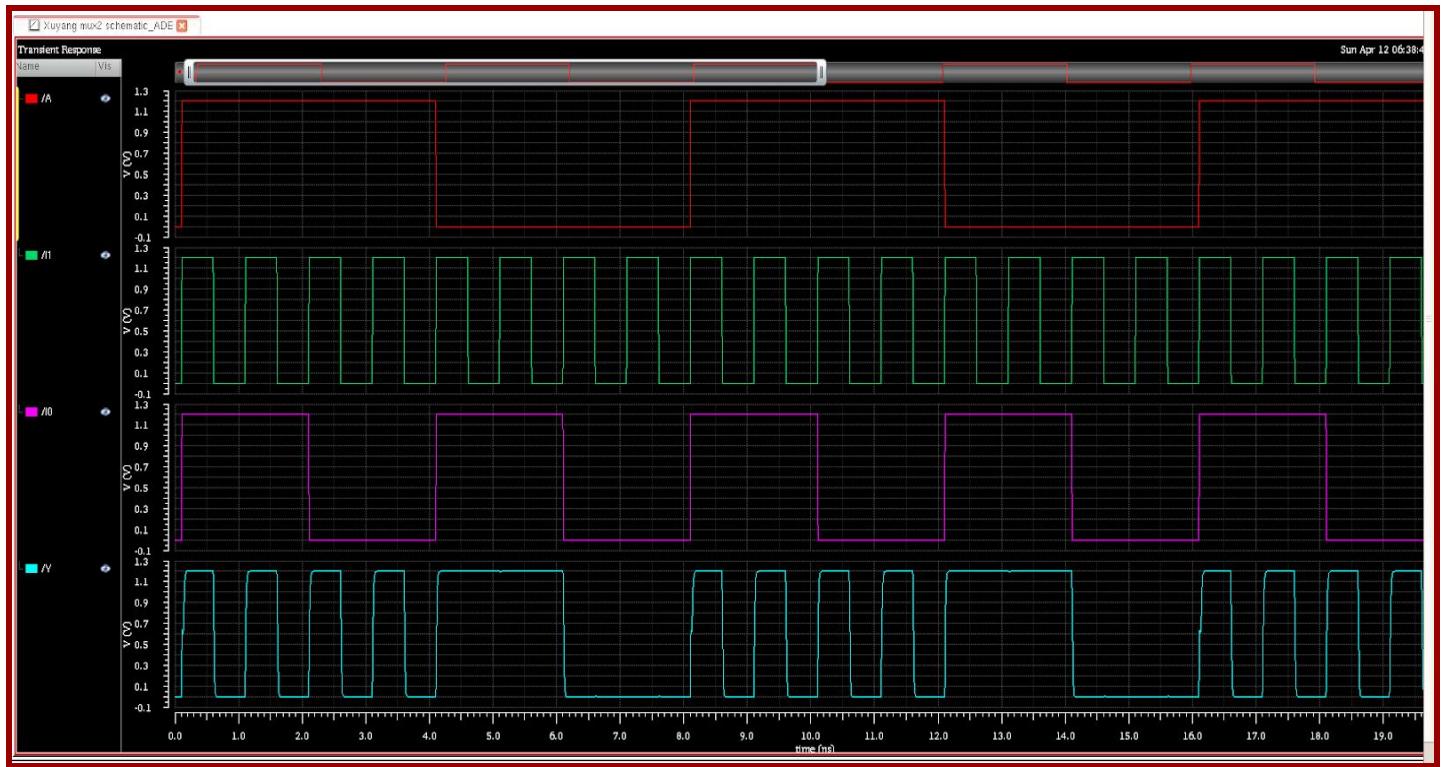


b) Symbol :-



END

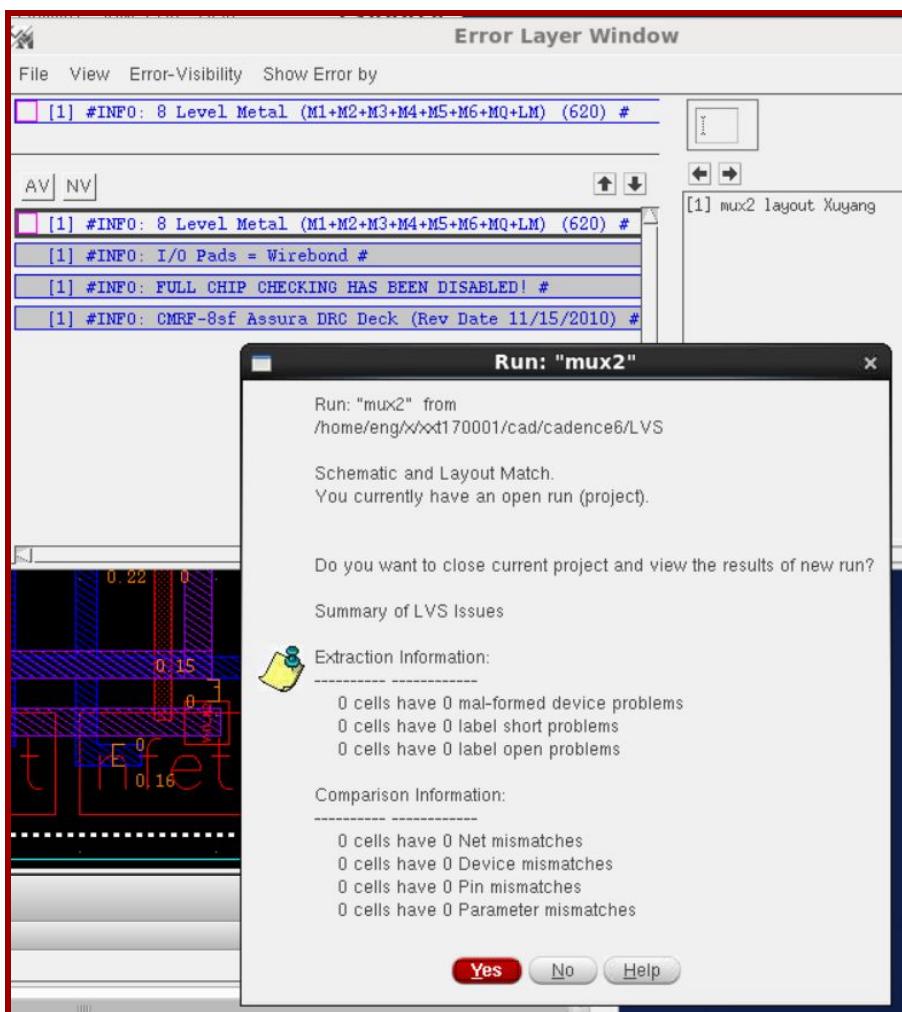
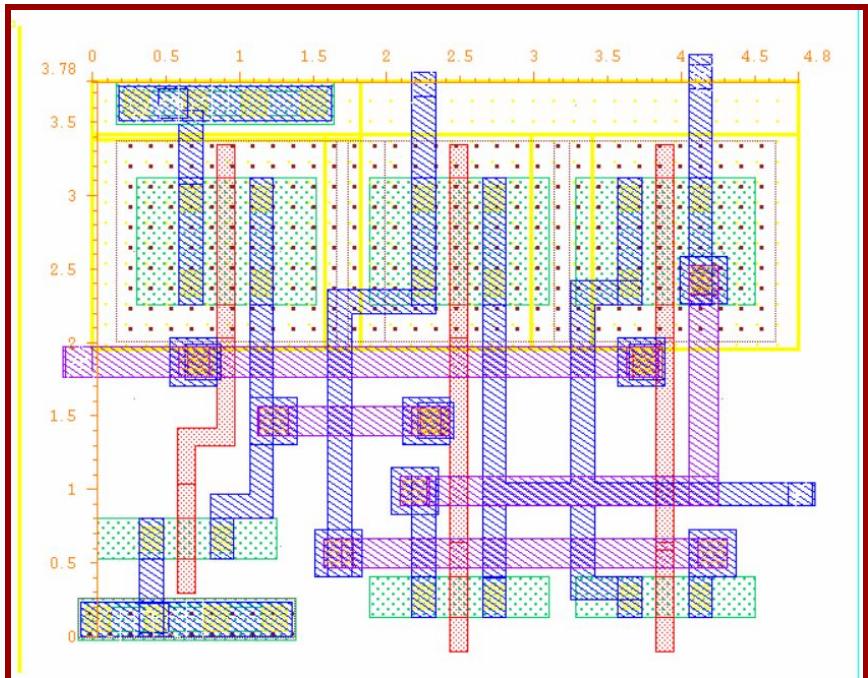
c) Simulation Waveform :-



d) Layout

Next Page

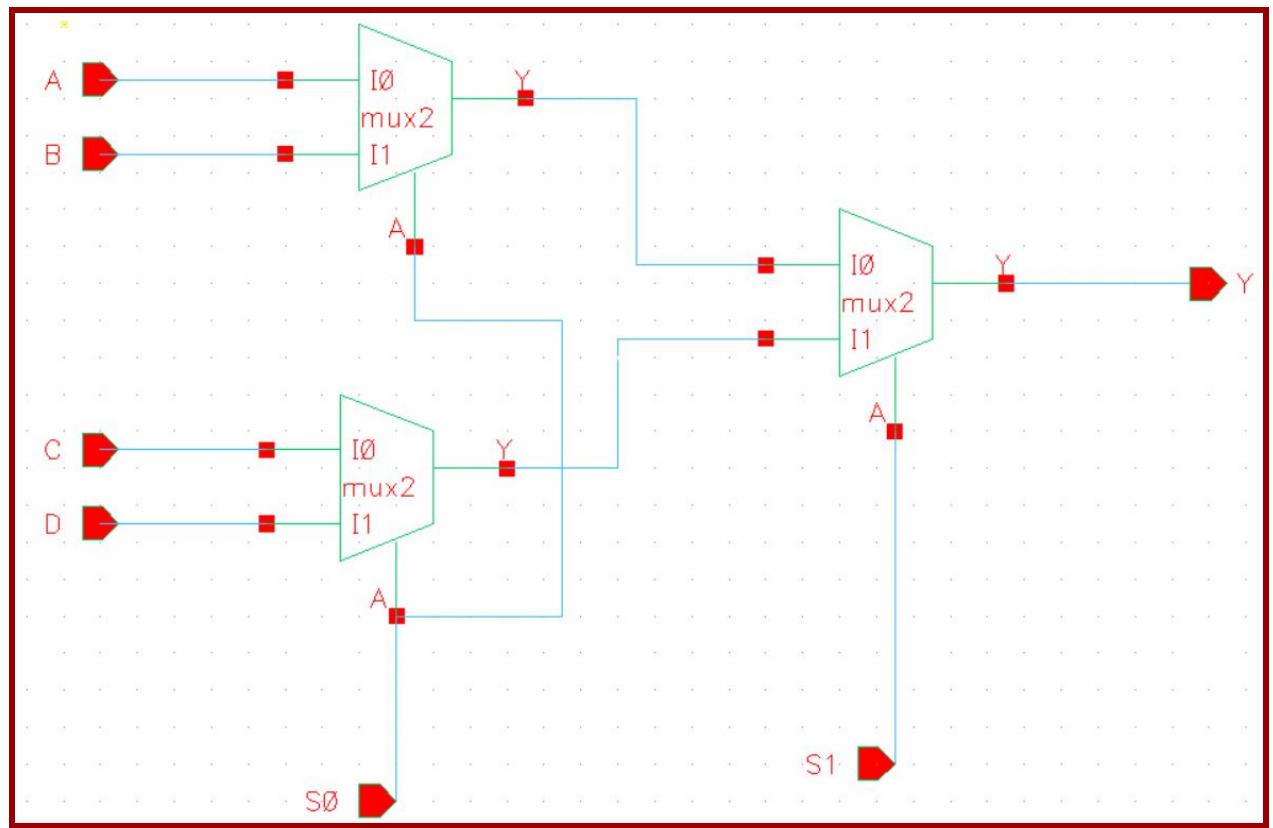
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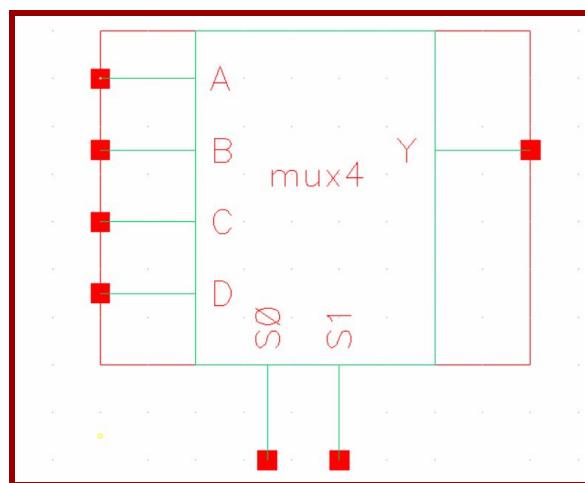
END

11) MUX4 Operation

a) Schematic

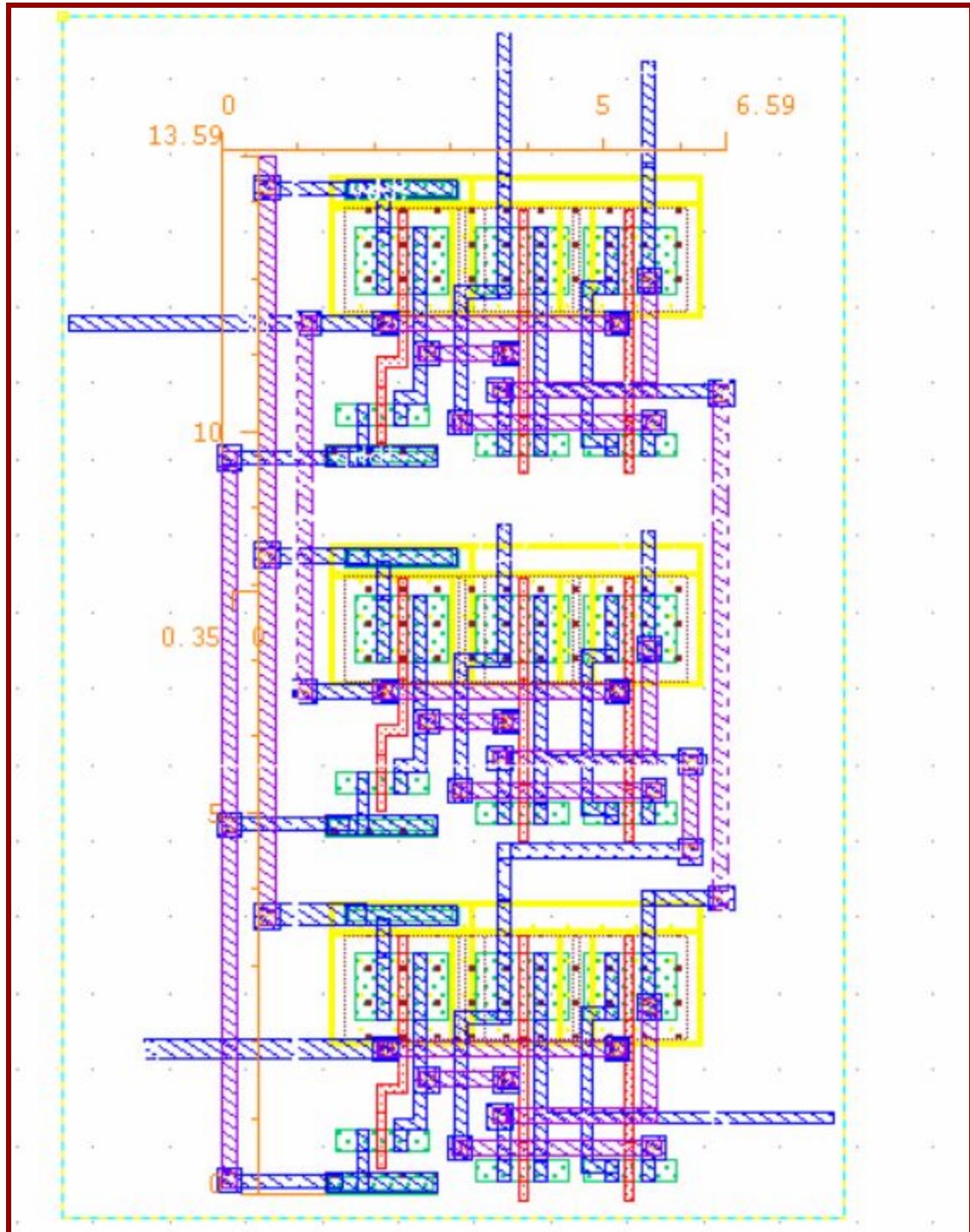


b) Symbol



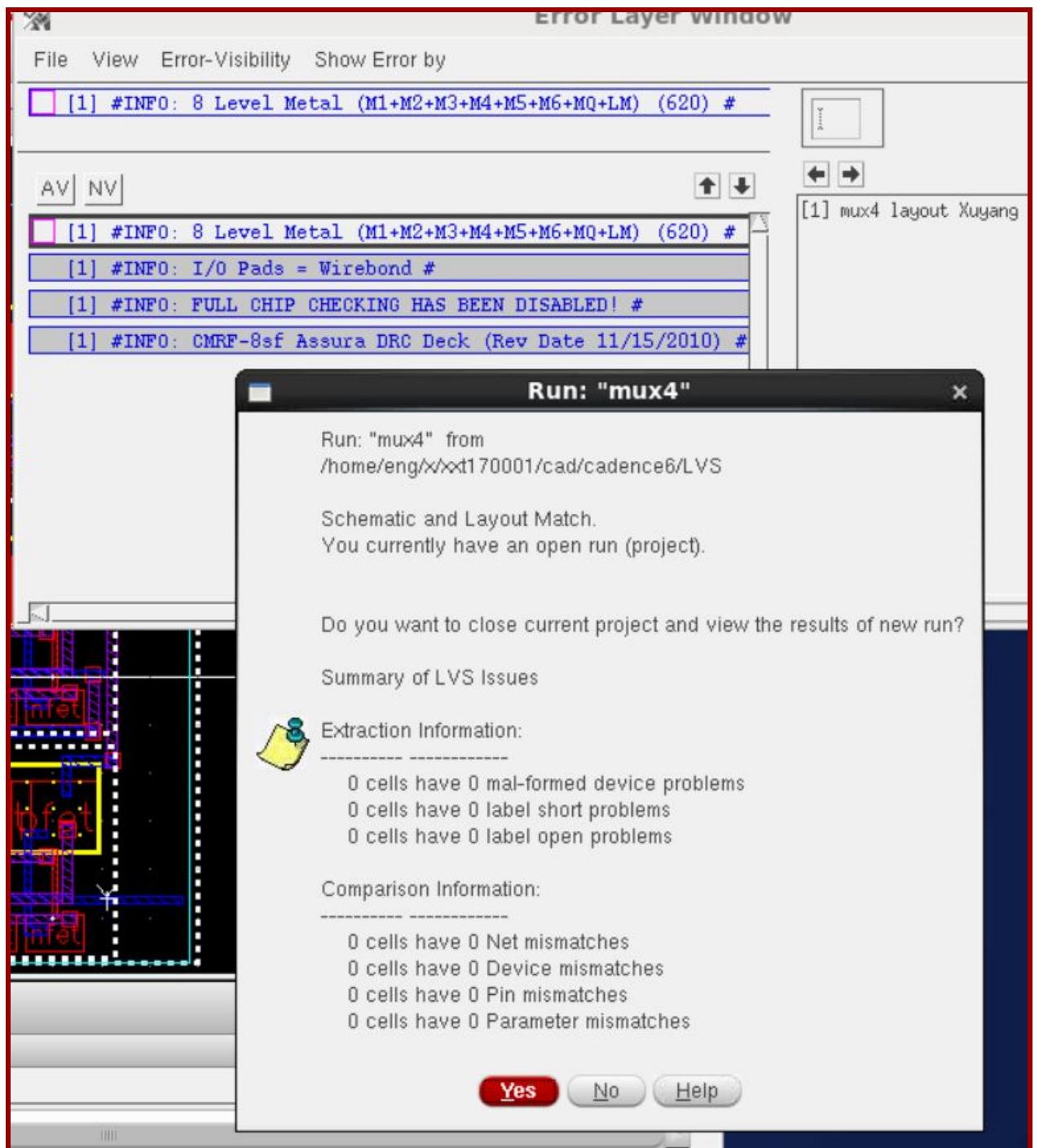
END

c) Layout



END

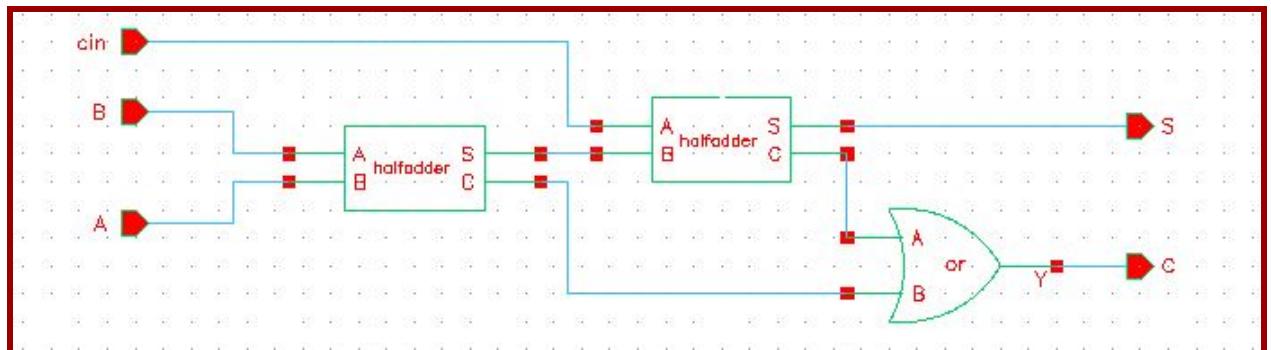
d) LVS Report



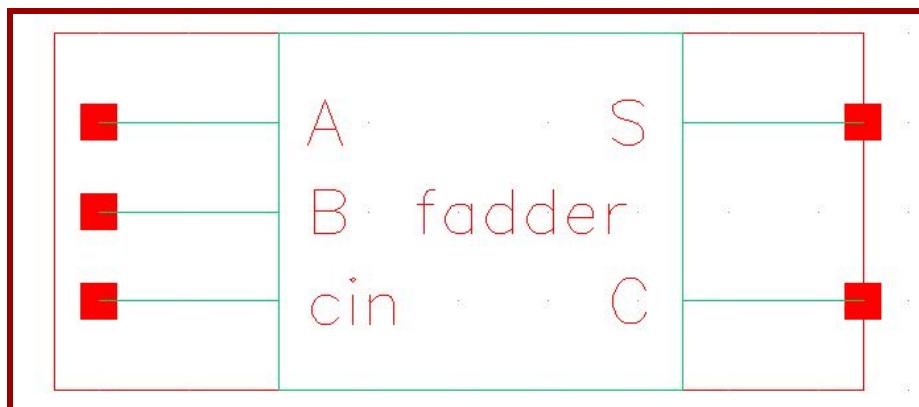
END

11.) Full Adder Operation

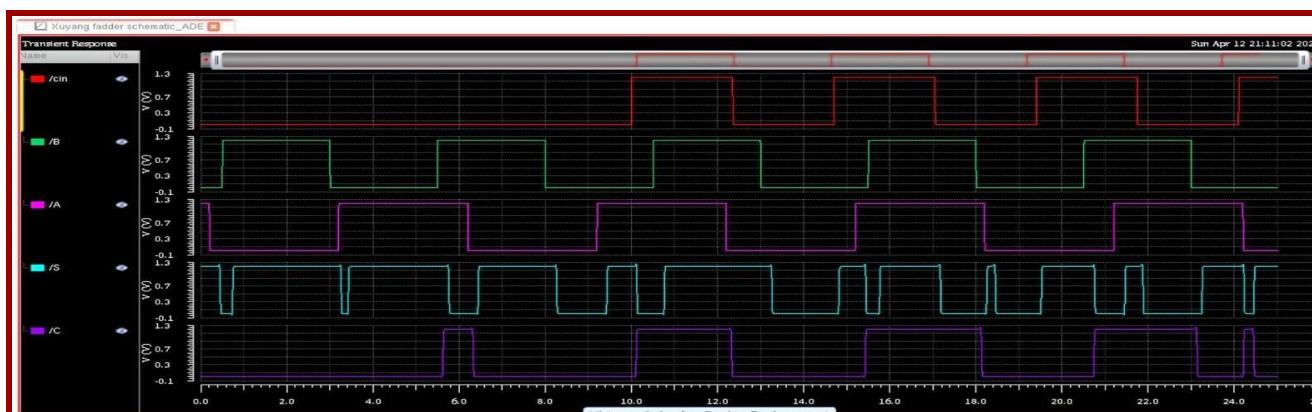
a) Schematic :-



b) Symbol :-

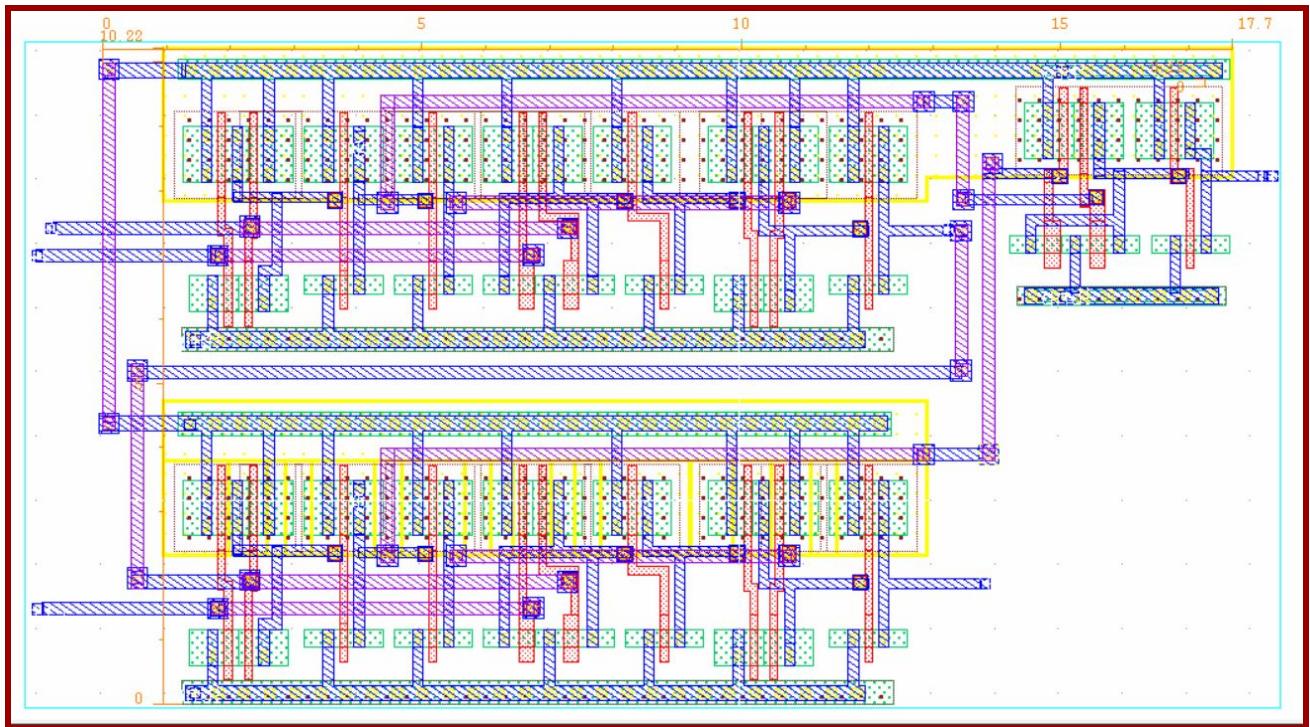


c) Simulation Waveform :-

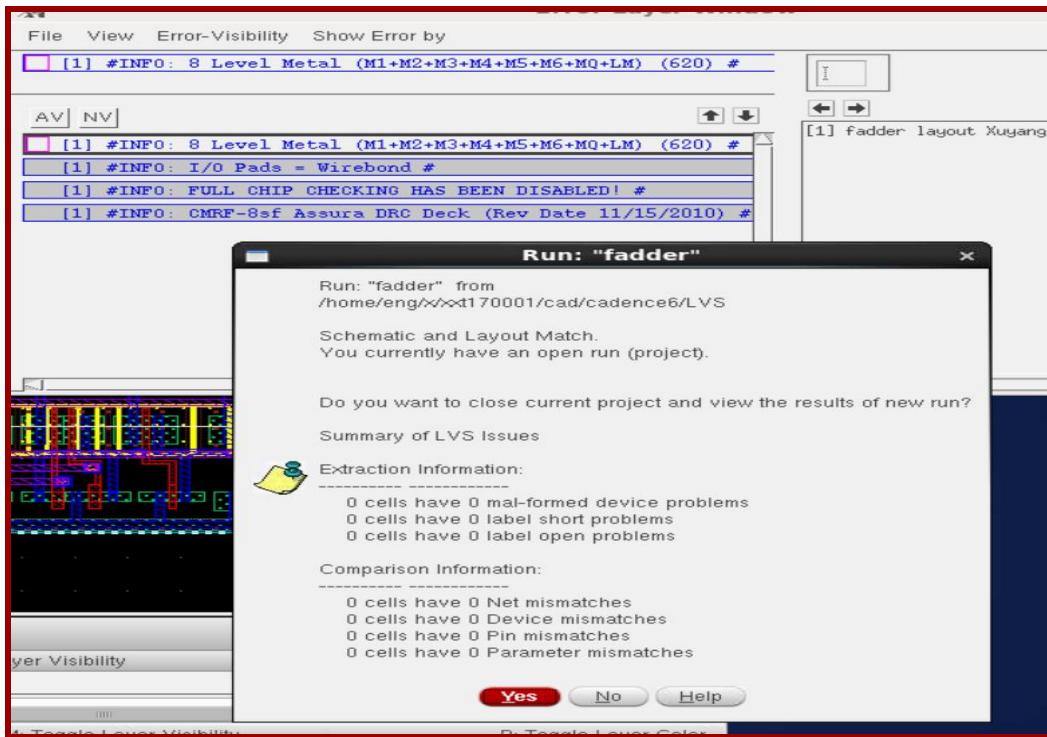


END

d) Layout



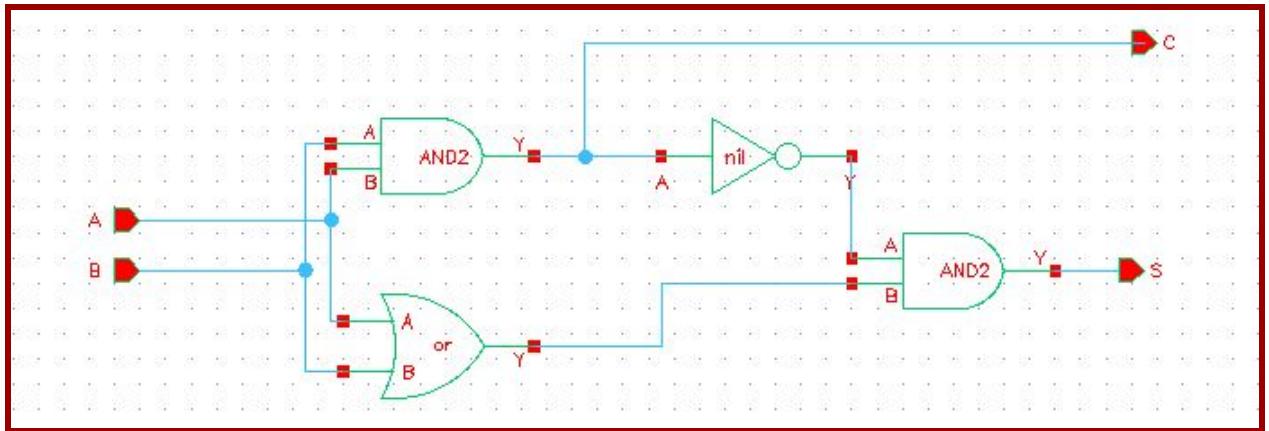
e) LVS Report



END

12.) Half Adder Operation

a) Schematic :-

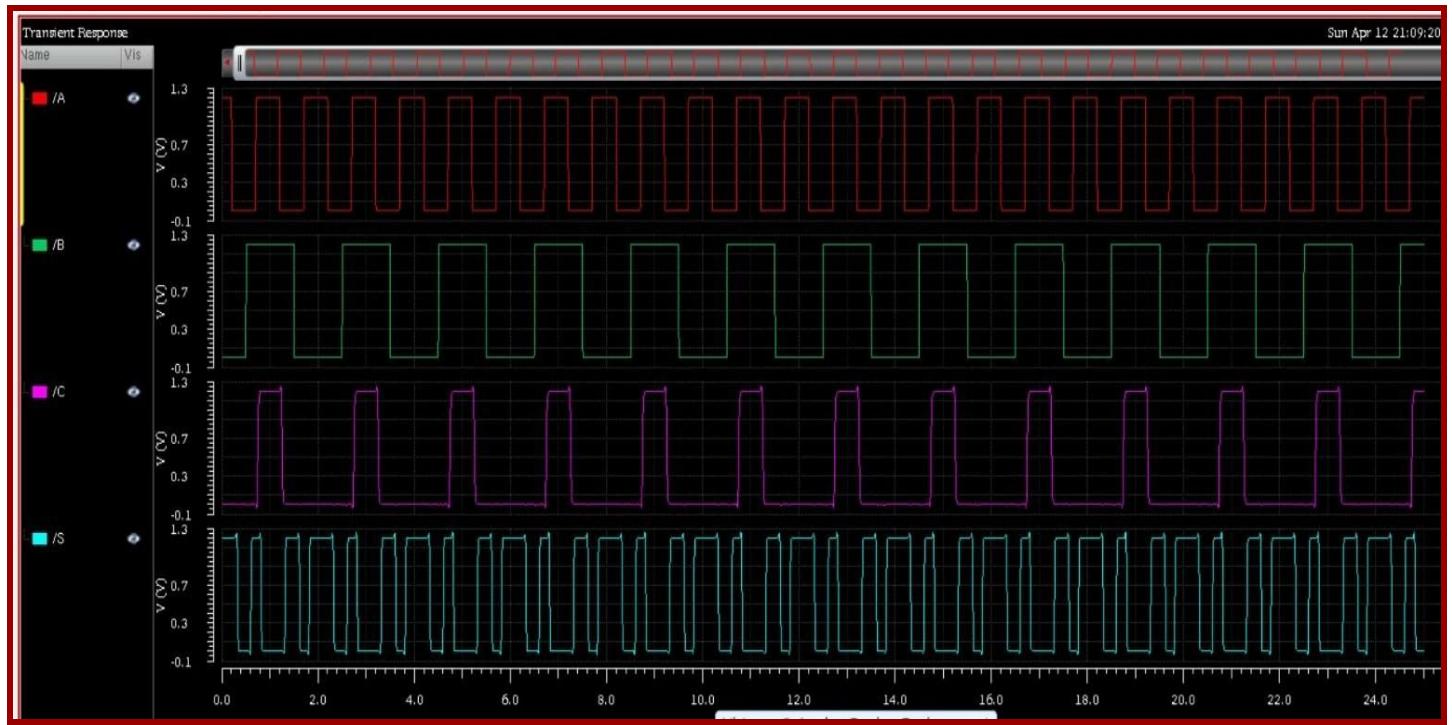


b) Symbol :-

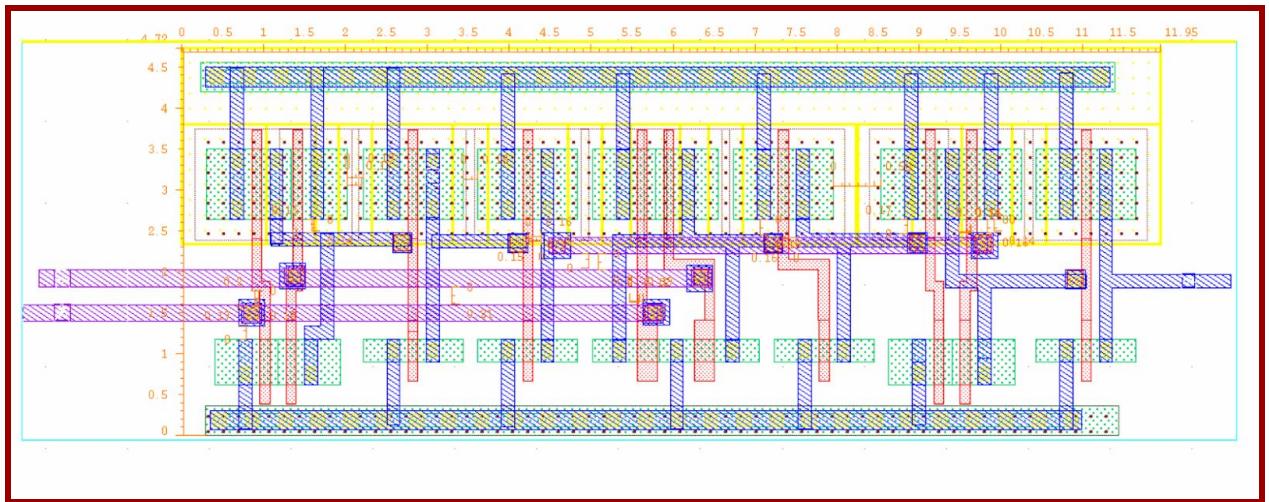


END

c) Simulation Waveform :-

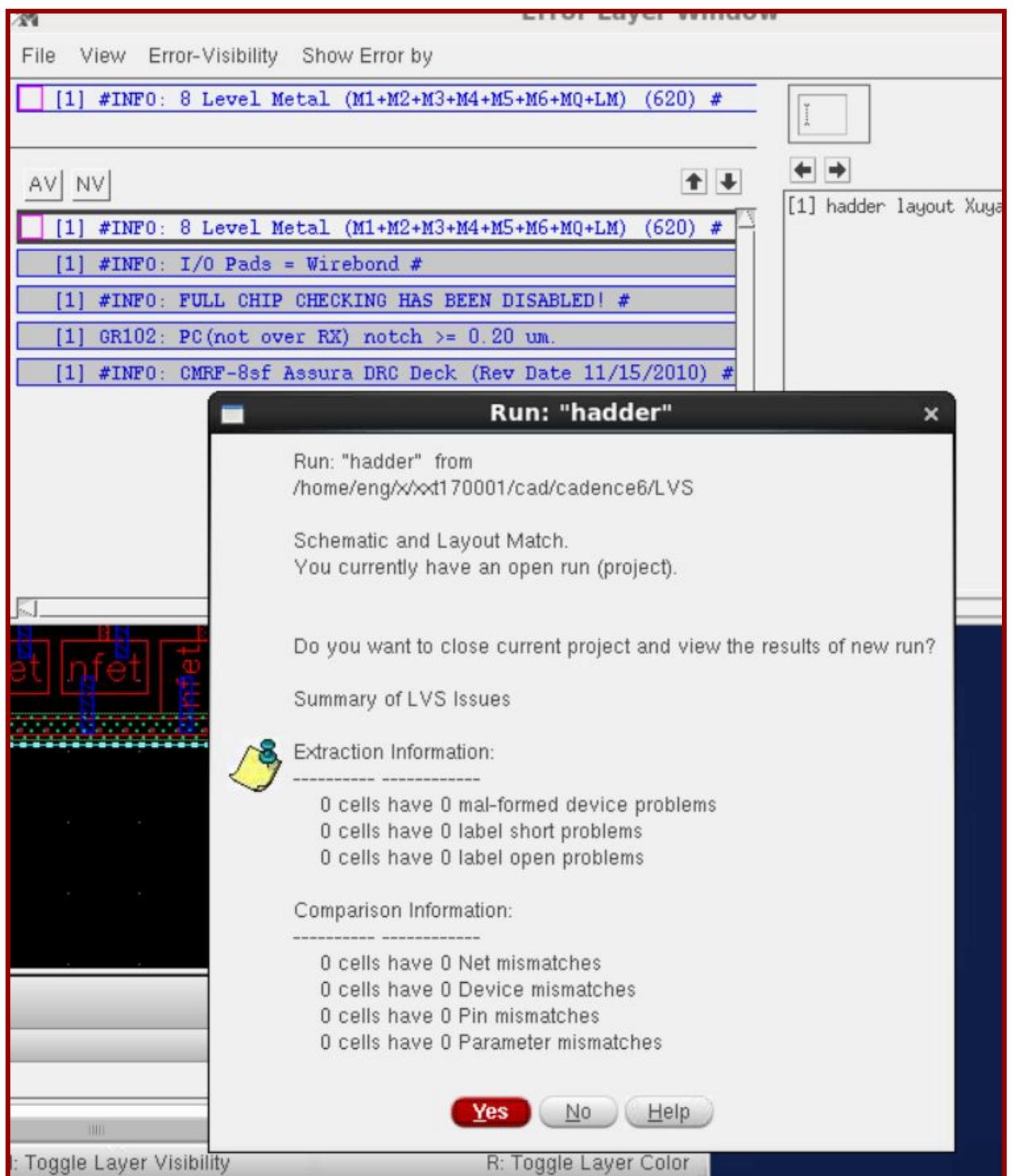


d) Layout :



END

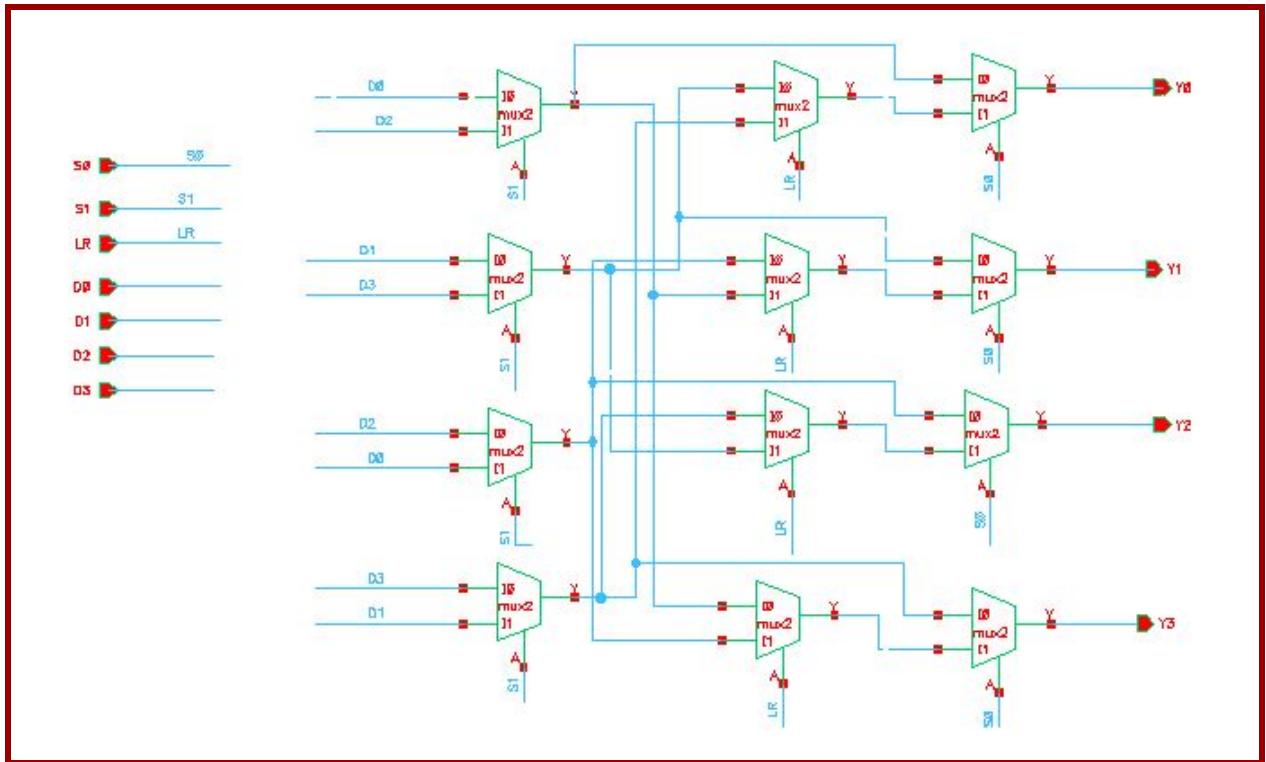
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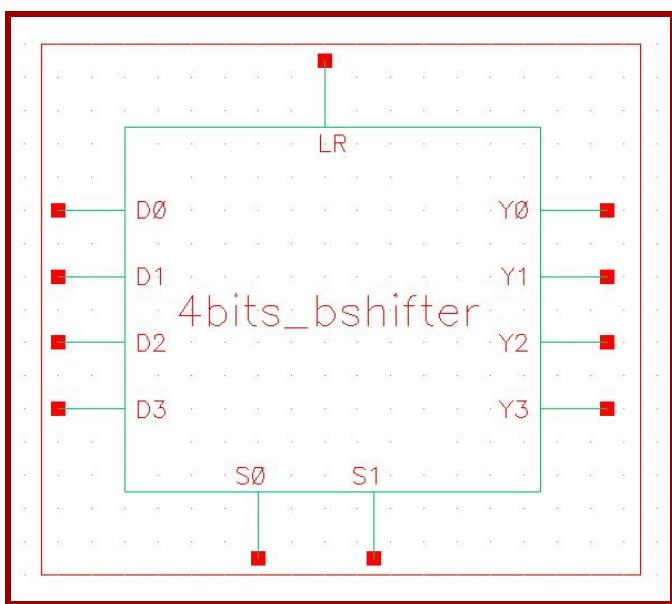
END

13.) Barrel Shifter Operation

a) Schematic :-



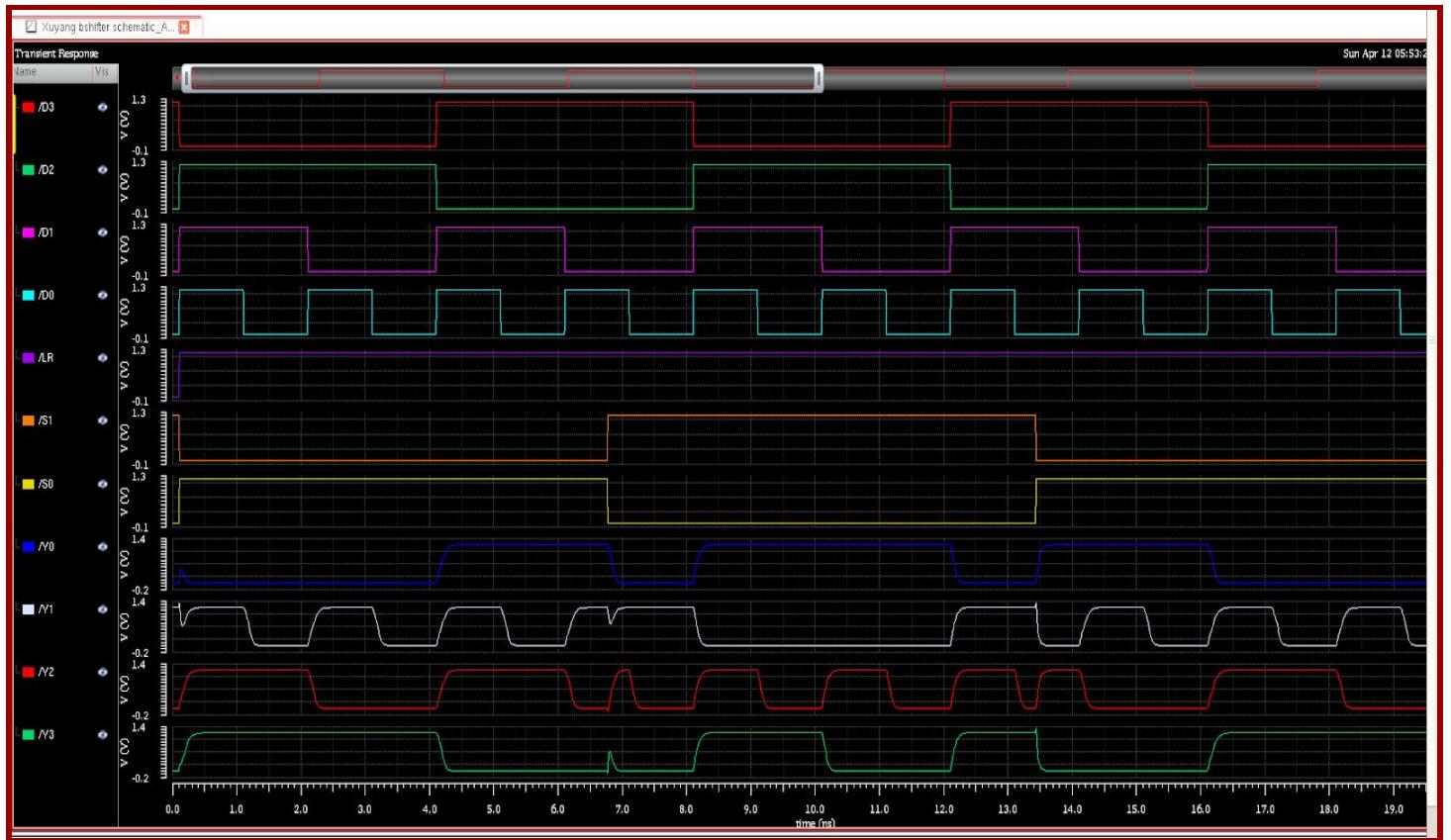
b) Symbol :-



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END

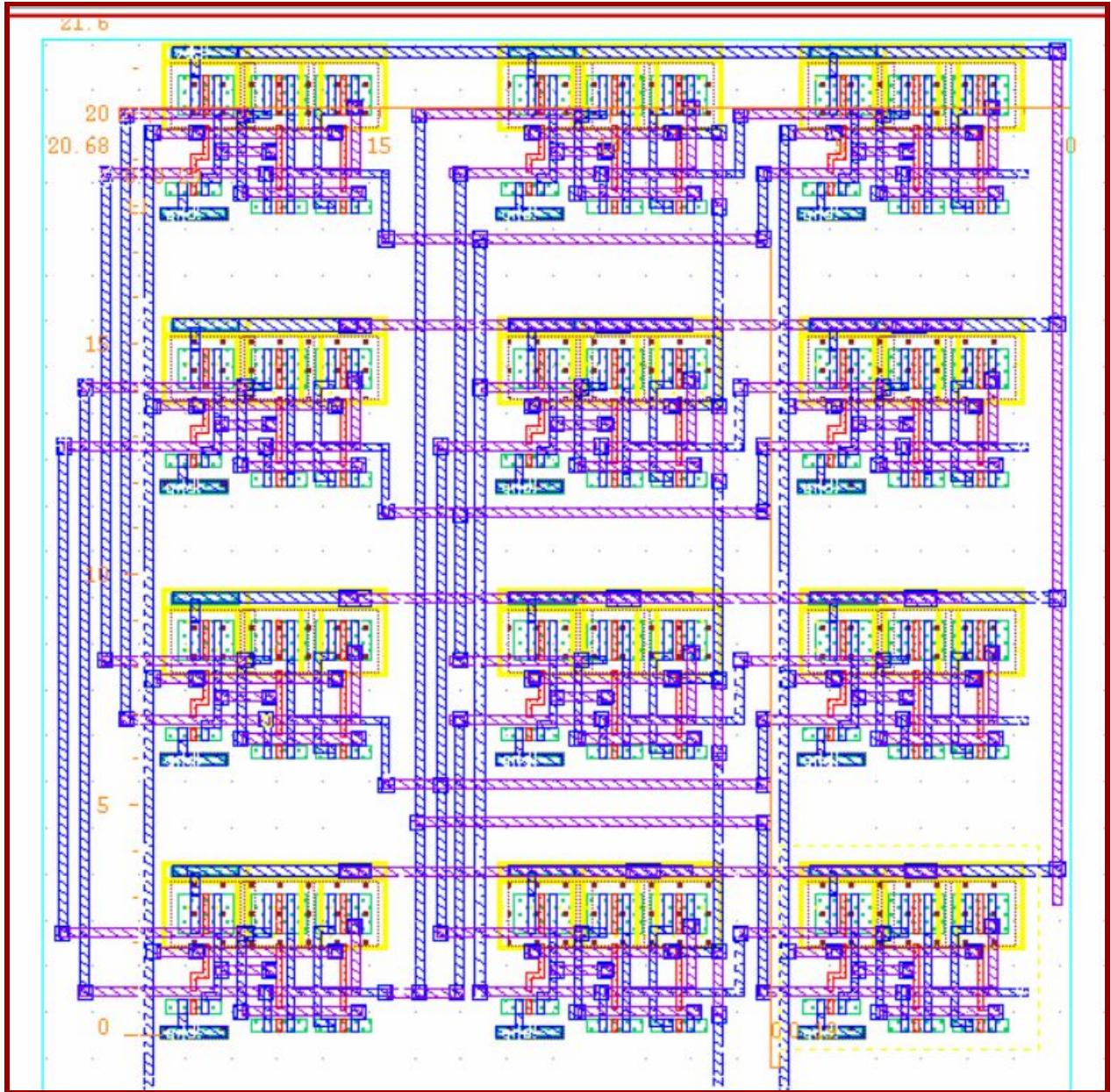
c) Simulation Waveform :-



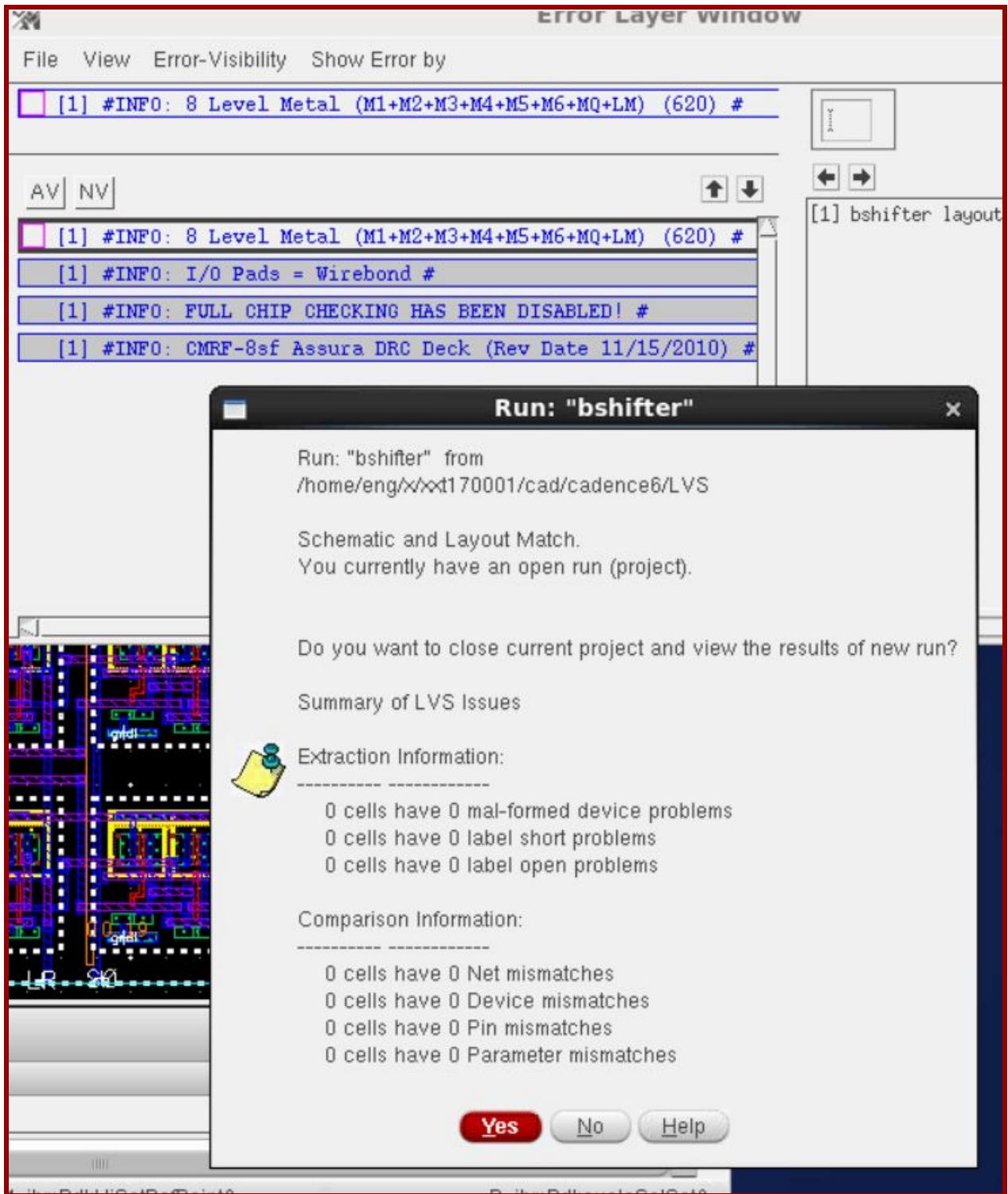
d) Layout

Next Page

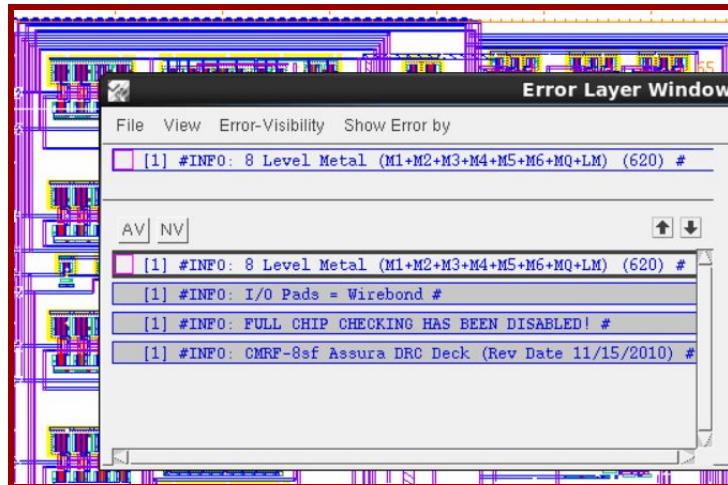
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END

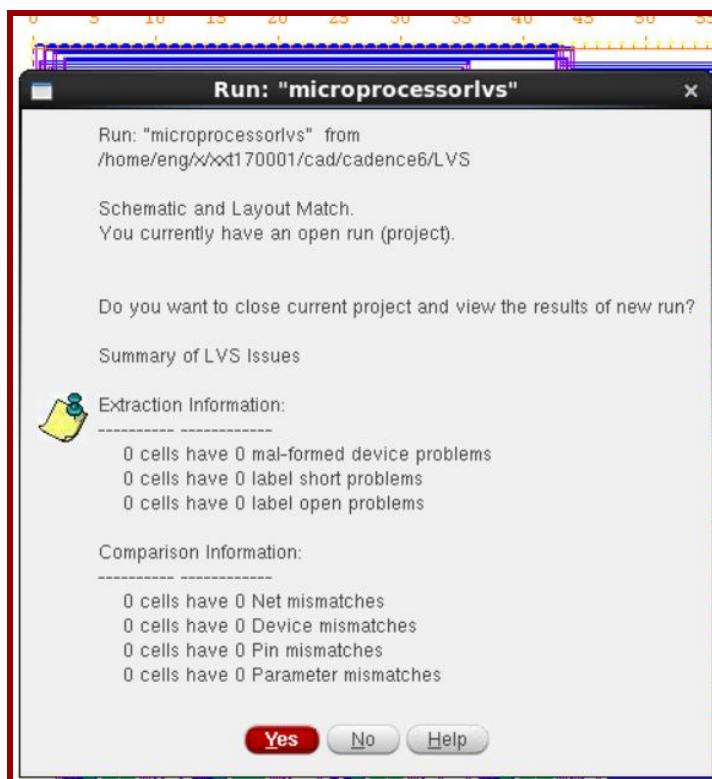


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DRC :

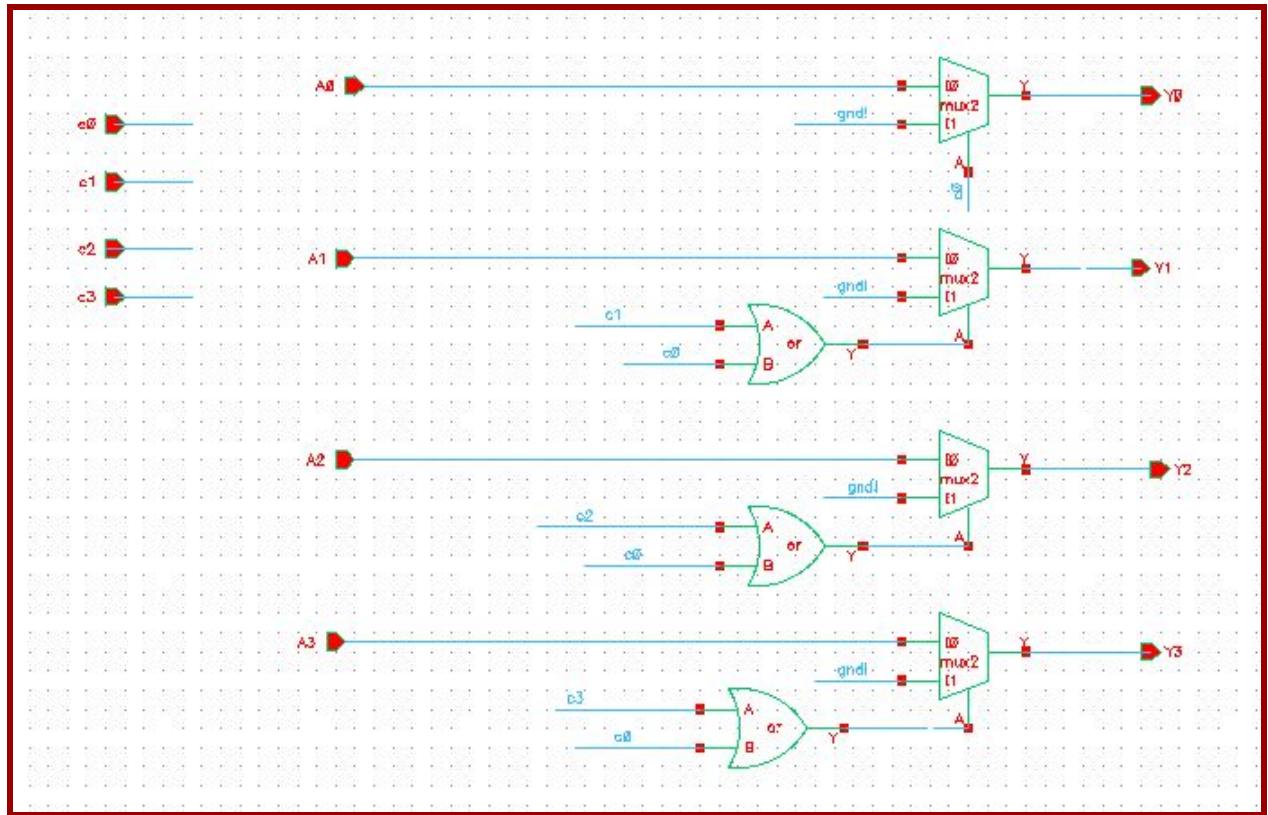
LVS :



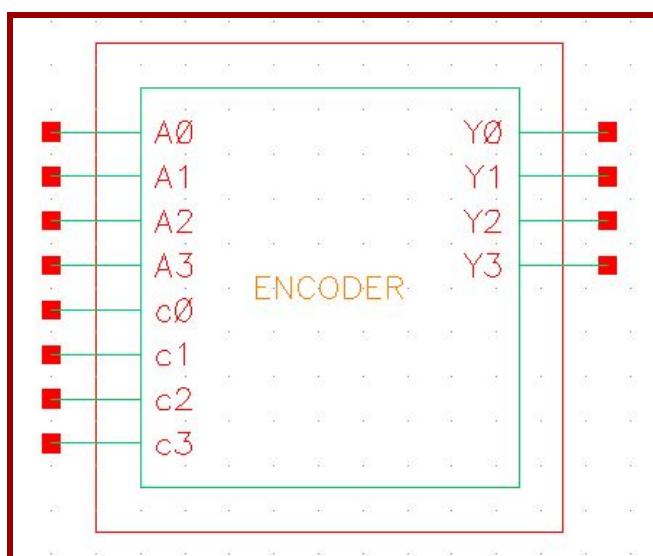
END

14.) Encoder Operation

a) Schematic :-



b) Symbol :-



END

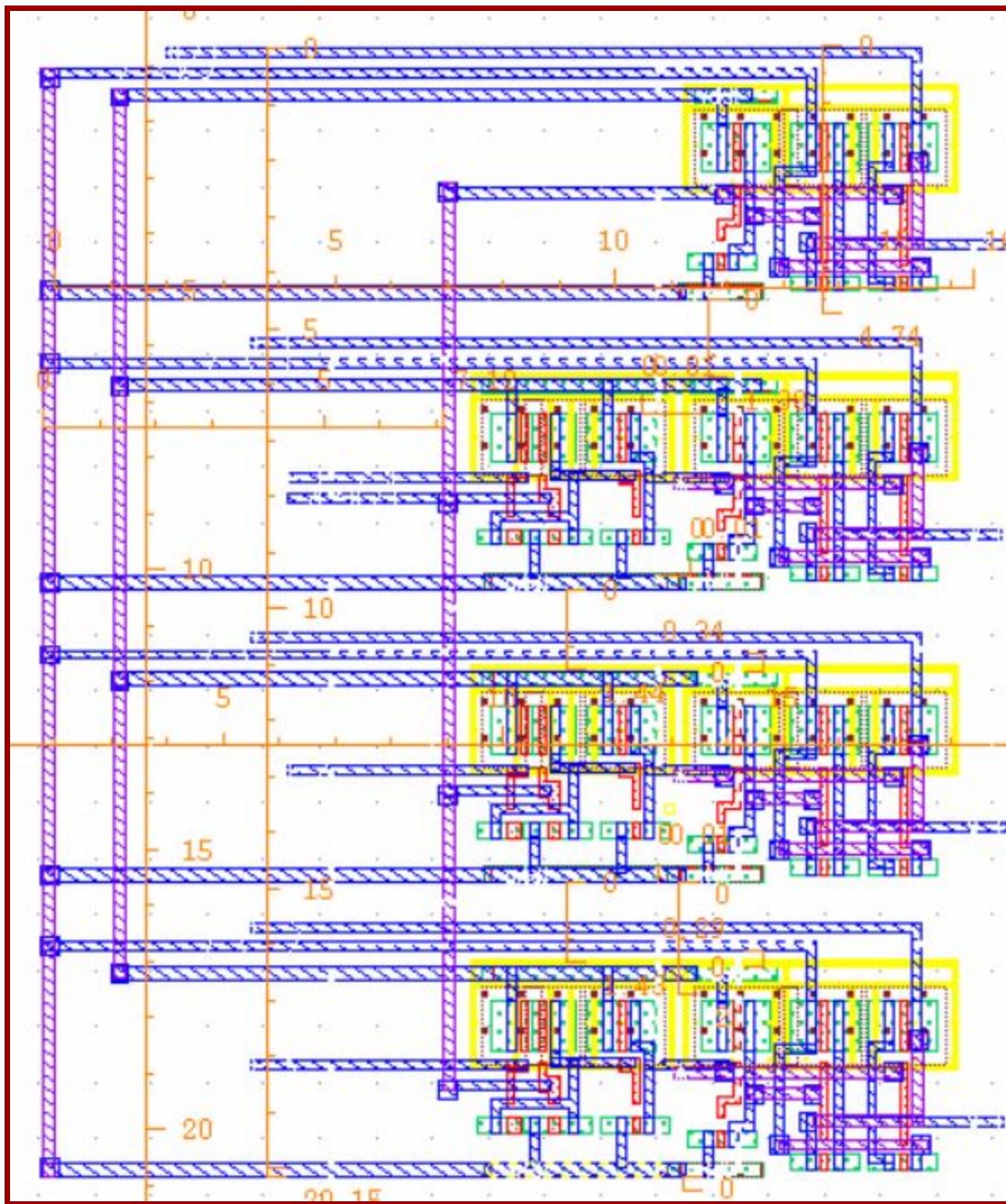
c) Simulation Waveform :-



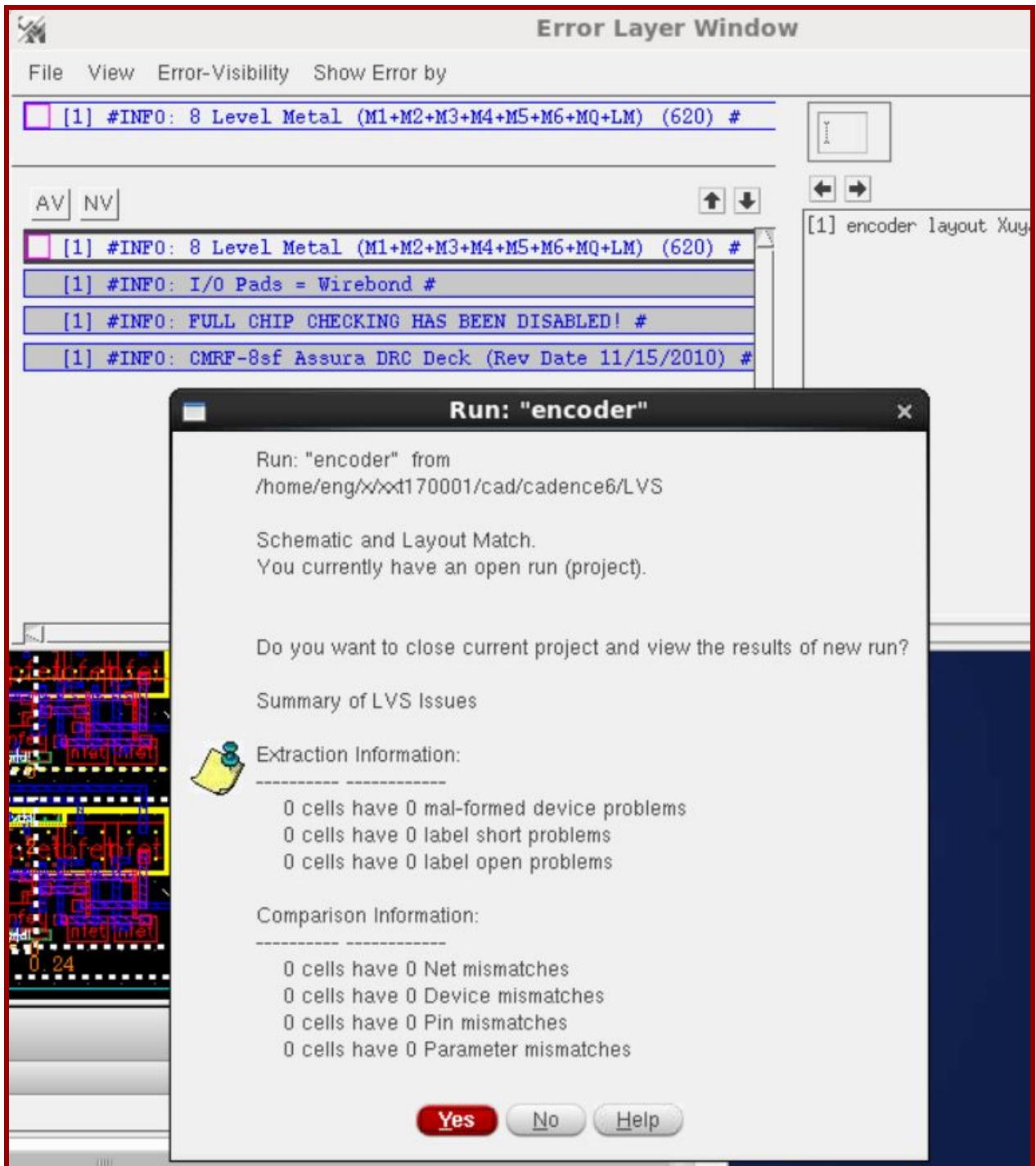
d) Layout

Next Page

END



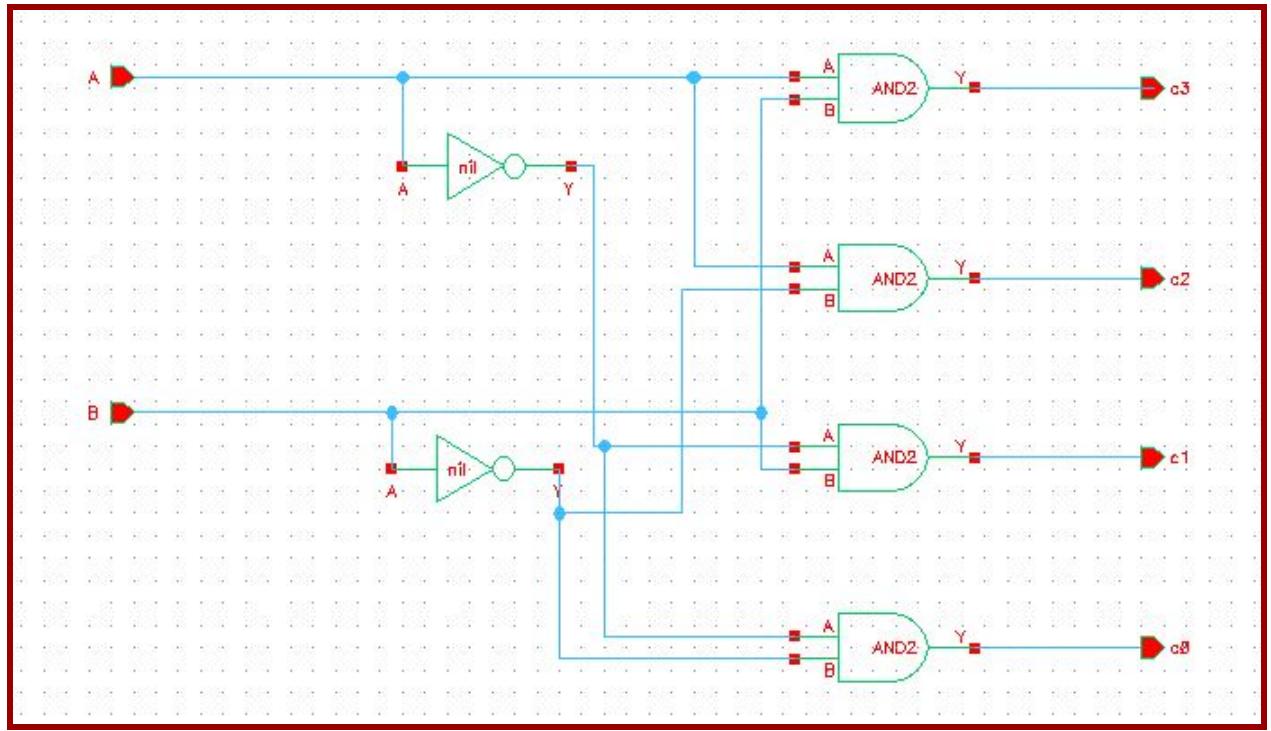
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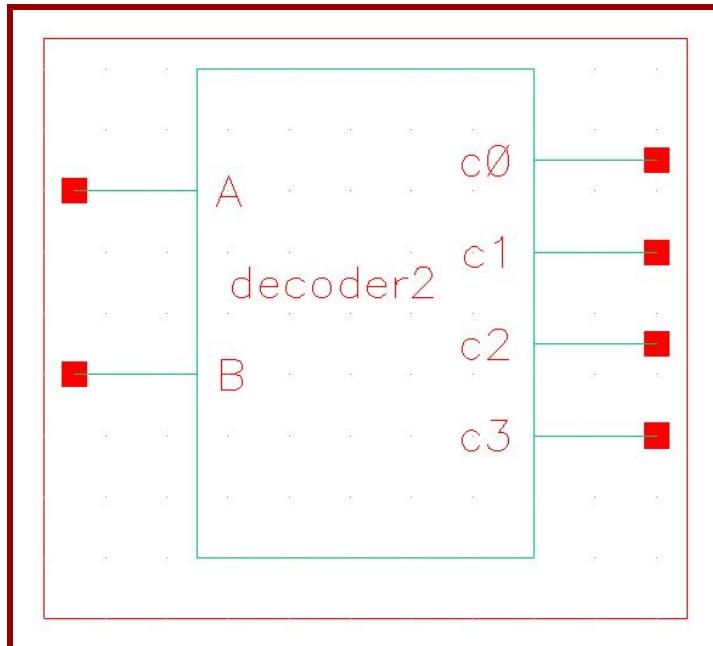
END

15.) Decoder Operation

a) Schematic :-

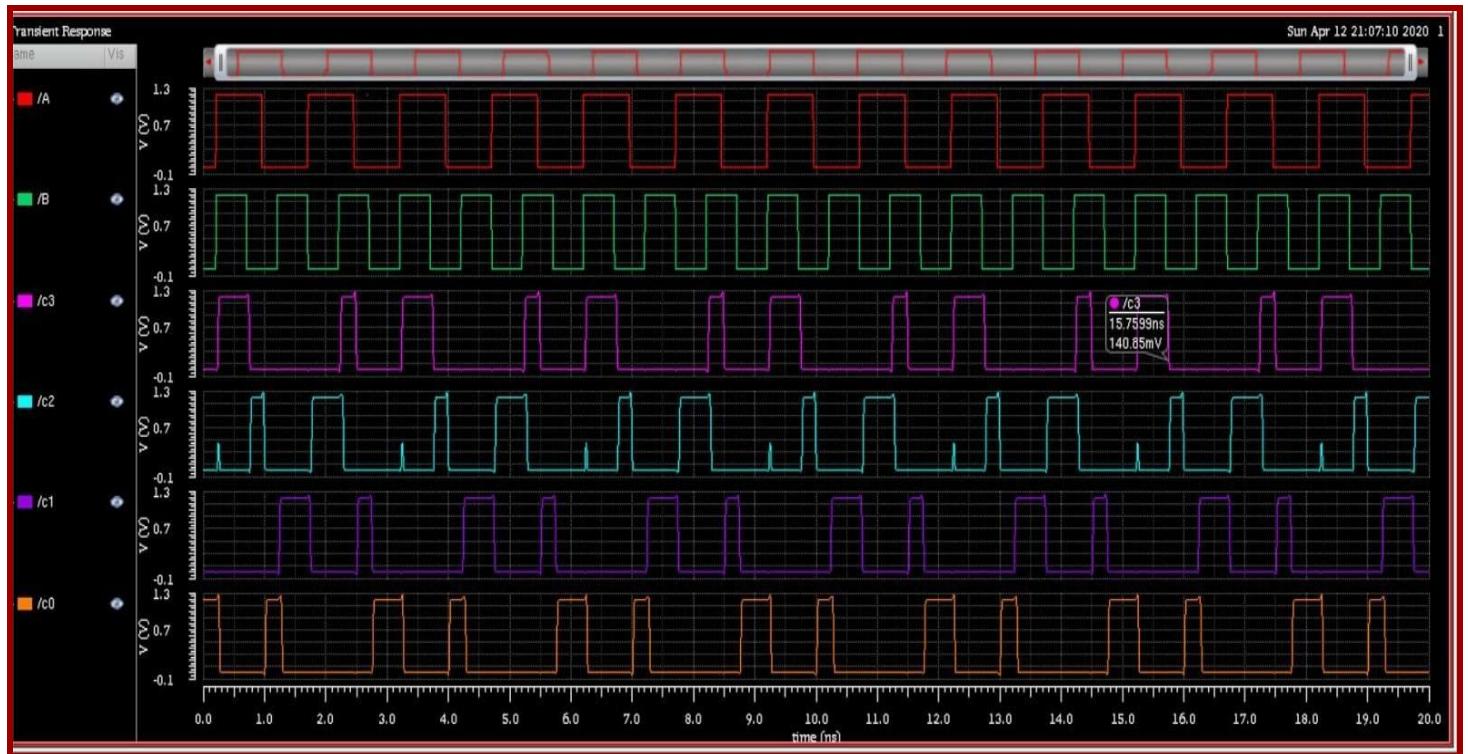


b) Symbol :-



END

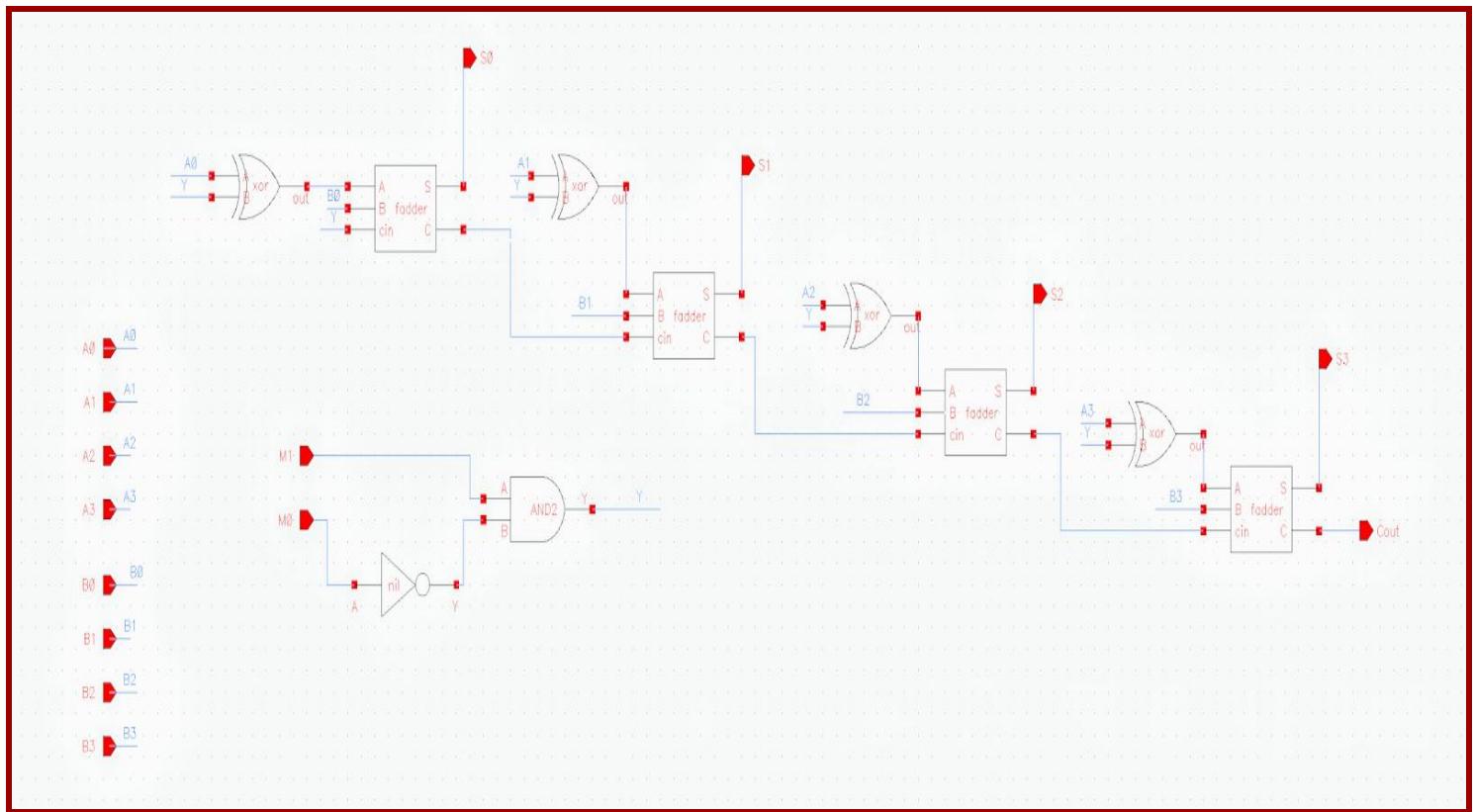
c) Simulation Waveform :-



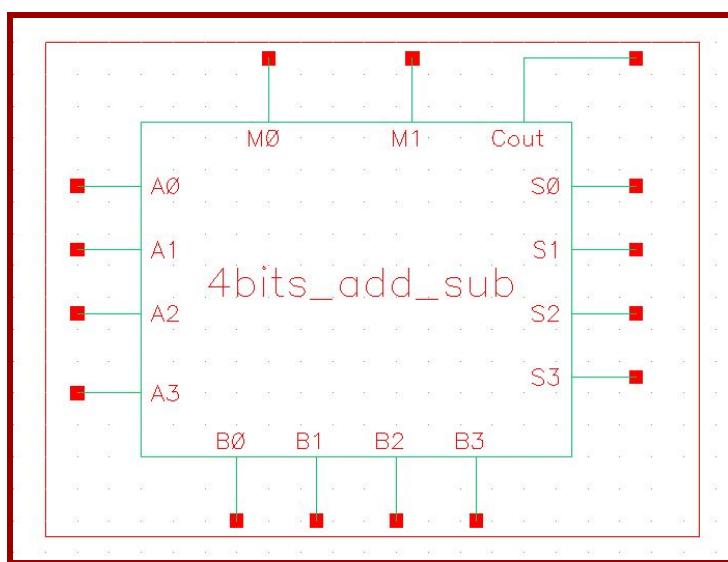
END

16.) Ripple Carry Adder-Subtractor (RCA) Operation

a) Schematic :-

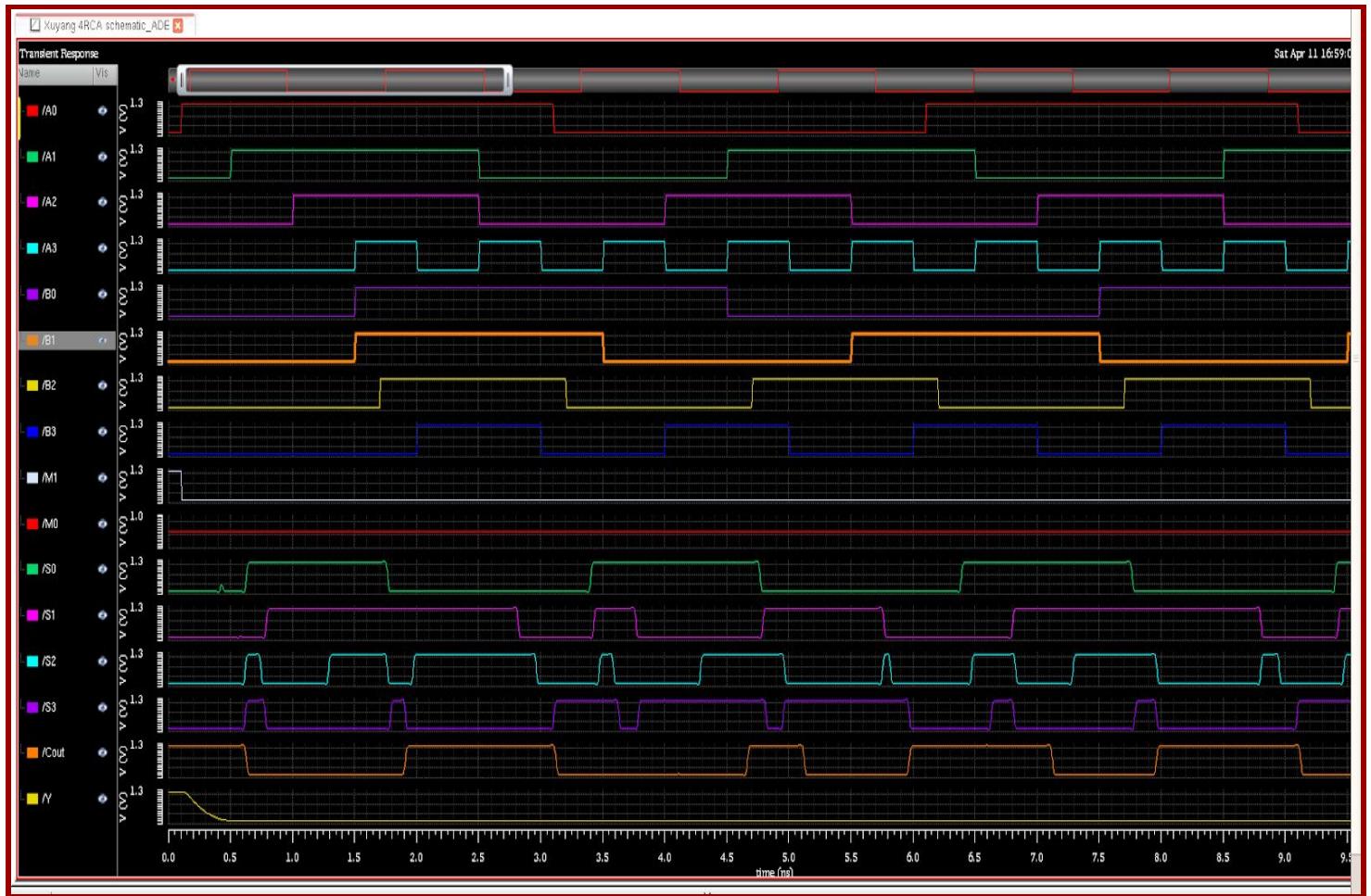


b) Symbol :-



END

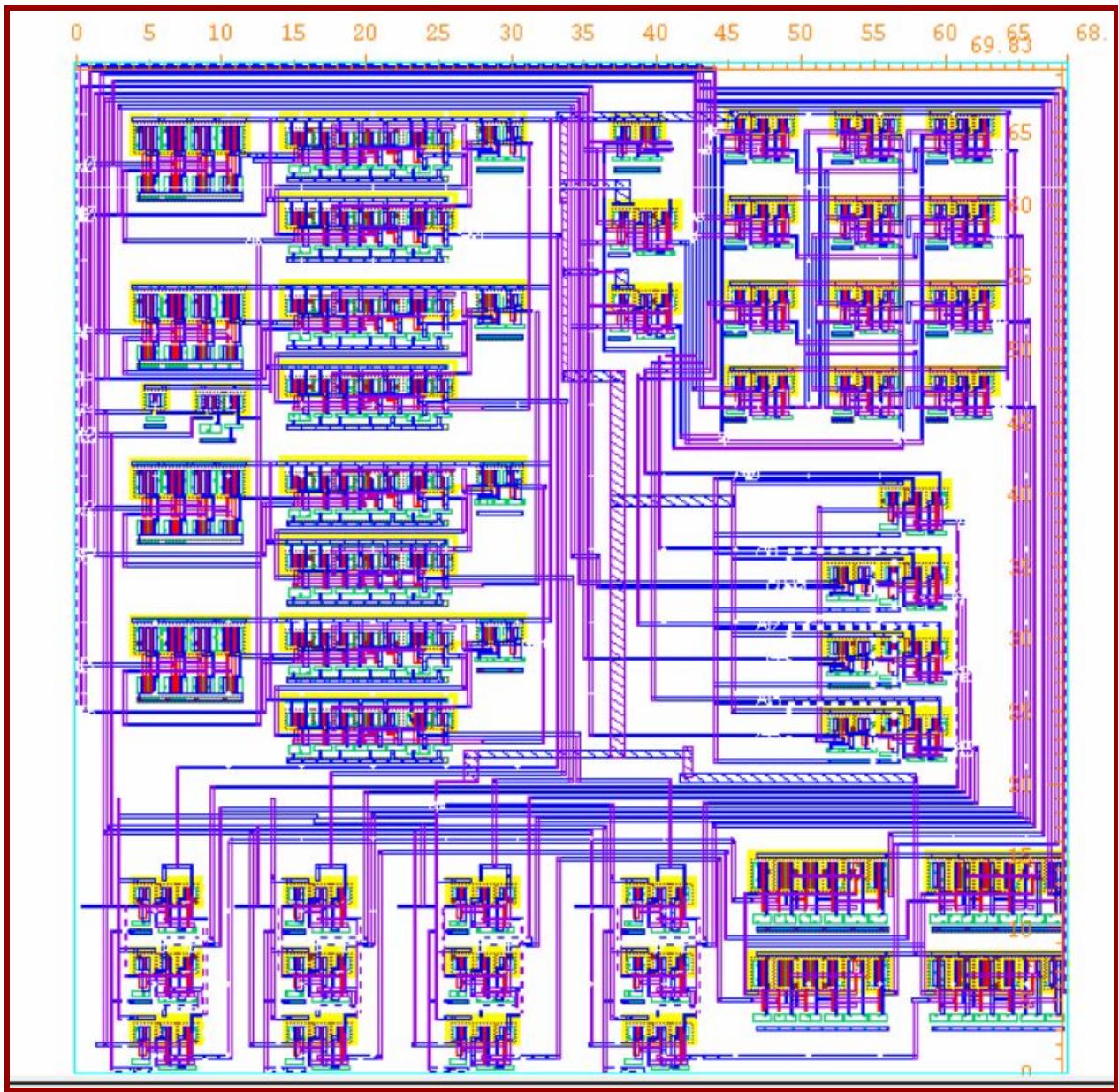
c) Simulation Waveform :-



d) Layout

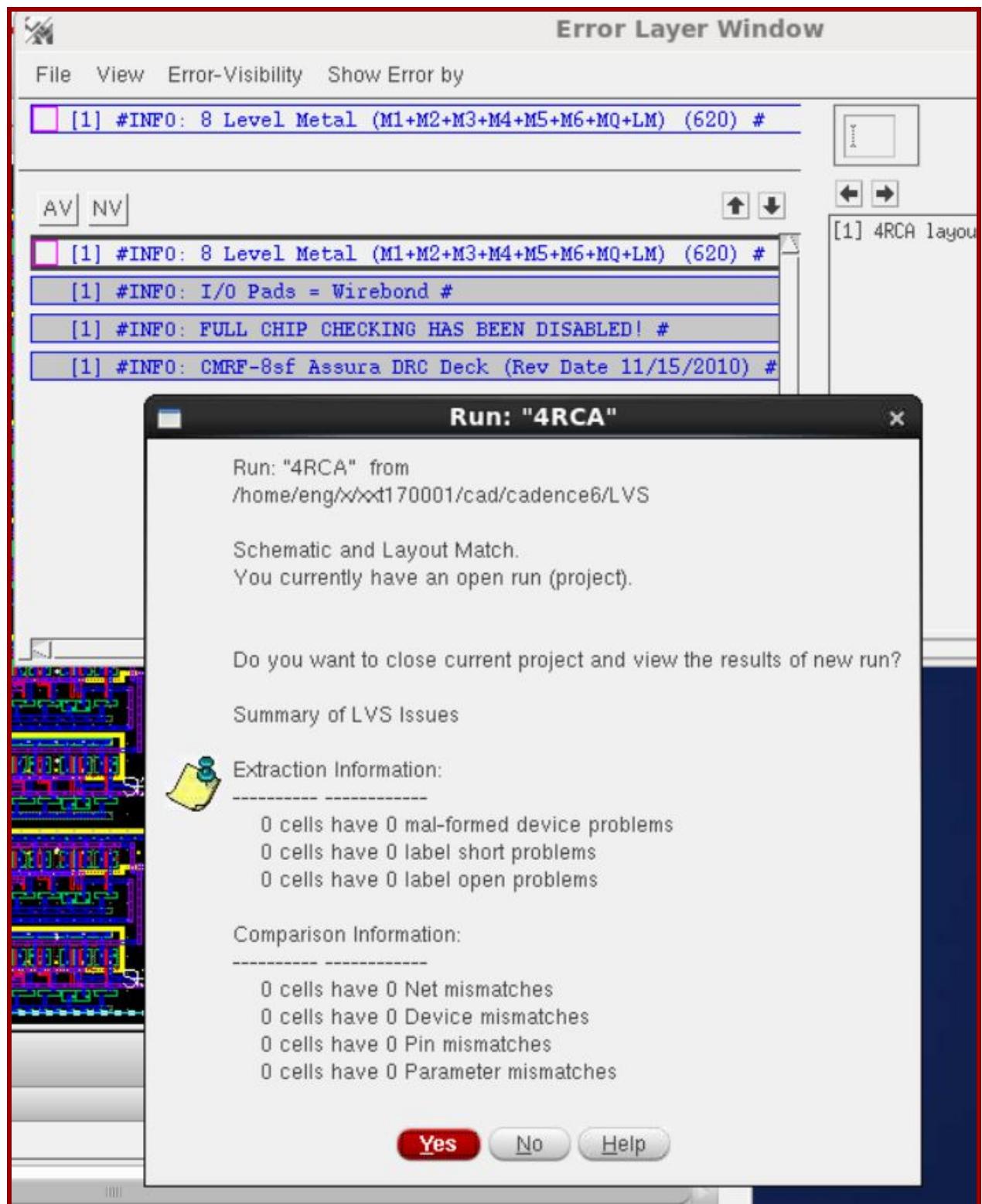
Next Layout

END



e) LVS Report

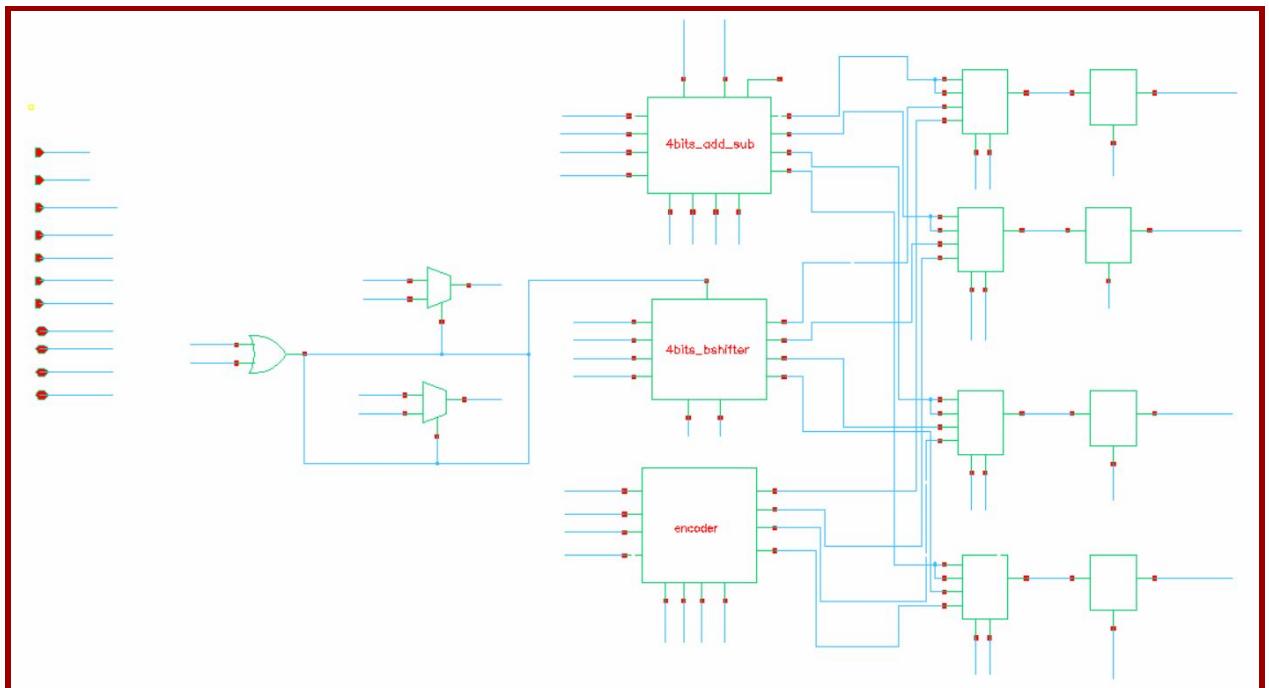
Next Page



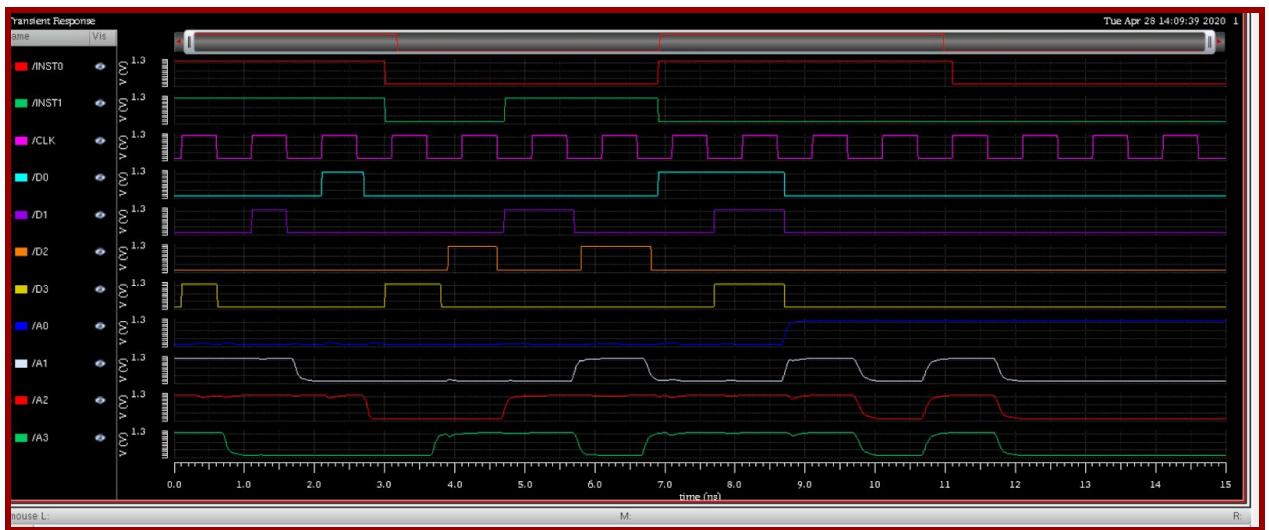
END

17.) 4-Bit Microprocessor Design for Calculator Operations

a) Schematic :

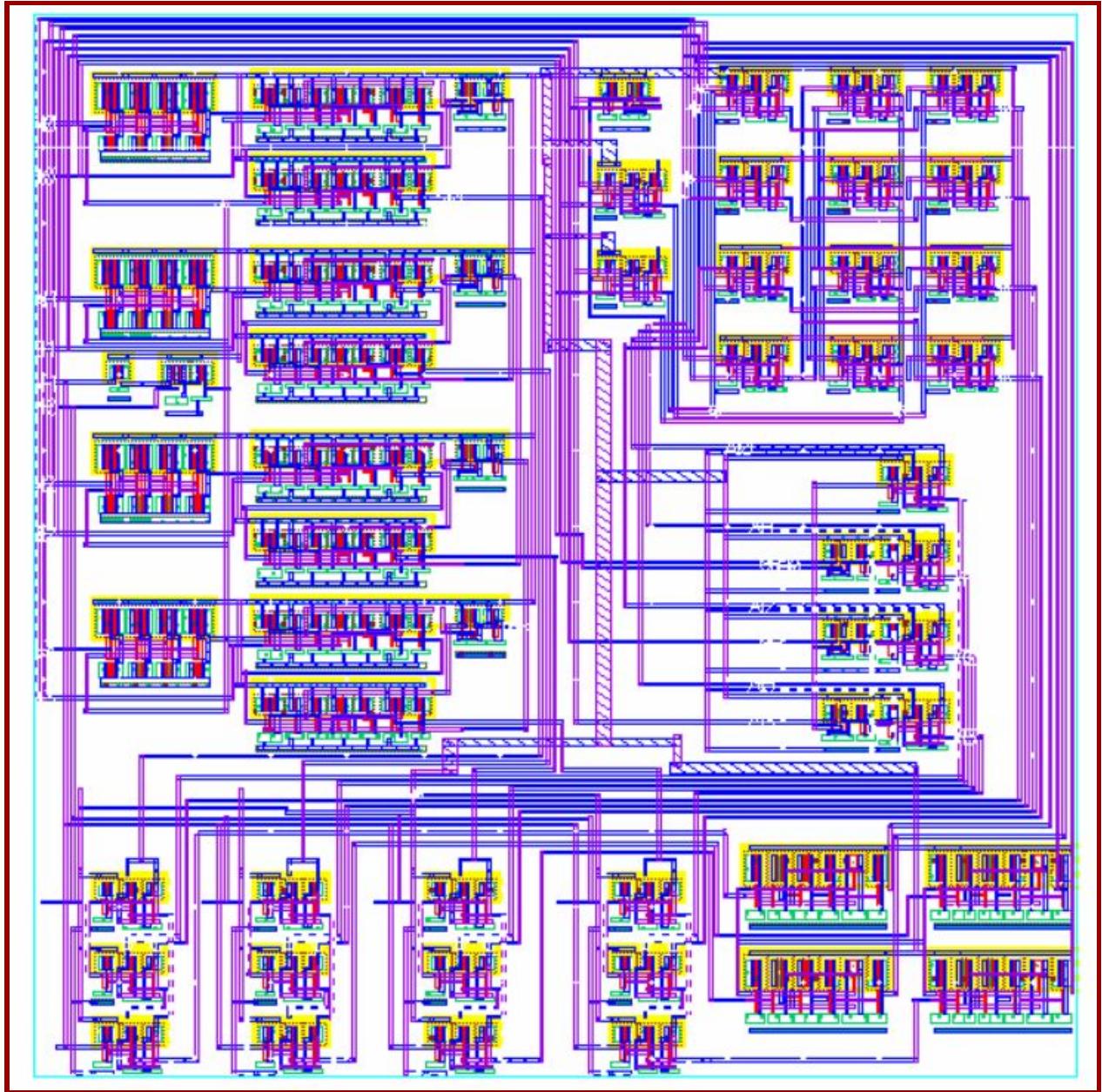


c) Simulation Waveform (pre simulation)



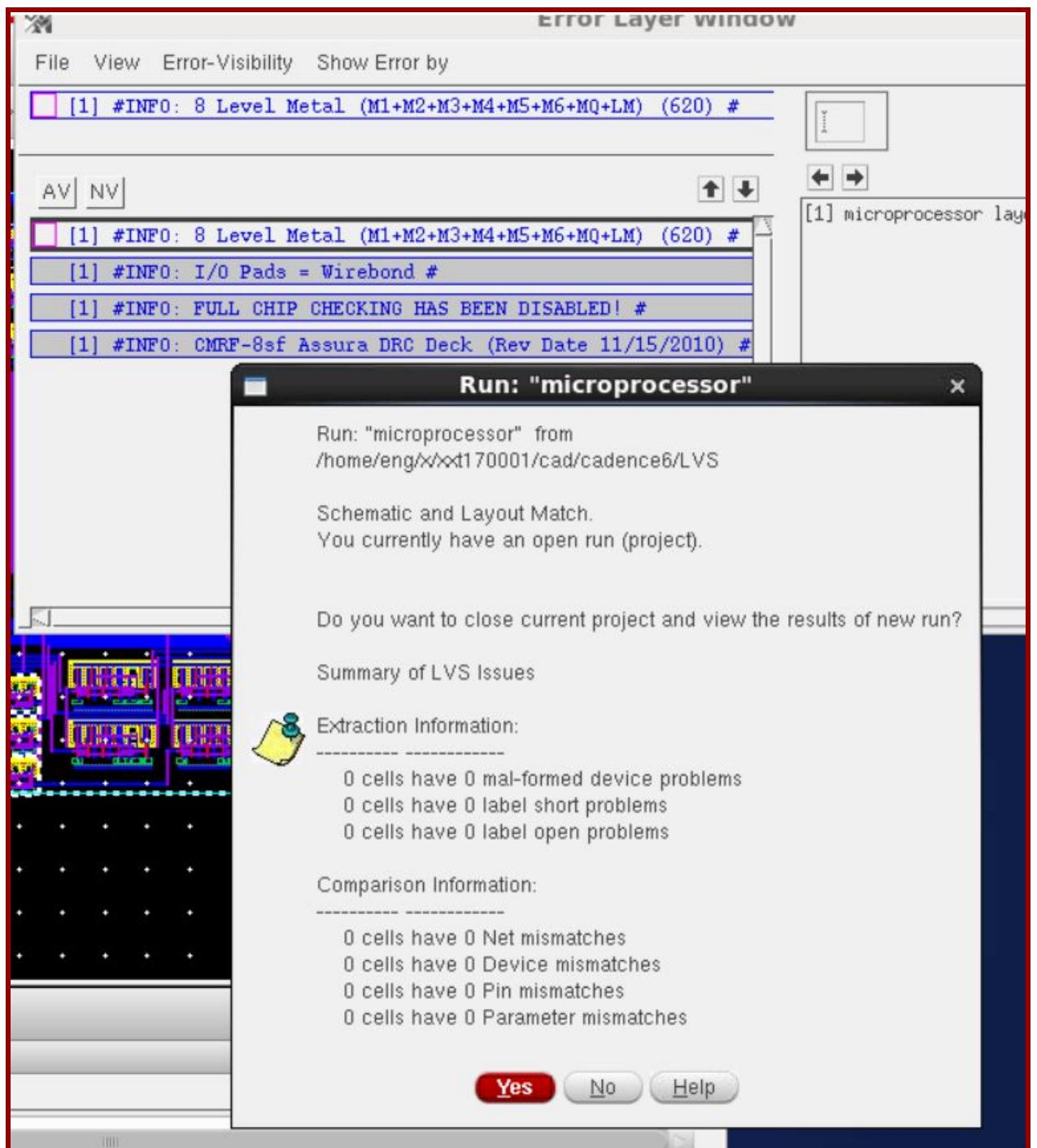
END

d) Layout



END

e) LVS Report



END

e) Post Simulation (HSPICE SYNOPSYS WAVEFORM OUTPUT)



Output files - Testbench

\$Testbench for measuring worstcase delay and average energy for DFF

```
$ transistor model
.include
"/home/cad/kits/IBM_CMRF8SF-LM013/IBM_PDK/cmrf8sf/V1.2.0.0LM/HSPICE/models/model013.lib_inc"
.include microprocessorlvs.sp

.global vdd!

.option post runlvl=5

$ xi A B out nand2
xi CLK IN0 IN1 IN2 IN3 INST0 INST1 OUT0 OUT1 OUT2 OUT3 microprocessor

vdd vdd! gnd! 1.2v
```

END

```

vCLK CLK gnd! pulse( 0v 1.2v 0ps 10ps 10ps 610pps 1120ps )
vIN0 IN0 gnd! pwl( 0ns 0v 2ns 0v 2.01ns 1.2v 2.9ns 1.2v 2.91ns 0v 7.5ns 0v 7.51ns 1.2v 8.46ns 1.2v
8.47ns 0v 15ns 0v)
    vIN1 IN1 gnd! pwl( 0ns 0v 1ns 0v 1.01ns 1.2v 1.75ns 1.2v 1.76ns 0v 2.9ns 0v 2.91ns 1.2v 5.1ns 1.2v
6.2ns 1.2v 6.21ns 0v 7.5ns 0v 7.51ns 1.2v 9.6ns 1.2v 9.61ns 0v 15ns 0v )
    vIN2 IN2 gnd! pwl( 0ns 0v 4ns 0v 4.01ns 0v 5.1ns 0v 5.11ns 0v 6.2ns 0v 6.21ns 1.2v 7.5ns 1.2v 7.51ns 0v
15ns 0v)
    vIN3 IN3 gnd! pwl( 0ns 0v 0.2ns 0v 0.21ns 1.2v 0.65ns 1.2v 0.66ns 0v 1.5ns 0v 1.51ns 0v 4ns 0v 4.01ns
1.2v 5ns 1.2v 5.01ns 0v 7.5ns 0v 7.51ns 0v 8.46ns 0v 8.47ns 0v 15ns 0v  )

vINST0 INST0 gnd! pwl(0ns 1.2v 2.5ns 1.2v 2.9ns 1.2v 2.91ns 0v 7.5ns 0v 7.51ns 1.2v 9.5ns 1.2v 11.7ns
1.2v 11.71ns 0v 15ns 0v)
vINST1 INST1 gnd! pwl(0ns 1.2v 2.5ns 1.2v 2.9ns 1.2v 2.91ns 0v 5.31ns 0v 5.32ns 1.2v 7.5ns 1.2v
7.51ns 0v 15ns 0v)

```

\$transient analysis

```

$.tr 100ps 48ns
.tr 0.1ps 15ns
$$$$$$$$$$$$$$$$ encoder delay
.measure tran tphl_encoder trig v(CLK) td=0.4ns val=0.6 fall=1 targ v(OUT3) val=0.6 fall=1

$$$$$$$$$$$$$$$$ adder delay
.measure tran tphl_adder trig v(CLK) td=5.2ns val=0.6 fall=1 targ v(OUT3) val=0.6 rise=1
.measure tran tphl_adder trig v(CLK) td=5ns val=0.6 fall=1 targ v(OUT1) val=0.6 fall=1

$$$$$$$$$$$$$$$$$$$$$$$$ shifter delay
.measure tran tphl_shifter trig v(CLK) td=6.2ns val=0.6 fall=1 targ v(OUT3) val=0.6 fall=1
.measure tran tphl_shifter trig v(CLK) td=7.3ns val=0.6 fall=1 targ v(OUT3) val=0.6 rise=1

$$$$$$$$$$$$$$$$ sub delay
.measure tran tphl_sub trig v(CLK) td=8.6ns val=0.6 fall=1 targ v(OUT3) val=0.6 fall=1
.measure tran tphl_sub trig v(CLK) td=8.4ns val=0.6 fall=1 targ v(OUT1) val=0.6 rise=1

.measure t_1 param='max(tphl_adder,tphl_encoder)'
.measure t_2 param='max(tphl_adder,t_1)'
.measure t_3 param='max(tphl_shifter,t_2)'
.measure t_4 param='max(tphl_shifter,t_3)'
.measure t_5 param='max(tphl_sub,t_4)'
.measure t_6 param='max(tphl_sub,t_5)'

```

END

```

.measure tran iavg avg i(vdd) from=0 to=10.5n

.measure energy_avg param='1.2*iavg*10.5n'
.measure edp param='abs(t_6*energy_avg)'

.end

$transient analysis
$.tr 100ps 48ns
.tr 0.1ps 15ns
$$$$$$$$$$$$$$$$ encoder delay
.measure tran tphl_encoder trig v(CLK) td=0.4ns val=0.6 fall=1 targ v(OUT3) val=0.6 fall=1

$$$$$$$$$$$$$$$$ adder delay
.measure tran tphl_adder trig v(CLK) td=5.2ns val=0.6 fall=1 targ v(OUT3) val=0.6 rise=1
.measure tran tphl_adder trig v(CLK) td=5ns val=0.6 fall=1 targ v(OUT1) val=0.6 fall=1

$$$$$$$$$$$$$$$$$$$$$$$$$$$$ shifter delay
.measure tran tphl_shifter trig v(CLK) td=6.2ns val=0.6 fall=1 targ v(OUT3) val=0.6 fall=1
.measure tran tphl_shifter trig v(CLK) td=7.3ns val=0.6 fall=1 targ v(OUT3) val=0.6 rise=1

$$$$$$$$$$$$$$$$ sub delay
.measure tran tphl_sub trig v(CLK) td=8.6ns val=0.6 fall=1 targ v(OUT3) val=0.6 fall=1
.measure tran tphl_sub trig v(CLK) td=8.4ns val=0.6 fall=1 targ v(OUT1) val=0.6 rise=1

.measure tran iavg avg i(vdd) from=0 to=10.5n
.measure energy_avg param='1.2*iavg*10.5n'

.end

```

.sto file

***** HSPICE -- L-2016.06-SP1-2 linux64 (Oct 14 2016) *****
Input File: microprocessorsetup.sp
lic:
lic: FLEXlm: v11.2.1
lic: USER: xxt170001 HOSTNAME: engnx08.utdallas.edu

END

```
lic: HOSTID: "047d7bd6c8cb"      PID:  63306
lic: Using FLEXlm license file:
lic: 1700@engdmv
lic: Checkout 1 hspice
lic: License/Maintenance for hspice will expire on 30-jun-2021/2019.06
lic: 4(in_use)/50(total) FLOATING license(s) on SERVER 1700@engdmv
lic:
init: begin read circuit files, cpu clock= 3.80E-01
      option search = /proj/cad/synopsys/hspice_vL-2016.06-SP1-2/hspic
            e/part/ad
      option runlvl
      option scalm = 1.00
      option post
      option runlvl = 5.00
init: end read circuit files, cpu clock= 4.20E-01 peak memory= 214 mb
init: begin check errors, cpu clock= 4.20E-01
init: end check errors, cpu clock= 4.60E-01 peak memory= 217 mb
init: begin setup matrix, pivot= 0 cpu clock= 4.60E-01
      establish matrix -- done, cpu clock= 4.60E-01 peak memory= 217 mb
      re-order matrix -- done, cpu clock= 4.70E-01 peak memory= 217 mb
init: end setup matrix, cpu clock= 4.80E-01 peak memory= 218 mb
dcop: begin dcop, cpu clock= 4.80E-01
dcop: end dcop, cpu clock= 6.10E-01 peak memory= 218 mb tot_iter= 56
output: microprocessorsetup.mt0
sweep: tran tran0 begin, stop_t= 1.50E-08 #sweeps=**** cpu clock= 6.10E-01
tran: time= 1.5145E-09 tot_iter= 1589 conv_iter= 561 cpu clock= 2.76E+00
tran: time= 3.0029E-09 tot_iter= 2919 conv_iter= 1032 cpu clock= 4.37E+00
tran: time= 4.5014E-09 tot_iter= 4370 conv_iter= 1549 cpu clock= 5.87E+00
tran: time= 6.0123E-09 tot_iter= 5653 conv_iter= 2008 cpu clock= 7.34E+00
tran: time= 7.5000E-09 tot_iter= 6890 conv_iter= 2439 cpu clock= 8.72E+00
tran: time= 9.0019E-09 tot_iter= 8971 conv_iter= 3179 cpu clock= 1.12E+01
tran: time= 1.0501E-08 tot_iter= 10421 conv_iter= 3690 cpu clock= 1.28E+01
tran: time= 1.2002E-08 tot_iter= 11724 conv_iter= 4158 cpu clock= 1.43E+01
tran: time= 1.3506E-08 tot_iter= 12732 conv_iter= 4522 cpu clock= 1.55E+01
tran: time= 1.5000E-08 tot_iter= 13046 conv_iter= 4639 cpu clock= 1.58E+01
sweep: tran tran0 end, cpu clock= 1.58E+01 peak memory= 213 mb
>info: **** hspice job concluded
lic: Release hspice token(s)
```

END

NETLIST FILE

NETLIST is too large, attached as a file outside.

```
##### NETLIST SAMPLE #####
*
*
*      LINUX      Mon Apr 27 23:41:43 2020
*
*
*
*
* PROGRAM advgen
*
* Name      : advgen - QRC - (64-bit)
* Version   : 9.1.3-p005
* Build Date: Tue Aug  3 12:36:00 PDT 2010
*
* HSPICE LIBRARY
*
*
*.GLOBAL gnd! vdd!
*

.SUBCKT microprocessor CLK IN0 IN1 IN2 IN3 INST0 INST1 OUT0 OUT1 OUT2 OUT3
*
*
* caps2d version: 10
*
*
* TRANSISTOR CARDS
*
*
MI1/I8/T5    net40  I1/I8/net11    I1/net35      gnd!    nfet    L=0.12U
+ W=0.28U
+ wt=2.8e-07 rf=0 nrs=0.93617 nrd=0.93617 ngcon=1 nf=1 mSwitch=0 m=1 blockParasiticsBetween="PC
sub" PWORIENT=1 PLORIENT=1
MI1/I9/T5    net41  I1/I9/net11    I1/net19      gnd!    nfet    L=0.12U
+ W=0.28U
+ wt=2.8e-07 rf=0 nrs=0.93617 nrd=0.93617 ngcon=1 nf=1 mSwitch=0 m=1 blockParasiticsBetween="PC
sub" PWORIENT=1 PLORIENT=1
```

END

MI1/I10/T5 net48 I1/I10/net11 I1/net16 gnd! nfet L=0.12U
+ W=0.28U
+ wt=2.8e-07 rf=0 nrs=0.93617 nrd=0.93617 ngcon=1 nf=1 mSwitch=0 m=1 blockParasiticsBetween="PC sub" PWORIENT=1 PLORIENT=1

MI1/I11/T5 net39 I1/I11/net11 I1/net3 gnd! nfet L=0.12U
+ W=0.28U
+ wt=2.8e-07 rf=0 nrs=0.93617 nrd=0.93617 ngcon=1 nf=1 mSwitch=0 m=1 blockParasiticsBetween="PC sub" PWORIENT=1 PLORIENT=1

MI1/I8/T3 I1/net13 S0 net40 gnd! nfet L=0.12U
+ W=0.28U
+ wt=2.8e-07 rf=0 nrs=0.93617 nrd=0.93617 ngcon=1 nf=1 mSwitch=0 m=1 blockParasiticsBetween="PC sub" PWORIENT=1 PLORIENT=1

MI1/I9/T3 I1/net10 S0 net41 gnd! nfet L=0.12U
+ W=0.28U
+ wt=2.8e-07 rf=0 nrs=0.93617 nrd=0.93617 ngcon=1 nf=1 mSwitch=0 m=1 blockParasiticsBetween="PC sub" PWORIENT=1 PLORIENT=1

MI1/I10/T3 I1/net7 S0 net48 gnd! nfet L=0.12U
+ W=0.28U
+ wt=2.8e-07 rf=0 nrs=0.93617 nrd=0.93617 ngcon=1 nf=1 mSwitch=0 m=1 blockParasiticsBetween="PC sub" PWORIENT=1 PLORIENT=1

MI1/I11/T3 I1/net14 S0 net39 gnd! nfet L=0.12U
+ W=0.28U
+ wt=2.8e-07 rf=0 nrs=0.93617 nrd=0.93617 ngcon=1 nf=1 mSwitch=0 m=1 blockParasiticsBetween="PC sub" PWORIENT=1 PLORIENT=1

MI25/I0/T5 net50 I25/I0/net11 OUT0 gnd! nfet L=0.12U
+ W=0.28U
+ wt=2.8e-07 rf=0 nrs=0.93617 nrd=0.93617 ngcon=1 nf=1 mSwitch=0 m=1 blockParasiticsBetween="PC sub" PWORIENT=1 PLORIENT=1

MI25/I1/T5 net46 I25/I1/net11 OUT1 gnd! nfet L=0.12U
+ W=0.28U
+ wt=2.8e-07 rf=0 nrs=0.93617 nrd=0.93617 ngcon=1 nf=1 mSwitch=0 m=1 blockParasiticsBetween="PC sub" PWORIENT=1 PLORIENT=1

MI25/I0/T3 gnd! IN0 net50 gnd! nfet L=0.12U W=0.28U
+ wt=2.8e-07 rf=0 nrs=0.93617 nrd=0.93617 ngcon=1 nf=1 mSwitch=0 m=1 blockParasiticsBetween="PC sub" PWORIENT=1 PLORIENT=1

MI25/I1/T3 gnd! I25/net21 net46 gnd! nfet L=0.12U
+ W=0.28U
+ wt=2.8e-07 rf=0 nrs=0.93617 nrd=0.93617 ngcon=1 nf=1 mSwitch=0 m=1 blockParasiticsBetween="PC sub" PWORIENT=1 PLORIENT=1

..... REST FOLLOWS SIMILARLY.....PLEASE CHECK NETLIST FILE IN PACKAGE.....

END