1. There are many digital logic gates. The 3 basic ones are AND, OR, NOT

The universal gates are NAND, NOR.

The two hybrid gates are XOR, XNOR

TTL stands for transistor-transistor logic. This is because the gates are made of multiple transistors

CMOS is a family of gates that use field-emmiter transistors than bipolar junction transistors.

CMOS is more favourable than TTL because of less power consumption and more sensitive.

2. Gate level

```
module ss(a, b, c, d, out);
    input a, b, c, d;
    output [0:6] out;

    not(abar, a);
    not(bbar, b);
    not(cbar, c);
    not(dbar, d);
    xnor(x1, b, d);
    or(out[0], a, c, x1);
    xnor(x2, c, d);
    or(out[1], bbar, x2);
    or(out[2], b, cbar, d);
    and(p1, bbar, c);
    and(p2, b, cbar, d);
    and(p3, dbar, bbar);
    and(p4, dbar, c);
    or(out[3], a, p1, p2, p3, p4);
    or(out[4], p3, p4);
    and(p5, b, cbar);
    and(p6, b, dbar);
```

```
    and (p7, cbar, dbar);
    or (out[5], a, p5, p6, p7);
    or (out[6], a, p5, p1, p4);
endmodule
```

Data Flow

```
module ss(a, b, c, d, out);
    input a, b, c, d;
    output [0:6] out;
    assign out[0] = a | c | ~(b ^ d);
    assign out[1] = ~b | ~(c ^ d);
    assign out[2] = b | ~c | d;
    assign out[3] = a | (~b & c) | (b & ~c & d) |
                    (~d & (~b | c));
    assign out[4] = ~d & (~b | c);
    assign out[5] = (b & ~c) | (b & ~d) | a |
                    (~c & ~d);
    assign out[6] = a | (b & ~c) | (~b & c) | (c & ~d);
endmodule
```

Behavioural

```
module ss(a,b,c,d,out);
    input a,b,c,d;
    output [0:6]out;
    reg [0:6]res;
    assign out = res;
    always @(*) begin
        case ({a,b,c,d})
            4'b0000 : res = 7'b1111110;
            4'b0001 : res = 7'b0110000;
            4'b0010 : res = 7'b1101101;
            4'b0011 : res = 7'b1111001;
            4'b0100 : res = 7'b0110011;
            4'b0101 : res = 7'b1011011;
            4'b0110 : res = 7'b1011111;
            4'b0111 : res = 7'b1110000;
            4'b1000 : res = 7'b1111111;
            4'b1001 : res = 7'b1111011;
        endcase
    end
endmodule
```

3. For common cathode, the input should be given as 1 (high) to light the LED

∴ The values of a to g are same as in the verilog code.

$a = A + C + \bar{B}\bar{D} + BD$

$L = \bar{B} + \bar{C}\bar{D} + CD$

$c = B + \bar{C} + D$

$d = A + \bar{B}L + B\bar{C}D + \bar{B}\bar{D} + L\bar{D}$

$e = \bar{D}\bar{B} + C\bar{D}$

$f = B\bar{C} + B\bar{D} + \bar{C}\bar{D} + A$

$g = A + B\bar{C} + \bar{B}C + C\bar{D}$

4. For common anode, the input should be given as 0 (low) to light the LED. So the input of common anode is opposite of common cathode

$a = \bar{A}B\bar{C}\bar{D} + \bar{A}\bar{B}\bar{C}D$

$b = BL\bar{D} + B\bar{C}D$

$c = \bar{B}C\bar{D}$

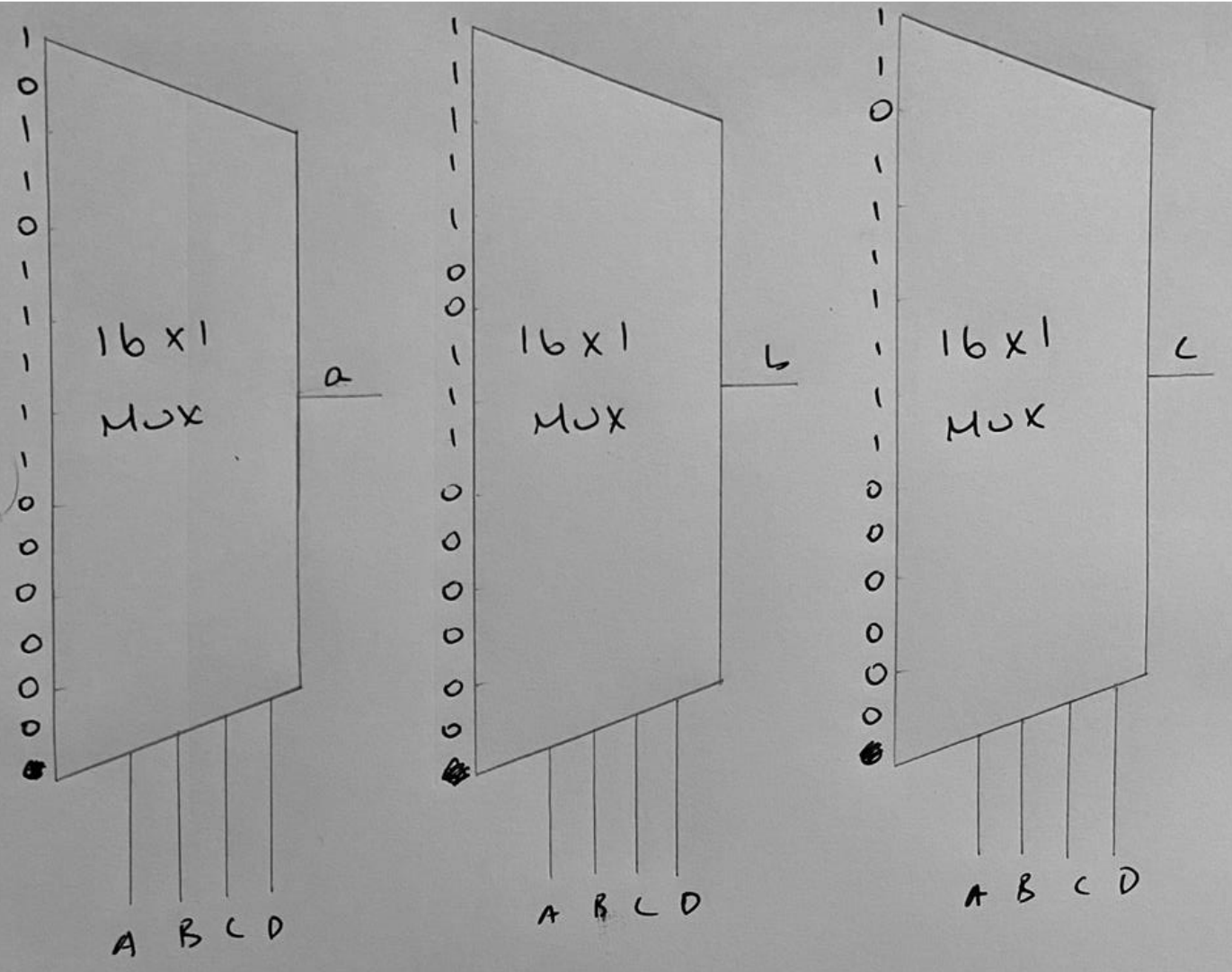
$d = \bar{A}BC + \bar{A}\bar{B}\bar{C}D$

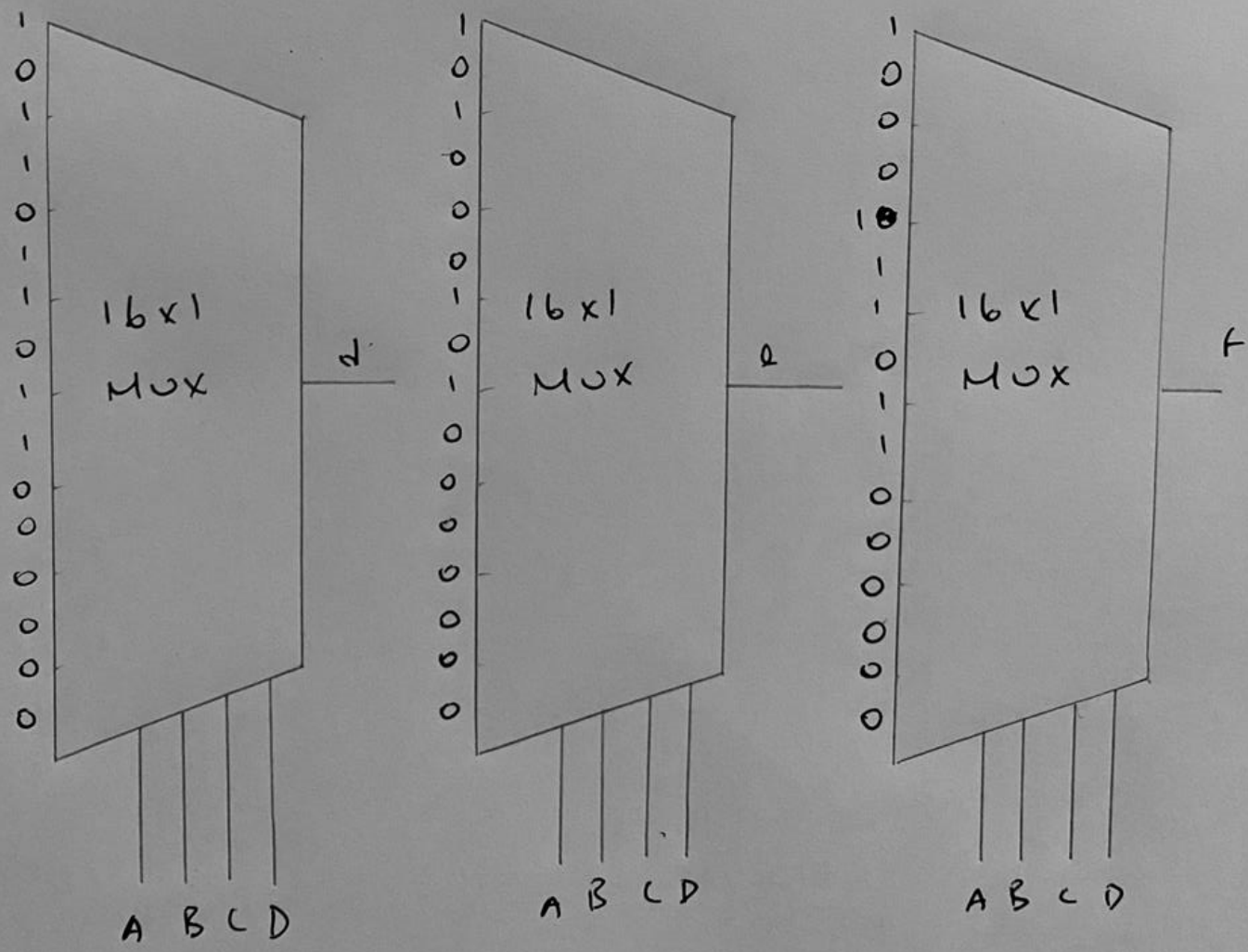
$e = B\bar{C} + BD + D\bar{C}$

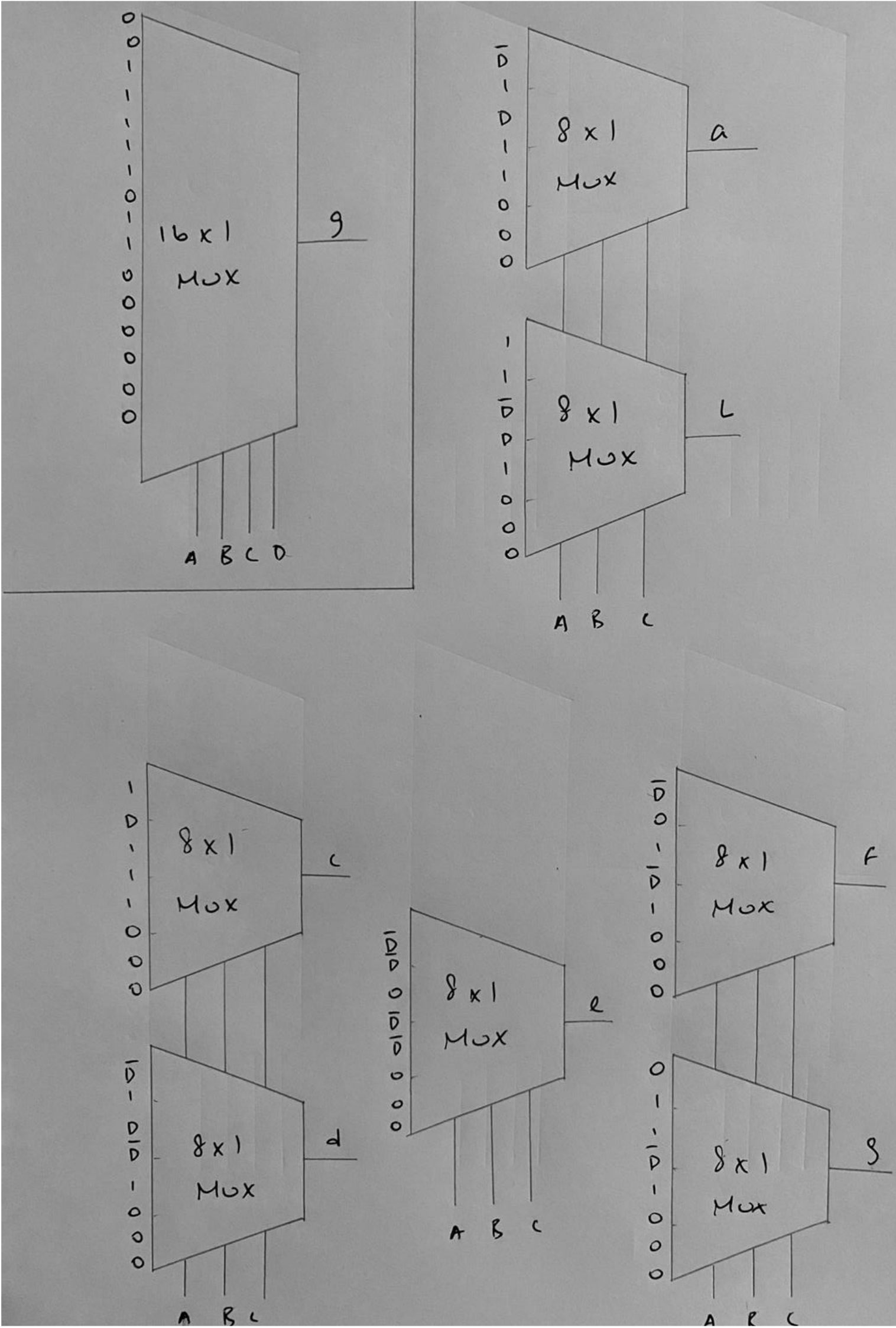
$f = \bar{A}\bar{B}C + \bar{A}\bar{B}D + \bar{A}CD$

$g = \bar{A}\bar{B}\bar{C} + \bar{A}BCD$

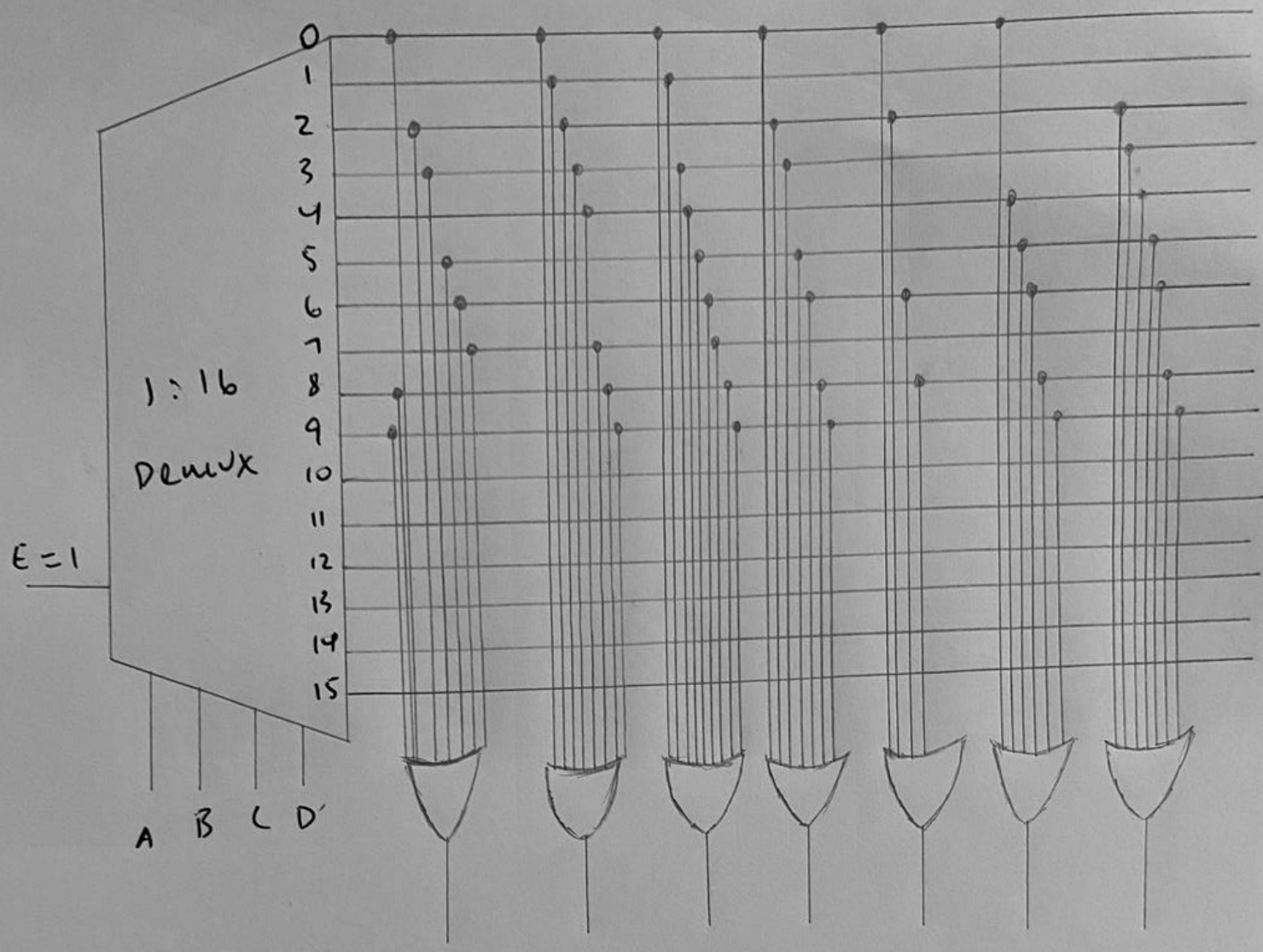
5.


16 x 1
MUX
a
A B C D
16 x 1
MUX
b
A B C D
16 x 1
MUX
c
A B C D

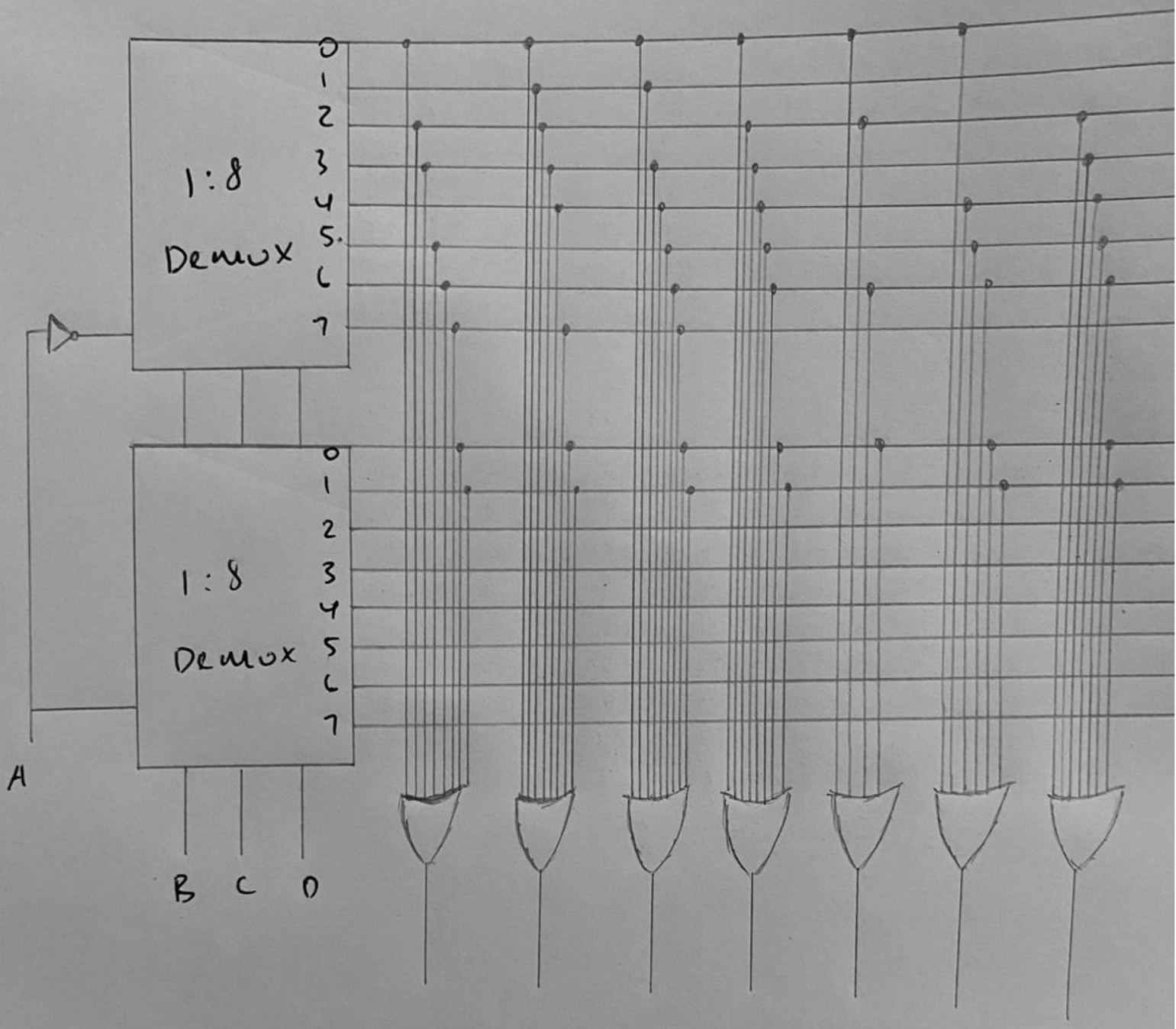

16 x 1
MUX
d
A B C D
16 x 1
MUX
e
A B C D
16 x 1
MUX
f
A B C D


0 0 - - - - - - - - 0 - - - 0 0 0 0 0 0 0 0
16 x 1 MUX
g
A B C D
$\bar{D}$ 1 D 1 - 1 0 0 0
8 x 1 MUX
a
1 - $\bar{D}$ D 1 - 0 0 0
8 x 1 MUX
L
A B C
1 D - - - 0 0 0
8 x 1 MUX
c
$\bar{D}$ - D $\bar{D}$ - 0 0 0
8 x 1 MUX
d
A B C
$\bar{D}$ $\bar{D}$ 0 $\bar{D}$ $\bar{D}$ 0 0 0
8 x 1 MUX
e
A B C
$\bar{D}$ 0 - $\bar{D}$ - 0 0 0
8 x 1 MUX
f
0 1 - $\bar{D}$ - 0 0 0
8 x 1 MUX
g
A B C

6.



6.6.



8.

	8	4	2	1	-1	3	6	-1
	W	X	Y	Z	A	B	C	D
0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	1	0	1
2	0	0	1	0	1	1	0	0
3	0	0	1	1	0	1	0	0
4	0	1	0	0	1	0	1	1
5	0	1	0	1	1	0	1	0
6	0	1	1	0	0	0	1	0
7	0	1	1	1	1	1	1	1
8	1	0	0	0	1	1	1	0
9	1	0	0	1	0	1	1	0

A:

	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{w}\bar{x}$	0	1	0	1
$\bar{w}x$	1	1	1	0
wx	x	x	x	x
$w\bar{x}$	1	0	x	x

$$A = x\bar{y} + \bar{x}y\bar{z} + \bar{w}\bar{y}z + z\bar{y}w + zx + w\bar{y}\bar{z}$$

B:

	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{w}\bar{x}$	0	1	1	1
$\bar{w}x$	0	0	1	0
wx	x	x	x	x
$w\bar{x}$	1	1	x	x

$$B = w\bar{x} + \bar{x}z + \bar{x}y + yz$$

C:

	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{w}\bar{x}$	0	0	0	0
$\bar{w}x$	1	1	1	1
wx	x	x	x	x
$w\bar{x}$	1	1	x	x

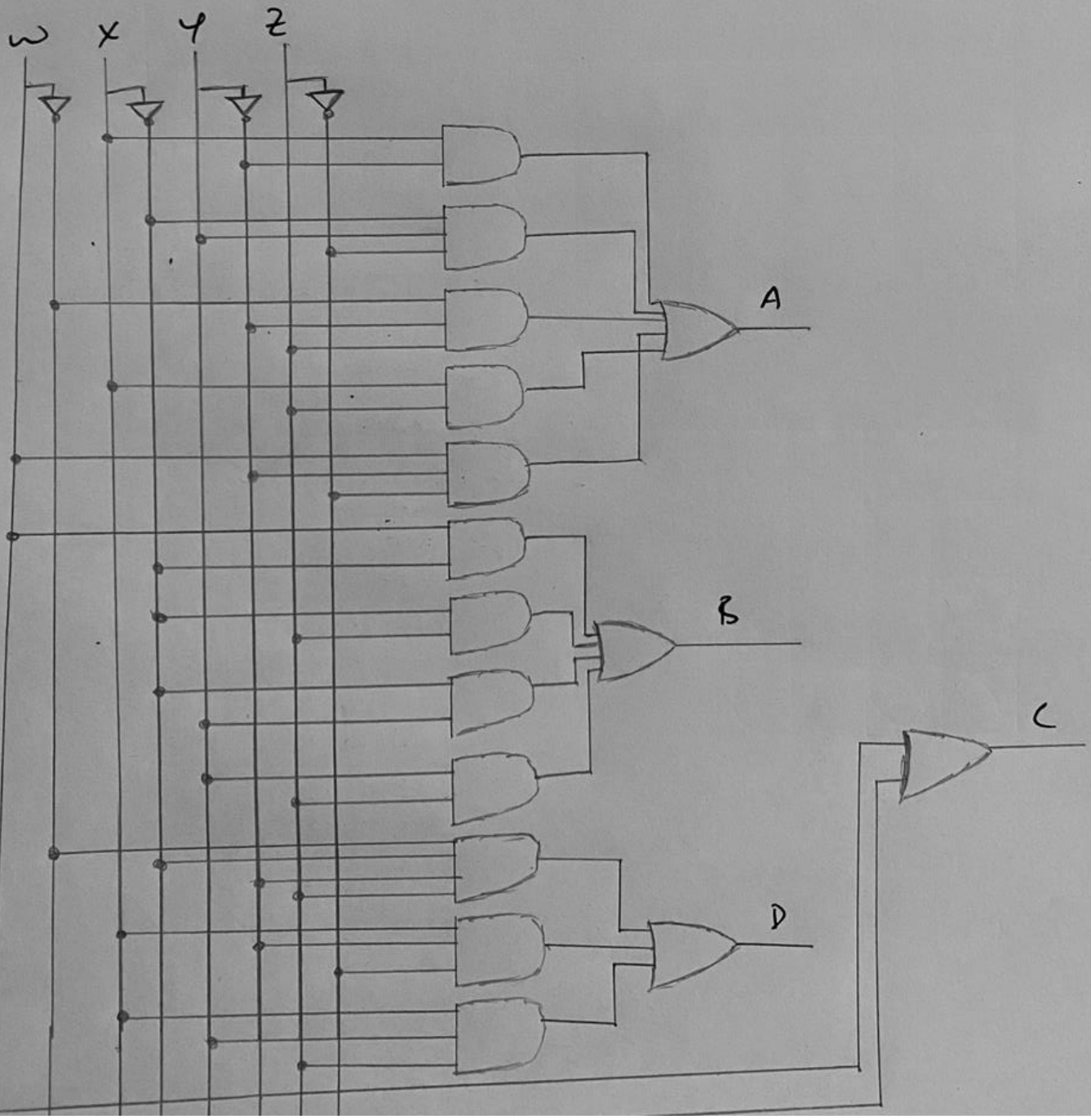
$C = x + w$

D:

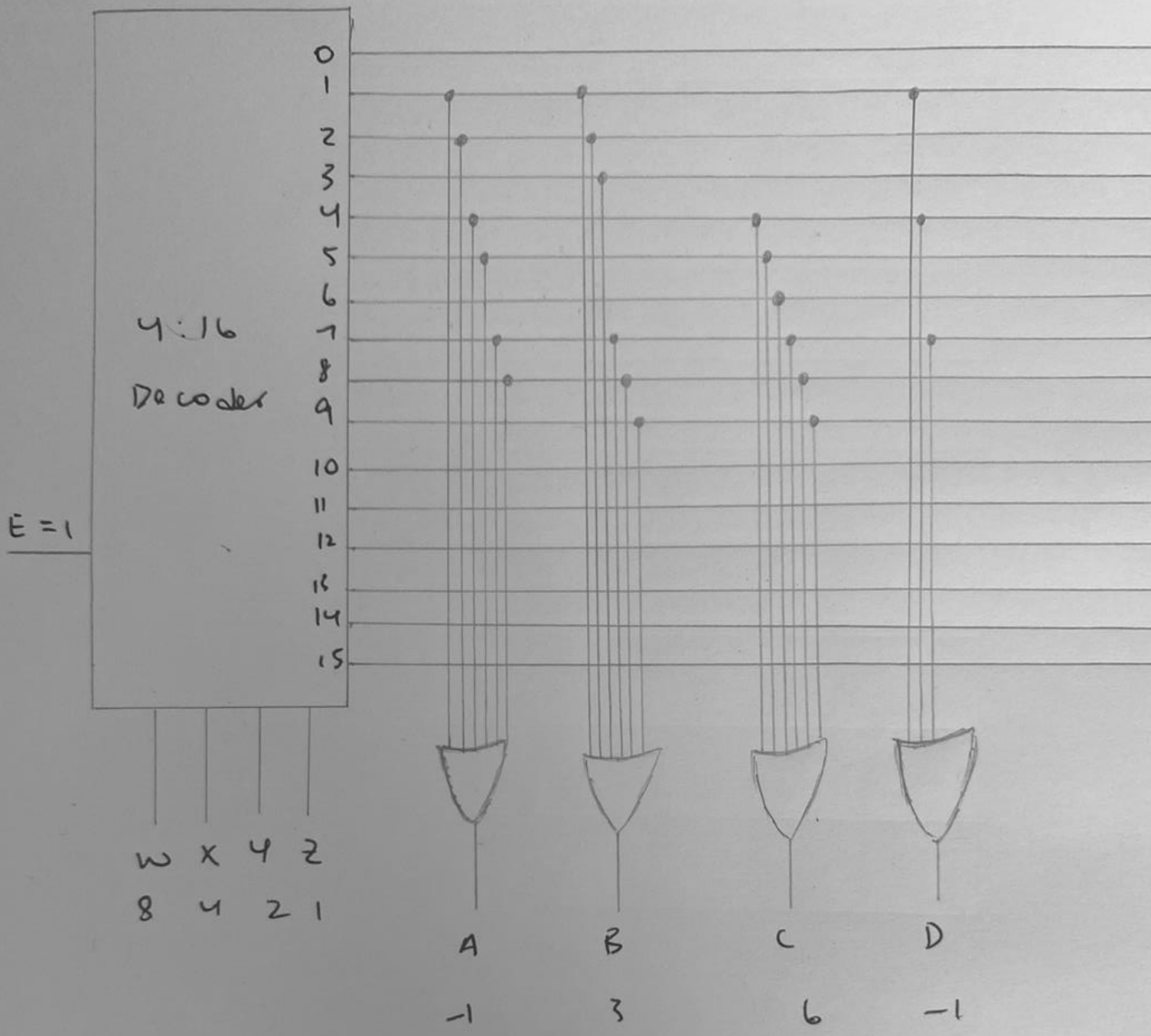
	$\bar{y}\bar{z}$	$\bar{y}z$	yz	$y\bar{z}$
$\bar{w}\bar{x}$	0	1	0	0
$\bar{w}x$	1	0	1	0
wx	x	x	x	x
$w\bar{x}$	0	0	x	x

$D = \bar{w}\bar{x}\bar{y}z + x\bar{y}\bar{z} + xyz$

Circuit diagram:



9.


4:16
Decoder
E = 1
0
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
W X Y Z
8 4 2 1
A
B
C
D
-1
3
6
-1

10.