A novel bandgap voltage reference based on folding compensation

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This letter proposes a novel bandgap reference circuit that utilizes both curvature and folding compensation to achieve a temperature coefficient (TC) of 2.23 ppm/°C. Unlike traditional BGRs, the unique folding compensation method of this circuit improves the performance at low temperature and can also be applied within a specific temperature range.

Introduction: The bandgap voltage reference is a crucial component in analog and mixed-signal integrated circuits, as its performance can impact other chips and circuits. In recent years, several high-order compensation circuits have been proposed to address the high-order term $V_T \ln(T/T_r)$, such as [1–7]. However, [1] uses transistor current gain, which is a function of temperature and results in poorer circuit reliability. Reference [2] relies on a temperature-dependent resistor ratio, which can be affected by manufacturing. Reference [3] uses a Complementary-to-Absolute-Temperature (CTAT) current which is free from thermal non-linearity to compensate for the current Proportional-to-Absolute-Temperature (PTAT). However, its static current is large and it occupies a huge layout space. Since the output bandgap reference voltage in [4, 5] is not generated using resistance, ensuring its accuracy can be challenging. Although [6, 7] perform better, they still exhibit significant deviations at low temperatures.

To address these limitations, this letter proposes a novel bandgap reference based on folding compensation with a temperature coefficient (TC) of 2.23 ppm/°C. The circuit exhibits good TCs at low temperatures and the compensation can be applied to specific temperature regions.

Circuit principle: This circuit uses folding compensation to compensate the output reference voltage. First, PTAT current and CTAT current are generated, and then the base current I_{BASE} and the I_{FOLD} for folding compensation are generated through the two currents above. I_{TRIM} is to compensate the unavoidable errors due to process variations. At last, the final V_{BG} is generated through the compensation of reference voltage with I_{FOLD}.

Figure 1a shows an I_{PTAT} generator. The emitter voltage difference between BJT transistors Q_2 and Q_3 is $\Delta V_{BE} = V_T \ln(N)$, where V_T is the thermal voltage and N is the ratio of the areas of Q_2 and Q_3. It can be seen that ΔV_{BE} is the PTAT voltage, so the current flowing through the resistor R_2 is also the PTAT current I_{PTAT}. Since the current flowing through the collector of BJT transistors $Q_2$and Q_4 is the same and the Q_2 and Q_4 have the same area, their base current I_{BASE} is also the same. The I_{BASE} of Q_4 is copied to the drain of MOSFET M_{18} through a current mirror, so by using KCL, the current flowing through M_6 is $I_{M6} = I_{PTAT} + I_{BASE} - I_{BASE} = I_{PTAT}$. The current through M_6 can be used by other modules.

Figure 1b shows the circuit for generating I_{CTAT} using I_{PTAT}. I_{PTAT} is copied to the collector of BJT transistor Q_7 through a current mirror, so that the base-emitter voltage V_{BE} of Q_7 has a negative TC. Since I_{PTAT} is also copied to the collector of Q_6,and since Q_6 and Q_7 have the same area, the base currents of Q_6 and Q_7 are the same, denoted as I_{BASE}. Thus, the current flowing through the drain of MOSFET M_{28} is $I_{M28} = I_{CTAT} + I_{BASE} - I_{BASE} = I_{CTAT}$. Therefore, we obtain the desired CTAT current. Because I_{CTAT} is used in many places, we design two I_{CTAT} ports, and through the same method, the second CTAT current $I_{M32} = I_{CTAT}$ can be obtained. Both of these CTAT currents can be used by other circuits through a current mirror.

The I_{FOLD} generator, as shown in Figure 2, is a key module for performing folding compensation. The generated I_{FOLD} must meet two

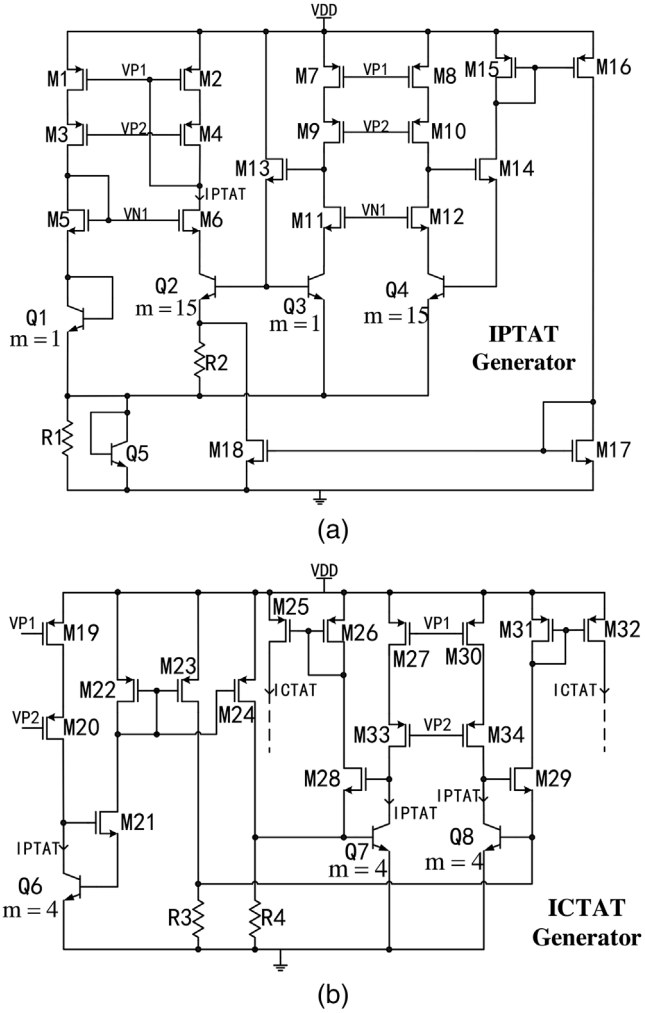

Fig. 1 *The circuits of* I_{PTAT} *generator and* I_{CTAT} *generator. (a)* I_{PTAT} *generator, (b)* I_{CTAT} *generator.*

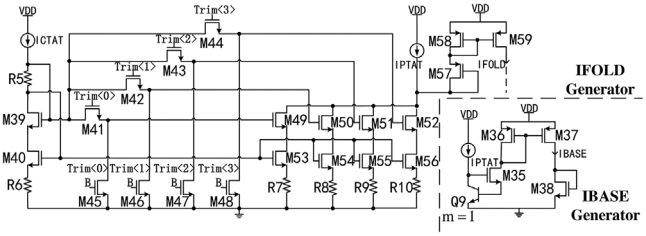

Fig. 2 *The circuits of* I_{FOLD} *generator and* I_{BASE} *generator.*

requirements: (1) The current value is non-zero only when the temperature is below a specific temperature; (2) The current magnitude must be sufficient to compensate for the deviation of the bandgap reference voltage at low temperatures. To meet these requirements, the previously generated I_{PTAT} and I_{CTAT} can be used to obtain the desired I_{FOLD}. By programming the switches Trim<0>~Trim<3>, Trim<0>B~Trim<3>B,

the four current mirrors containing MOSFETs M_{49}~M_{52} can be controlled to adjust the magnitude of I_{CTAT}. The adjusted I_{CTAT} current flows to the source of MOSFET M_{57} after subtracting I_{PTAT}. The role of M_{57} is to act as a cutoff switch, where MOSFET has current only when I_{CTAT}-I_{PTAT} is larger than zero; otherwise, it has no current. Therefore, the generated I_{FOLD} can be expressed as

$$I_{FOLD} = \begin{cases} I_{CTAT} - I_{PTAT} & I_{CTAT} \geq I_{PTAT} \\ 0 & I_{CTAT} < I_{PTAT} \end{cases} \quad (1)$$

The design purpose of the I_{BASE} generator in Figure 2 is to produce the current that compensates for the excess base current of Q_{16} in the V_{BG}

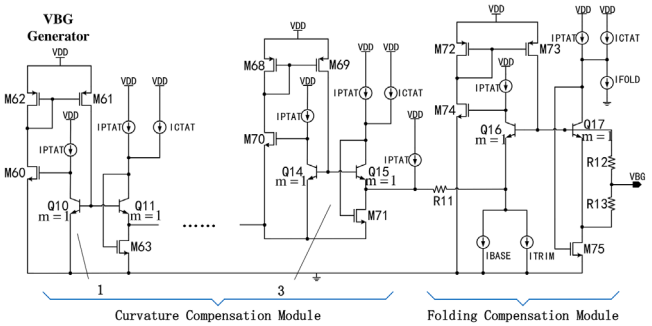

Fig. 3 *The circuit of* V_{BG} *generator.*

generator (Figure 3). As shown in Figure 2, by injecting I_{PTAT} into the collector of BJT transistor Q_9, the base current is obtained, and then the base current is copied to the source of MOSFET M_{37} through a current mirror to obtain I_{BASE}.

The V_{BG} generator, as shown in Figure 3, consists of two parts: curvature compensation module and folding compensation module, where the curvature compensation module consists of three identical sub-modules.

The principle of curvature compensation in this paper is similar to that in [1]: taking the first sub-module as an example, the voltage difference between the base and the emitter of BJT is

$$V_{BE} = V_{g0} - \left(V_{g0} - V_{BE,T_r}\right)\frac{T}{T_r} - (\eta - \theta)V_T \ln\frac{T}{T_r} \tag{2}$$

Since the collector current of transistor Q_{10} is the PTAT current and the collector current of transistor Q_{11} is a constant current, the base-emitter voltage of Q_{10} is

$$V_{BE10} = V_{g0} - \left(V_{g0} - V_{BE10,T_r}\right)\frac{T}{T_r} - (\eta - 1)V_T \ln\frac{T}{T_r} \tag{3}$$

The base-emitter voltage of Q_{11} is

$$V_{BE11} = V_{g0} - \left(V_{g0} - V_{BE11,T_r}\right)\frac{T}{T_r} - (\eta - 0)V_T \ln\frac{T}{T_r} \tag{4}$$

Therefore, the emitter voltage difference ΔV_{BE} between Q_{10} and Q_{11} is

$$\Delta V_{BE} = \left(V_{BE10,T_r} - V_{BE11,T_r}\right)\frac{T}{T_r} + V_T \ln\frac{T}{T_r} \tag{5}$$

As can be seen, the ΔV_{BE} above contains the non-linearity component $V_T \ln(T/T_r)$. This non-linearity is the same as the non-linearity in the V_{BE} (see Equation (2)). Due to this reason, as long as multiple ΔV_{BE} are added together, the high-order term in V_{BE} can be cancelled out effectively.

The principle of the folding compensation is as follows: the current flowing through the Q_{16} collector is I_{PTAT}, and the current flowing through the BJT Q_{17} collector is I_{PTAT}+I_{CTAT}-I_{FOLD}. The excess current I_{FOLD} will cause an additional voltage V_{FOLD} between the base and the emitter of Q_{17}, and this V_{FOLD} is the key to folding compensation. At this point, the emitter voltage difference between Q_{16} and Q_{17} is

$$\Delta V_{BE,FOLD} = \left(V_{BE16,T_r} - V_{BE17,T_r}\right)\frac{T}{T_r} + V_T \ln\frac{T}{T_r} + V_{FOLD} \tag{6}$$

Since the current flowing through resistor R_{11} is I_{TRIM}-I_{PTAT}, a voltage drop $V_{11} = R_{11}I_{TRIM} - R_{11}I_{PTAT}$ is generated across R_{11}. Using the KCL and KVL, the final bandgap reference voltage is obtained as

$$V_{BG}\frac{R_{13}\left(3\Delta V_{BE} + V_{11} + V_{BE16}\right) + R_{12}\left(3\Delta V_{BE} + \Delta V_{BE,FOLD}\right)}{R_{12} + R_{13}} \tag{7}$$

Here, to cancel out the process variations, we have generated the current I_{TRIM} through the combination of I_{PTAT} and I_{CTAT}. The I_{TRIM} generator includes several current mirrors which combine the I_{PTAT} and I_{CTAT} together. The digital codes in the I_{TRIM} generator can control both the magnitude and direction of I_{TRIM}. This programmable scheme effectively cancels out the process variations in the reference voltage.

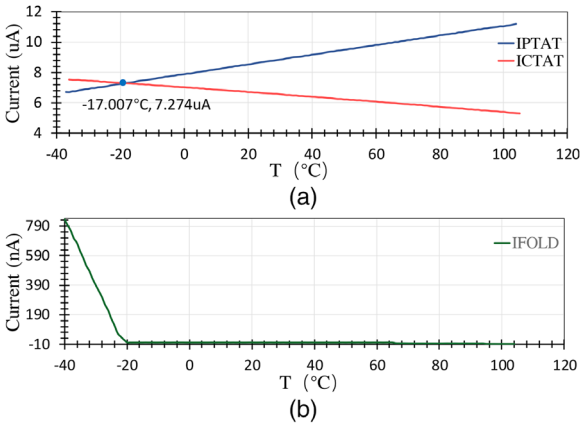

Fig. 4 *Simulation results of* I_{PTAT},I_{CTAT}, *and* I_{FOLD}. *(a)* I_{PTAT} *and* I_{CTAT}, *(b)* I_{FOLD}.

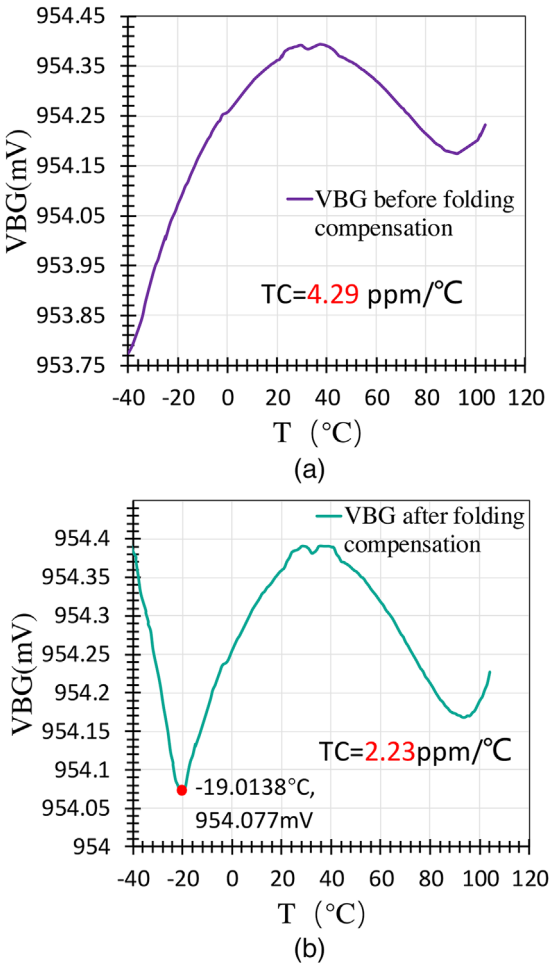

Fig. 5 *Simulation results of* V_{BG} *before and after folding compensation. (a)* V_{BG} *before folding compensation, (b)* V_{BG} *after folding compensation.*

Post-layout simulation results: The proposed bandgap reference was designed in a 0.18-μm CMOS process. Figure 4a shows the generated I_{PTAT} and I_{CTAT}, and Figure 4b shows the generated I_{FOLD}. It can be seen that I_{FOLD} is inversely proportional to temperature when the temperature is below −20°C and approximately zero when above −20°C.

The generated V_{BG} is shown in Figure 5. Figure 5a shows the uncompensated V_{BG}, which has a large deviation when the temperature is below −20°C. The TC is 4.29ppm/°C. Figure 5b shows the V_{BG} after folding compensation. It improves the TC significantly by compensating the part below −20°C with a folding current. It has a TC of 2.23 ppm/°C.

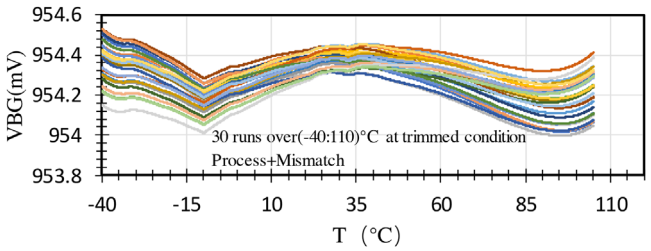

Fig. 6 *Monte Carlo simulation results after trimming.*

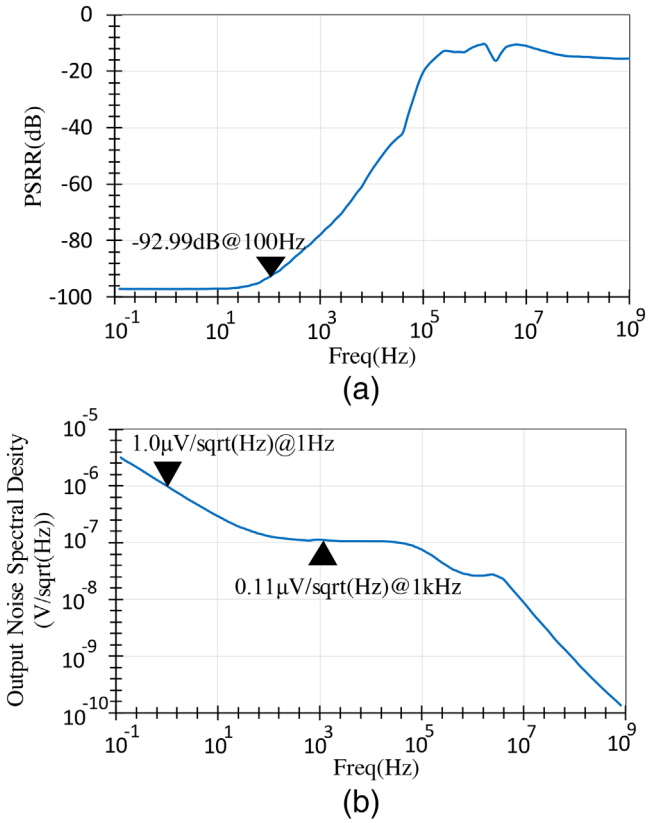

Fig. 7 *Simulation results of PSRR and output noise. (a) PSRR, (b) output noise spectral density.*

Figure 6 presents the V_{BG} as a function of temperature after trimming. Across 30 runs of Monte Carlo simulation, an average TC of 2.2 ppm/°C is achieved. And the max and min TCs are 3.6 and 1.5 ppm/°C.

The simulated PSRR is shown in Figure 7a, showing a rejection of −92.99 dB at 100 Hz. Figure 7b shows the simulated noise spectrum without output loading. It achieves 1.0 μV/$\sqrt{}$Hz at 1 Hz and 0.11 μV/$\sqrt{}$Hz at 1 kHz.

Table 1 compares this work with the state-of-the-art works. When compared to [1] and [8], this work obtains a better TC. Besides, it obtains better noise performance than [6] and [8] and less current consumption than [6]. Also, it is the only circuit that adopts the folding compensation.

Conclusion: This letter proposes a novel bandgap reference based on folding compensation. Folding current is used for folding compensation at the point of large output voltage deviation, and finally the TC is successfully reduced by half, achieving 2.23 ppm/°C.

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Table 1. Comparison between this work and other reported works

	[1]	[6]	[8]	**This work**[a]
Technology (nm)	180	180	350	**180**
V_{BG} (V)	3.11	2.14	2.47	**0.95**
PSRR (dB)	−92@ 100 Hz−74 @ 1 MHz	−63 @ 10 Hz −56 @ 1 kHz	−83 @ DC	**−93 @ 10 0Hz**
Noise(V/$\sqrt{Hz}$)	NA	0.92 μ @ 10 Hz0.44 μ @ 1 kHz	1.2μ@1Hz	**1.0 μ @ 1 Hz 0.11 μ @ 1 kHz**
Temp. range (°C)	−40 to 130	−25 to 125	−45 to 125	**−40 to 110**
TC (ppm/°C)	4.6 (Min) 6.3 (Avg)	0.7 (Min) 1.557 (Max) 1.183 (Avg)	0.9 (Min) 7.5 (Max) 3 (Avg)	**1.5 (Min) 3.6 (Max) 2.2(Avg)**
Current consumption (μA)	NA	409	94	**250**
Area (mm^2)	0.2225	0.256	0.0616	**0.215**
Curvature compensation	Yes	Yes	Yes	**Yes**
Folding compensation	No	No	No	**Yes**

[a]Simulation results.

Conflict of interest statement: The authors declare no conflict of interest.

Data availability statement: Research data are not shared.

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References

1 Zhu, G., et al.: A 4.6-ppm/°C high-order curvature compensated bandgap reference for BMIC. *IEEE Trans. Circuits Syst. II Express Briefs* **66**(9), 1492–1496 (2019)
2 Leung, K.N., et al.: A 2-V 23-μA 5.3-ppm/◦C curvature-compensated CMOS bandgap voltage reference. *IEEE J. Solid-State Circuits* **38**(3), 561–564 (2002)
3 Xu, H., et al.: A novel 0.84 ppm/°C CMOS curvature-compensated bandgap with 1.2 V supply voltage. *Int. J. Electron. Commun* **91**, 1434–8411 (2018)
4 Liu, N., et al.: Sub-ppm/◦C bandgap references with natural basis expansion for curvature cancellation. *IEEE Trans. Circuits Syst. I Reg. Papers* **68**(9), 3551–3561 (2021)
5 Zhou, Z.K., et al.: A resistorless high-precision compensated CMOS bandgap voltage reference. *IEEE Trans. Circuits Syst. I Reg. Papers* **66**(1), 428–437 (2019)
6 Huang, S., et al.: A sub-1 ppm/°C bandgap voltage reference with high-order temperature compensation in 0.18-μm CMOS process. *IEEE Trans. Circuits Syst. I Regul. Pap.* **69**(4), 1408–1416 (2022)
7 An, J., et al.: A wide temperature range 4.6 ppm/°C piecewise curvature-compensated bandgap reference with no amplifiers. In: International Conference on IC Design and Technology (ICICDT), pp. 1–4 (2019)
8 Liu, L., et al.: A 3.6 μVrms noise, 3 ppm/°C TC bandgap reference with offset/noise suppression and five-piece linear compensation. *IEEE Trans. Circuits Syst. I Regul. Pap.* **66**(10), 3786–3796 (2019)