Chapter 1

Basic matrix multiplication function

Chapter 2

Function Permutations

The CPU that the machines on the batch system has the following characteristics¿

Architecture: x86_64
CPU op-mode(s): 32-bit, 64-bit
Byte Order: Little Endian
CPU(s): 8
On-line CPU(s) list: 0-7
Thread(s) per core: 1
Core(s) per socket: 4
CPU socket(s): 2
NUMA node(s): 2
Vendor ID: GenuineIntel
CPU family: 6
Model: 26
Stepping: 5
CPU MHz: 2667.000
BogoMIPS: 5331.94
Virtualization: VT-x
L1d cache: 32K
L1i cache: 32K
L2 cache: 256K
L3 cache: 8192K
NUMA node0 CPU(s): 4-7
NUMA node1 CPU(s): 0-3

Chapter 3

Analysis of Implementation

Chapter 4

blocked version

Bibliography

[1] T. Moeslund, *Image and Video Processing*, Aalborg University, 2 ed., 2010.