Towards Triangle Counting on GPU using Stable Radix binning

Nishith Tirpankar
School of Computing
University of Utah
Salt Lake City, USA
tirpankar.n@utah.edu

Hari Sundar
School of Computing
University of Utah
Salt Lake City, USA
hari@cs.utah.edu

***Abstract*—The pattern of computations of graph algorithms makes them difficult to parallelize. They suffer from erratic data access patterns. We propose a set of algorithmic patterns that enable users to take advantage of fine grained parallelism provided by modern CPU and GPU architectures. This allows accesses to be regularized which improves hierarchical cache access. We also propose a parallel stable binning algorithm that can be used for computing set intersection. This is illustrated through its application to triangle counting in large graphs.**

***Index Terms*—graph algorithms, CUDA dynamic parallelism**

I. Introduction

A. Graph algorithms overview

A number of data and network analytics questions on relational data can be posed as graph problems. For example, the transitivity or clustering coefficient tells us how clustered the nodes in a graph are. Clustered or small world networks having large value of clustering co-efficient have enhanced signal-propagation speed, synchronizability and computational power [1]. Nodes in sub-graphs with this property can be targetted for quick or low energy information disbursement. Another example involves finding the count and presence of certain structures in a graph. Identifying clusters of these patterns [2] or sub-graphs can indicate classes of predators in a food-web or interactions between sensors and effectors in a neural network [3]. A commonly occuring use case is of recommendations to connect with friends of friends in large social networks. It can be computed using the length of the path between two users [4].

B. Triangle counting as an application

A k-truss is a maximal subgraph of a given graph such that each edge in it is contained in at least k-2 triangles. The k-truss in a graph is a sub-graph all the applications mentioned here can use. Triangles are the simplest subgraph in a graph. Counting the number of triangles in a graph is building block that can be used in finding the k-truss [5]. This makes triangle counting such a lucritive problem for the sub-graph isomorphism challenge [6].

C. Different approaches - set intersection/Linear algebra/map reduce/approximation methods for triangle counting

Among the prominent methods for computing the count of triangles in a graph are ones using set intersection, linear algebra, map reduce and approximation methods. Set intersection algorithms [7] involve computing a set of all the possible edges that could generate triangles and counting the number of intersections with the original adjacency list. Innovations in the ordering of the members of the sets as well as ease of distribution of the work among multiple processes makes this class of algorithms highly performant [8] and ideal for implementation on shared memory systems. This class of algorithms is what inspired our work. Linear algebra approaches involve variantions of $\sum_{i,j} A^2 \circ A$ where A is the adjacency matrix [6]. One variantion involves splitting up the adjacency matrix into lower and upper triangular matrices not including the diagonal $A = L + U$. The product $B = L * U$ counts the number of paths of length 2 in the graph. Finding if the wedges close by performing a Hadamard product $C = A \circ B$ gives us the triangle count $\sum_{ij}(C)/2$ [9], [10]. Map reduce approaches use frameworks such as Hadoop and distribute the adjacency lists among nodes arbitrarily. For a more detailed overview refer to [11], [12]. An interesting class of algorithms rely on wedge sampling to get an approximate count of the number of triangles. The work done in [13] shows an excellent use case that uses the birthday paradox to sample a set of wedges from the set of vertices and finding the approximate number of triangles by finding the number of closed wedges in this set.

D. Challenges of parallelizing graph algorithms on modern architectures

Graph algorithms are hard to parallelize and even harder to get good performance on modern architectures, both on many-core CPUs as well as on GPUs. The key challenge is that the nature of computations depends on the structure of the graph, i.e., the sparsity and specifically the sparsity pattern of the adjacency matrix of the graph. This means that the performance of the algorithm is directly dependent on the input graph's structure. This makes it very challenging to implement graph algorithms on parallel architectures where exclusive write access would be needed to obtain good parallel performance. At a more fundamental level, we also have to deal with having indirect memory access, due to the nature of adjacency lists, the most popular and efficient way to store graphs. Indirect memory access is bad for performance

as it is difficult to utilize the cache effectively, leading to even higher costs for data access. One of the reasons for the popularity of linear algebra formulations for graph algorithms is the maturity of sparse linear algebra codes, especially on multicore CPU and GPUs. While these do indeed improve the performance to a certain extent, they are still sub-optimal. For one, unlike numerical algorithms, most graph algorithms, including triangle counting, are discrete in nature. Secondly, linear algebra formulations, especially those involving matrix-matrix products can require extensive data-movement and potentially increase both storage and compute requirements to $\mathcal{O}(n^2)$. For this reason, we wish to develop efficient graph algorithms that expose fine-grained parallelism and avoid indirect memory access. Such a formulation will enable efficient implementations on manycore processors and on GPUs. We now illustrate this idea using an example of set intersection, as that is one of the most expensive parts of triangle counting.

E. Data-access concerns for set intersection

Set intersection among two lists is an expensive operation if the lists are large. Consider the problem of finding the number of edges in a list E', of length m, that are also present in list E of length n. A common approach for solving this problem is to sort E with cost $\mathcal{O}(n \log n)$ and then perform m binary searches for a total cost of $\mathcal{O}((m+n)\log n)$. In many cases this is reasonable. However, from a performance perspective, if n is large, although the complexity of $\log n$ appears reasonable, it is very expensive on modern architectures, as this is random access into a very large array, each access potentially being retrieved from main-memory. An alternate approach is to sort both E and E', and performing a linear scan to determine matches. The complexity of this approach is similar at $\mathcal{O}(n \log n + m \log m)$, but this can be much faster, especially if using efficient sorting algorithms. This is in principle similar to using efficient linear algebra routines to obtain efficient implementations. However, it is possible to do even better if we design from first principles. We describe one such approach now.

If we use a most significant bit radix sort to sort the lists E and E', we can improve the performance significantly, especially if we sort the lists simultaneously and use early termination. Note that a radix sort is efficient becuase data is accessed directly and in a streaming fashion, making it extremely amenable to deep cache hierarchies. Each element of the list is an ordered integer tuple (u, v). For a value (u, v) in E to be equal to a value (u', v') in E', each bit in the binary representation of u must match u' and each bit in v must match v'. We use this idea to bucket the entire list one bit at a time. Figure 1 gives an example of how a recursive bucket traversal can be used to perform intersection.

To perform bucketing, we first take the integer u and mask the highest bit. The resultant value is concatenated with the masked highest bit of v. The resultant value is a number between 0 and 3. This lets us put each value in E and E' into the buckets r_0 through r_3 as shown in the last figure in figure 1. From this point we will recursively compute intersections

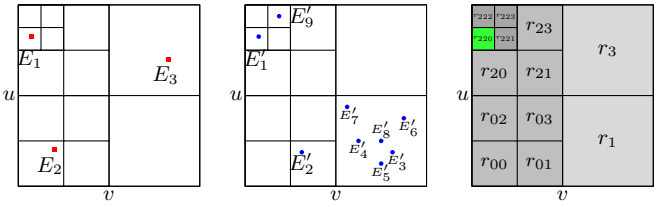

Fig. 1. From left to right: Elements of edge list E with the bucket traversal overlay; elements of edge list E' with the bucket traversal overlay; bucket traversal with region labels.

only if both E and E' have edges in the bucket. As shown in the first and second of figure 1 we can see that bucket r_1 in E does not have any edges while bucket r_3 in E' does not have any edges. Hence, we do not need to recurse in these buckets at all. Now r_1 has edges E'_3 through E'_8 which do not need to be tested. We have eliminated the need to test 6 out of 9 edges in E'. This is a significant reduction in work. Also, r_3 is eliminated as a potential bucket for recursion in E removing the need to test edge E_3. In the next level of recursion we eliminate buckets r_{00} through r_{03} as well as r_{20}, r_{21}, r_{23}. Recursing on r_{22} further we see that r_{220} is the only bucket which has edges both in lists E and E'. E'_9 in bucket r_{223} does not have corresponding edges in E. Since r_{220} has very few elements in both E and E' we can compare each element in E' to each element in E for r_{220} to find that E'_1 has a matching edge E_1 and is the only edge also present in list E. Although this is a synthetic example, it demonstrates that sparse distributions on E and E' will result in elimination of a large set of candidates for intersection quickly. Each level of recursion is $O(|E| + |E'|)$ i.e. it is $O(n)$ in the size of the lists.

II. Methods

A. Linear algebra approach to triangle counting

The problem of finding the count of triangles can be interpreted as counting all paths(walks) of length 2 between two vertices if there is a closure i.e. an edge between the two vertices. An element $A(i, j)$ in the square adjacency matrix defines the number of paths or the weight of an edge between nodes i and j. For an undirected unweighted graph the adjacency matrix elements are 0 or 1. We know that the n^{th} power of an adjacency matrix A^n gives us the number of walks $A^n(i, j)$ of length n that exist between nodes i and j. For $n = 2$ the walks are paths if the diagonal of the adjacency matrix is 0. Thus, each element of A^2 defines the number of paths of length 2. Let C denote the Hadamard product or elementwise product of A^2 with the adjacency matrix $C = A^2 \circ A$. An element of matrix $C(i, j)$ gives us the number of triangles that the edge (i, j) is a part of. Hence, the sum of all the elements of this matrix gives us the total number of triangles in the graph. Each triangle is counted three times in the matrix C - once for each edge. Also, in an undirected graph each edge is counted twice as $A(i, j)$ and $A(j, i)$ both indicating the same edge. This implies that $\sum_{ij}(C)$ counts

each triangle 6 times. The total number of triangles is given by equation 1:

$$n_T = \sum_{ij}(C)/6 \tag{1}$$

Triangle counting using this method has a high work complexity and is viable only for graphs with dense adjacency matrices. Most graphs tend to have sparser adjacency matrices. We can reduce the work complexity by techniques such as using masked multiplication after LU decomposition [10]. The decomposition as well as the masked multiplication is computationally expensive since it uses a significant amount of communication between workers. We can reduce the amount of communication by using a set intersection approach.

B. Two step algorithm

Our algorithm consists of two main steps. The first step involves finding out all the possible combinations of wedges that exist in our graph. This is computed using the adjacency list representation of the graph. The result of this step is a list of edges closing the wedges, hence forming a triangle. The second step is the radix bucket based set intersection. In this step we find out if the list of candidate edges computed before is actually present in the graph. The following sections describe these steps in detail.

C. Finding candidate closure edges E'

While generating the set of candidate edges we have focused on maintaining exclusive access to the input and output buffers as well as coalescing our reads and writes. This ensures that the memory accesseses which are sequential will benefit from hierarchical memory caches in GPU architectures. Ensuring exclusive read and exclusive writes for large E and E' requires us two know two things. The size of the E' output buffer to allocate in the global memory. The read boundaries of E in which each thread will operate to generate the wedges along with the write boundaries of E' where it will write the candidate edges closing these wedges. This is performed by the algorithm 1.

Algorithm 1 Compute candidate edges for closure test.

1: **function** COMPUTE_$E'(E)$
2: $E \leftarrow$ RADIX_SORT(E) ▷ $E(u, v)$ by u first then v
3: $cnt[p] \leftarrow$ PARALLEL_COUNT(E) ▷ use transitions
4: $E_{len} \leftarrow$ PARALLEL_REDUCE($cnt[p]$)
5: ALLOCATE($E_{index}, E_{degree}, E'_{size}$) ▷ size E_{len}
6: $E_{index} \leftarrow$ PARALLEL_OFFSETS(E, p)
7: $E_{degree} \leftarrow$ PARALLEL_DEGREE_CALC(E_{index}, p)
8: $E'_{size} \leftarrow$ PARALLEL_SIZE_CALC(E_{degree}, p)
9: $E'_{size\_scan} \leftarrow$ INCLUSIVE_SUM_SCAN(E'_{size})
10: $E' \leftarrow$ PARALLEL_GEN(E, E_{index}, E'_{size_scan})
11: **return** E'

The input to algorithm 1 is the edge list E. Each element in the list E is an ordered tuple (u, v) representing a pair of vertices. If the number of vertices in the graph fit within the bounds of an integer container, a single element of E can be interpreted as a long integer. Accounting for endianness might require reordering (u, v) to (v, u). The radix sort in line 2 of algorithm 1 is performed on the edge list E using the fast double buffered tunable radix sort from [19]. The resultant list is the adjacency list since it is sorted by u first and v next. We refer to the adjacency list as E here onwards. Since radix sort has a work complexity of $O(bn)$ where b is the number of bits in the container which is fixed, the asymptotic work complexity of radix sort is $O(n)$. The parallel time complexity of this shared memory implementation is $O(n/p)$ where p is the number of threads executing simultaneously. In steps 3 and 4 of algorithm 1, the total number of vertices which is the length of the first dimension of the adjacency list E_{len} is found. The next 4 steps are used to calculate the indexes in the input buffer E_{index} and output buffer E'_{size_scan}.

Each step from lines 6 through 8 is performed in the same kernel although they have been explicitly separated in the algorithm 1. In line 6 the p processors compute the index locations of the beginning of the adjacency list of each vertex and write the result to E_{index}. The difference between consecutive index values in E_{index} is used in line 7 to compute the degree of each vertex. The number of wedges centered on a vertex in the adjacency list is dependent on the degree of the vertex. For each vertex in the adjacency list, a wedge can be formed by selecting one other edge in the adjacency list. We can remove duplicate wedges by only considering the $\binom{deg}{2} = \frac{deg(deg-1)}{2}$ combinations instead of the deg^2 permutations. The number of candidate edges is the number of closing edges which is 1 for each wedge. This value is computed in line 8 and stored in E'_{size}.

The inclusive scan sum of E'_{size} gives us the index locations in E' where the combinations corresponding to each vertex in the adjacency list will be written. The inclusive sum is computed using the NVIDIA cubs radix sort [19]. In the final step in algorithm 1, line 10, each thread takes ownership of one or more vertices in the adjacency list E. For each vertex u having degree deg in the adjacency list, the $\frac{deg(deg-1)}{2}$ combinations of edges corresponding to wedges will be written out to the index locations in E' pointed out by E'_{size_scan}.

D. Set intersection using radix bucketing

Counting of the triangles is done by finding out if each edge in E' is actually present in E. Performing a lookup for each member from E' in E can be a $O(|E'|log(|E|))$ operation if E is sorted using a naive binary tree. But E itself can be very large and may not fit in memory even if we batch the lookups of members of E'. In this case we need an algorithm which can scale well and work on shared as well as distributed memory architectures. Although our implementation is on a shared memory SIMD device, we have designed the algorithm to be extended onto distributed memory SPMD architectures. The motivation for our algorithm is the MSD bucketing algorithm which is at the core of the fastest sorting algorithms [14]. It is easy to split up the work among threads with a low communication overhead between recursions and small amount of inter-thread communication.

Note that this algorithm is recursive. It fits very well with the NVIDIA CUDA Dynamic Parallelism extension [21]. The algorithm is shown in algorithm 2.

Algorithm 2 Count triangles by counting $|E \cap E'|$.

```
1:  t_cnt = 0
2:  b = 2^d                          ▷ d = radix bits, b = radix buckets
3:  function INTERSECT_COUNT(E, E', t_cnt, depth)
4:      if |E| = 0 ∧ |E'| = 0 then
5:          return
6:      if depth ≥ depth_max then
7:          t_cnt = t_cnt + |E'|
8:          return
9:      if |E| ≤ thr ∨ |E'| ≤ thr then
10:         t_cnt = t_cnt+SEQ_INTERSECT_CNT(E, E')
11:         return
12:     E_cnt[b] ← PARALLEL_COUNT(E, depth)
13:     E'_cnt[b] ← PARALLEL_COUNT(E', depth)
14:     E_cnt_scan ← vec^-1(INC_SUM_SCAN(vec(E_cnt^T)))
15:     E'_cnt_scan ← vec^-1(INC_SUM_SCAN(vec(E'_cnt^T)))
16:     for all b do
17:         E_buf[b] ← MOVE(E, E_cnt_scan[b])
18:     for all b do
19:         E'_buf[b] ← MOVE(E', E'_cnt_scan[b])
20:     for all b do
21:         INTERSECT_COUNT(E_buf[b], E'_buf[b], t_cnt, depth + 1)
```

In algorithm 2, the triangle count t_cnt is initialized to 0 and it will be updated atomically by the threads as they find valid candidate edges in E'. We can specify the number of radix bits and hence the number of buckets to use for the algorithm up front. The recursive function takes as parameters the edge list E, the candidate edge list E', the pointer to the triangle count t_cnt and the current depth of the recursion $depth$. Early recursion termination happens on lines 4, 6 and 9. The termination conditions on lines 4, 6 are self-explanatory. A hybrid approach towards the tail end of the recursion is known to perform better [16]. When the input is small i.e. $|E|$ and $|E'|$ are smaller than a threshold thr we perform a simple sequential intersection count and add it to t_cnt. Although we have not implemented it, its worth mentioning that the OrderedMerge demonstrated in [17], [18] are alternatives that can yield substantial improvements at the tail end of the recursion.

The first step of the recursion is the parallel count. The parallel count in lines 12 and 13 of algorithm 2 distributes the input list among p threads. Each thread will process $\frac{n}{p}$ edges. A simple masking operation for the vertices of each edge as shown in equation 2 tells us the bucket to which q will belong.

$$(q \gg (2^{depth_{max}-depth} - (d-1))) \wedge (b-1) \qquad (2)$$

The b counts E_{cnt}, E'_{cnt} shown in line 12 of algorithm 2 will be populated with a time complexity $O(\frac{|E|}{p})$ and $O(\frac{|E'|}{p})$ assuming the p threads work simultaneously. This count is computed in global shared memory and is a matrix of size $p \times b$ since the local count computed by each thread is not summed up yet. For the move to be performed in parallel by p threads in lines 17 and 19, we need to know the index location in the output buffers E_{buf} and E'_{buf} where the data will be moved.

The steps in lines 14, 15 of algorithm 2 perform the task of computing the index locations for the move. The operator vec used in line 14 is the vectorization operator [20] that will convert the $p \times b$ matrix into a column vector of size $bp \times 1$. An inclusive scan of this vector gives us the index location boundaries where each thread will perform a move operation for each bucket. The inclusive sum scan has a work complexity of $O(pb \cdot log(pb))$ and a time complexity defined by the Kogge-Stone or Hillis-Steele scan algorithms [14]. This enables us to perform the move as an EREW(exclusive read, exclusive write) operation in the final step. The vec^{-1} operator simply converts the $bp \times 1$ vector into a $p \times b$ matrix. Note that the vec and vec^{-1} and transpose operations do not have to be performed explicitly if the E_{cnt} is stored in column major order.

The last step before recursion in algorithm 2 is the data movement. In line 17 the edges in E are moved based on the bucket they belong, to the offsets pointed by E_{cnt_scan} in the output buffer E_{buf}. The move is done for E' in line 19. This stable operation requires just two buffers of size $2\times(|E|+|E'|)$ since the input buffer at $depth$ can be used as the output buffer at recursion $depth + 1$ and vice versa.

Intersect_count will be called recursively for each bucket with the corresponding data as shown in line 21. The pointer to a global memory t_cnt is also passed on. The recursive call is made to all the buckets simultaneously - the loop over all buckets has only been shown for clarity. Similarly, the loops in lines 17, 19 also run simultaneously.

III. Results and conclusion

A. Experimental setup

We used a single node in the CHPC cluster with the NVIDIA Tesla P100 GPU card for our experiments. The Tesla P100 of the Pascal architecture has 16GB of global memory with 56 streaming multiprocessors. Each multiprocessor has 64 cores bringing the total number of cores to 3584. Its single precision performance is rated at 9.3 TFlops. The host node has 2 14-core Intel Broadwell processors E5-2680 v4 running at 2.4 GHz with 256 GB RAM.

B. Effect of changing the size of graph sets $|E|$ and $|E'|$ on the running time

To test scaling we demonstrate the effect of changing two major properties of the graph. The number of edges $|E|$ in the graph and the density of the graph which changes as $|E'|$ changes. In the first part of the table I we can see that increasing the number of edges $|E|$ in a graph does not have a significant impact on the time taken to COMPUTE_E'. For example, although the graph Theory-3-4-5-9-B1k.tsv has more edges 13166 than the graph Theory-25-81-B1k.tsv 8312, the time taken to construct E' is higher for the graph with a smaller number of edges $|E|$. The time taken to COMPUTE_E' is directly proportional to the number of candidate edges $|E'|$.

Ideally we expect that INTERSECTION_COUNT would take the same amount of time to compute with larger $|E'|$ as evidence of strong scalability. Practically, if the rate of increase of the the time taken to compute INTERSECTION_COUNT increases slower than the rate of increase in $|E'|$, we can expect the algorithm to scale. The graphs Theory-3-4-5-B*k.tsv have 3360, 10830 and 5339 candidate edges each. The time to compute their intersection with E is on average 0.079 seconds. In graphs Theory-16-25-B*k.tsv, the number candidate edges goes up by more than 10 times to 87600, 105620 and 88943 compared to Theory-3-4-5-B*k.tsv. But the time to compute INTERSECTION_COUNT less than doubles at an average of 0.146 seconds. This trend continues as the size of the graphs increases.

For the graphs Theory-3-4-5-9-B1k.tsv and Theory-25-81-B*k.tsv the time to compute INTERSECTION_COUNT increases at a significantly higer rate. The disparity in this increase in the time taken by INTERSECTION_COUNT can be attributed to the maximum recursion depth at which the recursion terminates. For the graph Theory-3-4-5-9-B2k.tsv, 85 recursive calls are made to the INTERSECTION_COUNT kernel while for the graph Theory-3-4-5-9-B1k.tsv 2647 recursive calls are made. The overhead of invoking a kernel is significantly high resulting in a lower performance. For the graphs Theory-25-81-Bk.tsv, Theory-25-81-B1k.tsv and Theory-25-81-B2k.tsv, the number of recursive calls to INTERSECTION_COUNT is 6502, 6877 and 6522 respectively. We are still working on the problem of tuning the threshold parameter at which to perform sequential intersection counting which is responsible for this. This paremeter is referred to in algorithm 2 line 9 as thr. In our current implementation this is fixed at 1024.

It should be noted that the number of triangles in the actual graph does not really have an effect on the running time. The running time for dataset Theory-3-4-5-Bk.tsv at 0.075923 seconds is close to the total running time for Theory-3-4-5-B1k.tsv of 0.083499 seconds. The difference in the number of triangles 0 against 287 does not increase the total running time significantly.

C. Effect of changing the structure of the graph on the running time

The p2p-Gnutella dataset has roughly the same density and connectivity for its graphs since $|E'|$ is about 450000 except for p2p-Gnutella30_adj.tsv and p2p-Gnutella31_adj.tsv while the number of edges range from 40000 to about 100000. This can be seen in the second set of the results in table I. The structure and connectivity characteristics of the graph do not have a significant effect on the running time which is constant at about 1.8 seconds as seen in table I. The last 2 graphs in this set p2p-Gnutella30_adj.tsv and p2p-Gnutella31_adj.tsv have a larger size of the candidate set E' resulting in longer running time. Thus, if the number of candidate edges is approximately constant, changing the number of edges does not have a pronounced impact on the total running time.

D. Comparision with the serial implementation miniTri

To provide a baseline comparision we have provided the running times of miniTri for the same graphs in the last column in table I. miniTri is a triangle based data analytics tool. It has a linear algebra based triangle enumeration implementation which is discussed in [22]. The running times of the sequential linear algebra algorithm are lower than the running times of our technique especially for smaller graphs. But as the size of the graphs increase, the run times are more comparable. This points to the incompatibility of our algorithm with the CUDA Dynamic Parallelism extension [21]. The overhead of launching kernels recursively is large. This becomes significant if the depth of the recursion is high or the number of recursive calls is large.

E. Conclusion

The strategy to generate the offsets where we can read from and write processed results can be effectively applied for various parallel tasks. It is scalable as can be seen by the run timings for similar graphs in table I. The isolation of data buffers between different workers implies that we can not only use this technique on a shared memory architecture but on distributed architectures as well. Although we have not demonstrated that capability of the technique, we can extend the algorithm to work on a hybrid shared and distributed memory architecture. This will enable us to process larger graphs on a cluster of GPU nodes which is a part of our ongoing effort. This initial implementation has highlighted several areas of improvement. The CUDA dynamic parallelism extension suffers from the overhead of launching kernels. The number of threads that can be launched as well as the recursion depth is also limited by the compute capability of device [21] and the amount of global memory on the device. It is ideal for traversing wide and short recursive trees. The large overhead of kernel launces for dynamic parallelism implies that an iterative solution will work better on CUDA architectures. The iterative approach needs to be explored. Tuning the threshold for early termination of the recursion while switching to a non-recursive parallel version of SEQ_INTERSECT_CNT(E, E') is another area that needs to be explored.

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				Run time(seconds)			miniTri run time(seconds)
Dataset	$\#edges\|E\|$	size of $\|E'\|$	$\#triangles$	COMPUTE_E'	INTERSECT_COUNT	Total	Total
Effect of varying size of the graph $\|E\|$							
Theory-3-4-Bk.tsv	48	96	0	0.002314	0.039135	0.041449	0.001309
Theory-3-4-B1k.tsv	62	225	36	0.002321	0.034009	0.03633	0.002192
Theory-3-4-B2k.tsv	62	138	1	0.002464	0.032879	0.035343	0.001144
Theory-3-4-5-Bk.tsv	480	3360	0	0.00336	0.072563	0.075923	0.007645
Theory-3-4-5-B1k.tsv	692	10830	287	0.004287	0.079212	0.083499	0.013159
Theory-3-4-5-B2k.tsv	692	5339	7	0.003132	0.08584	0.088972	0.006041
Theory-16-25-Bk.tsv	1600	87600	0	0.015061	0.119477	0.134538	0.087803
Theory-16-25-B1k.tsv	1682	105620	400	0.017741	0.189551	0.207292	0.07311
Theory-16-25-B2k.tsv	1682	88943	1	0.015112	0.129343	0.144455	0.093247
Theory-3-4-5-9-Bk.tsv	8640	319680	0	0.025373	0.374776	0.400149	0.193648
Theory-3-4-5-9-B1k.tsv	13166	1223427	9107	0.11025	12.35139	12.46164	0.76838
Theory-3-4-5-9-B2k.tsv	13166	522804	35	0.02512	0.797365	0.822485	0.32836
Theory-25-81-Bk.tsv	8100	2154600	0	0.296968	58.645665	58.942633	1.309457
Theory-25-81-B1k.tsv	8312	2378865	2025	0.322544	65.225054	65.547598	1.432732
Theory-25-81-B2k.tsv	8312	2165433	1	0.300018	58.99413	59.294148	1.30335
Effect of changing edge density by keeping $\|E'\|$ constant and changing $\|E\|$ on running time.							
p2p-Gnutella04_adj.tsv	79988	518694	934	0.006057	2.112742	2.118799	0.436732
p2p-Gnutella05_adj.tsv	63678	439066	1112	0.006267	1.968307	1.974574	0.363753
p2p-Gnutella06_adj.tsv	63050	422567	1142	0.006463	1.633593	1.640056	0.339405
p2p-Gnutella08_adj.tsv	41554	346033	2383	0.006026	1.893056	1.899082	0.273986
p2p-Gnutella09_adj.tsv	52026	411347	2354	0.006432	1.783205	1.789637	0.313568
p2p-Gnutella25_adj.tsv	109410	533121	806	0.006618	1.998373	2.004991	0.486104
p2p-Gnutella30_adj.tsv	176656	923756	1590	0.006855	3.528112	3.534967	0.80267
p2p-Gnutella31_adj.tsv	295784	1568174	2024	0.007118	5.746889	5.754008	1.521094

TABLE I

TWO SETS OF RESULTS. THE FIRST SET CONSISTS OF GRAPHS WITH ZERO, MANY AND SOME TRIANGLES. WE SEE THE EFFECT OF CHANGING THE SIZE OF THE GRAPH HERE. THE SECOND SET REPRESENTS GRAPHS WHERE THE NUMBER OF EDGES $|E|$ VARIES BUT THE SIZE OF THE SET E' IS ROUGHLY CONSTANT.

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