

Stereo Camera for Parallelia

Variant: [No Variations]

2016-02-18
VIII

RELEASED

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DESIGN CONSIDERATIONS

DESIGN NOTE:
Example text for informational design notes.

DESIGN NOTE:
Example text for critical design notes.

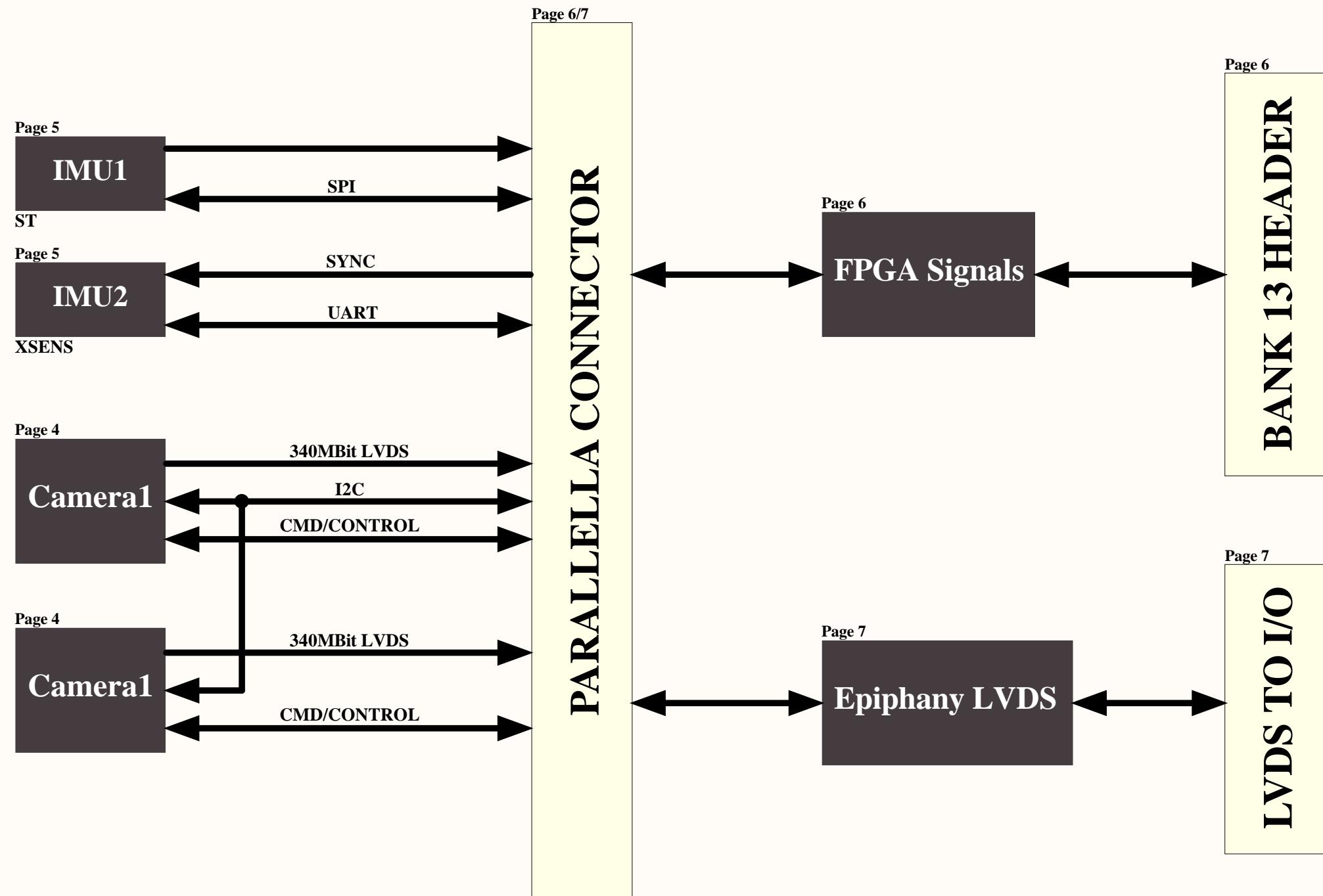
DESIGN NOTE:
Example text for cautionary design notes.

LAYOUT NOTE:
Example text for critical layout guidelines.

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Title:	Stereo Camera for Parallelia
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Stereo Camera for Parallella

(Block Diagram)

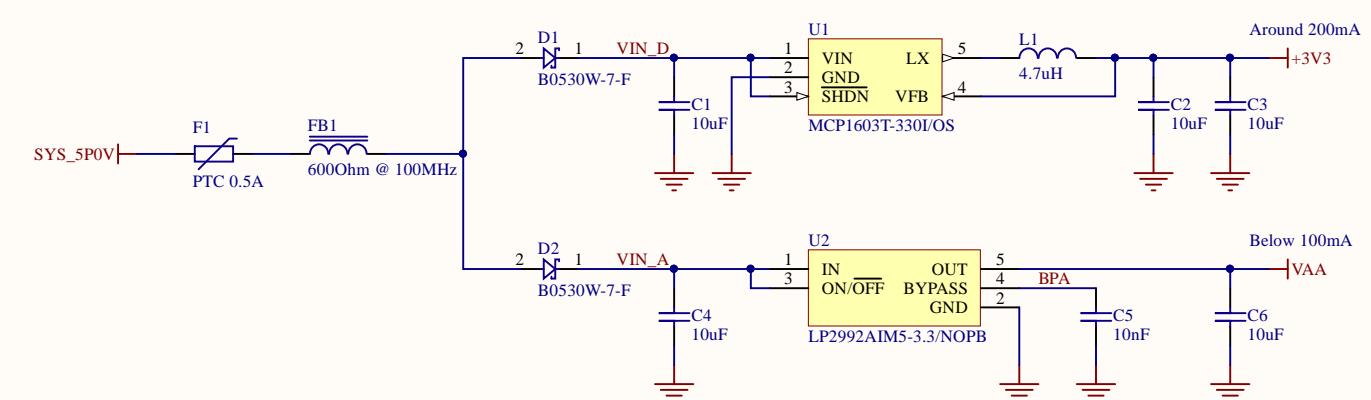


CLOCKS/TOP & PCI

Page 3
ANALOG/DIGITAL POWER

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Title:	Stereo Camera for Parallella
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Power

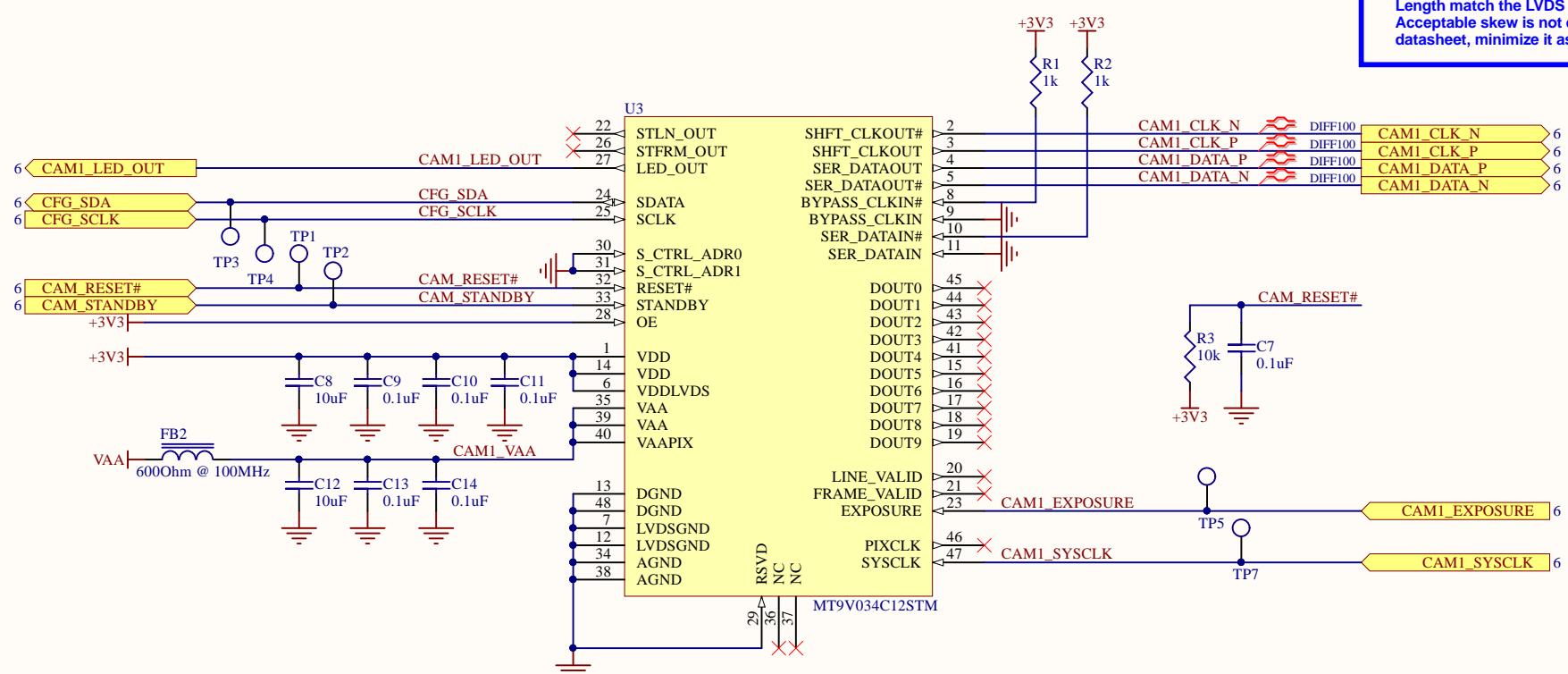


CLOCKS/PLL & PCIE

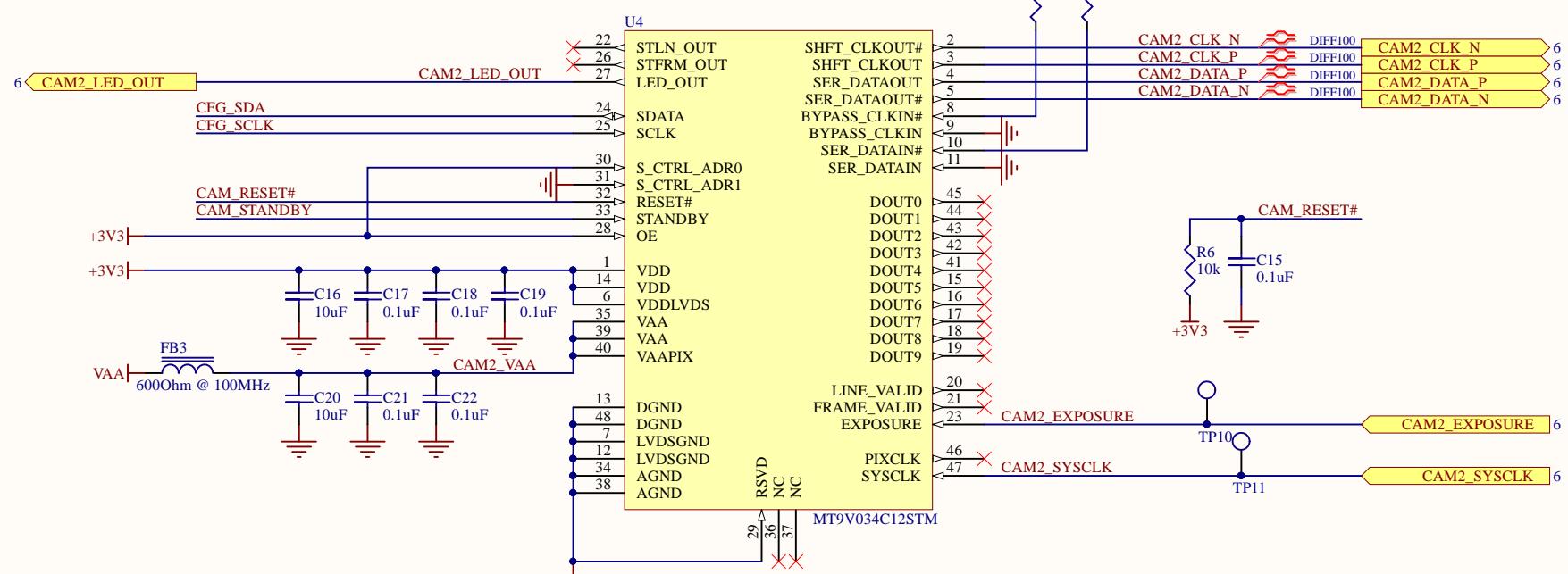
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Title: Stereo Camera for Parallella	Variant: [No Variations]
Page Contents: [03] - POWER.SchDoc	Checked by
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Image Sensors

LAYOUT NOTE:
Length match the LVDS traces.
Acceptable skew is not defined in the
datasheet, minimize it as much as possible.



LAYOUT NOTE:
Length match the LVDS traces.
Acceptable skew is not defined in the
datasheet, minimize it as much as possible.



LM1
CMT821

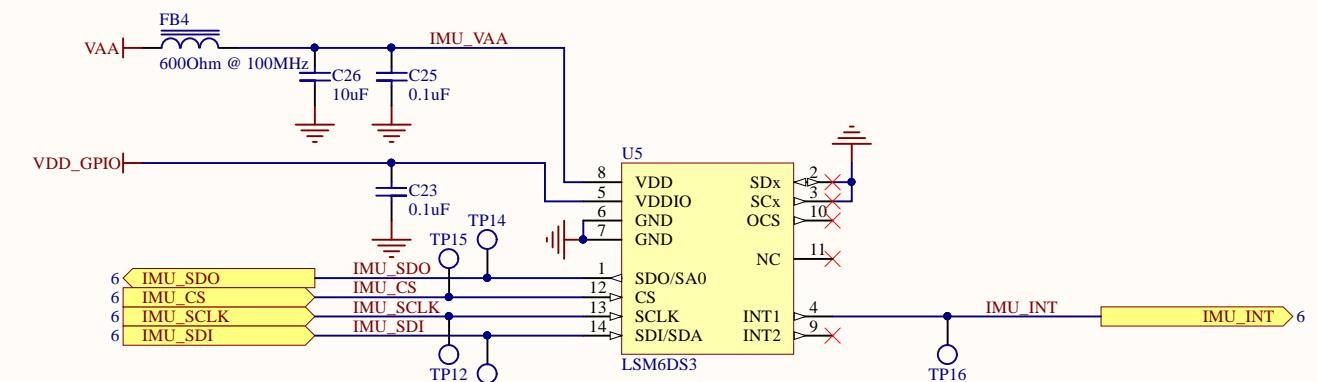
LM2
CMT821

CLOCKS FOR IMAGE

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Title: Stereo Camera for Parallella	Variant: [No Variations]
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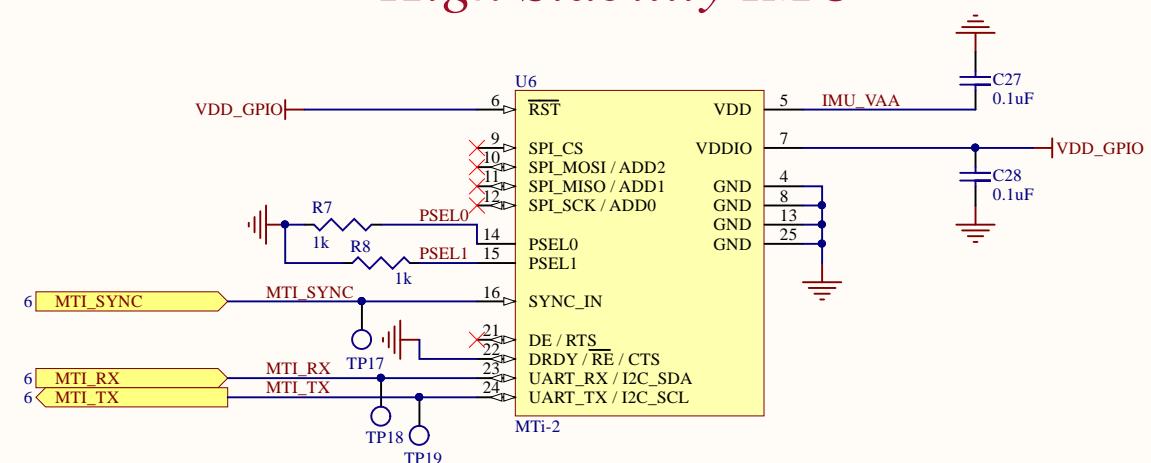
XSENS & ST IMUS

High Rate IMU



2.5V I/O voltage

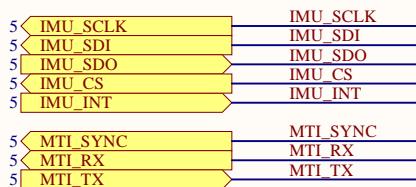
High Stability IMU



CLOCKS (CPU & PCI)

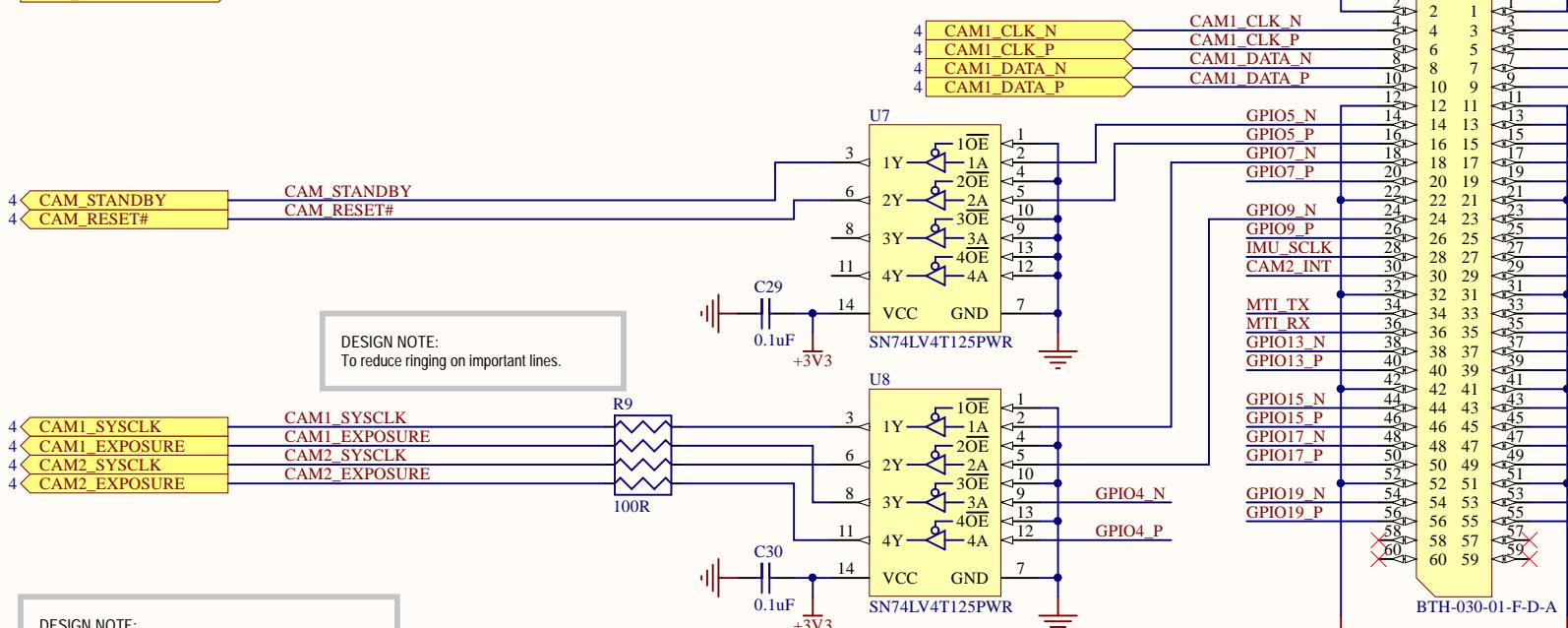
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Title:	Stereo Camera for Parallella
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IMU signals are 2.5V

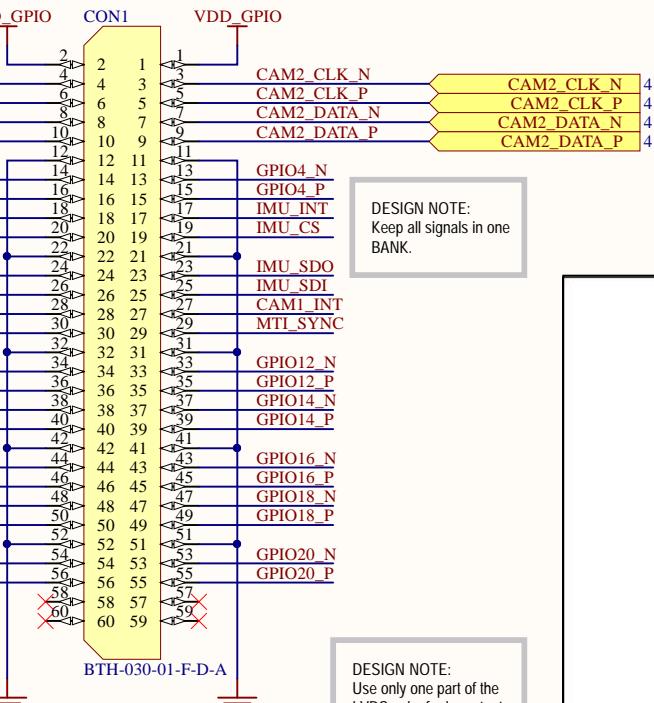


Connectors 1

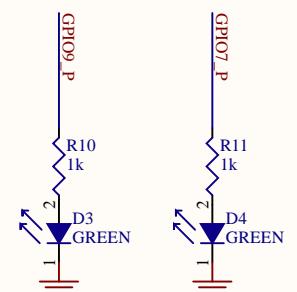
GPIO



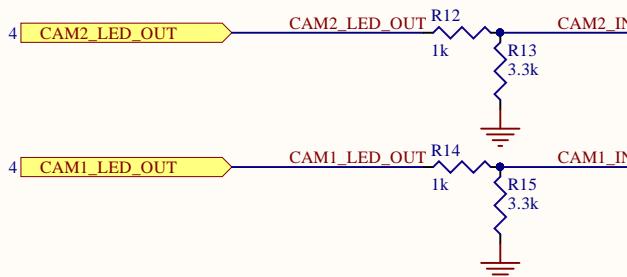
VDD_GPIO | CON1 | VDD_GPIO

DESIGN NOTE:
Keep all signals in one
BANK.

Camera ID LEDs

CAM_STANDBY
CAM_RESET#CAM_STANDBY
CAM_RESET#CAM_STANDBY
CAM_RESET#CAM_STANDBY
CAM_RESET#CAM1_SYSCLK
CAM1_EXPOSURE
CAM2_SYSCLK
CAM2_EXPOSURECAM1_EXPOSURE
CAM2_EXPOSURECAM1_SYSCLK
CAM2_SYSCLKCAM2_EXPOSURE
CAM1_EXPOSURE

3.3V Domain (CAM)



CAM2_LED_OUT

CAM1_LED_OUT

CAM2_LED_OUT

CAM1_LED_OUT

CAM2_INT

CAM1_INT

CAM2_INT

CAM1_INT

CFG_SCLK

CFG_SDA

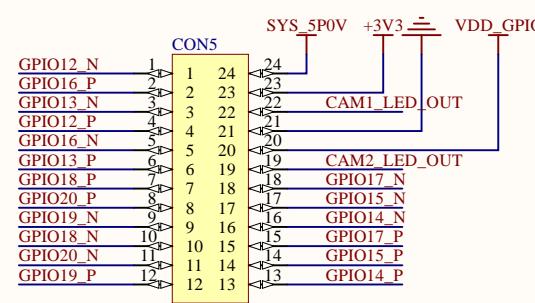
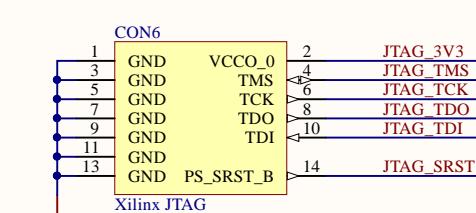
UART_RX

UART_TX

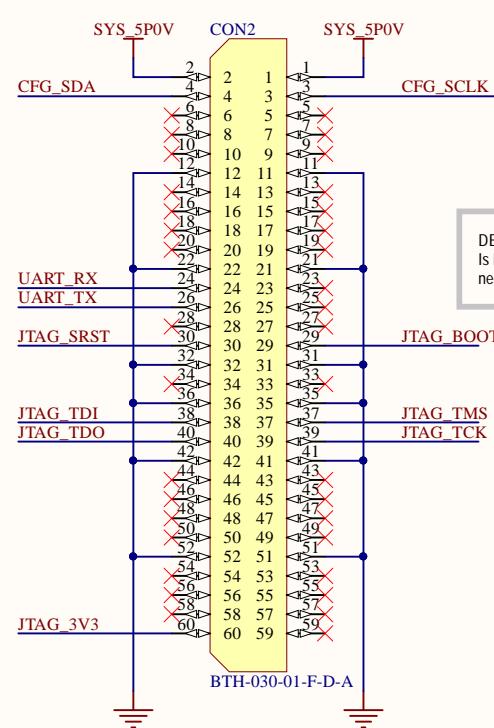
UART_RX

UART_TX

BANK13 Expansion

DESIGN NOTE:
The +3.3V rail has a total of 200 mA
left for external usage.

POWER

DESIGN NOTE:
Is BOOT EN really
needed?

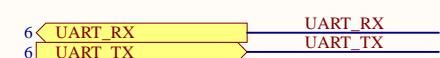
"Paracard" Daughtercard template for
Adapteva Parallel-I.
This schematic and associated PCB
design may be used as a starting point
for Parallel-I daughtercard design.

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94105, USA.

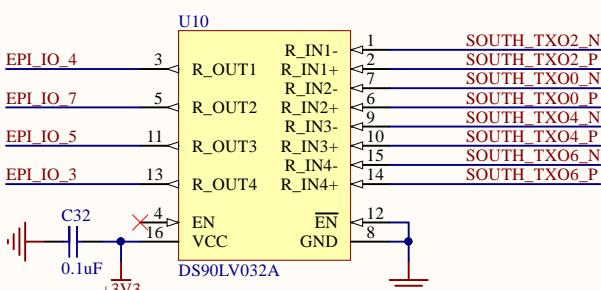
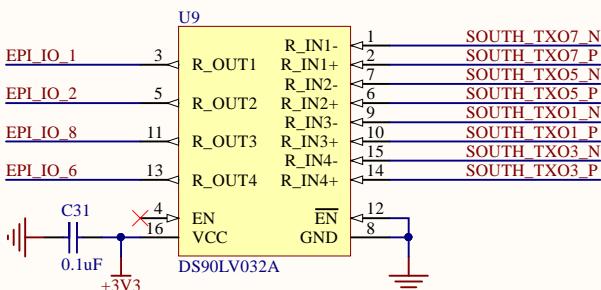
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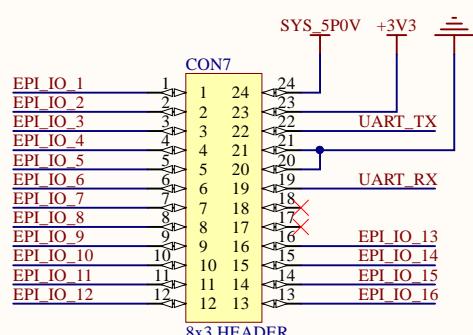
Connectors 2



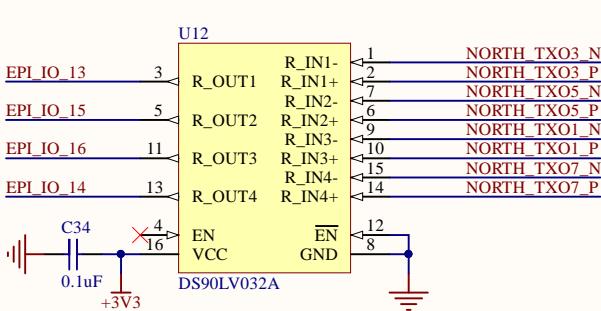
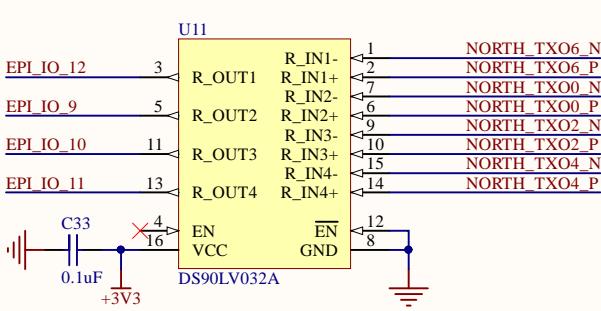
LAYOUT NOTE:
These are connected to LVDS lanes but
are not meant to be used at LVDS speed.
Assume the signal pairs to be "low"
speed signals.



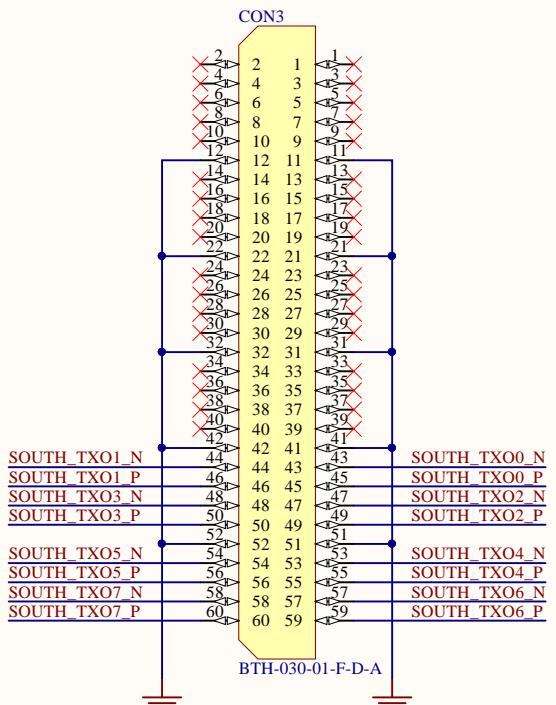
Epiphany Expansion



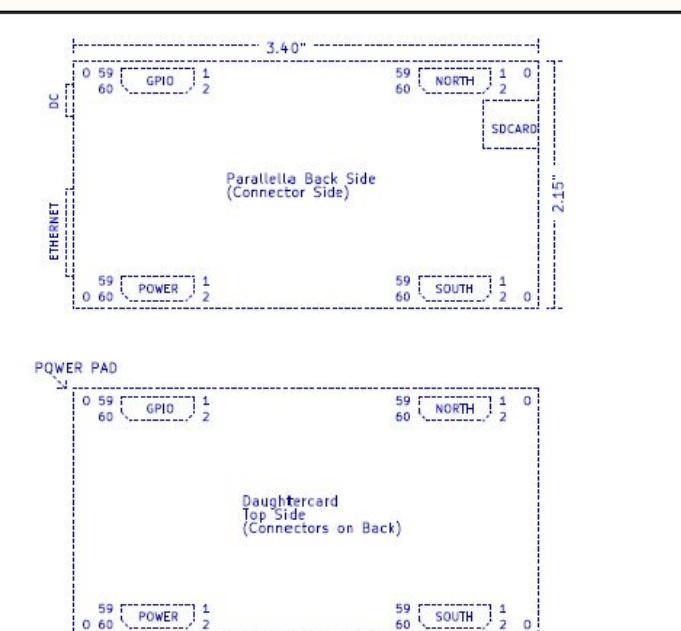
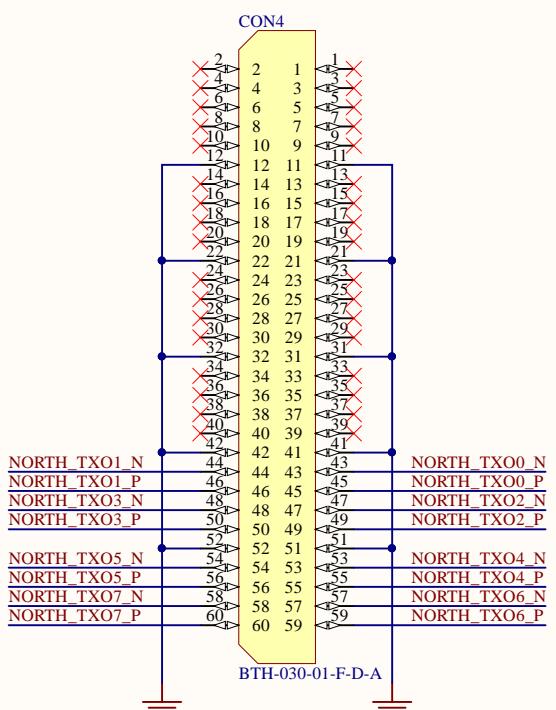
DESIGN NOTE:
The +3.3V rail has a total of 200 mA
left for external usage.



SOUTH



NORTH



"Paracard" Daughtercard template for
Adapteva Parallella-I.
This schematic and associated PCB
design may be used as a starting point
for Parallella-I daughtercard design.

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DOC: Revision History

A A

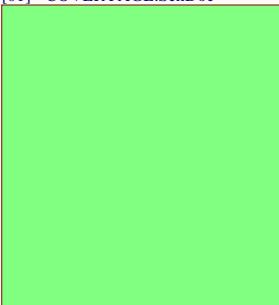
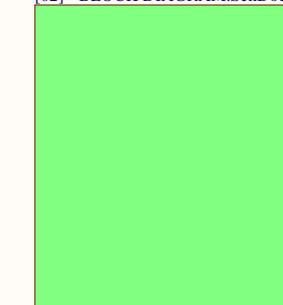
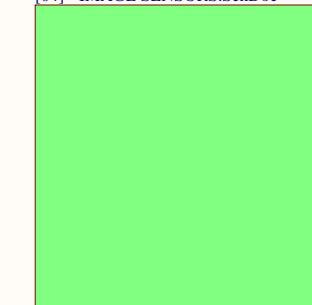
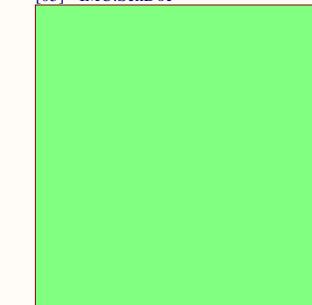
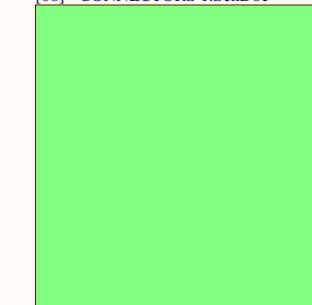
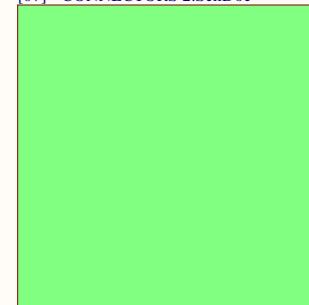
B B

C C

D D

CLOCKS (CPU & PCIE)

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Designator
[01] - COVER PAGE.SchDocDesignator
[02] - BLOCK DIAGRAM.SchDocDesignator
[03] - POWER.SchDocDesignator
[04] - IMAGE SENSORS.SchDocDesignator
[05] - IMU.SchDocDesignator
[06] - CONNECTORS 1.SchDocDesignator
[07] - CONNECTORS 2.SchDoc

TEMPLATE NOTES

Set Project Parameters

- 1) Go to Project -> Project Options -> Parameters
- 2) Set Company, Project and Version Revision

Mark Not Fitted Components as
NF

Net Class Example



Differential signal example



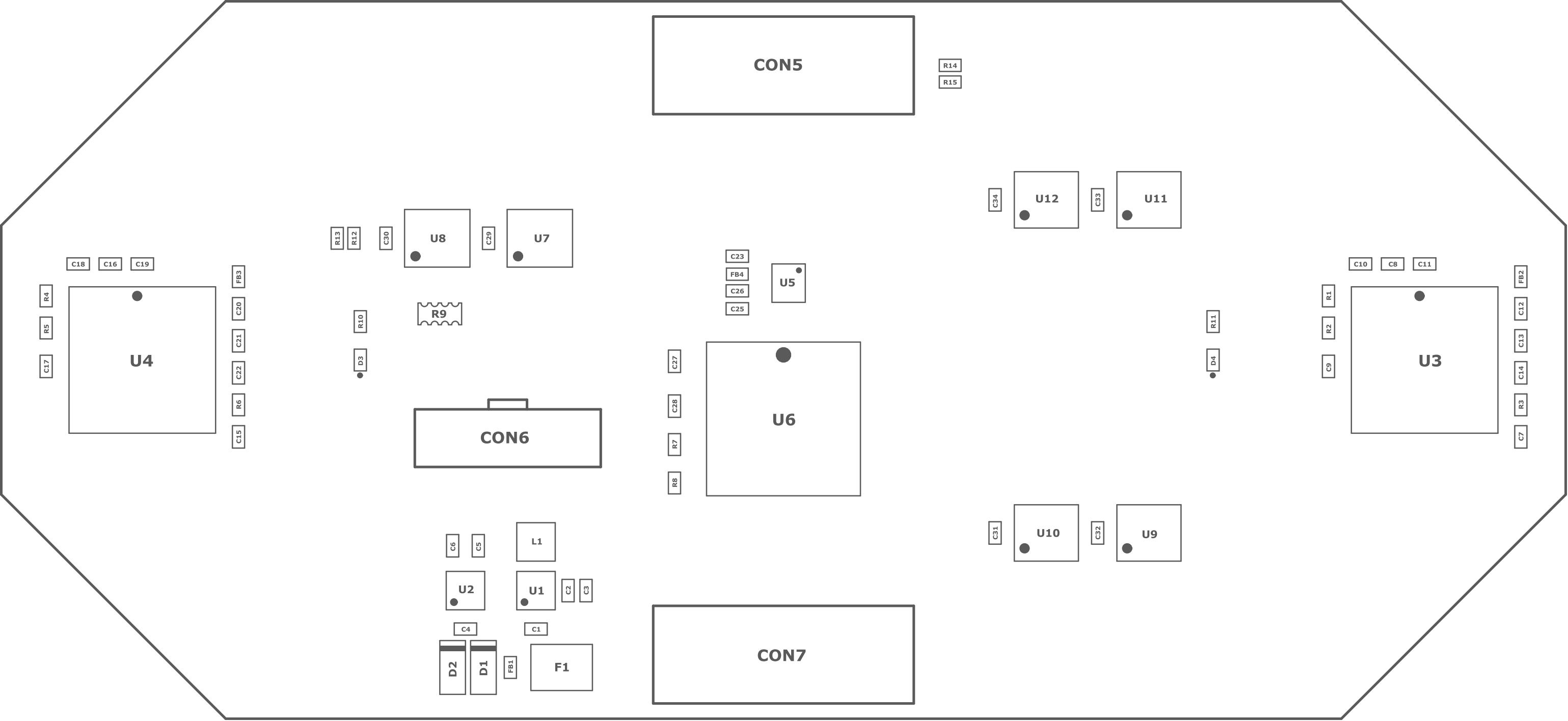
TITLE Examples (You can change the color to reflect your company color)

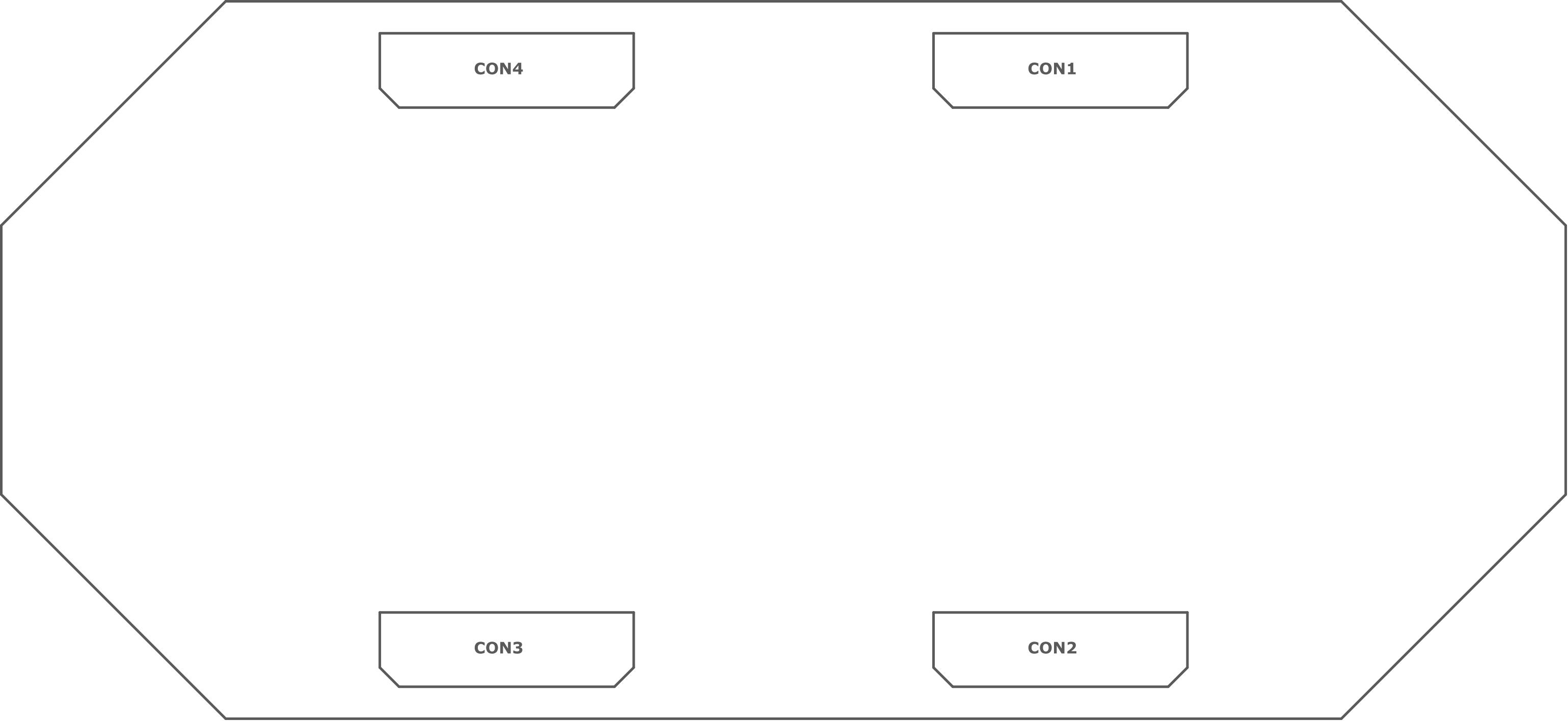
PAGE TITLE*Peripheral / Group of component title**Smaller Title*

Schematic Status Explanation

DRAFT - Very early stage of schematic, ignore details.**PRELIMINARY** - Close to final schematic.**CHECKED** - There should not be any mistakes. Tell the engineer if you find one.**RELEASED** - A board with this schematic has been sent to production.

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CON4

CON1

CON3

CON2

