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DEPARTMENT OF ELECTRONICS ENGINEERING
ELECTRONIC CIRCUITS
Cascade Amplifier Design

Numerical 1: Design a two stage RC coupled cascade amplifier for following specifications: $A_V \geq 1500$, $V_{ORMS} = 2$ V, $S \leq 8$, $f_L \geq 15$ Hz. Also, find out it's DC parameters, 1st stage and 2nd stage voltage gain, overall voltage gain in dB, input and output impedance.

Solution: **Step 1:** Selection of transistor and circuit

Transistor BC 147 A

$$h_{fe(typ)} = 220, h_{ie} = 2.7 \text{ k}\Omega, h_{FE(typ)} = 180, V_{CE(sat)} = 0.25 \text{ V}$$

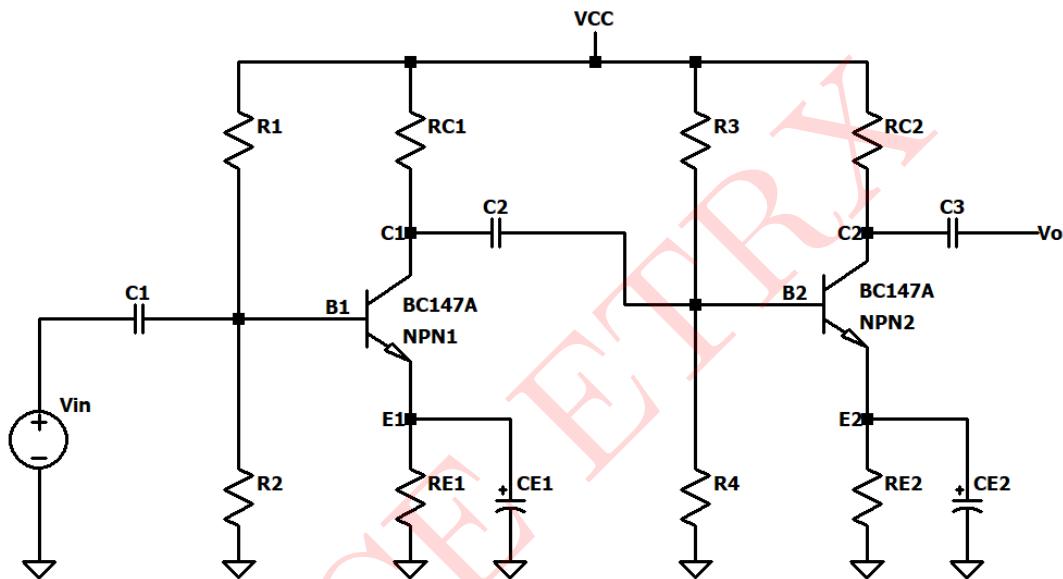


Figure 1: Circuit 1

Selecting voltage divider biasing because it provides stability of Q point against variations in β or temperature.

Step 2: Selection of voltage gain

$$A_{VT} = A_{V_1} A_{V_2} = 1500$$

$$\text{Let, } A_V \simeq 0.5 A_{V_2}$$

$$A_{VT} = 0.5 A_{V_2}^2$$

$$0.5 A_{V_2}^2 = 1500$$

$$A_{V_2}^2 = 3000$$

$$A_{V_2} = \mathbf{54.77}$$

$$A_{V_1} = 0.5 A_{V_2}$$

$$A_{V_1} = 0.5 \times 54.77 = \mathbf{27.386}$$

Design of 2nd stage:

Step 3: Calculation for R_{C_2}

$$|A_{V_2}| = \frac{h_{fe(typ)}R_{C_2}}{h_{ie}}$$

$$54.77 = \frac{220 \times R_{C_2}}{2.7 \times 10^3}$$

$$R_{C_2} = 672.17 \Omega$$

$$R_{C_2} = \mathbf{680 \Omega, 1/4 W (H.S.V)}$$

Step 4: Selection of Q point (V_{CEQ_2} , I_{CQ_2})

$$V_{o\ peak} = V_{ORMS} \times \sqrt{2}$$

$$V_{o\ peak} = 2 \times \sqrt{2} = \mathbf{2.828 V}$$

$$V_{CEQ_2} \geq 1.5(V_{o\ peak} + V_{CE(sat)})$$

The value is multiplied by 1.5 to take care of saturation voltages, variations in resistors, variation in supply voltage and device parameters variation.

$$V_{CEQ_2} \geq 1.5(2.828+0.25)$$

$$V_{CEQ_2} \geq 4.617$$

$$V_{CEQ_2} = \mathbf{4.7 V}$$

$$I_{o\ peak} = \frac{V_{o\ peak}}{R_{C_2}}$$

$$I_{o\ peak} = \frac{2.828}{680} = \mathbf{4.158 mA}$$

$$I_{CQ_2} \geq I_{o\ peak}$$

$$I_{CQ_2} \geq 4.158 \text{ mA}$$

$$I_{CQ_2} = \mathbf{4.2 mA}$$

Step 5: Selection of DC power supply (V_{CC})

In order to achieve maximum symmetrical output swing, select Q point at the center of the load line,

$$\text{i.e } V_{CC} \geq 2V_{CEQ_2}$$

$$V_{CC} \geq 2 \times 4.7$$

$$V_{CC} \geq 9.4 \text{ V}$$

$$V_{CC} = \mathbf{10 V (H.S.V)}$$

Step 6: Calculation of R_{E_2}

Voltage across E_2 should be 10% of V_{CC} or 1 V

$$V_{RE_2} = 10\% \text{ of } V_{CC}$$

$$V_{RE_2} = 0.1 \times V_{CC}$$

$$V_{RE_2} = 0.1 \times 10 = 1 \text{ V}$$

$$V_{RE_2} = I_{EQ_2} R_{E_2}$$

$$R_{E_2} = \frac{V_{RE_2}}{I_{EQ_2}}$$

$$R_{E_2} = \frac{V_{RE_2}}{I_{CQ_2}}$$

$$R_{E_2} = \frac{1}{4.2 \times 10^3} = 238.09 \Omega$$

$$R_{E_2} = 220 \Omega, 1/4 \text{ W (L.S.V)}$$

Step 7: Calculation of biasing resistors (R_3 and R_4)

$$S = \frac{1 + \beta}{1 + \beta \left(\frac{R_{E_2}}{R_{E_2} + R_{B_2}} \right)}$$

$$\beta = h_{FE(\text{typ})} = 180$$

$$S = \frac{1 + 180}{1 + 180 \left(\frac{220}{220 + R_{B_2}} \right)} = 1.611 \text{ k}\Omega$$

Applying KVL at B_2-E_2 loop,

$$V_{B_2} - I_{B_2} R_{B_2} - V_{BE_2} - I_{E_2} R_{E_2} = 0$$

$$V_{B_2} = R_{B_2} \frac{I_{C_2}}{\beta} + V_{BE_2} + I_{E_2} R_{E_2}$$

$$V_{B_2} = 1.737 \text{ V}$$

$$R_{B_2} = \frac{R_3 \times R_4}{R_3 + R_4} \quad \dots(1)$$

$$V_{B_2} = \frac{V_{CC} \times R_4}{R_3 + R_4} \quad \dots(2)$$

$$R_B = R_3 \times \frac{V_{B_2}}{V_{CC}} \quad \dots(\text{from 1 \& 2})$$

$$1.611 \times 10^3 = R_3 \times \frac{1.737}{10}$$

$$R_3 = 9.27 \text{ k}\Omega$$

$$R_3 = 10 \text{ k}\Omega, 1/4 \text{ W (H.S.V)}$$

$$1.611 \times 10^3 = \frac{10 \times 10^3 \times R_4}{10 \times 10^3 + R_4} \quad \dots(\text{from 1})$$

$$R_4 = 1.92 \text{ k}\Omega$$

$$R_4 = 1.8 \text{ k}\Omega, 1/4 \text{ W (L.S.V)}$$

Design of 1st stage:

step 8: Calculation for R_{C_1}

$$|A_{V_2}| = \frac{h_{fe(typ)} \times R_{C_2}}{h_{ie}}$$

$$|A_{V_2}| = \frac{220 \times 680}{2.7 \times 10^3} = \mathbf{52.96}$$

$$A_{V_1} = \frac{A_{VT}}{A_2}$$

$$A_{V_1} = \frac{1500}{52.96} = \mathbf{28.32}$$

$$|A_{V_1}| = \frac{h_{fe(typ)} \times R_{L_1}}{h_{ie}} \quad \dots(3)$$

$$\text{Where, } R_{L_1} = R_{C_1} \parallel R_3 \parallel R_4 \parallel h_{ie}$$

$$R_{L_1} = R_{C_1} \parallel (974.73)$$

Substituting in 3,

$$28.32 = \frac{h_{fe(typ)} \times R_{C_1} \times 974.73}{h_{ie} \times (R_{C_1} + 974.73)}$$

$$28.32 = \frac{220}{2.7 \times 10^3} \times \frac{R_{C_1} \times 974.73}{R_{C_1} + 974.73}$$

$$R_{C_1} = 540.176 \Omega$$

$$R_{C_1} = \mathbf{560} \Omega, 1/4 \text{ W (H.S.V)}$$

Step 9: Calculation for R_{E_1}

$$\text{Assuming, } V_{CEQ_1} = V_{CEQ_2} = 4.7 \text{ V}$$

$$V_{RE_1} = V_{RE_2} = 1 \text{ V}$$

$$V_{RC_1} = V_{RC_2}$$

$$\text{i.e } I_{CQ_1} R_{C_1} = I_{CQ_2} R_{C_2}$$

$$I_{CQ_1} = \frac{I_{CQ_2} R_{C_2}}{R_{C_1}}$$

$$I_{CQ_1} = \frac{4.2 \times 10^{-3} \times 680}{560} = \mathbf{5.1 \text{ mA}}$$

$$V_{RE_1} = I_{EQ_1} R_{E_1}$$

$$R_{E_1} = \frac{V_{RE_1}}{I_{EQ_1}} = \frac{V_{RE_1}}{I_{CQ_1}} = \frac{1}{5.1 \times 10^{-3}} = \mathbf{196.078 \Omega}$$

$$R_{E_1} = \mathbf{180 \Omega, 1/4 \text{ W (H.S.V)}}$$

Step 10: Calculation of biasing resistors (R_1 & R_2)

$$S = \frac{1 + \beta}{1 + \beta \left(\frac{R_{E_1}}{R_{E_1} + R_{B_1}} \right)}$$

where, $\beta = h_{FE}(typ) = 180$

$$8 = \frac{1 + 180}{1 + 180 \left(\frac{180}{180 + R_{B_1}} \right)}$$

$$R_{B_1} = 1.38 \text{ k}\Omega$$

Applying KVL at the B_1-E_1 loop,

$$V_{B_1} - I_{BQ_1}R_{B_1} - V_{BE_1} - I_{E_1}R_{E_1} = 0$$

$$V_{B_1} = R_{B_1} \frac{I_{CQ_1}}{\beta} + V_{BE_1} + I_{E_1}R_{E_1}$$

$$V_{B_1} = 1.737 \text{ V}$$

$$V_{B_1} = \frac{R_2}{R_1 + R_2} V_{CC}$$

$$\frac{R_2}{R_1 + R_2} = \frac{V_{B_1}}{V_{CC}}$$

$$R_{B_1} = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_{B_1} = R_1 \frac{V_{B_1}}{V_{CC}}$$

$$1.318 \times 10^3 = R_1 \times \frac{1.737}{10}$$

$$R_1 = 7.58 \text{ k}\Omega$$

$$R_1 = 8.2 \text{ k}\Omega, 1/4 \text{ W (H.S.V)}$$

$$\frac{1.737}{10} = \frac{R_2}{8.2 \times 10^3 + R_2}$$

$$R_2 = 1.723 \text{ k}\Omega$$

$$R_2 = 1.6 \text{ k}\Omega, 1/4 \text{ W (L.S.V)}$$

..(4)

...(from 4)

Step 11: Calculation of coupling capacitors C_1 , C_2 , C_3

$$a) C_1 = \frac{1}{2\pi R_{eq} f_L}$$

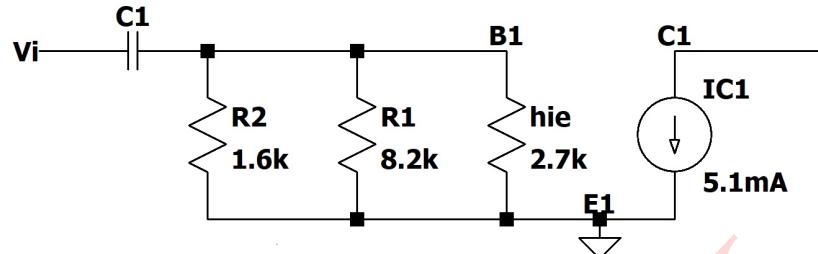


Figure 2: Low Frequency Equivalent Circuit for capacitor C_1

$$R_{eq} = R_1 \parallel R_2 \parallel h_{ie}$$

$$R_{eq} = 8.2 \times 10^3 \parallel 1.6 \times 10^3 \parallel 2.7 \times 10^3 = 894.99 \Omega$$

$$C_1 = \frac{1}{2\pi \times 894.99 \times 15}$$

$$C_1 = 11.85 \mu F$$

$$C_1 = 15 \mu F, 25 V$$

$$b) C_2 = \frac{1}{2\pi R_{eq} f_L}$$

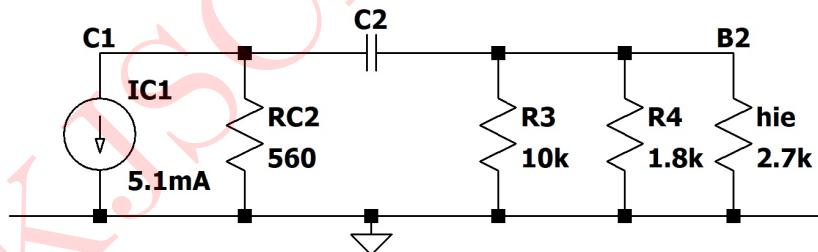


Figure 3: Low Frequency Equivalent Circuit for capacitor C_2

$$R_{eq} = R_{C_1} + (R_3 \parallel R_4 \parallel h_{ie})$$

$$R_{eq} = 560 + (10 \times 10^3 \parallel 1.8 \times 10^3 \parallel 2.7 \times 10^3) = 1.53 k\Omega$$

$$C_2 = \frac{1}{2\pi \times 1.53 \times 10^3 \times 15}$$

$$C_2 = 6.93 \mu F$$

$$C_2 = 10 \mu F, 25 V \text{ (H.S.V)}$$

$$c) C_3 = \frac{1}{2\pi R_{eq} f_L}$$

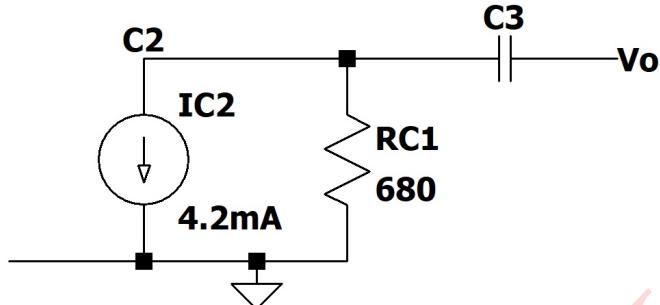


Figure 4: Low Frequency Equivalent Circuit for capacitor C_3 .

$$R_{eq} = R_{C_2} = 680 \Omega$$

$$C_3 = \frac{1}{2\pi \times 680 \times 15}$$

$$C_3 = 156 \mu F$$

$$C_3 = 22 \mu F, 25 V \text{ (H.S.V)}$$

Step 12: Calculation of bypass capacitors C_{E_1}, C_{E_2}

a) To ensure complete bypass of R_E

$$X_{CE_1} < R_{E_1}$$

$$X_{CE_1} = \frac{R_{E_1}}{10} = 0.1R_{E_1}$$

$$C_{E_1} = \frac{1}{2\pi f_L X_{CE_1}}$$

$$C_{E_1} = \frac{1}{2\pi f_L 0.1 \times R_{E_1}}$$

$$C_{E_1} = \frac{1}{2\pi \times 15 \times 0.1 \times 180}$$

$$C_{E_1} = 589.46 \mu F$$

$$C_{E_1} = 680 \mu F, 25 V \text{ (H.S.V)}$$

$$b) X_{CE_2} = \frac{R_{E_2}}{10} = 0.1R_{E_2}$$

$$C_{E_2} = \frac{1}{2\pi f_L 0.1 \times X_{CE_2}}$$

$$C_{E_2} = \frac{1}{2\pi \times 15 \times 0.1 \times 220}$$

$$C_{E_2} = 482.28 \mu F$$

$$C_{E_2} = 560 \mu F, 25 V \text{ (H.S.V)}$$

Step 13: Complete designed circuit

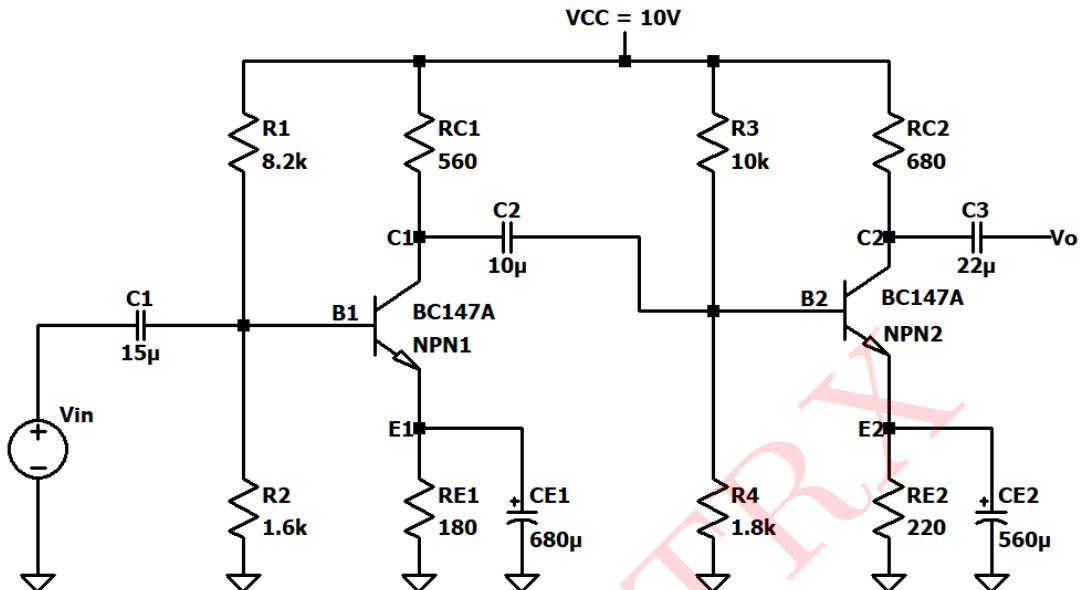


Figure 5: Designed Circuit

DC Analysis:

For DC biasing, the capacitors acts as an open source.

1st stage:

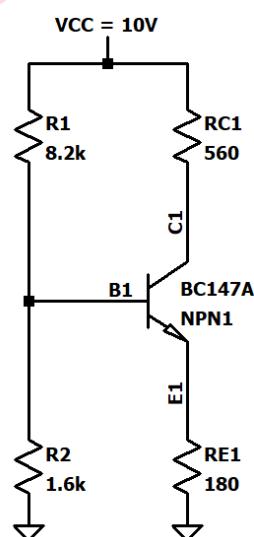


Figure 6: DC Equivalent circuit

$$V_{B_1} = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

$$V_{B_1} = \frac{10 \times 1.6 \times 10^3}{8.2 \times 10^3 + 1.6 \times 10^3} = 1.63 \text{ V}$$

$$R_{B_1} = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_{B_1} = \frac{8.2 \times 10^3 \times 1.6 \times 10^3}{8.2 \times 10^3 + 1.6 \times 10^3} = 1.34 \text{ k}\Omega$$

Thevenin's Equivalent Circuit:

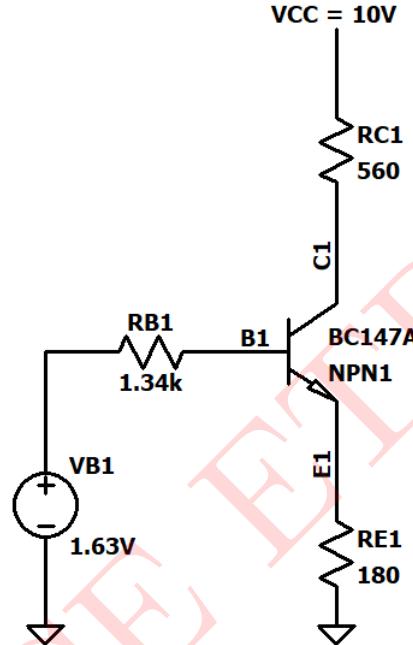


Figure 7: Thevenin's Equivalent circuit

Applying KVL to the B_{E_1} - E_{E_1} loop,

$$V_{B_1} - R_{B_1}I_{B_1} - V_{BE_1} - I_{E_1}R_{E_1} = 0$$

$$R_{B_1}I_{B_1} + (1 + \beta)I_{B_1}R_{E_1} = V_{B_1} - V_{BE_1}$$

$$I_{B_1} = \frac{V_{B_1} - V_{BE_1}}{R_{B_1} + (1 + \beta)} R_{E_1}$$

$$I_{B_1} = \frac{1.63 - 0.7}{1.34 \times 10^3 + (1 + 180) \times 180} = 27.41 \mu\text{A}$$

$$I_{C_1} = \beta I_{B_1}$$

$$I_{C_1} = 180 \times 27.41 \times 10^{-6} = 4.93 \text{ mA}$$

$$I_{E_1} = (1 + \beta)I_{B_1}$$

$$I_{E_1} = (1 + 180) \times 27.41 \times 10^{-6} = 4.96 \text{ mA}$$

V_{C_1} and V_{E_1} is given as:

$$V_{C_1} = V_{CC} - I_{C_1}R_{C_1}$$

$$V_{C_1} = 10 - 4.93 \times 10^{-3} \times 560 = 7.2392 \text{ V}$$

$$V_{E_1} = I_{E_1} R_{E_1}$$

$$V_{E_1} = 4.96 \times 10^{-3} \times 180 = \mathbf{0.8928 \text{ V}}$$

2nd stage:

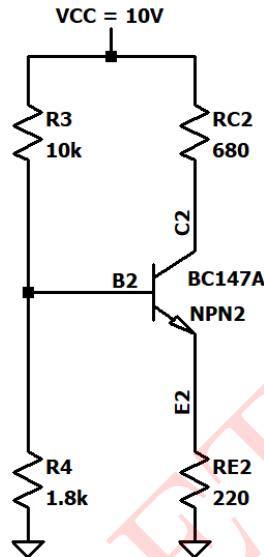


Figure 8: DC Equivalent circuit

$$V_{B_2} = \frac{V_{CC} \times R_4}{R_3 + R_4}$$

$$V_{B_2} = \frac{10 \times 1.8 \times 10^3}{10 \times 10^3 + 1.8 \times 10^3} = \mathbf{1.52 \text{ V}}$$

$$R_{B_2} = \frac{R_3 \times R_4}{R_3 + R_4}$$

$$R_{B_2} = \frac{10 \times 10^3 \times 1.8 \times 10^3}{10 \times 10^3 + 1.8 \times 10^3} = \mathbf{1.52 \text{ k}\Omega}$$

Thevenin's Equivalent Circuit:

Applying KVL to the B_{E_2} - E_{E_2} loop,

$$V_{B_2} - R_{B_2} I_{B_2} - V_{BE_2} - I_{E_2} R_{E_2} = 0$$

$$R_{B_2} I_{B_2} + (1 + \beta) I_{B_2} R_{E_2} = V_{B_2} - V_{BE_2}$$

$$I_{B_2} = \frac{V_{B_2} - V_{BE_2}}{R_{B_2} + (1 + \beta)} R_{E_2}$$

$$I_{B_2} = \frac{1.52 - 0.7}{1.52 \times 10^3 + (1 + 180) \times 220} = \mathbf{19.83 \mu\text{A}}$$

$$I_{C_2} = \beta I_{B_2}$$

$$I_{C_2} = 180 \times 19.83 \times 10^{-6} = \mathbf{3.56 \text{ mA}}$$

$$I_{E_2} = (1 + \beta) I_{B_2}$$

$$I_{E_2} = (1 + 100) \times 19.83 \times 10^{-6} = \mathbf{3.58 \text{ mA}}$$

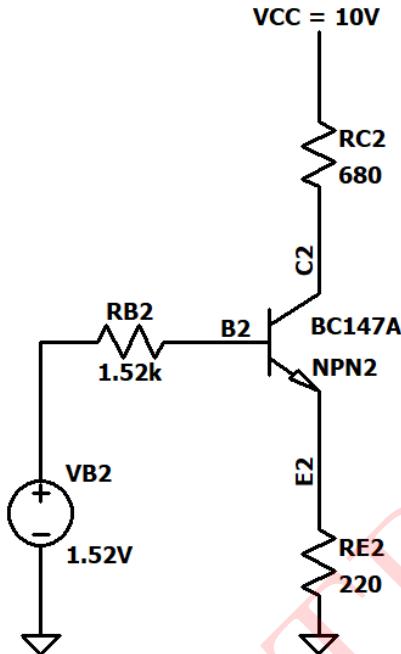


Figure 9: Thevenin's Equivalent circuit

V_{C_2} and V_{E_2} is given as:

$$V_{C_2} = V_{CC} - I_{C_2} R_{C_2}$$

$$V_{C_2} = 10 - 3.56 \times 10^{-3} \times 680 = 7.57 \text{ V}$$

$$V_{E_2} = I_{E_2} R_{E_2}$$

$$V_{E_2} = 3.58 \times 10^{-3} \times 220 = 0.7876 \text{ V}$$

AC Analysis:

Small signal parameters:

$$r_{\pi_1} = \frac{\beta V_T}{I_{E_1}}$$

$$r_{\pi_1} = \frac{180 \times 26 \times 10^{-3}}{4.96 \times 10^{-3}} = 943.55 \Omega$$

$$r_{\pi_2} = \frac{\beta V_T}{I_{E_2}}$$

$$r_{\pi_2} = \frac{180 \times 26 \times 10^{-3}}{3.58 \times 10^{-3}} = 1.3407 \text{ k}\Omega$$

$$g_{m1} = \frac{I_{C_1}}{V_T}$$

$$g_{m1} = \frac{4.93 \times 10^{-3}}{26 \times 10^{-3}} = 189.61 \text{ mA/V}$$

$$g_{m2} = \frac{I_{C_2}}{V_T}$$

$$g_{m2} = \frac{3.56 \times 10^{-3}}{26 \times 10^{-3}} = \mathbf{136.92 \text{ mA/V}}$$

Small Signal Equivalent Circuit is shown in figure 10:

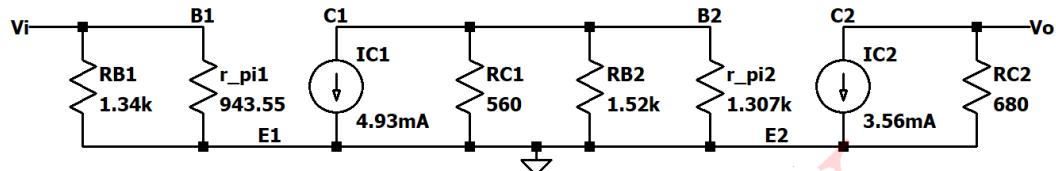


Figure 10: Small Signal Equivalent Circuit

Stage 2 Voltage gain:

$$A_{V_2} = \frac{-g_m V_{\pi_2} (R_{C_2})}{V_{\pi_2}}$$

$$A_{V_2} = -g_m R_{C_2}$$

$$A_{V_2} = -136.92 \times 10^{-3} \times 680 = \mathbf{-93.1056}$$

Stage 1 voltage gain:

$$A_{V_1} = \frac{-g_m V_{\pi_1} (R_{C_1} \parallel R_{B_2} \parallel r_{\pi_2})}{V_{\pi_1}}$$

$$A_{V_1} = -g_m (R_{C_1} \parallel R_{B_2} \parallel r_{\pi_2})$$

$$A_{V_1} = -189.61 \times 10^{-3} (560 \parallel 1.34 \times 10^3 \parallel 1.307 \times 10^3) = \mathbf{-57.5082}$$

Overall voltage gain:

$$A_{VT} = A_{V_1} \times A_{V_2}$$

$$A_{VT} = (-57.5082) \times (-93.1056) = \mathbf{535.433}$$

$$A_{VT} \text{ in dB} = 20 \log_{10}(|A_{VT}|)$$

$$A_{VT} \text{ in dB} = 20 \log_{10}(535.433) = \mathbf{74.57 \text{ dB}}$$

Input impedance of stage 1:

$$Z_i = (R_{B_1} \parallel r_{\pi_1})$$

$$Z_i = (1.34 \times 10^3 \parallel 943.55) = \mathbf{553.68 \Omega}$$

Output impedance of stage 2:

$$Z_o = R_{C_2} = \mathbf{680 \Omega}$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

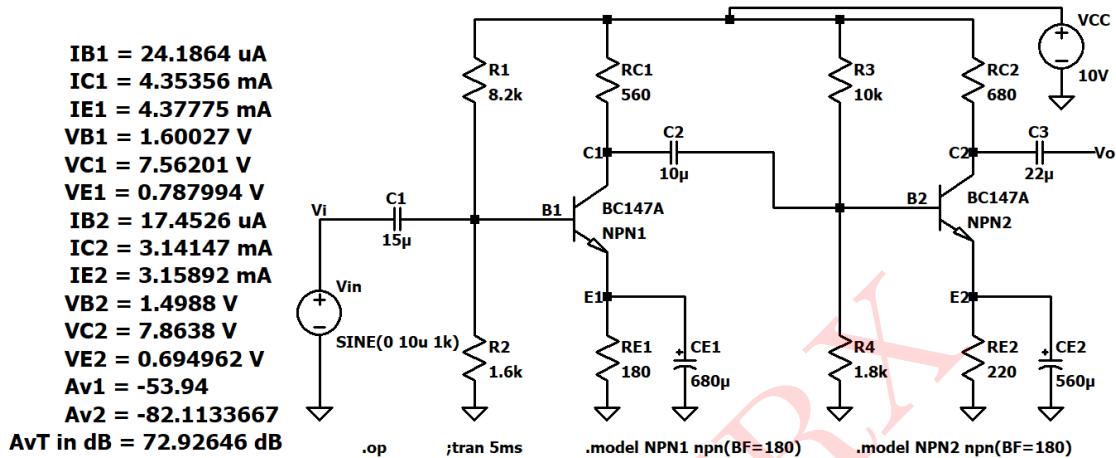


Figure 11: Circuit Schematic 1: Results

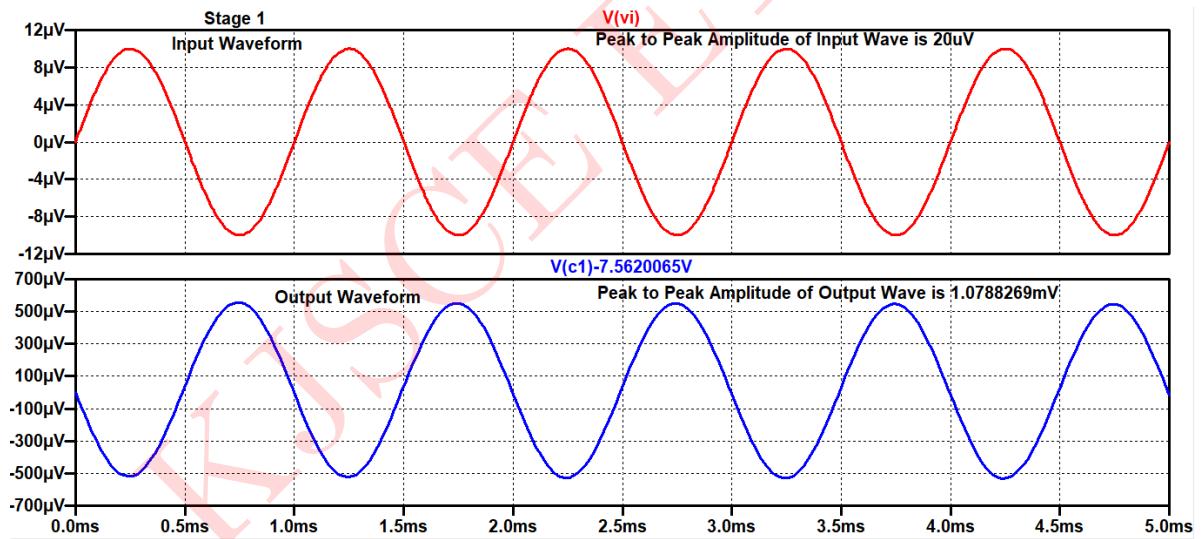


Figure 12: Input & Output waveforms for stage 1 voltage gain

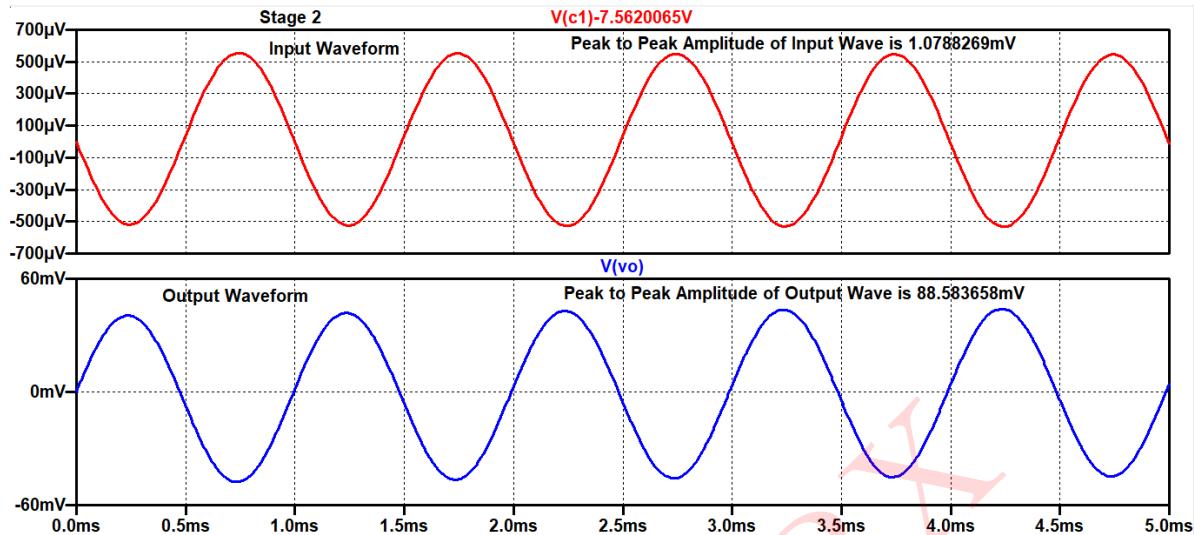


Figure 13: Input & Output waveforms for stage 2 voltage gain

Comparison of theoretical and simulated values:

Parameters	Theoretical Values	Simulated Values
I_{B_1}	$27.41 \mu\text{A}$	$24.1864 \mu\text{A}$
I_{C_1}	4.93 mA	4.3535 mA
I_{E_1}	4.96 mA	4.3777 mA
V_{B_1}	1.63 V	1.6002 V
V_{C_1}	7.2392 V	7.5620 V
V_{E_1}	0.8928 V	0.7879 V
I_{B_2}	19.83 mA	17.4526 mA
I_{C_2}	3.56 mA	3.1414 mA
I_{E_2}	3.58 V	3.1589 mA
V_{B_2}	1.52 V	1.4988 V
V_{C_2}	7.57 V	7.8638 V
V_{E_2}	0.7876	0.6949 V
Voltage gain of stage 1: A_{V_1}	-57.5082	-53.94
Voltage gain of stage 2: A_{V_2}	-93.1056	-82.1133
Overall voltage gain: A_{VT} in dB	74.57 dB	72.9264 dB
Input impedance of stage 1	553.68Ω	—
Output impedance of stage 2	680Ω	—

Table 1: Numeical 1

Numerical 2: Design a two stage RC coupled cascade amplifier for following specifications: $A_V \geq 420$, $V_{CC} = 18$ V, $S \leq 10$, $R_i \geq 1 \text{ M}\Omega$. Calculate 1st stage and 2nd stage DC parameters, 1st stage and 2nd stage voltage gain, overall voltage gain in dB, input and output impedance.

Solution:

The above requirements can be fulfilled by a CS-SE stage.

Since, $R_i \geq 1 \text{ M}\Omega$, select CS as 1st stage.

Step 1: Selection of transistor and circuit

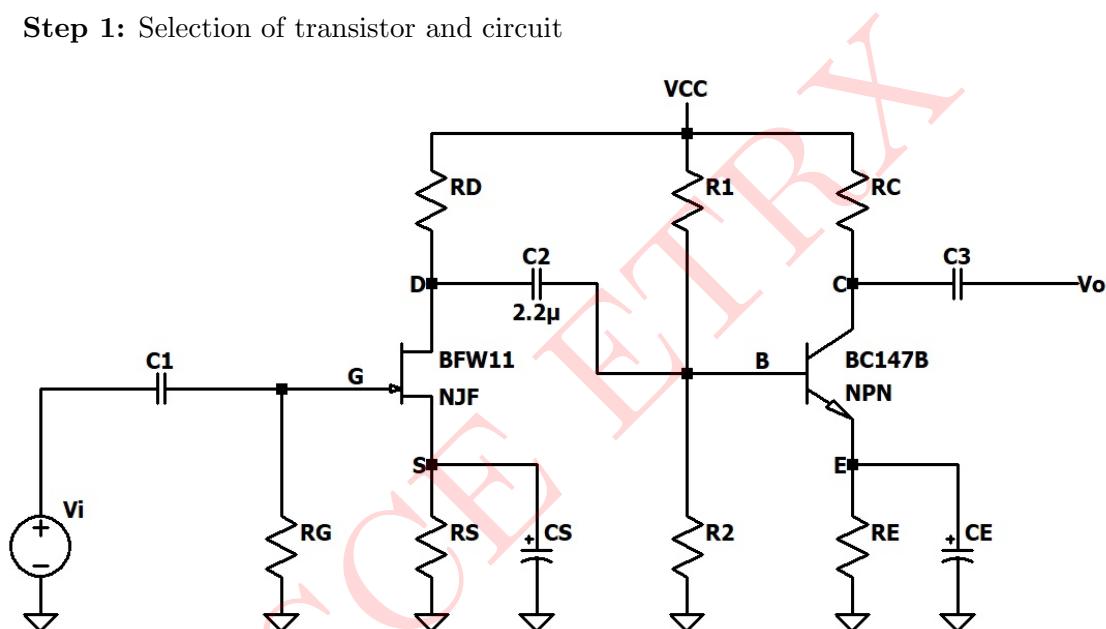


Figure 14: Circuit 2

Transistor BC147B:

$$h_{fe(typ)} = 330, h_{ie} = 4.5 \text{ k}\Omega, h_{FE(typ)} = 290 = \beta, V_{CE(sat)} = 0.25 \text{ V}$$

Transistor BC147B:

$$I_{DSS} = 7 \text{ mA}, g_{mo} = 5600 \mu\Omega, V_P = -2.5 \text{ V}, r_d = 50 \text{ k}\Omega$$

Step 2: Selection of gains

$$A_V \geq 420$$

$$\text{Let, } A_V = 4$$

...(\because JFET amplifier gain is less)

$$A_V = A_{V_1} A_{V_2}$$

$$A_{V_2} = \frac{A_V}{A_{V_1}}$$

$$A_{V_2} = \frac{420}{4} = 105$$

Design of 2nd stage:

Step 3: Selection of R_C

$$|A_{V_2}| = \frac{h_{fe(typ)}R_C}{h_{ie}}$$

$$105 = \frac{330 \times R_C}{4.5 \times 10^3}$$

$$R_{C_2} = 1.43 \text{ k}\Omega$$

$$R_{C_2} = 1.5 \text{ k}\Omega, 1/4 \text{ W (H.S.V)}$$

Step 4: Selection of Q point (V_{CEQ} , I_{CQ})

$$V_{CC} = 18 \text{ V}$$

...(given)

$$\text{Let, } V_{CEQ} = \frac{V_{CC}}{2}$$

$$V_{CEQ} = \frac{18}{2} = 9 \text{ V}$$

$$V_{RE} = 10\% \text{ of } V_{CC}$$

$$V_{RE} = 0.1 \times V_{CC}$$

$$V_{RE} = 0.1 \times 18 = 1.8 \text{ V}$$

Applying KVL at C-E loop of BJT,

$$V_{CC} - I_C R_C - V_{CEQ} - I_E R_E = 0$$

$$V_{CC} - V_{RC} - V_{CEQ} - V_{RE} = 0$$

$$V_{RC} = V_{CC} - V_{CEQ} - V_{RE}$$

$$V_{RC} = 18 - 9 - 1.8 = 7.2 \text{ V}$$

$$V_{RC} = I_{CQ} R_C$$

$$I_{CQ} = \frac{V_{RC}}{R_C}$$

$$I_{CQ} = \frac{7.2}{1.5 \times 10^3} = 4.8 \text{ mA}$$

Step 5: Selection of R_E

$$V_{RE} = 1.8 \text{ V}$$

$$I_{EQ} R_E = 1.8$$

$$R_E = \frac{1.8}{I_{EQ}}$$

$$R_E = \frac{1.8}{I_{CQ}}$$

$$R_E = \frac{1.8}{4.8 \times 10^{-3}} = 375 \Omega$$

$$R_E = 390 \Omega, 1/4 \text{ W (L.S.V)}$$

Step 6: Selection of biasing resistors (R_1 and R_2)

$$S \leq 10 \quad \dots(\text{given})$$

$$\beta = 290 \quad \dots(\text{given})$$

$$S = \frac{1 + \beta}{1 + \beta \left(\frac{R_E}{R_E + R_B} \right)}$$

$$10 = \frac{1 + 290}{1 + 290 \left(\frac{390}{390 + R_B} \right)}$$

$$R_B = \mathbf{3.63 \text{ k}\Omega}$$

Applying KVL at B-E loop of BJT,

$$V_B - I_B R_B - V_{BE} - I_E R_E = 0$$

$$V_B = R_B \frac{I_C}{\beta} + V_{BE} + V_{RE}$$

$$V_B = \frac{4.8 \times 10^{-3}}{290} \times 3.63 \times 10^3 + 0.7 + 1.8 = \mathbf{2.56 \text{ V}}$$

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

$$\frac{R_2}{R_1 + R_2} = \frac{V_B}{V_{CC}} \quad \dots(1)$$

$$R_B = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_B = R_1 \times \frac{V_B}{V_{CC}} \quad \dots(\text{from 1})$$

$$3.63 \times 10^3 = R_1 \times \frac{2.56}{18}$$

$$R_1 = 25.52 \text{ k}\Omega$$

$$R_1 = \mathbf{27 \text{ k}\Omega, 1/4 \text{ W (H.S.V)}}$$

$$\frac{R_2}{27 \times 10^3 + R_2} = \frac{2.56}{18} \quad \dots(\text{from 1})$$

$$R_2 = 4.47 \text{ k}\Omega$$

$$R_2 = \mathbf{4.2 \text{ k}\Omega, 1/4 \text{ W (L.S.V)}}$$

Design of 1st stage:

Step 7: Selection of Q point (I_{DQ} , V_{GSQ})

Using mid-point biasing,

$$I_{DQ} = \frac{I_{DSS}}{2}$$

$$I_{DQ} = \frac{7 \times 10^{-3}}{2}$$

$$I_{DQ} = 3.5 \text{ mA}$$

$$I_{DQ} = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$V_{GSQ} = V_P \left(1 - \sqrt{\frac{I_{DQ}}{I_{DSS}}}\right)$$

$$V_{GSQ} = -2.5 \left(1 - \sqrt{\frac{3.5 \times 10^{-3}}{7 \times 10^{-3}}}\right) = -0.732 \text{ V}$$

$$g_m = g_{mo} \left(1 - \frac{V_{GSQ}}{V_P}\right)$$

$$g_m = 5600 \times 10^{-6} \left(1 - \frac{(-0.732)}{(-2.5)}\right) = 3.96 \text{ mA/V}$$

Step 8: Selection of R_D :

$$|A_{V_2}| = \frac{h_{fe(typ)} \times R_C}{h_{ie}}$$

$$|A_{V_2}| = \frac{330 \times 1.5 \times 10^3}{4.5 \times 10^3} = 110$$

$$|A_{V_1}| = \frac{A_V}{|A_2|}$$

$$|A_{V_1}| = \frac{420}{110} = 3.81$$

Let, $|A_{V_1}| = 3.9$

$$|A_{V_1}| = g_m R_L$$

Where, $R_L = R_D \parallel r_d \parallel R_1 \parallel R_2 \parallel h_{ie}$

$$R_{R_L} = R_D \parallel 50 \times 10^3 \parallel 27 \times 10^3 \parallel 4.2 \times 10^3 \parallel 4.5 \times 10^3$$

$$R_L = \frac{R_D \times 1.93 \times 10^3}{R_D + 1.93 \times 10^3}$$

$$|A_{V_1}| = g_m \frac{R_D \times 1.93 \times 10^3}{R_D + 1.93 \times 10^3}$$

$$3.9 = 3.96 \times 10^{-3} \left(\frac{R_D \times 1.93 \times 10^3}{R_D + 1.93 \times 10^3}\right)$$

$$R_D = 2.01 \text{ k}\Omega$$

$$R_D = 2.2 \text{ k}\Omega, 1/4 \text{ W (H.S.V)}$$

Step 9: Selection of R_S

$$V_{GSQ} = -I_{DQ} \times R_S$$

$$R_S = \frac{V_{GSQ}}{I_{DQ}}$$

$$R_S = \frac{-0.732}{3.5 \times 10^{-3}} = 209.14 \Omega$$

$R_S = 180 \text{ k}\Omega, 1/4 \text{ W}$ (L.S.V)

Step 10: Selection of R_G

Let, $R_G = 2 \text{ M}\Omega, 1/4 \text{ W}$

(Since, $R_i = 1 \text{ M}\Omega$, to prevent loading take $R_G \geq 1 \text{ M}\Omega$)

Step 11: Selection of coupling capacitors C_1, C_2, C_3

a) C_1 :

$$C_1 = \frac{1}{2\pi R_G f_L}$$

Since, f_L is not given, consider audio frequency $f_L = 20 \text{ Hz}$

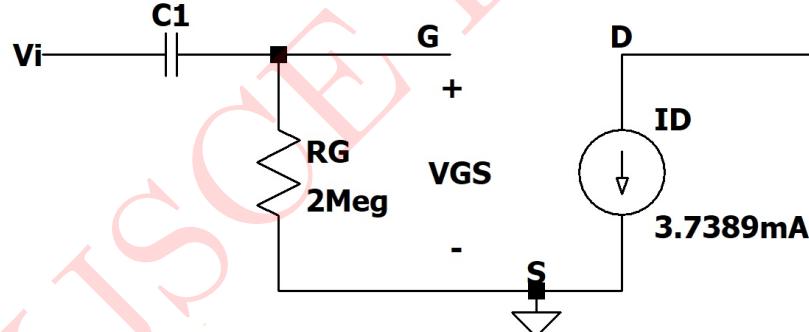


Figure 15: Low Frequency Equivalent Circuit for capacitor C_1

$$C_1 = \frac{1}{2\pi \times 2 \times 10^6 \times 20}$$

$$C_1 = 3.97 \text{ nF}$$

$C_1 = 4.7 \text{ nF}, 50 \text{ V}$ (H.S.V)

b) C_2 :

$$C_2 = \frac{1}{2\pi f_L R_{eq}}$$

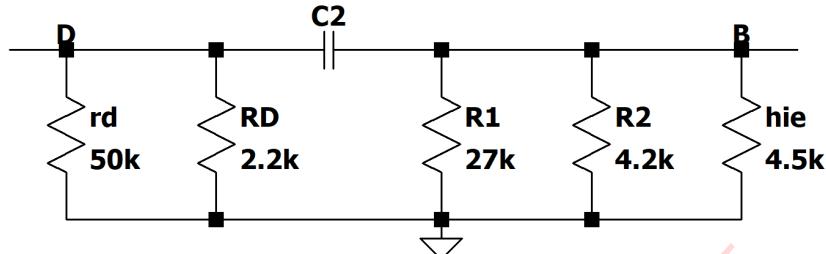


Figure 16: Low Frequency Equivalent Circuit for capacitor C_2

$$R_{eq} = (r_d \parallel R_D) + (R_1 \parallel R_2 \parallel h_{ie})$$

$$R_{eq} = (50 \times 10^3 \parallel 2.2 \times 10^3) + (27 \times 10^3 \parallel 4.2 \times 10^3 \parallel 4.5 \times 10^3) = 4.117 \text{ k}\Omega$$

$$C_2 = \frac{1}{2\pi \times 4.117 \times 10^3 \times 20}$$

$$C_2 = 1.93 \mu\text{F}$$

$$C_2 = \mathbf{2.2 \mu F, 50 V (H.S.V)}$$

c) C_3 :

$$C_3 = \frac{1}{2\pi R_{eq} f_L}$$

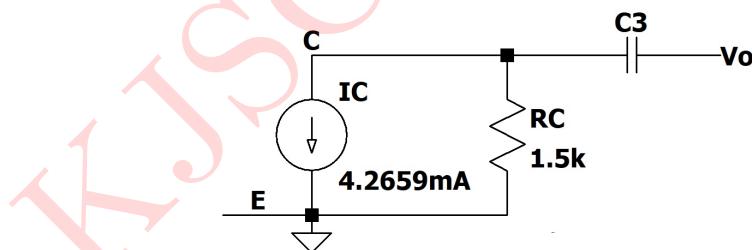


Figure 17: Low Frequency Equivalent Circuit for capacitor C_3

$$R_{eq} = R_C = 1.5 \text{ k}\Omega$$

$$C_3 = \frac{1}{2\pi \times 1.5 \times 10^3 \times 20}$$

$$C_3 = 5.3 \mu\text{F}$$

$$C_3 = \mathbf{5.6 \mu F, 50 V (H.S.V)}$$

Step 12: Selection of bypass capacitors C_S , C_E

a) C_S

$$C_S = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = \left(\frac{1}{g_m} \parallel R_S \right)$$

$$R_{eq} = \left(\frac{1}{3.96 \times 10^{-3}} \parallel 180 \right) = 105.09 \Omega$$

$$C_S = \frac{1}{2\pi \times 105.09 \times 20}$$

$$C_S = 75.72 \mu F$$

$$C_S = 82 \mu F, 50 V \text{ (H.S.V)}$$

b) C_E

$$C_E = \frac{1}{2\pi R_{eq} f_L}$$

$$R_{eq} = X_{CE} = 0.1 R_E$$

$$C_E = \frac{1}{2\pi \times 0.1 \times R_E \times R_L}$$

$$C_E = \frac{1}{2\pi \times 0.1 \times 390 \times 20}$$

$$C_E = 204.04 \mu F$$

$$C_E = 220 \mu F, 50 V \text{ (H.S.V)}$$

Step 13: Complete designed circuit

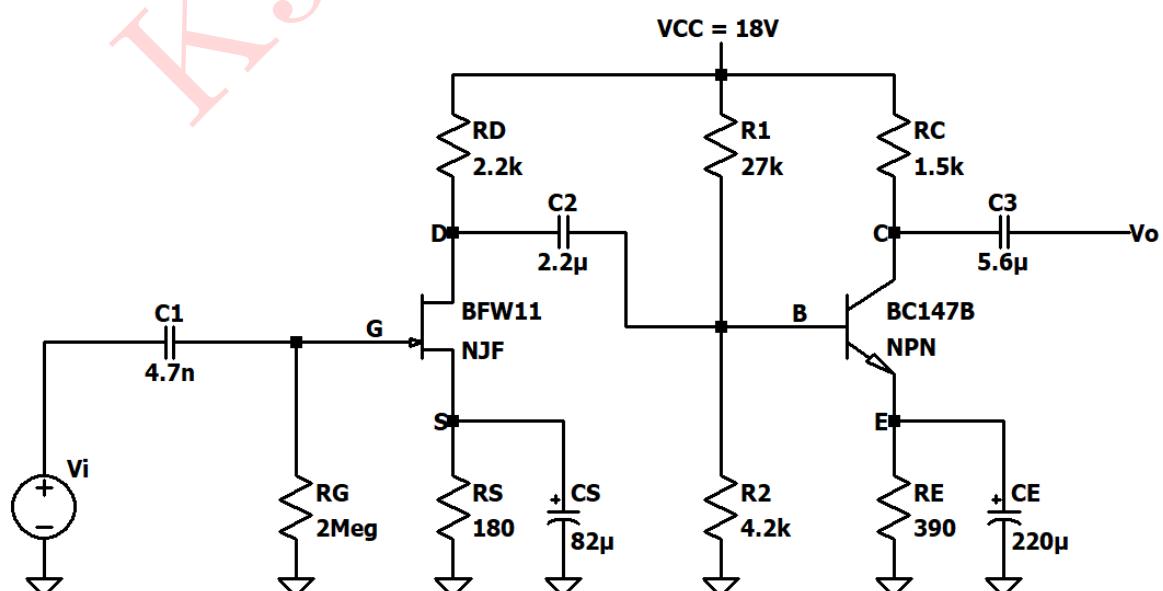


Figure 18: Designed Circuit

DC Analysis:

For DC biasing, the capacitors acts as an open source.

1st stage:

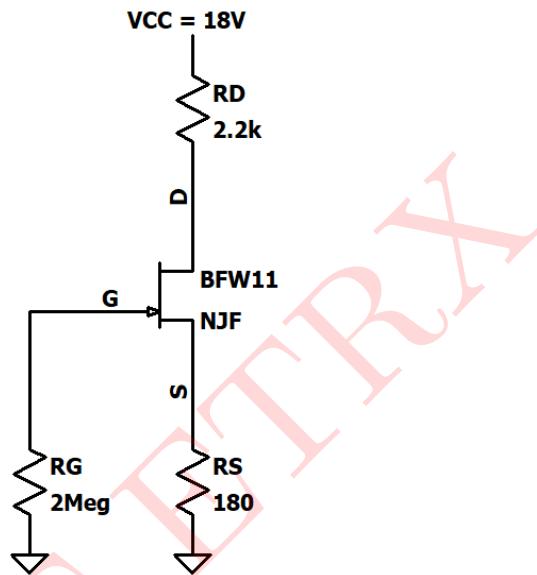


Figure 19: DC Equivalent circuit

Applying KVL to the G-S loop,

$$-I_G R_G - V_{GS} - I_D R_S = 0$$

$$V_{GSQ} = -I_D R_S \quad \dots (\because I_G = 0)$$

$$V_{GSQ} = -I_D 180$$

$$I_D = -\frac{V_{GS}}{180} \quad \dots (1)$$

From current equation,

$$I_D = I_{DS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

$$\frac{-V_{GS}}{180} = 7 \times 10^{-3} \left(1 - \frac{V_{GS}}{-2.5} \right)^2$$

$$-V_{GS} = 1.26 \left(1 + \frac{V_{GS}}{2.5} \right)^2$$

$$-V_{GS} = \frac{1.26}{6.25} (2.5 + V_{GS})^2$$

$$-V_{GS} = 2.2016 (6.25 + 5V_{GS} + V_{GS}^2)$$

$$-V_{GS} = 1.26 + 1.008V_{GS} + 0.2016V_{GS}^2$$

$$0.2016V_{GS}^2 = -0.673 \text{ V or } V_{GS} = -9.287 \text{ V}$$

V_{GS} should be greater than V_P

$$V_{GSQ} = -0.673 \text{ V}$$

$$I_D = -\frac{(-0.673)}{180} = \mathbf{3.7389 \text{ mA}}$$

2nd stage:

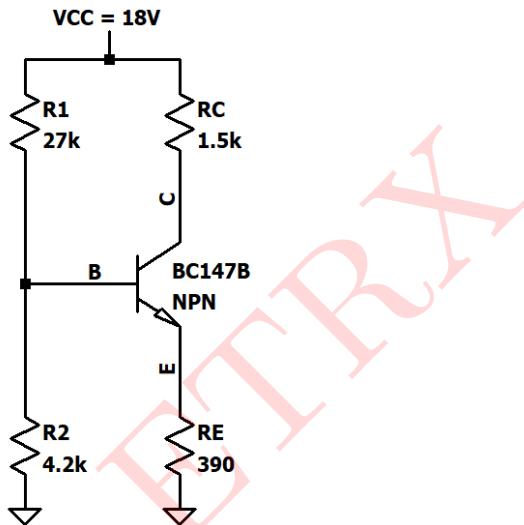


Figure 20: DC Equivalent circuit

$$V_B = \frac{V_{CC} \times R_2}{R_1 + R_2}$$

$$V_B = \frac{18 \times 4.2 \times 10^3}{27 \times 10^3 + 4.2 \times 10^3} = \mathbf{2.423 \text{ V}}$$

$$R_B = \frac{R_1 \times R_2}{R_1 + R_2}$$

$$R_B = \frac{27 \times 10^3 \times 4.2 \times 10^3}{27 \times 10^3 + 4.2 \times 10^3} = \mathbf{3.63 \text{ k}\Omega}$$

Applying KVL to the B-E loop,

$$V_B - R_B I_B - V_{BE} - I_E R_E = 0$$

$$R_B I_B + (1 + \beta) I_B R_E = V_B - V_{BE}$$

$$I_B = \frac{V_B - V_{BE}}{R_B + (1 + \beta)} R_E$$

$$I_B = \frac{2.423 - 0.7}{3.63 \times 10^3 + (1 + 290) \times 390} = \mathbf{14.71 \mu\text{A}}$$

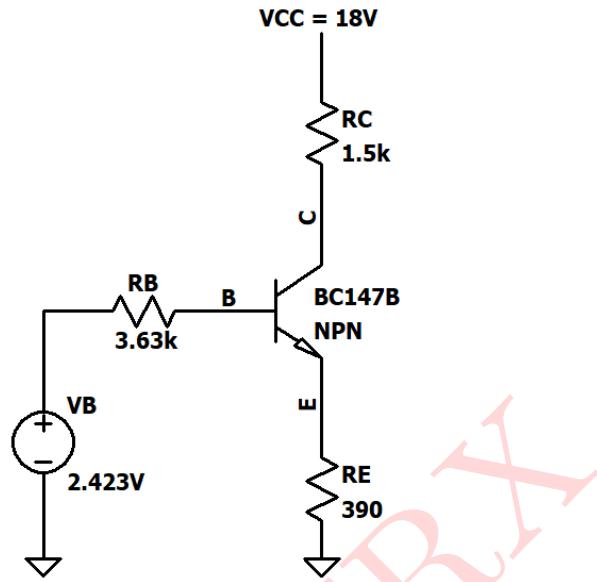


Figure 21: Thevenin's Equivalent circuit

$$I_C = \beta I_B$$

$$I_C = 290 \times 14.71 \times 10^{-6} = 4.2659 \text{ mA}$$

$$I_E = (1 + \beta)I_B$$

$$I_E = (1 + 290) \times 14.71 \times 10^{-6} = 4.2806 \text{ mA}$$

$$V_E = I_E R_E$$

$$V_E = 4.2806 \times 10^{-3} \times 390 = 1.6694 \text{ V}$$

AC Analysis:

Small signal parameters:

$$r_\pi = \frac{\beta V_T}{I_E}$$

$$r_\pi = \frac{290 \times 26 \times 10^{-3}}{4.289 \times 10^{-3}} = 1.761 \text{ k}\Omega$$

$$g_{m2} = \frac{I_C}{V_T}$$

$$g_{m2} = \frac{4.2659 \times 10^{-3}}{26 \times 10^{-3}} = 164.07 \text{ mA/V}$$

$$g_{m1} = g_{mo} \left(1 - \frac{V_{GS}}{V_P} \right)$$

$$g_{m1} = 5600 \times 10^{-6} \left(1 - \frac{(-0.673)}{(-2.5)} \right) = 4.092 \text{ mA/V}$$

Small Signal Equivalent Circuit is shown in figure 22:

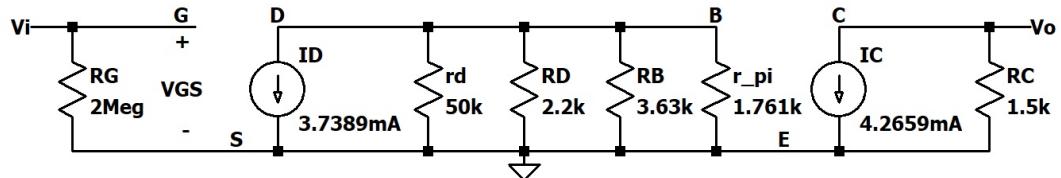


Figure 22: Small Signal Equivalent Circuit

Stage 2 Voltage gain:

$$A_{V2} = \frac{-g_{m2} V_\pi (R_C)}{V_\pi}$$

$$A_{V2} = -g_{m2} R_C$$

$$A_{V2} = -164.07 \times 10^{-3} \times 1.5 \times 10^3 = -246.105$$

Stage 1 voltage gain:

$$A_{V1} = \frac{-g_{m1} V_{GS} (R_D \parallel r_d \parallel R_B)}{V_{GS}}$$

$$A_{V1} = -g_{m1} (R_D \parallel r_d \parallel R_B)$$

$$A_{V1} = -4.092 \times 10^{-3} (2.2 \times 10^3 \parallel 50 \times 10^3 \parallel 3.7 \times 10^3 \parallel 1.761 \times 10^3) = -3.1049$$

Overall voltage gain:

$$A_{VT} = A_{V1} \times A_{V2}$$

$$A_{VT} = (-3.1049) \times (-246.105) = 764.131$$

$$A_{VT} \text{ in dB} = 20 \log_{10} (|A_{VT}|)$$

$$A_{VT} \text{ in dB} = 20 \log_{10} (764.131) = 57.66 \text{ dB}$$

Input impedance of stage 1:

$$Z_i = R_G = 2 \text{ M}\Omega$$

Output impedance of stage 2:

$$Z_o = R_C = 1.5 \text{ k}\Omega$$

SIMULATED RESULTS:

Above circuit is simulated in LTspice. The results are presented below:

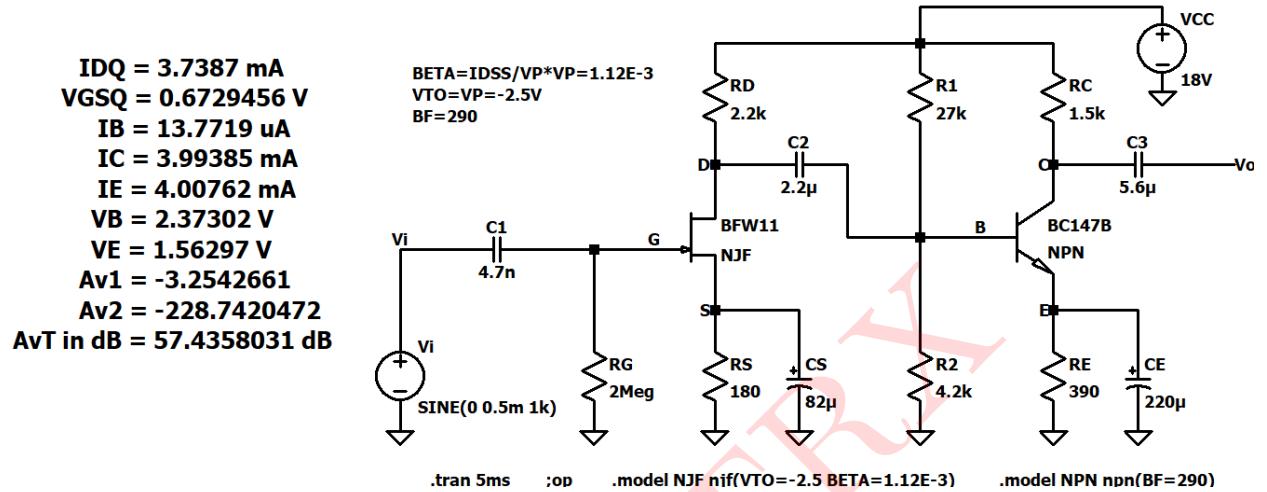


Figure 23: Circuit Schematic 2: Results

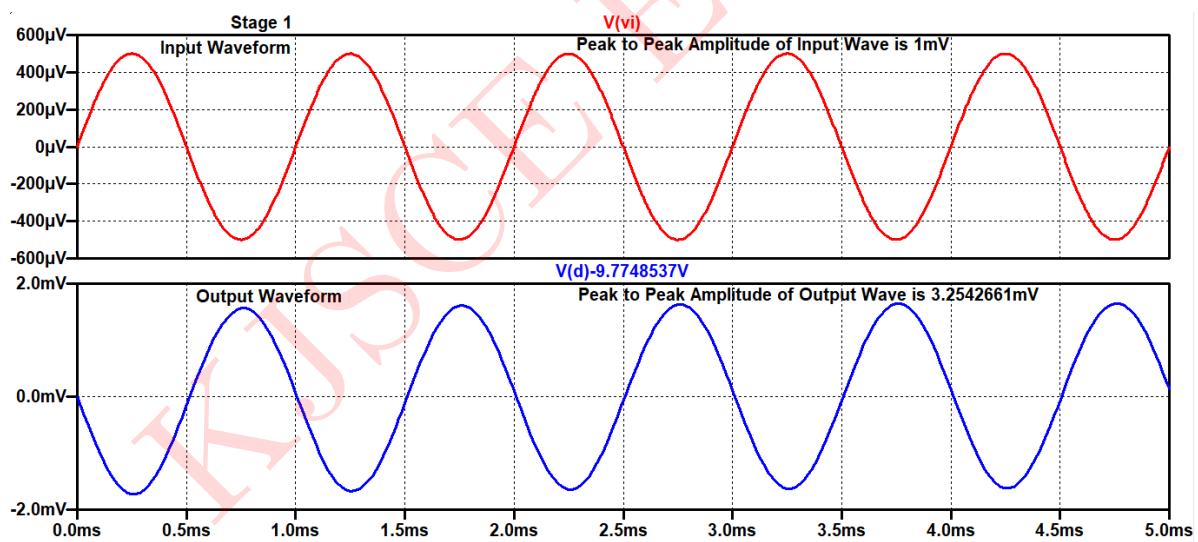


Figure 24: Input & Output waveforms for stage 1 voltage gain

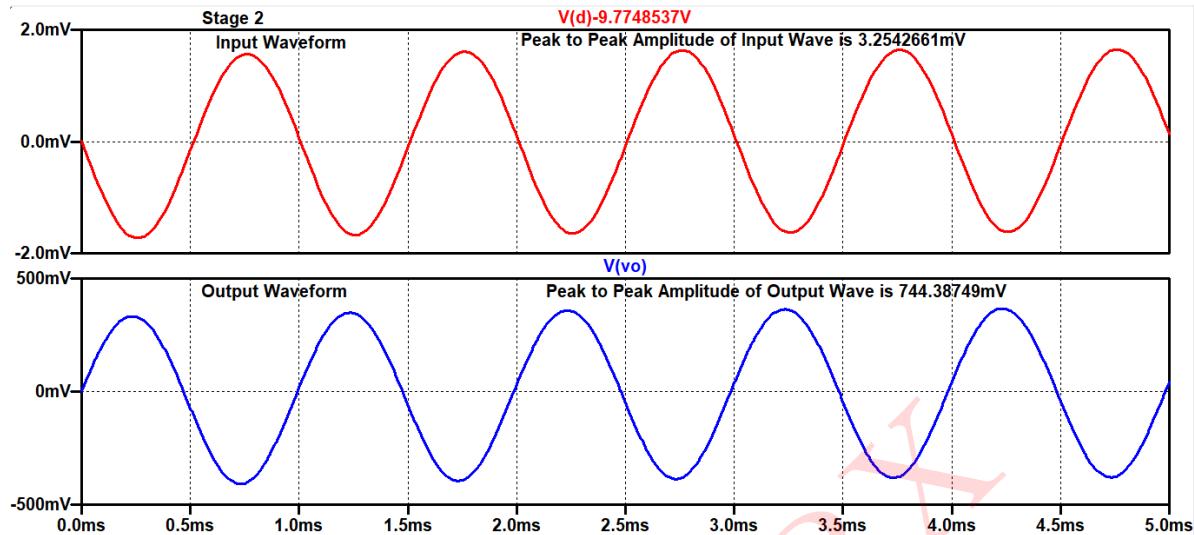


Figure 25: Input & Output waveforms for stage 2 voltage gain

Comparison of theoretical and simulated values:

Parameters	Theoretical Values	Simulated Values
I_{DQ}	3.7389 mA	3.7387 mA
V_{GSQ}	-0.673 V	-0.6729 V
I_B	14.71 μ A	13.7719 μ A
I_C	4.2659 mA	3.9938 mA
I_E	4.2806 mA	4.0076 mA
V_B	2.423 V	2.3730 V
V_E	1.6694 V	1.5629 V
Voltage gain of stage 1: A_{V_1}	-3.1049	-3.2542
Voltage gain of stage 2: A_{V_2}	-246.105	-228.7420
Overall voltage gain: A_{VT} in dB	57.66 dB	57.4358 dB
Input impedance of stage 1	2 M Ω	-
Output impedance of stage 2	1.5 k Ω	-

Table 2: Numerical 2
