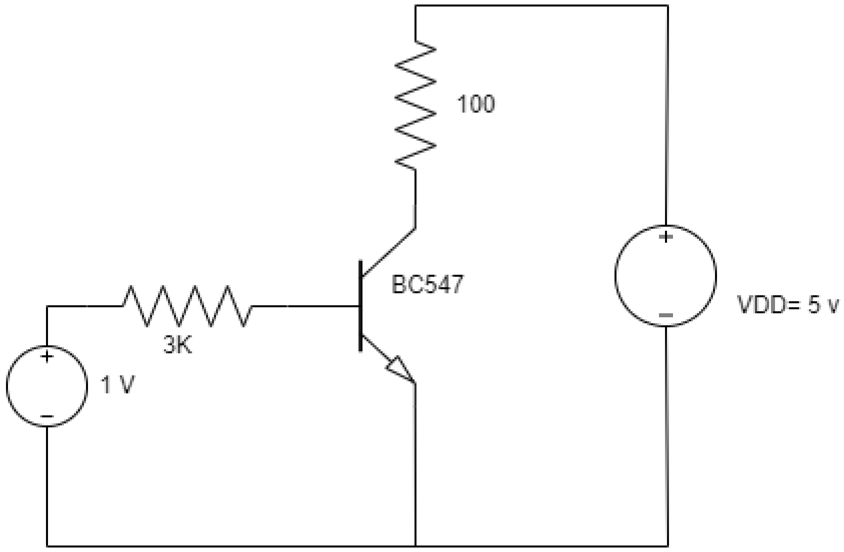
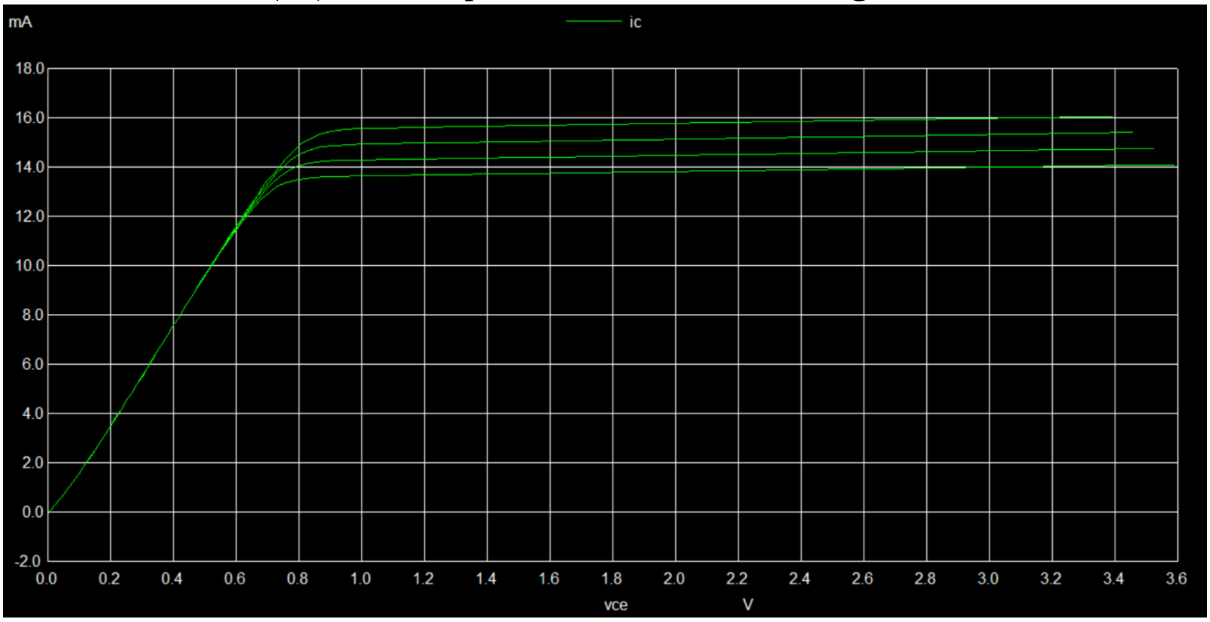
End-Sem Solution

Q1.

a) BJT temperature dependency:
   Common emitter circuit schematic:

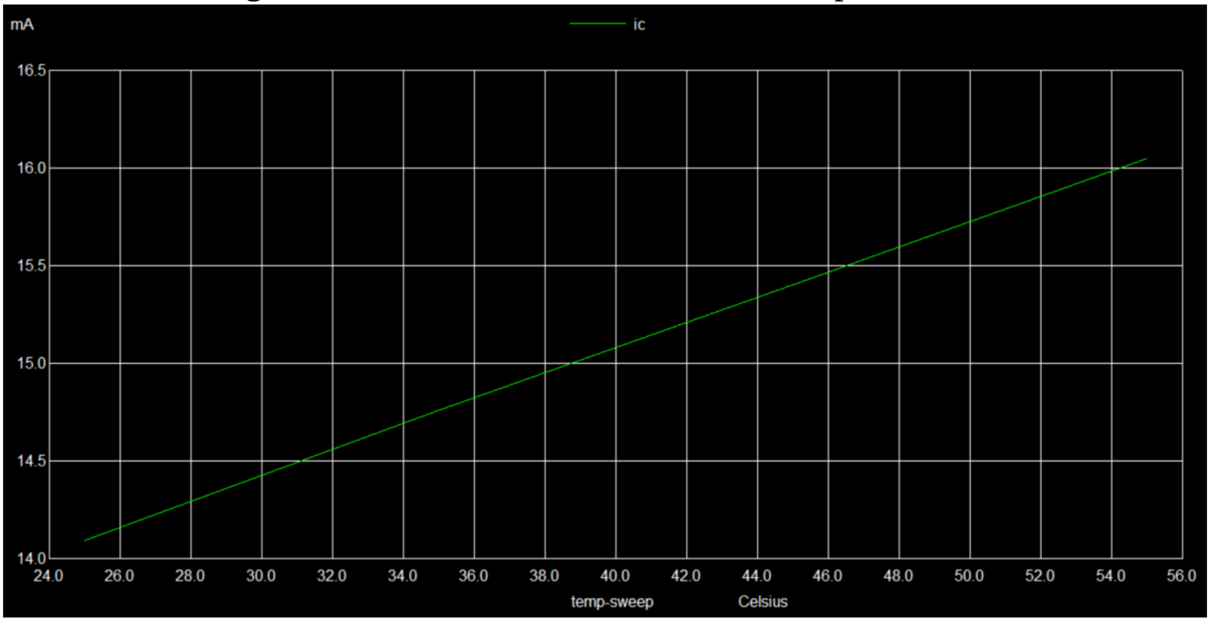


Vin= 1 V for IB=0.1 mA VBE= 0.7 V(approx)
Collector current (IC) vs VCE plot for T=25,35,45,55 degrees celsius:

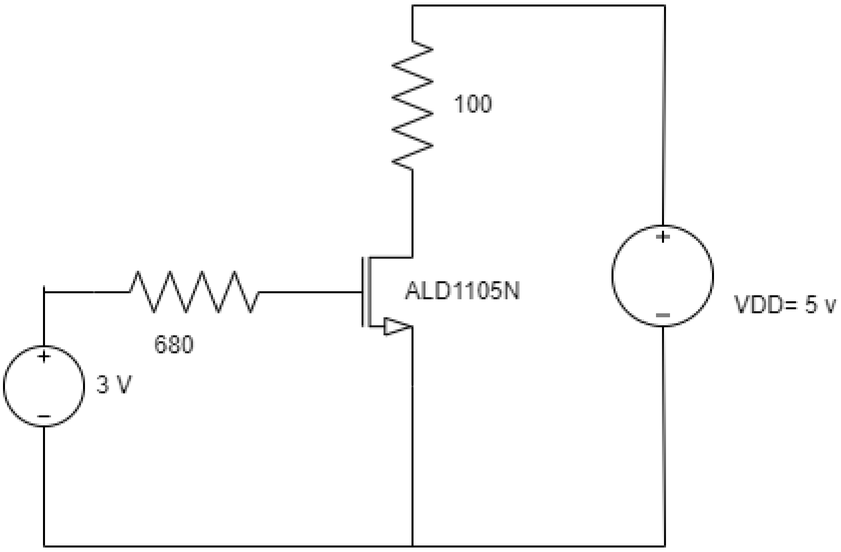


Temperature(degrees)	IC (mA) @VCE=3V
25	14.07
35	14.74
45	15.25
55	16

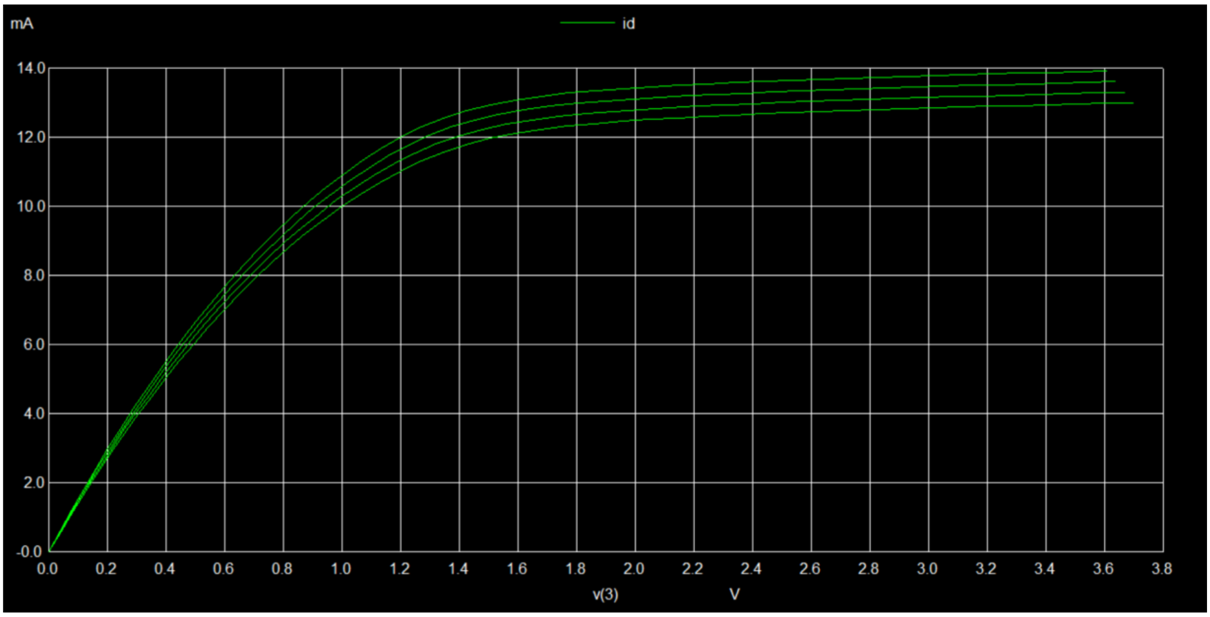
IC vs Temperature plot: As Temperature increases IC increases because electrons, holes get freer from the valance bonds as temperature increases



b) MOSFET temperature dependency:
Common source circuit schematic:

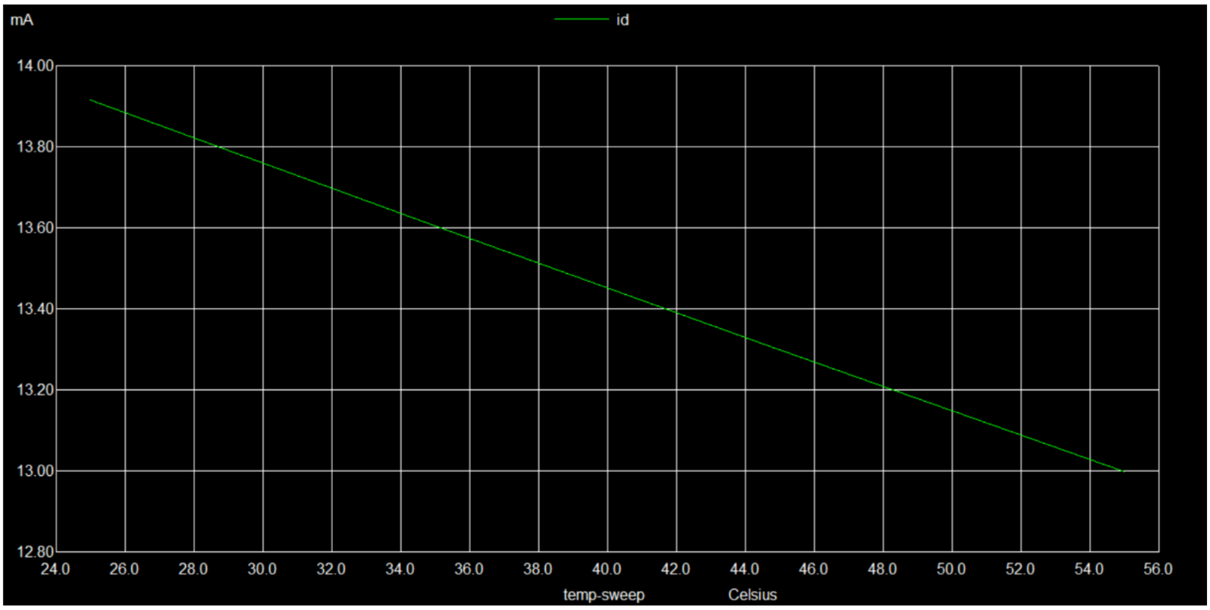


ID vs VDS for T=25,35,45,55 degree celsius



Temperature (degree Celsius)	ID (mA) @VDS=3V
25	13.8
35	13.5
45	13.1
55	12.8

ID vs temperature: As temperature increases Vth decreases and current should decrease but at the same time mobility also decreases and is dominant (at high temperatures i.e., > 150 kelvin temperatures. Considered temperatures are above 298 kelvin) hence current decreases

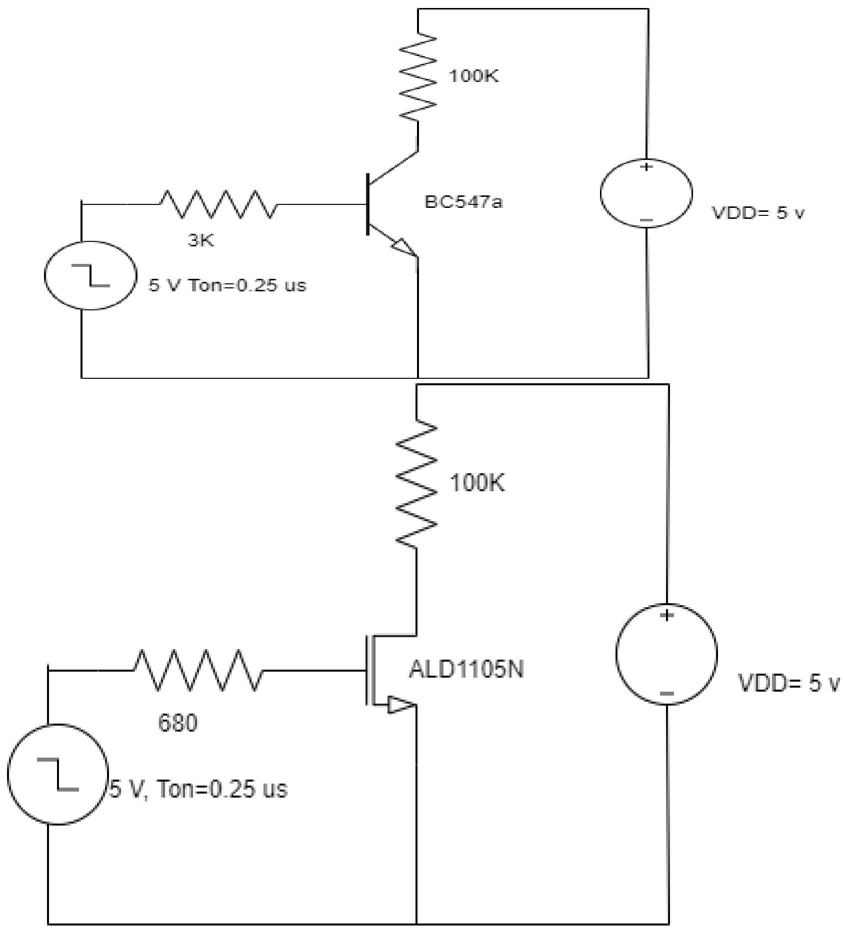


c) BJT vs MOSFET storage time: In BJT both electrons and holes contribute to current and when the device is supposed to turn off reverse recombination will take some time whereas in case of NMOSFET only electrons so when device is supposed to turn off no reverse recombination take place hence MOSFETs are faster compared to BJT

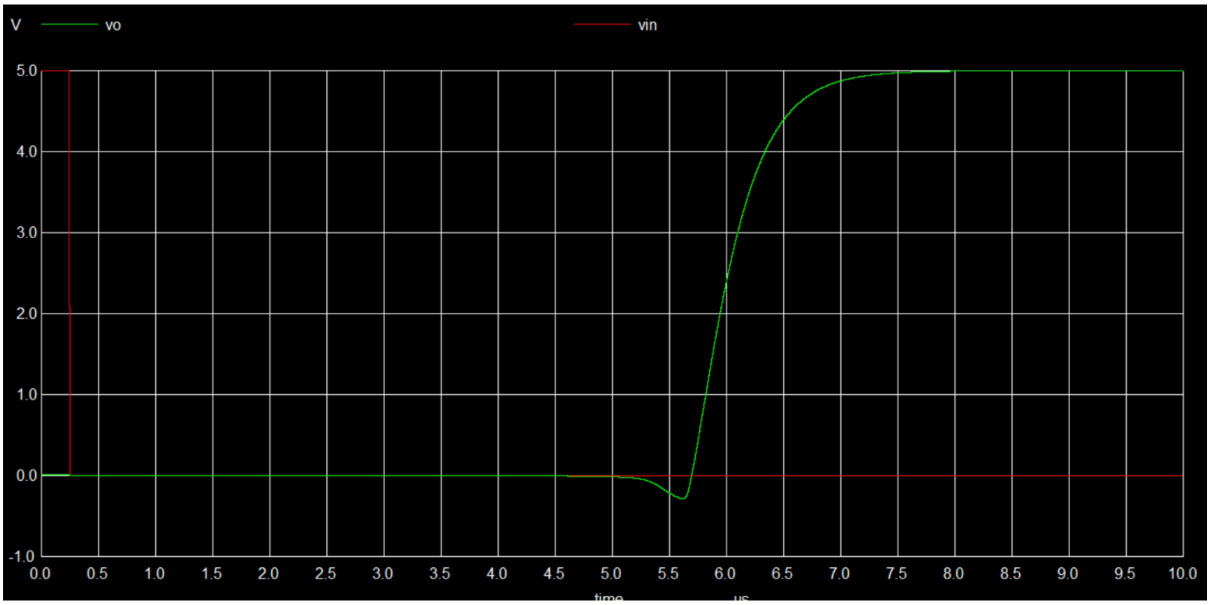
Turn off time of BJT and MOSFET:

BJT	MOSFET
7.25 **us**	20 **ns**

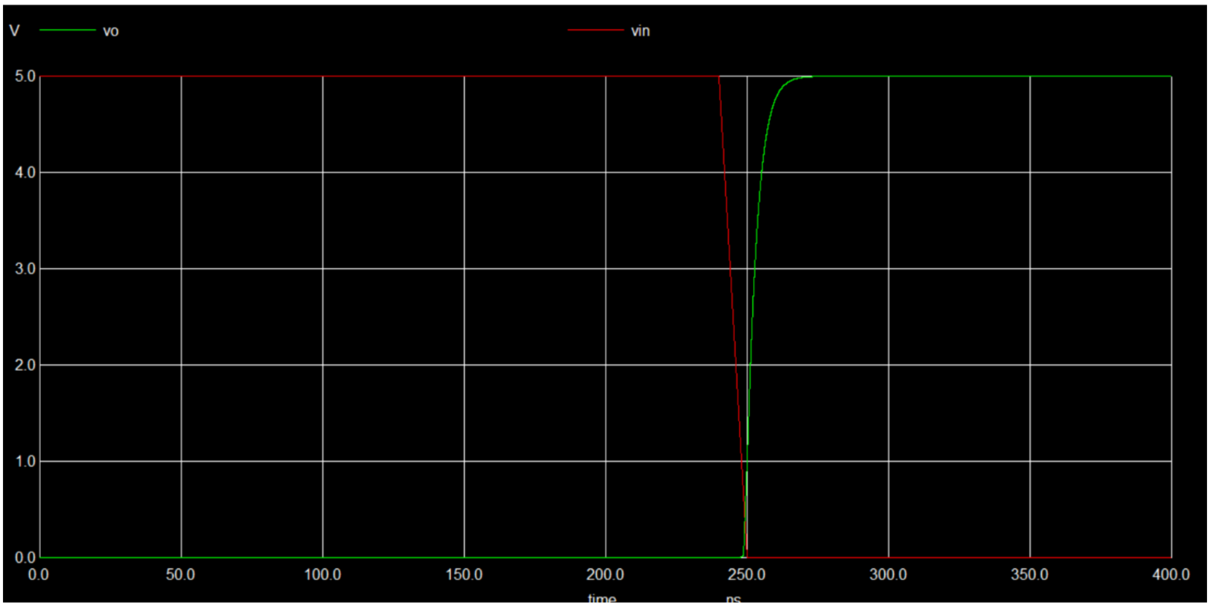
Circuit schematic for measurement of BJT, MOSFET turn off time: Output measured at collector and drain respectively



BJT turn off time plot:

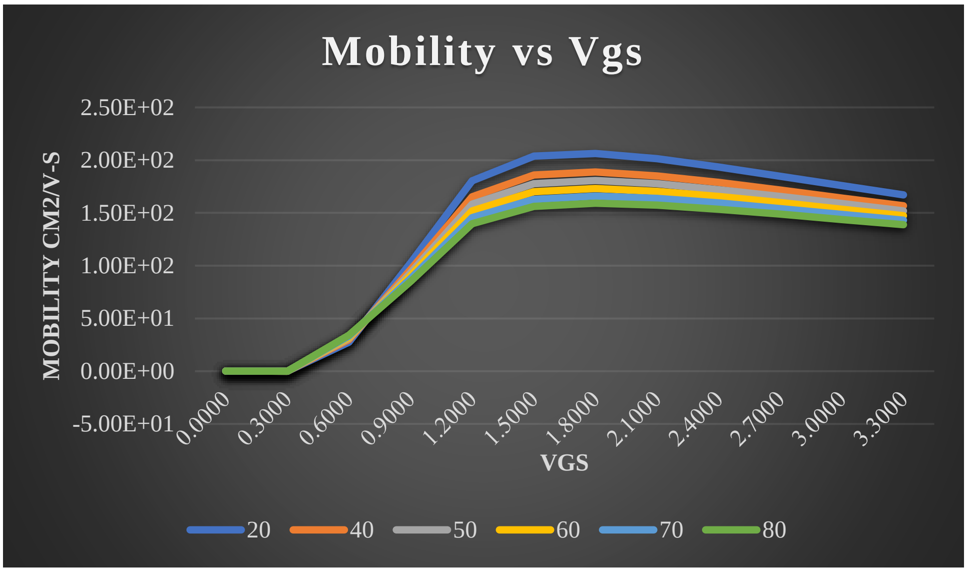


MOSFET turn off time plot:

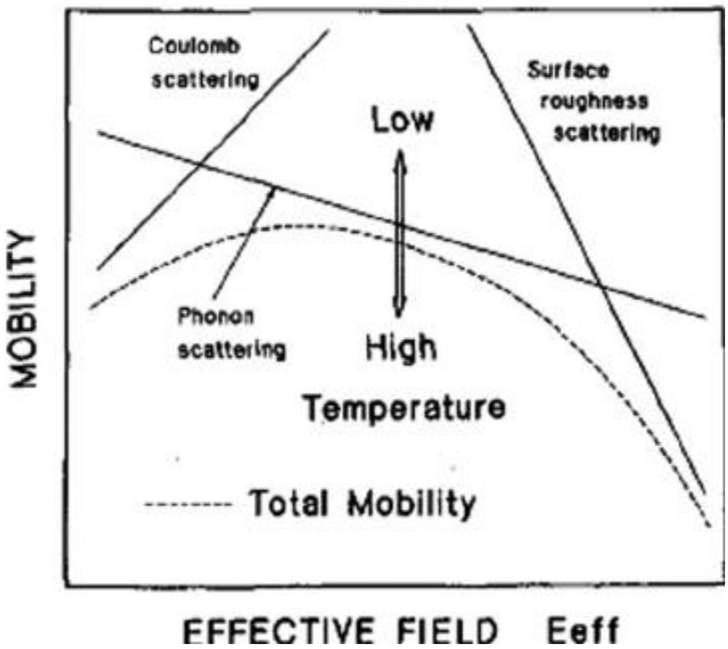


Q2.

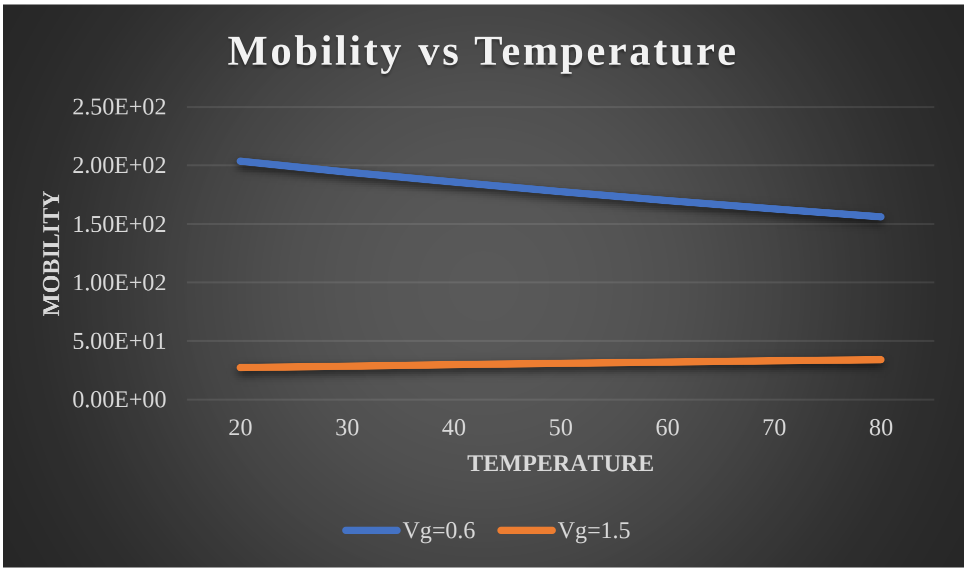
a)



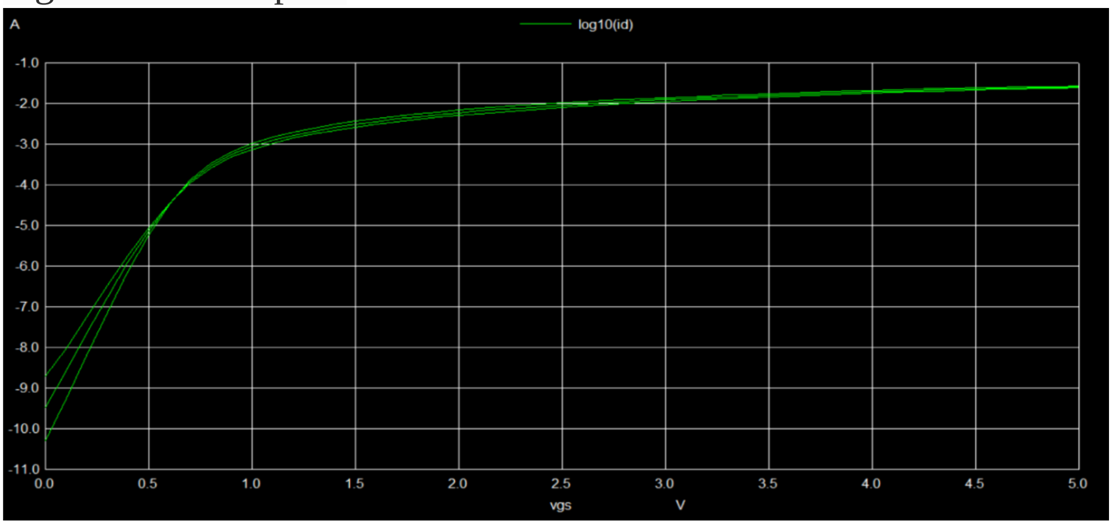
Explanation:



b)



c) $\log_{10}$ ID vs VGS plot:



Subthreshold slope (S.S) vs temperature: As temperature increases the subthreshold slope increases i.e., S.S. is directly proportional to temperature

$S=2.3 * kT/q * (1+C_{dm}/C_{ox})$. It should be ≥ 60mv/dec for T≥ 25 degree Celsius

K=Boltzmann constant

Cdm =depletion capacitance per unit area

Cox=oxide capacitance per unit area

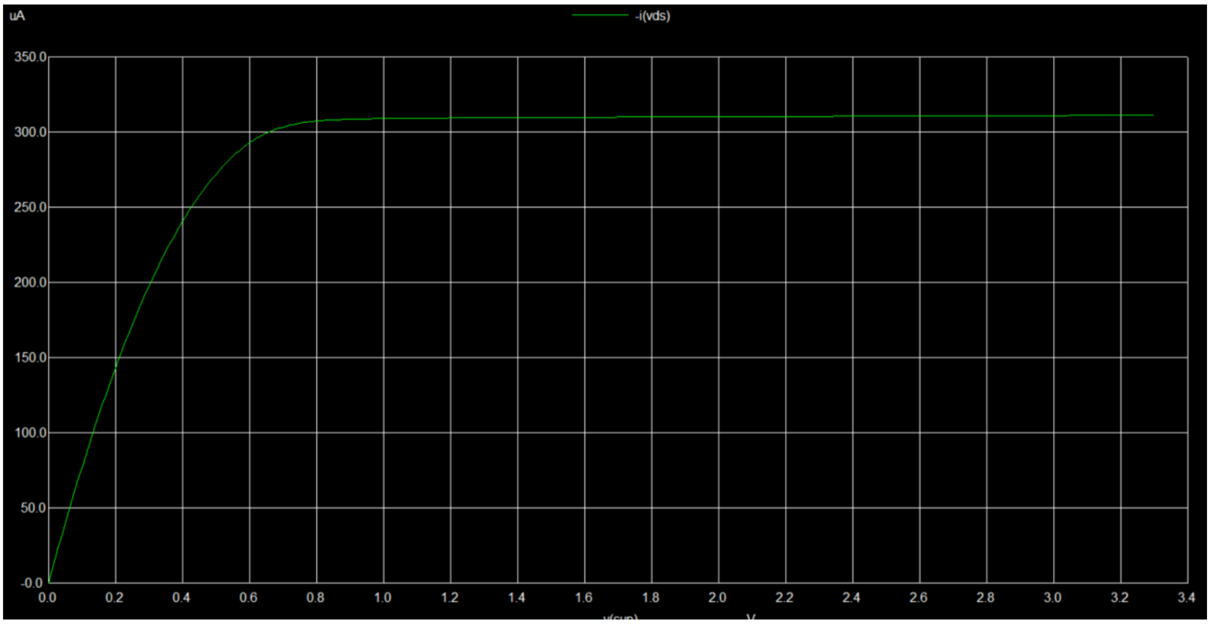
Off current (Ioff) vs temperature: As temperature increases the off current increases

Ideally both subthreshold slope and off current should be low

Temperature (Degree Celsius)	Subthreshold slope (mv/dec)	Off current (pA)
25	101	60.9
75	114	389
125	136	2398

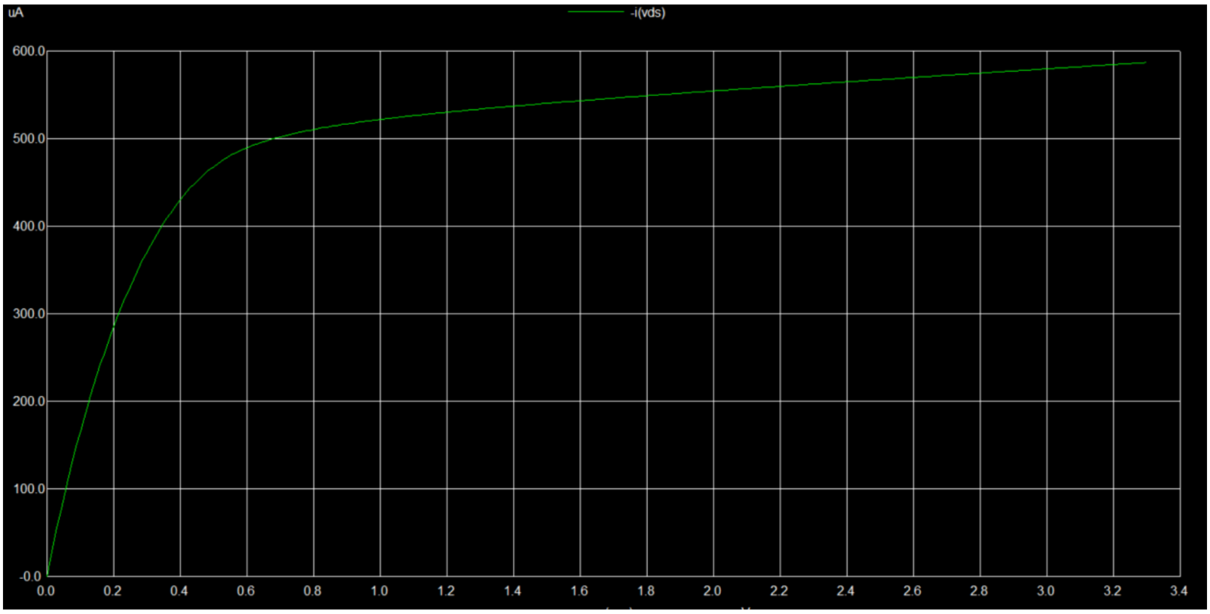
Q3.

a)



Long-Channel

R_0 = x MΩ (In the range of Mega ohm)



Short-channel

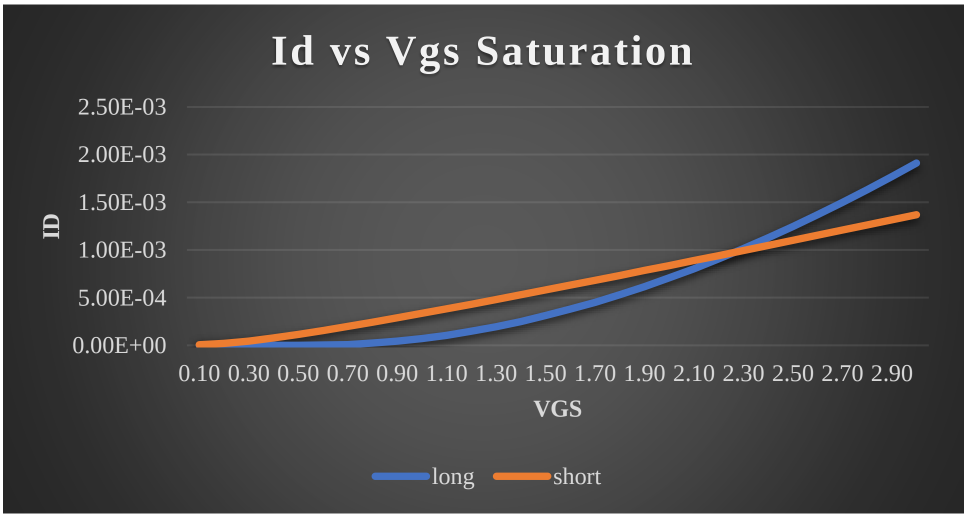
R_0 = 35kΩ (20 – 50 kΩ will be fine)

Reason: $R_0 = L/(\Delta L I_d)$

b)

For Short channel V_{th} = 0.3V

For long channel V_{th} = 0.8V – 1V

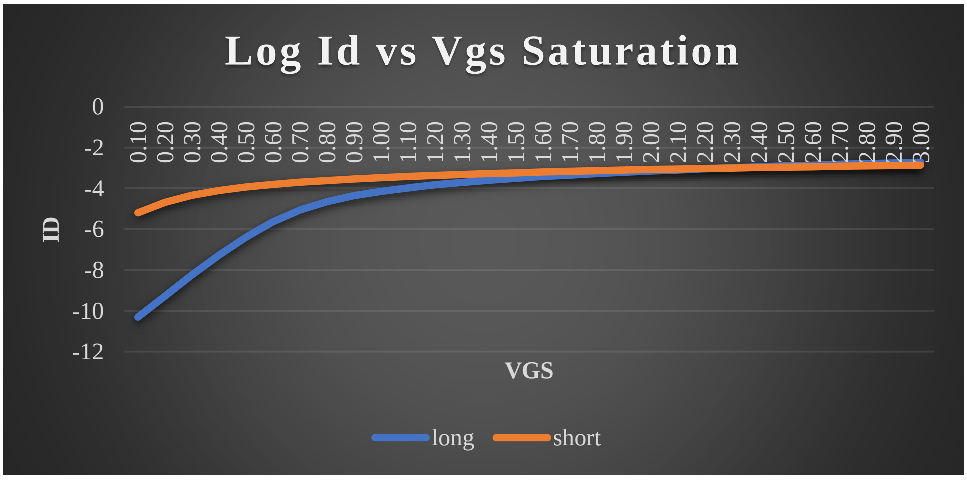


Explanation: Ability of gate & body to control channel charge diminishes as L decreases, resulting in Vt-roll-off and body effect reduction.

Short-channel Vt equation:

$$\boxed{V_t = V_{fb} + |2\phi_B| + \frac{\lambda_b}{C_{ox}}\sqrt{2qN_a\varepsilon_s(|2\phi_B| + V_{sb})} - \lambda_d V_{ds}}$$

$$V_t = V_{fb} + |2\phi_B| + \frac{\sqrt{2qN_a\varepsilon_{si}|2\phi_B|}}{C_{ox}}$$ **(Long channel V_t equation)**



Explanation: DIBL increases leakage current in short-channel devices

Q4.

a)

Rise time and fall time equations are

$$T_r \times K_p = 2C \times \frac{V_{iL} + V_{Tp}}{\left(V_{DD} - V_{iL} - V_{Tp}\right)^2} + log\left(\frac{V_{DD} + V_{oH} - 2V_{iL} - 2V_{Tp}}{V_{DD} - V_{oH}}\right) \times \frac{C}{V_{DD} - V_{iL} - V_{Tp}}$$

$$T_f \times K_n = 2C \times \frac{(V_{DD} - V_{iH} + V_{Tn})}{(V_{iH} - V_{Tn})^2} + log\left(\frac{2(V_{iH} - V_{Tn}) - V_{oL}}{V_{oL}}\right) \times \frac{C}{V_{iH} - V_{Tn}}$$

By using above and sweeping, wn and wp we will get as

Wn=1.51u

Wp=3.63u

Netlist:

```
.include models
.param Lmin=0.4u
.param Wp=3.63u
.param Wn=1.51u

MP1 out in supply supply cmosp
+ L=Lmin W=Wp AD= (2*Wp*Lmin) AS =(2*Wp*Lmin) PD= (2*Wp+4*Lmin) PS= (2*Wp+4*Lmin)
MN1 out in 0 0 cmosn
+ L=Lmin W=Wn AD= (2*Wn*Lmin) AS =(2*Wn*Lmin)  PD =(2*Wn+4*Lmin) PS = (2*Wn+4*Lmin)

vdd supply 0 dc 3.3
CL out 0 0.05pf

*TRANSIENT ANALYSIS with pulse inputs
Vin in 0 dc PULSE(0 3.3 4ns 25pS 25pS 4nS 8nS)
.tran 1p 40n 0ns
 .control
  run
   plot V(in)+4,V(out)
   meas tran inrise TRIG v(in) VAL=0.33 RISE=2 TARG v(in) VAL=2.97 RISE=2
   meas tran infall TRIG v(in) VAL=2.97 FALL=2 TARG v(in) VAL=0.33 FALL=2
   meas tran outrise TRIG v(out) VAL=0.33 RISE=2 TARG v(out) VAL=2.97 RISE=2
   meas tran outfall TRIG v(out) VAL=2.97 FALL=2 TARG v(out) VAL=0.33 FALL=2
  .endc
.end
```

```
Doing analysis at TEMP = 27.000000 and TNOM = 27.000000


Initial Transient Solution
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Node                                       Voltage
----                                       -------
out                                            3.3
in                                               0
supply                                         3.3
vin#branch                                       0
vdd#branch                            -4.80881e-12

 Reference value :  3.61605e-08

No. of Data Rows : 40062
inrise             =  2.000000e-11 targ=  1.202250e-08 trig=  1.200250e-08
infall             =  2.000000e-11 targ=  1.604750e-08 trig=  1.602750e-08
outrise            =  2.502118e-10 targ=  1.632630e-08 trig=  1.607609e-08
outfall            =  2.503765e-10 targ=  1.231045e-08 trig=  1.206007e-08
ngspice 1 ->
The file "/tmp/hc15252" may be printed on a postscript printer.
```
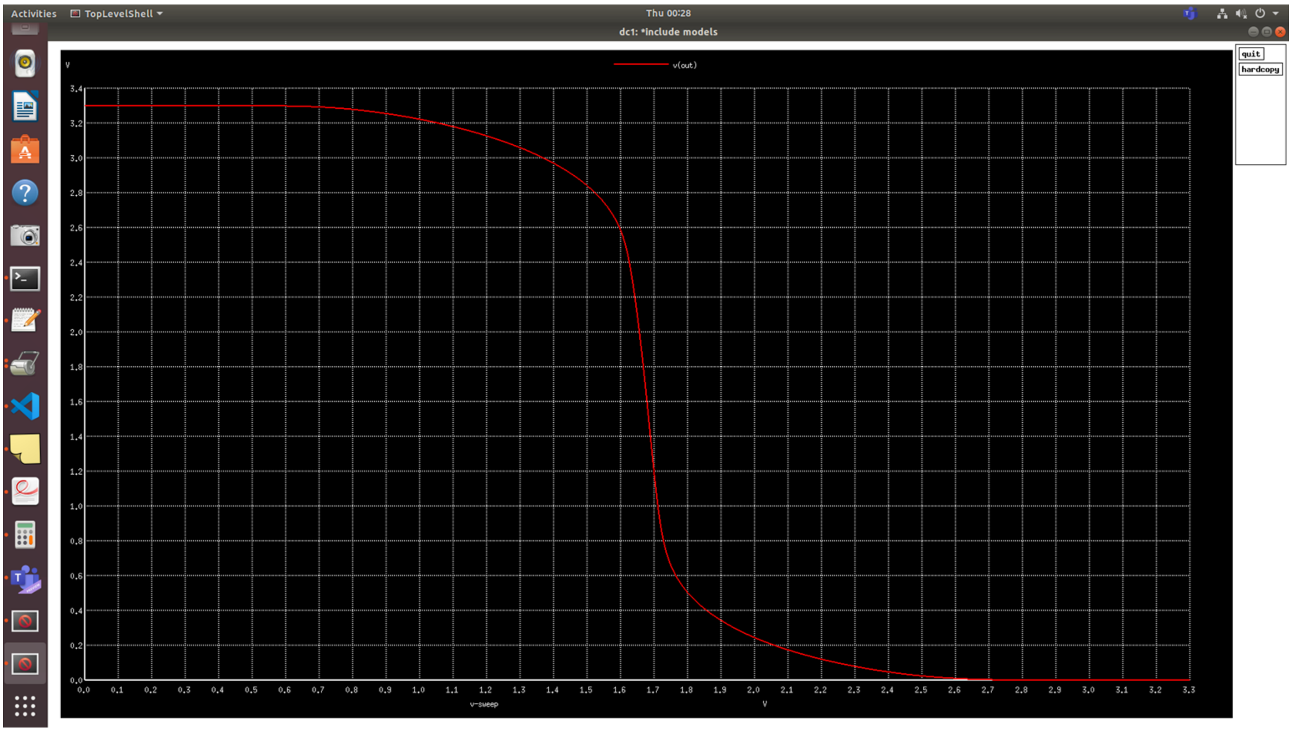

b)

```
.include models
.param Lmin=0.4u
.param Wp=3.63u
.param Wn=1.51u

MP1 out in supply supply cmosp
+ L=Lmin W=Wp AD=(2*Wp*Lmin) AS=(2*Wp*Lmin)
PD=(2*Wp+4*Lmin) PS=(2*Wp+4*Lmin)
MN1 out in 0 0 cmosn
+ L=Lmin W=Wn AD=(2*Wn*Lmin) AS=(2*Wn*Lmin)
PD=(2*Wn+4*Lmin) PS=(2*Wn+4*Lmin)

CL out 0 0.05pf
vdd supply 0 dc 3.3v
vin in 0  dc 3.3v

.dc vin 0 3.3 0.0001
.control
 run
 let x=deriv(v(out))
 plot V(out)
 plot -I(vdd)
```

```
  meas dc voh find v(out) when x=-1
  meas dc vil find v(in) when out=voh
  meas dc vol find v(out) when x=-1 cross=2
  meas dc vih find v(in) when out=vol
let NM_H=voh-vih
let NM_L=vil-vol
print NM_H NM_L

.endc
.end
```

```
nm_h = 1.037510e+00
nm_l = 1.093354e+00
ngspice 1 ->
x0 = 2.176, y0 = 2.32308
```



c)

From the graph, it can be seen that short circuit current flows when both NMOS and PMOS are on at switching threshold