Roll Number: 190070049

Name: Rathour Param Jitendrakumar

Course: Electronic Devices Lab

Course Code: EE236

Q1) Part 1

Body Bias NMOS (in V)	Body Bias PMOS (in V)	Peak Charging Current (in A)	Peak Discharging Current (in A)	Delay Time (in s)
0.3	3	6.913996e-04	5.975586e-04	6.585508e-10
0.1	3.2	6.918728e-04	5.970618e-04	6.612506e-10
0	3.3	6.893650e-04	5.945589e-04	6.652150e-10
-0.5	3.8	6.728170e-04	5.792506e-04	6.885459e-10
-1	4.3	6.590579e-04	5.669193e-04	7.085675e-10

For each of the above cases, I made rise time ≈ fall time by varying W_p

W_p (in μm)	Rise Time (in s)	Fall Time (in s)
2.855	1.128212e-09	1.128324e-09
2.868	1.136146e-09	1.136140e-09
2.8742	1.143771e-09	1.143708e-09
2.9075	1.185133e-09	1.185185e-09
2.942	1.220952e-09	1.220808e-09

If W_p is fixed then let W_p ≈ W_p_0 = 2.8742 (W_p_avg = 2.88934)

For this W_p,

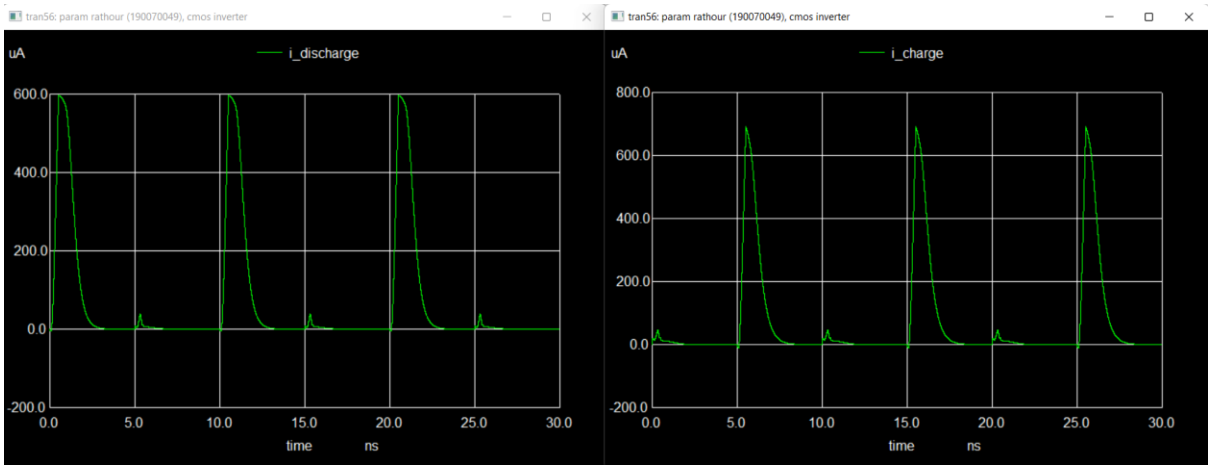
Body Bias NMOS (in V)	Body Bias PMOS (in V)	Peak Charging Current (in A)	Peak Discharging Current (in A)	Delay Time (in s)
0.3	3	6.913996e-04	5.975586e-04	6.585508e-10
0.1	3.2	6.933391e-04	5.970618e-04	6.613078e-10
0	3.3	6.893650e-04	5.945589e-04	6.652150e-10
-0.5	3.8	6.652463e-04	5.792434e-04	6.882675e-10
-1	4.3	6.441193e-04	5.669057e-04	7.080215e-10

Part 2

Peak Charging Current decreases (down the table) due to decreasing substrate voltage

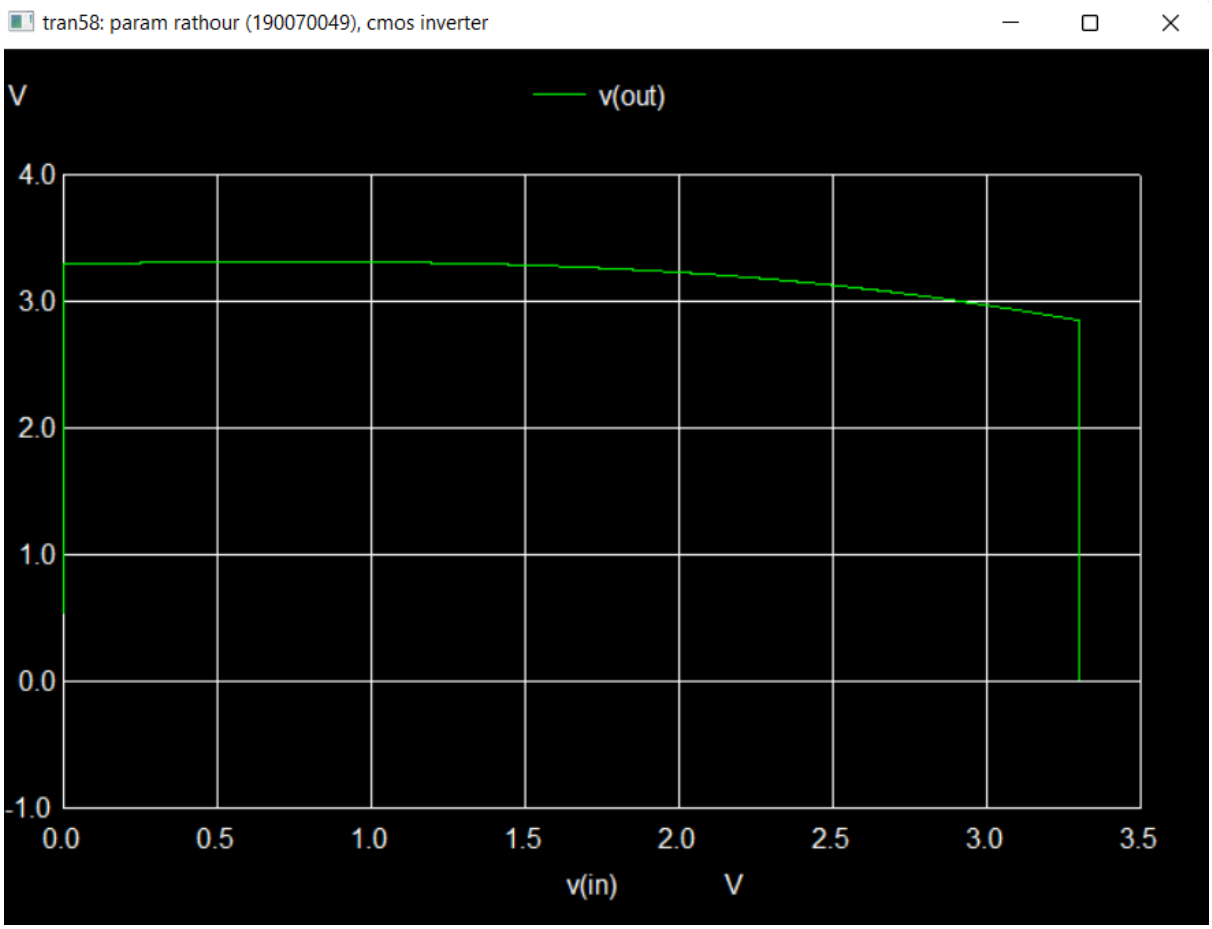
Peak Discharging Current decreases (down the table) due to increasing substrate voltage

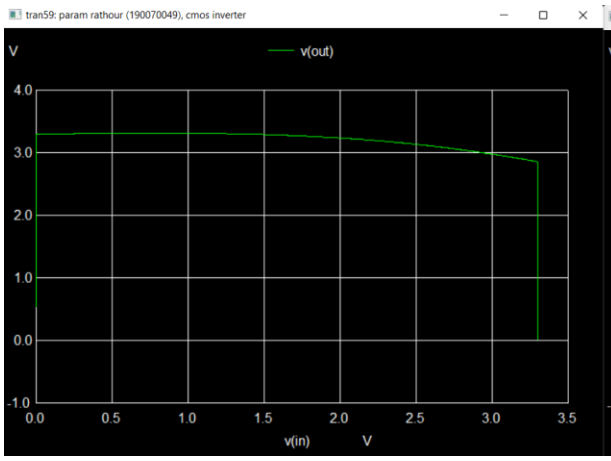
Delay time increases (down the table) as it is positively correlated with rise time and fall time and both increases as W_p increases

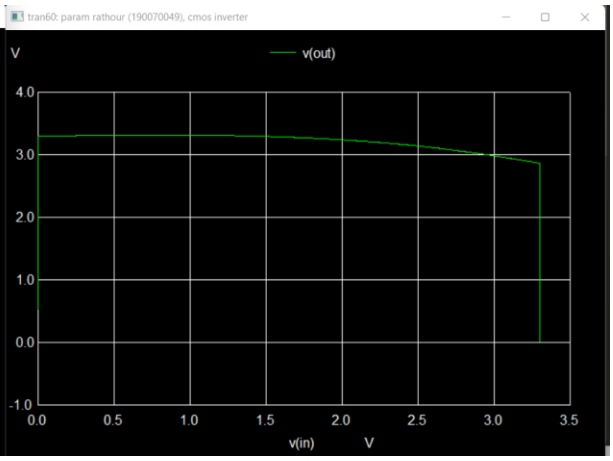


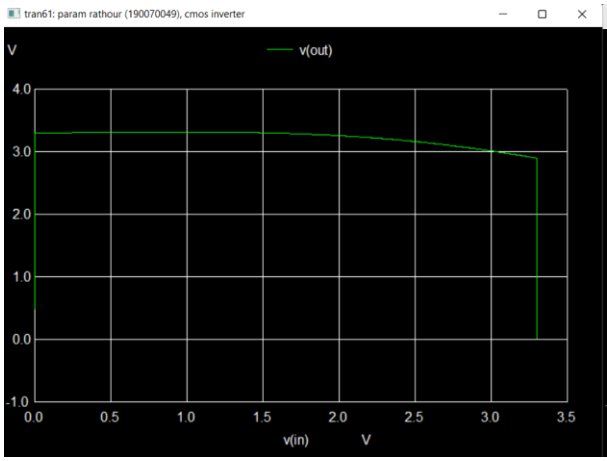
Part 3

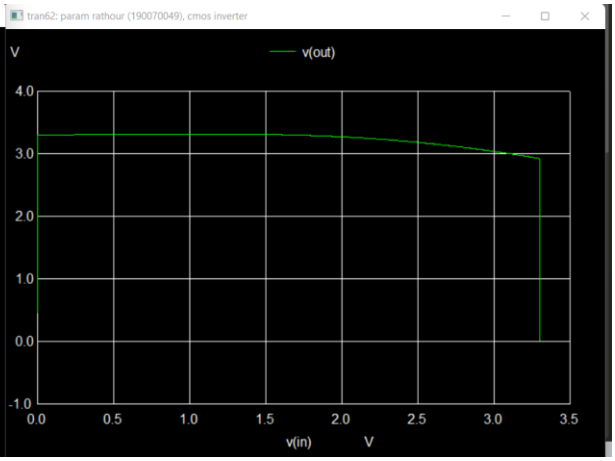
Vth remains almost same











Part 4

0.3V and 3V for low power