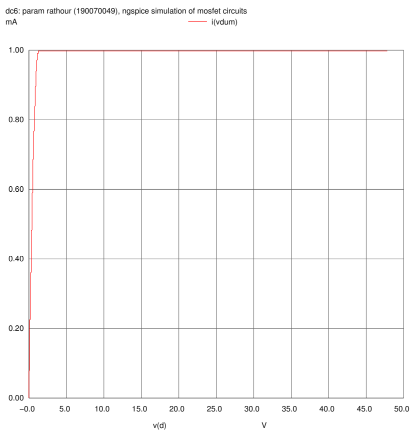
EE230 - Experiment 5

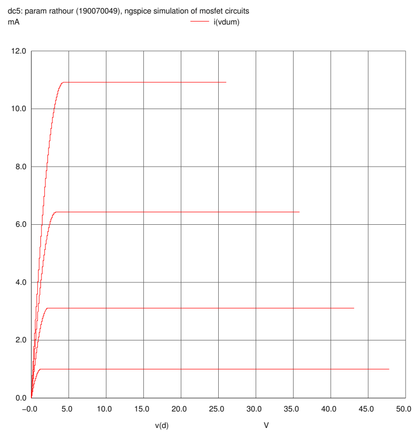
Param Rathour - 190070049
Autumn Semester 2021-22

1 NMOS Output Characteristics

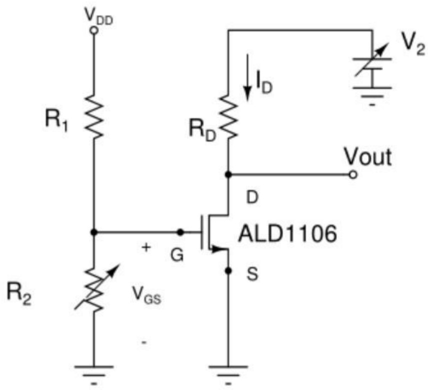
1.1 Plots



(a) I_D vs V_{DS} (for $V_{GS} = 2V$)



(b) I_D vs V_{DS} (for $V_{GS} = 2V, 3V, 4V \ \&5V$)



(c) BJT current source

1.2 Code

To get $I_D = 1mA$, $K_P = \mu_n \cdot C_{\text{ox}} = 1.1834319 \cdot 10^{-4} A/V^2$ (using $I_d = \frac{W}{2L} K_p (V_{GS} - V_{th})^2$)

1.2.1 $V_{GS} = 2$

```
Param Rathour (190070049), NGSPICE Simulation of MOSFET Circuits
.model NXYAA5U nmos Level=1 Vto=0.7 KP=118.34u w=10u L=1u
+ Gamma=0 Phi=0.65 Lambda=0.0
M1 d g gnd gnd NXYAA5U
VDD Vdd gnd 10                                   ; Supply Voltage
V2 V2 gnd 5
Vdum V2 Vdum 0
R1 Vdd g 2.2k                                    ; Resistor
R2 g gnd 550                                     ; Resistor
RD d Vdum 2.2k                                   ; Resistor
.dc V2 0 50 0.01                                 ; DC Analysis
.control                                         ; Control Functions
run
plot I(Vdum) vs V(d)
.endc
.end
```

1.2.2 All V_{GS} values (only changes)

I directly changed V_{GS} value, as the resistance R_2 doesn't vary linearly. So, dc analysis with R_2 step was not possible. Remove R_1, R_2, V_{dd} and dc analysis from previous code and add below lines

```
VGS g gnd 2
.dc V2 0 50 0.01 VGS 2 5 1                       ; DC Analysis
```

1.3 Learnings

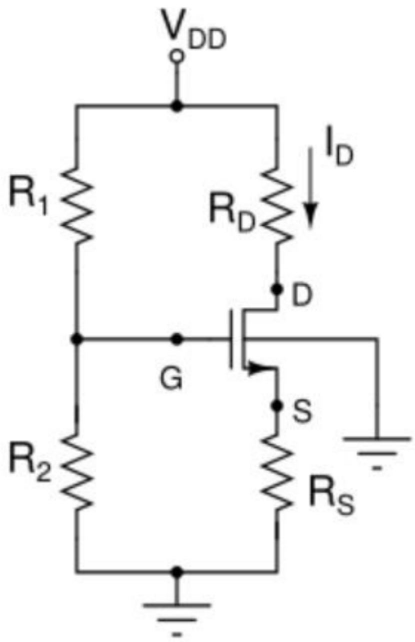
As V_{GS} increases, I_D (saturated) increases
As V_{GS} increases, V_{GS} (threshold) also increases
Understood the overall output characteristics of an NMOS transistor and the dependence of I_D on V_{GS} and V_{DS}

2 Common-Source Amplifier

2.1 NMOS Common-Source Amplifier (Bias Circuit)

2.1.1 NGSPICE Values

$V_G = 3.443478V,\ V_D = 8.643329V,\ V_S = 1.017173V,\ I_D = 1.017173 \cdot 10^{-3}mA$



(a) Bias Circuit

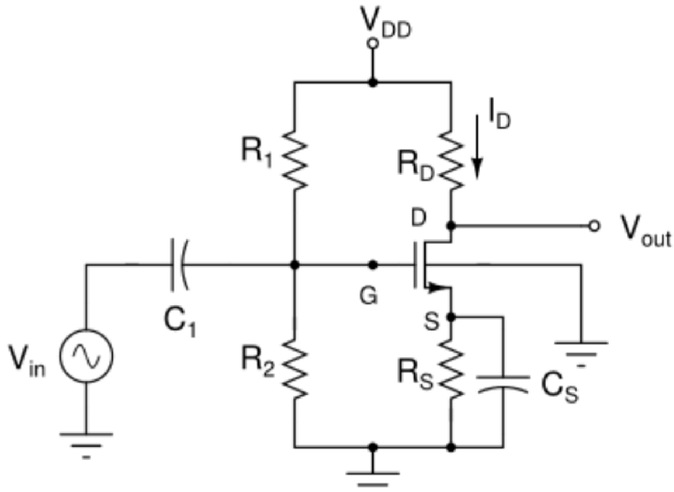
2.1.2 Code

```
Param Rathour (190070049), Common-Source Amplifier (Bias Circuit)

.model NXYAA5U nmos Level=1 Vto=1 KP=100u w=10u L=1u
+ Gamma=0 Phi=0.65 Lambda=0.0

M1 d g s gnd NXYAA5U
VDD Vdd gnd 12                                      ; Supply Voltage
Vdum Vdd Vdum 0

R1 Vdd g 8.2k                                       ; Resistor
R2 g gnd 3.3k                                       ; Resistor
RD d Vdum 3.3k                                      ; Resistor
RS s gnd 1k                                         ; Resistor

.op                                                 ; Operating Point Analysis
.control                                            ; Control Functions
run
print v(g) v(d) v(s) I(Vdum)
.endc
.end
```

2.1.3 Learnings

Analysis Values are close to Simulation values.
Understood the biasing of an NMOS Common-Source amplifier.

2.2 NMOS Common-Source Amplifier



(a) Common-Source Amplifier

2.2.1 Analysis

$g_m = \sqrt{2\mu_n C_{ox}\frac{W}{L}I_D} = 1.41\mho$, Gain $= -g_m \cdot (R_D \| r_o) = -4.5V/V$

2.2.2 NGSPICE Values

Midband voltage Gain $\approx -4.76392V/V$

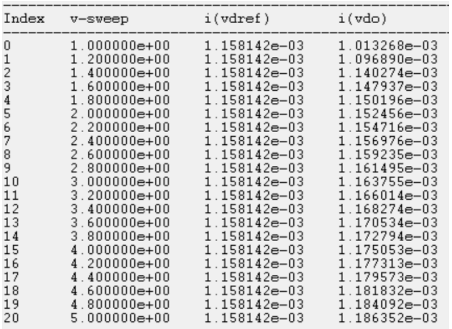
2.2.3 Code

```
Param Rathour (190070049), Common-Source Amplifier
.model NXYAA5U nmos Level=1 Vto=1 KP=100u w=10u L=1u
+ Gamma=0 Phi=0.65 Lambda=0.01
M1 d g s gnd NXYAA5U
VDD Vdd gnd 12                                         ; Supply Voltage
Vdum Vdd Vdum 0
Vin in gnd sin(0 50m 1000 0 0)                         ; Input Voltage
R1 Vdd g 8.2k                                          ; Resistor
R2 g gnd 3.3k                                          ; Resistor
RD d Vdum 3.3k                                         ; Resistor
RS s gnd 1k                                            ; Resistor
C1 g in 10u                                            ; Capacitor
CS s gnd 100u                                          ; Capacitor
.tran 0.001m 10m                                       ; Transient Analysis
.control                                               ; Control Functions
run
plot v(d)
meas trans V01 avg v(d)                                ; Finds DC op value
meas trans V01pp max v(d)
meas trans Vinpp max v(in)
let Gain = (V01pp-V01) / Vinpp
print Gain
.endc
.end
```

2.2.4 Learnings

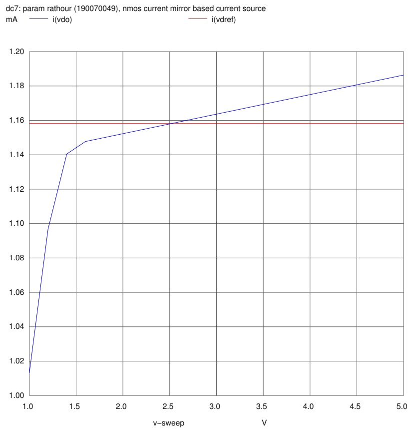
Analysis Values are close to Simulation values.
Understood the performance of an NMOS Common-Source amplifier.

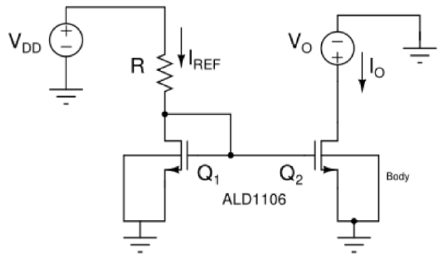
3 NMOS Current Mirror based Current Source



Index	v-sweep	i(vdref)	i(vdo)
0	1.000000e+00	1.158142e-03	1.013268e-03
1	1.200000e+00	1.158142e-03	1.096890e-03
2	1.400000e+00	1.158142e-03	1.140274e-03
3	1.600000e+00	1.158142e-03	1.147937e-03
4	1.800000e+00	1.158142e-03	1.150196e-03
5	2.000000e+00	1.158142e-03	1.152456e-03
6	2.200000e+00	1.158142e-03	1.154716e-03
7	2.400000e+00	1.158142e-03	1.156976e-03
8	2.600000e+00	1.158142e-03	1.159235e-03
9	2.800000e+00	1.158142e-03	1.161495e-03
10	3.000000e+00	1.158142e-03	1.163755e-03
11	3.200000e+00	1.158142e-03	1.166014e-03
12	3.400000e+00	1.158142e-03	1.168274e-03
13	3.600000e+00	1.158142e-03	1.170534e-03
14	3.800000e+00	1.158142e-03	1.172794e-03
15	4.000000e+00	1.158142e-03	1.175053e-03
16	4.200000e+00	1.158142e-03	1.177313e-03
17	4.400000e+00	1.158142e-03	1.179573e-03
18	4.600000e+00	1.158142e-03	1.181832e-03
19	4.800000e+00	1.158142e-03	1.184092e-03
20	5.000000e+00	1.158142e-03	1.186352e-03

(a) NGSPICE Values





(c) Current Mirror based Current Source

(b) I_{ref} and I_O

3.1 Analysis

$I_D = \frac{W}{2L} K_p (V_{GS} - V_{th})^2 = 1.15mA$

$I_O = I_{\text{ref}} \left(1 + \frac{V_O - V_{GS}}{V_A}\right) = 1.13mA, 1.14mA, 1.15mA, 1.16mA, 1.17mA$ for $V_O = 1V, 2V, 3V, 4V, 5V$ respectively

3.2 Code

```
Param Rathour (190070049), NMOS Current Mirror based Current Source

.model NXYAA5U nmos Level=1 Vto=1 KP=100u w=10u L=1u
+ Gamma=0 Phi=0.65 Lambda=0.01

M1 d1 d1 gnd gnd NXYAA5U
M2 VdO d1 gnd gnd NXYAA5U
VDD Vdd gnd 12                                      ; Supply Voltage
VdRef Vdd VdRef 0
Vo Vo gnd 1                                         ; Voltage
VdO Vo VdO 0

R VdRef d1 8.2k                                     ; Resistor

.dc Vo 1 5 0.2                                      ; DC Analysis
.control                                            ; Control Functions
run
print I(VdRef) I(VdO)
plot I(VdRef) I(VdO)
* plot I(Vdd)
* plot I(Vo)
.endc
```

3.3 Learnings

Analysis Values are close to Simulation values.
Understood the design and implementation of a practical current mirror using a general purpose NMOS arrays IC (ALD1106).