ECE M216A Project, Fall 2023

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Group-4 Performance Summary

Max f_{clk} [MHz]	Area [μm^2]	Energy [pJ]	Hold Time Slack [ps]
6666.67MHz	3538.192845 μm^2	1.5235 pJ	71.1 ps

Top-Level Architecture

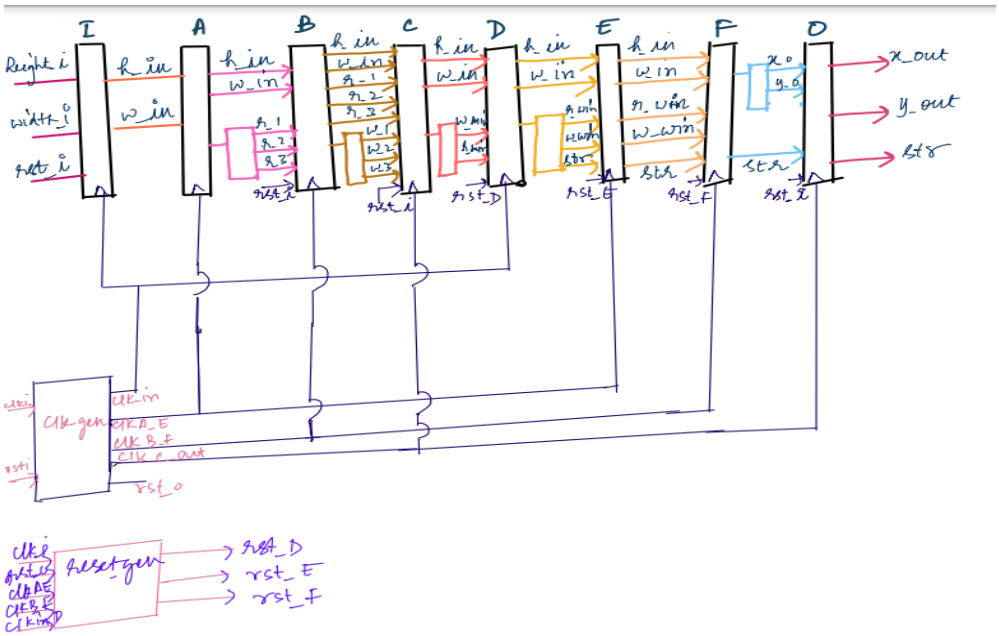

Figure. Architecture block diagram and its key building blocks

Design Highlights:

- Six-stage pipeline to utilize the 8 clock cycle latency, preventing false placement of programs
- Clock and reset controller strategically triggers paired stages, enhancing the frequency
- Memory operations in distinct sequential stages to ensure that data correctness is upheld
- First half of the design (I,A,B,C) samples input, reads memory and prepares for computation
- Second half (D,E,F,O) executes computation, updates memory and samples the output